MicroLAB Systems

Ultimate DSP Development Solutions

TORNADO-AZU+/FMC+

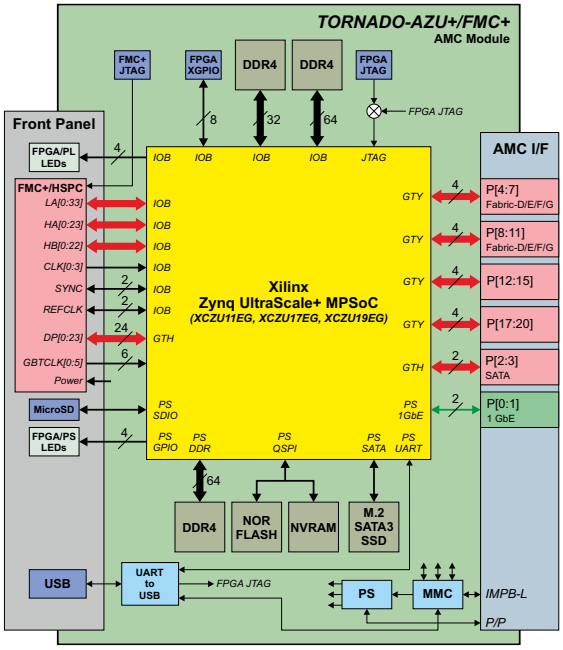
AMC-module with Zynq UltraScale+ MPSoC FPGA and FMC+/HSPC site

Key Features

- AMC-module with Zynq UltraScale+ EG MPSoC for modular DSP systems
- Complies PICMG® 3.0 Rev.3.0, MicroTCA.0 R1.0, AMC.0 R2.0, IPMI 1.5, HPM.1 R1.0, VITA® 57.4-2018 and VITA® 57.1-2019 specifications
- Installs into MicroTCA® chassis and AdvancedTCA® carrier
- Up to 544Gbps aggregated bandwidth for AMC-to-AMC data transfer
- Remote control from host PC and Android® devices via 1GbE ports
- In-chassis AMC-to-AMC control communication via 1GbE ports
- FMC+/HSPC site for user adopted I/O via FMC submodule (AD/DA, etc.) with up to 384Gbps aggregated bandwidth via FMC GBT ports
- *TASDK*® tools for applications development and control
- Stand-alone operation from +12V power for embedded applications

Details

- Xilinx Zynq UltraScale+ EG-grade MPSoC (XCZU11EG, XCZU17EG, XCZU19EG) FPGA with six ARM® cores (PS), high-density logic (PL) and two transceiver pools (28Gbps/32Gbps GTY and 16Gbps GTH)
- VITA® 57.4-2018 FMC+/HSPC site for FMC submodule (160 I/O, 24 GBTs 16Gbps/lane) with variety of activation modes
- AMC Fabric-DEFG ports 4-7/8-11 (28Gbps/lane) for data transfer with AMC.2 (10GbE, 40GbE, 100GbE), AMC.4 Serial RapidIO (20Gbps, 50Gbps, 100Gbps), AMC.1 PCIe (32Gbps, 64Gbps, 128Gbps) protocols via in-chassis fabric switch
- Optional support for AMC ports 12-15/17-20 (28Gbps/lane, "free" protocol) for direct in-chassis AMC-to-AMC data transfer
- AMC Fabric-B ports 2-3 (16Gbps/lane, AMC.3 6Gbps SATA/SAS or "free" protocol) for direct in-chassis data transfer with adjacent AMC-modules
- AMC Fabric-A 1GbE ports 0-1 from PS for remote device control and in-chassis AMC-to-AMC control communication
- PS x64 DDR4 memory (up to 8GB)
- PL x64 and x32 DDR4 memory banks (up to 8GB and 4GB)
- 2Gb PS NOR FLASH memory for applications and data
- 4Mb NVRAM memory for critical PS application data
- Removable M.2 2280 SSD SATA3 module (up to 2TB) for PS
- Front panel MicroSD card slot (up to 2TB) for PS
- Front-panel PS and PL controlled LEDs
- High-performance MMC controller with proprierity *TAMMC*® Gen2 MMC-kernel, power/temperature monitoring, status indication and more, all for reliable and safe device operation and protection
- PS and MMC UART ports for remote control and management
- Embedded high-speed FPGA USB JTAG emulator, optional external JTAG



TORNADO-AZU+/FMC+ Block Diagram

TORNADO-MTCA® DSP modular system including TORNADO-AZU+/FMC+ and TORNADO-A6678/FMC AMC modules with FMC A/D submodules, TORNADO-ARX1 RF AMC module and T/AX-DSFPX AMC module with 10GbE SFP+ ports all installed into MicroTCA® 1U chassis with 10GbE switching fabric

Mini TORNADO-mMTCA® DSP modular system including TORNADO-AZU+/FMC+ AMC-module with FMC A/D submodule and T/AX-DSPX AMC-module with 10GbE SFP+ ports all installed into dual-slot MicroTCA® mini chassis with passive backplane

Development Tools

- *TASDK*® tools for *TORNADO* AMC modules with high-level API for quick development of PS/PL applications and host Windows, Linux and Android® remote control applications
- Linux, FreeRTOS, or "bare-metal" API for PS applications
- Pre-certified Express Logic ThreadX® RTOS for demanding applications
- PS and PL demos for device tests and user projects startup
- Xilinx *SDK* and *Vivado* tools and IP

Applications

- Telecommunication and cell telephony
- DSP systems
- RF, SDR, Radars and astrophysics
- Image processing
- Industrial, instrumentation and medical

XILINX ALLIANCE PROGRAM MEMBER

AdvancedMC™ FMC+™

MicroLAB Systems

83 Dubninskaya street, #612, Moscow 127591, Russian Federation

Phone/fax: +7-(499)-900-6208 WEB: www.mlabsys.com E-mail: info@mlabsys.com

Technical Specifications (*TORNADO-AZU+/FMC+ rev.1A*)

Zynq UltraScale MPSoC FPGA and on-board FPGA environment

- Xilinx Zynq UltraScale+ MPSoC FPGA: XCZU[11EG/17EG/19EG]-[1/2/3]FFVC1760[E/I] (specified during ordering).
  (*) Default FPGA: XCZU19EG-2FFVC1760E (28Gbps/16Gbps GTY/GTH, commercial temperature range). Other FPGA are optional with extended delivery time.
- On-board FPGA DDR4 memory banks (specified during ordering):
  - Zynq/PS DDR4: 256M/512M/1Gx64 (2GB/4GB/8GB, 2400MTPS) (mandatory, specified during ordering).
  - Zynq/PL DDR4 bank #0: 256M/512M/1Gx64 (2GB/4GB/8GB, 2666MTPS) (optional, specified during ordering).
  - Zynq/PL DDR4 bank #1: 256M/512M/1Gx32 (1GB/2GB/4GB, 2666MTPS) (optional, specified during ordering).
- Zynq/PS QSPI NOR FLASH memory: 128M/256Mx8 (1Gb/2Gb) (mandatory).
- Zynq/PS QSPI NVRAM memory: 512Kx8 (4Mb) (optional, specified during ordering).
- M.2 2280 SATA3 SSD memory module interface (2TB max capacity) (optional, specified during ordering).
- Front-panel MicroSD card slot (2TB max capacity) (optional, specified during ordering).
- Zynq/PS UART (available via front panel USB port).
- 8-bit external Zynq/PL *XGPIO*[0:7] (LVTTL 3V) with individual direction control (optional, specified during ordering).
- GTY transceivers available/used: 16/16 (25Gbps/28Gbps/32Gbps for FPGA with '-1'/'-2'/'-3' speed grades correspondingly).
- GTH transceivers available/used: 32/26 (12.5bps/16.375Gbps for FPGA with '-1' and '-2'/'-3' speed grades correspondingly).
- Zynq/PS bootmode: None, QSPI NOR FLASH, MicroSD card.
- Zynq/PS GTR transceivers available/used: 4/3 (2x AMC.2 Fabric-A 1GbE ports 0-1, 1x for M.2 SATA3 SSD module).
- Zynq/PL bitstream loading modes: from Zynq/PS applications, via JTAG.
- Zynq/PL bitstream decryption key battery (optional, specified during ordering). User replaceable every 4 years.
- Debug port: Embedded high-speed USB JTAG emulator, external Xilinx JTAG emulator via adapter cable (14-pin, LVTTL 3V).

FMC+/HSPC site interface

- Complies VITA 57.4-2018 and VITA57.1-2019 specifications.
- FMC+/HSPC mezzanine submodule width: single.
- FMC+/HSPC mezzanine submodule stacking: 10mm (default), 8.5mm (optional, extended delivery time applies).
- FMC+/HSPC interface type: HPC, LPC, HSPC.
- FMC sub-module activation: via MMC, various activation modes, small/large FMC FRU SEEPROM support, optional "no-FRU" activation.
- Number of I/O: 160 (LA[0:33]_p/n, HA[0:23]_p/n, HB[0:21]_p/n).
- Number of I/O clocks: 4 (CLK_M2C[0:1_p/n, CLK[2:3]_BIDIR_p/n with CLK_DIR direction indicator).
- Number of FMC+ Reference Clocks: 2 (REFCLK_M2C_p/n, REFCLK_C2M_p/n). REFCLK_C2M_p/n is generated by low-jitter high-resolution clock synthesizer.
- Number of FMC+ Trigger signals: 2 (SYNC_M2C_p/n, SYNC_C2M_p/n).
- FMC Vadj voltage (I/O logic levels for LA/HA/HB I/O and CLK_M2C/CLK_BIDIR clocks): 1.0V-1.8V with 0.1V increment (is set upon FMC activation mode).
- FMC *VIO_B_M2C* voltage: 0V-*Vadj.*
- FMC *VREF_A_M2C* voltage: 0V-*Vadj*.
- FMC *VREF_B_M2C* voltage range: 0V- *VIO_B_M2C*.
- Number of GBT transceivers: 24 (DP[0:23]_p/n, up to 16Gbps/lane, connected to FPGA GTH transceivers).
- Number of GBT reference clocks: 6 (GBTCLK_M2C[0:5]_p/n).
- FMC power: 1Amax..3Amax@+12V (is set upon FMC activation mode), 3Amax@3P3V, 4Amax@Vadj, 0.1Amax@3P3VAUX.
- Zynq/PL FMC+/HSPC I/F IOB power consumption: 0.3Amax@VIO_B_M2C, 0.5mA@VREF_A_M2C, 0.5mA@VREF_B_M2C.
- Debug port: external JTAG emulator (10-pin, LVTTL 3V) via adapter cable.

Front-panel

- A "window" for FMC front bezel.
- AMC status LEDs: BLUE LED, AMC LED1 ("Power" status), AMC LED2 ("t°" status).
- FMC submodule status LED.
- Zynq/PS+PL configuration status LED.
- User application controlled LEDs: 2x Zynq/PS LEDs, 3x Zynq/PL LEDs.
- Zynq/PS System Manager Status LED.
- MicroSD card slot (optional, specified during ordering) and MicroSD card power status LED.
- Micro-USB port with MMC UART port (115kBaud), Zynq/PS UART port (up to 1MBaud), FPGA JTAG port.

AMC interface

- Complies PICMG® AMC.0 R2.0, MicroTCA.0 R1.0 specifications.
- AMC Fabric-DEFG ports 4-7/8-11 (up to 32Gbps/lane, AMC.2 Ethernet, AMC.4 Serial RapidIO, AMC.1 PCIe, connected to FPGA GTY transceivers).
- AMC Fabric-DEFG ports 12-15/17-20 (up to 32Gbps/lane, "free" protocol) (optional, specified during ordering, connected to FPGA GTY transceivers).
- AMC Fabric-B ports 2-3 (up to 16Gbps/lane, AMC.3 SATA/SAS or "free" protocol, connected to FPGA GTH transceivers).
- AMC-Fabric-A ports 0-1 (AMC.2 1GbE, connected to Zynq/PS GTR transceivers).
- AMC FCLKA, TLCKA, TCLKB, TCLKC, TCLKD clocks (connected to FPGA).
- MMC ports: IPMB-L port

MMC and AMC-module management

- High-performance MMC controller with proprierity *TAMMC®* Gen2 MMC-kernel based firmware.
- Complies IPMI 1.5, IPMB CPS v1.0, PICMG® 3.0 rev.3.0, MicroTCA.0 R1.0, AMC.0 R2.0, HPM.1 R1.0 and VITA® 57.4-2018 specifications.
- High-speed monitoring of AMC payload and management powers (P/P and M/P), and all AMC/FMC backend power supplies.
- Multi-point temperature monitoring of PCB, FPGA, M.2 SSD module and FMC submodule.
- Activation and management of FMC submodule.
- LED indicators for AMC power/temperature status and FMC activation/power/temperature status.
- Remote MMC console via MMC UART 115kbaud port.

Physical

- Dimensions (specified during ordering): Single width either Full-size (F/S, 181 x 74 x 29 mm) (default) or Mid-size (M/S, 181 x 74 x 19 mm) AMC module.
- Weight 0.4 kg.

Power and temperature

- AMC +12V P/P payload power or external +12V power for stand-alone applications: 0.9A (min) (11W), 2.5A (typ) (30W), 10A (max) (120W).
- AMC M/P management power: +3.3V @130mA (typ).
- Operating temperature (ambient): 0ºC…+55ºC (FPGA with 'E' temperature grade), -40ºC…+55ºC (FPGA with 'I' temperature grade).
- Storage temperature (ambient): -40ºC…+80ºC.

Ordering information

TAZUPFMCP1A/XCZU19EG2E/D4/F2/E512/N4/SSD1T/SD/L1D4/L2D2/LI/A12/A17/FC+/FB/SA/FS

TORNADO-AZU+/FMC+ rev.1A AMC-module, Xilinx Zynq UltraScale+ XCZU19EG-2FFVC1760E (***XCZU19EG2E***), 4GB (512Mx64) Zynq/PS DDR4 memory (***D4***), 2Gb (256Mx8) Zynq/PS QSPI FLASH memory (***F2***), 512Kb (64Kx8) Zynq/PS I^2C SEEPROM memory (***E512***), 512Kx8 Zynq/PS nonvolatile QSPI NVRAM (***N4***), M.2 SSD 1TB memory module (***SSD1T***), front panel MicroSD card slot (***SD***), 4GB (512Mx64) Zynq/PL DDR4 memory bank #1 (***L1D4***), 2GB (512Mx32) Zynq/PL DDR4 memory bank #2 (***L2D2***), 8-bit external Zynq/PL *XGPIO* interface (***LI***), AMC ports 12-15 28Gbps (***A12***), AMC ports 17-20 28Gbps (***A17***), FMC+/HSPC site interface (***FC+***), Zynq/PL bitstream decryption key battery (***FB***), stand-alone/embedded operation mode support (***SA***), single-width full-size (F/S) AMC-module dimension (***FS***), standard 10mm FMC mezzanine module stacking, 0ºC…+55ºC operating temperature range (derived from FPGA p/n).

DOC: MDS-424E2 02/2020

MicroLAB Systems

83 Dubninskaya street, #612, Moscow 127591, Russian Federation
Phone/fax: +7-(499)-900-6208 WEB: www.mlabsys.com E-mail: info@mlabsys.com