TORNADO-6x

Ultra-High Performance 32-bit Fixed-/Floating-Point TMS320C6x DSP Systems
and Universal Emulators for TMS320 DSP
for Host ISA-bus PC and MicroPC Computers

User's Guide

covers:
TORNADO-62/67 rev.2A
TORNADO-62MX/67MX rev.1A

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About this Document

This user's guide contains description for *TORNADO-6x* (*TORNADO-62/67* rev.2A, *TORNADO-62MX/67MX* rev.1A) ultra-high performance 32-bit fixed-/floating-point TMS320C6201/C6701 digital signal processing (DSP) systems and TMS320 emulators for ISA-bus PC and ISA-bus MicroPC host computers.

This document does not include detail description neither for TI TMS320C6x DSP nor for the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C6201/TMS320C6701 Peripheral Reference Guide.*** Texas Instruments Inc, SPRU190B, USA, 1998.
2. ***TMS320C62x/TMS320C67x CPU and Instruction Set.*** Texas Instruments Inc, SPRU189C, USA, 1998.
3. ***TMS320C62x/TMS320C67x Programmer's Guide.*** Texas Instruments Inc, SPRU198B, USA, 1998.
4. ***TMS320C6x Optimizing C Compiler User`s Guide.*** Texas Instruments Inc, SPRU187C, USA, 1998.
5. ***TMS320C6x Assembly Language Tools User`s Guide.*** Texas Instruments Inc, SPRU186C, USA, 1998.

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Chapter 1. Introduction

This chapter contains general description for *TORNADO-6x* DSP systems for ISA-bus host PC product line, which comprises of *TORNADO-62/67* and *TORNADO-62MX/67MX* DSP systems.

CAUTION

'*TORNADO-6x*' DSP systems are designed to accommodate either 32-bit fixed-point TMS320C6201 DSP or code-compatible 32-bit floating-point TMS320C6701 DSP from Texas Instruments Inc. The particular DSP installed specifies the final name of *TORNADO-6x* DSP system, i.e. *TORNADO-62* and *TORNADO-67*, or *TORNADO-62MX* and *TORNADO-67MX*.

Since the only differences between the TMS320C6201 and TMS320C6701 DSPs are implied to the performance value and absence/presence of on-chip floating-point unit, then there is no difference for the on-board architecture and DSP/host environments between the corresponding *TORNADO-6x* DSP systems, i.e. *TORNADO-62* and *TORNADO-67*, or *TORNADO-62MX* and *TORNADO-67MX*.

CAUTION

The '*TORNADO-6x*' notation denotes that the supplied information is applicable to all *TORNADO-6x* DSP systems (*TORNADO-62/67* and *TORNADO-62MX/67MX* products).

Should information be a product specific, then the name of the corresponding product (*TORNADO-62/67* or *TORNADO-62MX/67MX*) will be highlighted.

1.1 General Information

TORNADO-6x are ultra-high performance fixed- and floating-point DSP systems and emulators for host ISA-bus PC and industrial MicroPC (from Octagon Systems Inc) computers. *TORNADO-62/67* are designed to plug into 16-bit ISA-bus slot of host PC, whereas *TORNADO-62MX/67MX* are designed to plug into 8-bit/16-bit ISA-bus slot of either conventional host PC or industrial MicroPC computer. All *TORNADO-6x* DSP systems feature flexible modular system architecture in order to meet requirements of multiple applications while keeping a cost to a minimum.

TORNADO-6x product line comprises of *TORNADO-62/67* and *TORNADO-62MX/67MX* DSP systems, which feature compatible host ISA-bus interface and TMS320C6x DSP environment. The only differences include extended on-board memory capacity, enhanced PIOX/SIOX expansion facilities and enhanced emulation

facility for *TORNADO-62/67* , whereas *TORNADO-62MX/67MX* meet industrial MicroPC form-factor from Octagon Systems Inc with 8-bit ISA-bus interface.
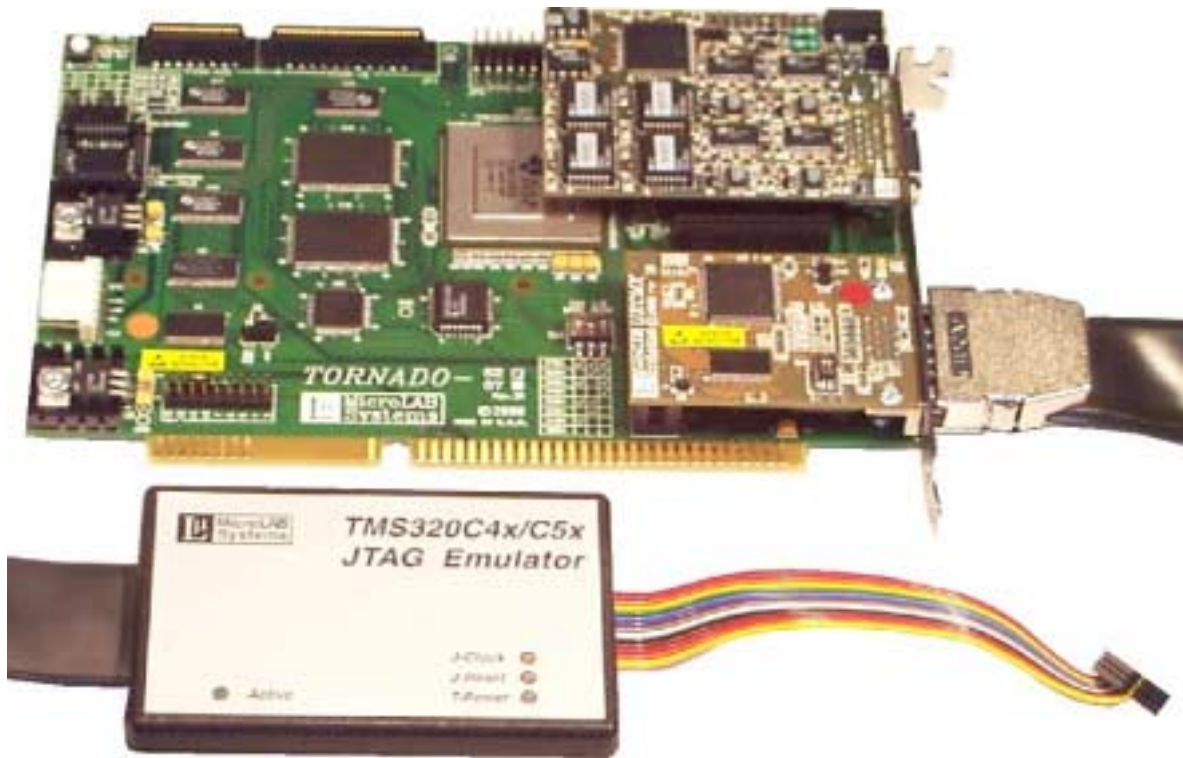
Fig.1-1a.   TORNADO-62/67 DSP system board with SIOX daughter-card module, *UECMX* universal emulation control daughter-card module and external JTAG pod.
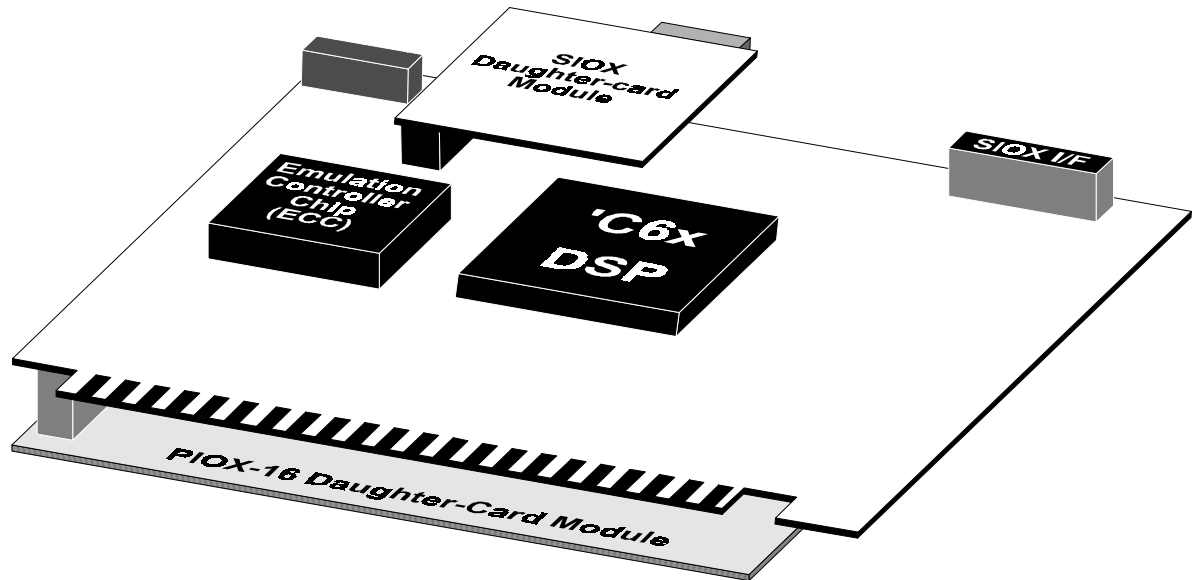
Fig.1-1b.   TORNADO-62MX/67MX DSP system board with SIOX and PIOX-16 daughter-card
modules and *ECC* emulation controller.

The following are some applications for *TORNADO-6x* DSP systems:
- *real-time DSP and signal acquisition*
- *high-speed multichannel fax/modem communication*
- *multichannel vocoders and speech signal processing*
- *audio and acoustics signal processing*
- *multimedia*
- *radars*
- *digital radio*
- *instrumentation and industrial*
- *universal emulator for any external TI TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP (TORNADO-62/67 only with UECMX and external MPSD/JTAG pod)*
- *TMS320C6x DSP evaluation and education*
- many more ...

TORNADO-6x utilize TMS320C6x 32-bit fixed- or floating- point DSP (1600 MIPS TMS320C6201 or 1000 MFLOPS TMS320C6701) and feature up to 1Mx32 (*TORNADO-62/67*) and 512Kx32 (*TORNADO-62MX/67MX*) on-board synchronous burst static RAM (SBSRAM) for program and data, and up to 1Mx8 FLASH for boot code when the board is used in stand-alone applications.

TORNADO-6x have on-board shared bus (SB) architecture, which shares access to SBSRAM, FLASH and PIOX shared resources between the on-board TMS320C6x DSP and host ISA-bus memory interface. Host ISA-bus memory interface can provide access to SBSRAM, FLASH and PIOX both in random and block data transfer modes in parallel with DSP operation and almost without consuming the DSP time.

TORNADO-6x feature optional facility for installation of serial I/O expansion (SIOX) daughter-card modules from a variety of AD/DA and digital I/O daughter-card modules for real-time instrumentation, industrial and speech, telecommunication and audio signal processing applications.

TORNADO-6x feature optional facility for installation of parallel I/O expansion (PIOX or PIOX-16) daughter-card modules from a variety of AD/DA and digital I/O daughter-cards modules for high-speed real-time instrumentation, industrial and speech, telecommunication and audio signal processing applications. *TORNADO-62/67* features universal PIOX/PIOX-16 site, whereas *TORNADO-62MX/67MX* features PIOX-16 site.

TORNADO-6x offer access to HPI (host port interface) of on-board TMS320C6x DSP from host ISA-bus I/O interface. Along with host ISA-bus memory interface this provides a second data path for communication between host and DSP environment.

TORNADO-6x feature optional stand-alone operation facility, which allows the customers to proceed with testing of designed DSP software in embedded environment. The customer can utilize all AD/DA daughter-card modules installed, and the power can be applied via dedicated on-board connector.

TORNADO-6x use scan-path emulation control for the on-board TMS320C6x DSP in order to debug resident TMS320C6x DSP software. Scan-path emulation control of the on-board TMS320C6x DSP is available either via external TI XDS510 or MicroLAB' *MIRAGE-510DX* scan-path emulators, or by means of optional *emulation controller chip (ECC)* for *TORNADO-62MX/67MX*, which plugs into dedicated on-board socket, or by means of optional *emulation control daughter-card module (UECMX)* for *TORNADO-62/67*, which plugs into the dedicated on-board daughter-card site. Both *ECC* and *UECMX* are low cost replacements for TI XDS510 and MicroLAB's *MIRAGE-510DX* scan-path emulators and run under identical industry standard TI C6000 Code Composer Studio IDE. Furthermore, *UECMX* allows optional connection to external MPSD and JTAG pods (which are the pods used with MicroLAB's *MIRAGE-510DX* scan-path emulator) in order to emulate any external TI TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP using TI HLL Debuggers and Code Composer IDE. This converts *TORNADO-62/67* into universal emulator for all TI DSPs.

TORNADO-6x software development tools include TI TMS320C6x DSP C compiler and Assembly language tools.

TORNADO-6x are supported by a variety of industry standard 3rd party DSP software tools, that include real-time operating systems (RTOS), digital filter design tools, DSP/vector/math function libraries, vocoder/fax/modem function libraries, and many more...

TORNADO-6x provide unique burn-in device serial codes, that are available for host software and might be used for hardware copyright protection for software vendors and DSP system integrators.

1.2   Host PC Specifications

TORNADO-6x require that host ISA-bus PC configuration should be at least 80386SX CPU and provides at least one 16-bit ISA-bus slot.

In order to learn configuration requirements for host PC running TMS320C6x DSP software development and debugging tools, refer to the corresponding documentation from TI as well as to MicroLAB' "*MIRAGE-510DX/UECMX User's Guide*".

1.3   Technical Specification

The following are the technical specifications for *TORNADO-6x* system.

Parameter description	*parameter value*
power supply voltage	+5V for *TORNADO-6x* board,
	optional ±5V/±12V for SIOX/PIOX daughter-card modules
power consumption (no *ECC* or *UECMX* installed)	+5V@2.1A (t=+20°C)
DSP performance	1600 MIPS (*TORNADO-62/62MX*) 1000 MFLOPS (*TORNADO-67/67MX*)
dimensions	180x120 mm (*TORNADO-62/67*) 123x113 mm (*TORNADO-62MX/67MX*)
operating temperature	0..+50°C
I/O expansion interfaces	*TORNADO-62/67*: two sites (SIOX-A and SIOX-B) for two TORNADO/SIOX daughter-card modules. One site for TORNADO/PIOX daughter-card module.
	TORNADO-62MX/67MX: two SIOX-A parallel sites for one TORNADO/SIOX daughter-card module. One site for TORNADO/PIOX-16 daughter-card module.
host ISA-bus interface:	
number of 8-bit I/O ports in host ISA-bus I/O interface	32
size of ISA-bus memory page in the UMB memory address area for SB access via host ISA-bus memory interface	32Kx8
host ISA-bus data format requirement	*TORNADO-62/67*: 16-bit host ISA-bus
	TORNADO-62MX/67MX: 8-bit/16-bit host ISA-bus
host timeout control time for SB grant, SB ready and HPI ready	6 us
host IRQ lines	*TORNADO-62/67*: IRQ 3, 4, 5, 6, 7, 10, 11, 12, 15
	TORNADO-62MX/67MX: IRQ 3, 4, 5, 6, 7

on-board SBSRAM and FLASH/EPROM:

      SBSRAM capacity   32K..1Mx32 1ws (*TORNADO-62/67*)
                                                           32K..512Kx32 1ws (*TORNADO-62MX/67MX*)

      FLASH/EPROM memory capacity   128K..1Mx8 (Ta=100ns) with write-protection feature

watchdog timer:

      latency period   0.8 sec

external clock generators for McBSP-0/1 serial ports of DSP:

      maximum frequency for external clocks for McBSP-0/1   100 MHz (*TORNADO-62/62MX*)
      TMS320C6x DSP serial ports   80MHz (*TORNADO-67/67MX*)

Chapter 2. System Architecture and Construction

This chapter contains description for *TORNADO-6x* system architecture, construction, host ISA-bus interface, and SIOX/PIOX I/O expansion sites.

2.1 *TORNADO-6x* System Architecture

TORNADO-6x DSP system mainboard installs into 16-bit or 8-bit (*TORNADO-62MX/67MX* only) ISA-bus slot of host PC or MicroPC (*TORNADO-62MX/67MX* only).

TORNADO-62/67 and *TORNADO-62MX/67MX* system architectures are presented at fig.2-1.
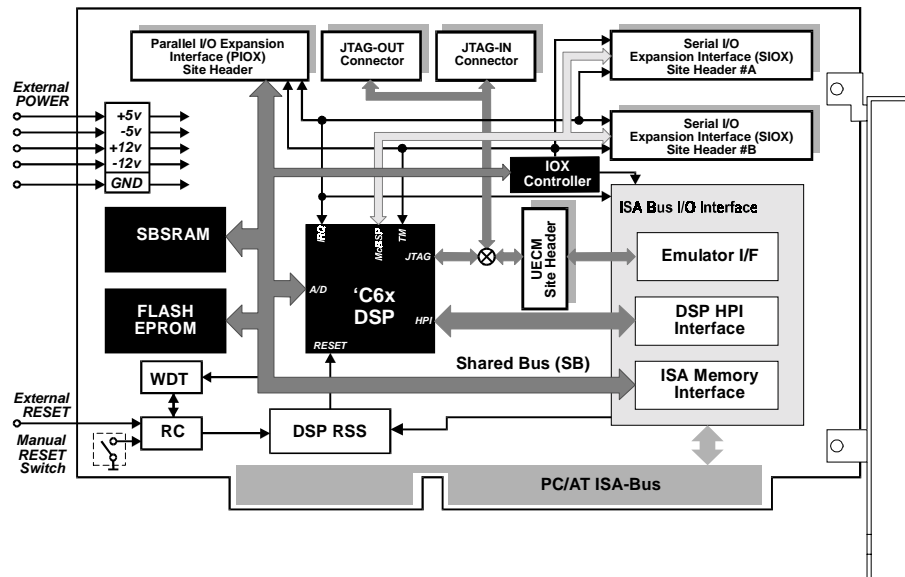
Fig.2-1a. Architecture of *TORNADO-62/67* mainboard.
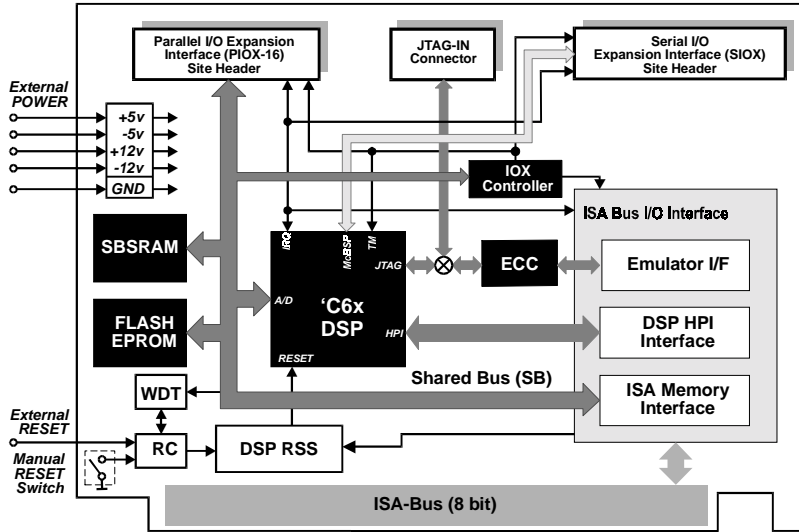
Fig.2-1b.   Architecture of *TORNADO-62MX/67MX* mainboard.

Main components of *TORNADO-6x* mainboard comprise of:
- *32-bit fixed-point TMS320C6201 (TORNADO-62/62MX) DSP or 32-bit floating-point TMS320C6701 (TORNADO-67/67MX) DSP*
- *on-board SBSRAM for program and data*
- *on-board FLASH for source boot code during stand-alone operation*
- *DSP reset controller (RC) with watchdog timer (WDT), and DSP Reset Source Selector (RSS)*
- *I/O expansion controller (IOX)*
- *serial I/O expansion interface (SIOX) sites*
- *32/16-bit parallel I/O expansion interface (PIOX) site or 16-bit parallel I/O expansion interface (PIOX-16) site*
- *host ISA-bus memory and I/O interfaces*
- *emulation controller chip (ECC) for TORNADO-62MX/67MX or site for universal emulation control daughter-card module (UECMX) for TORNADO-62/67.*

The on-board TMS320C6x DSP, SBSRAM, FLASH, PIOX and host ISA-bus memory interface are linked together by means of the on-board *Shared Bus (SB)*. SB shares SBSRAM, FLASH, and PIOX resources between two 'bus masters', that can execute SB access cycles: the on-board TMS320C6x DSP and host ISA-bus memory interface. On-board SB arbitration assumes that TMS320C6x DSP bus master has highest SB access priority whereas ISA-bus memory interface is designed to access SB in-parallel with DSP internal operation, without any DSP and host software overhead and almost without consuming the DSP time.

Constructions for *TORNADO-62/67* and *TORNADO-62MX/67MX* mainboards are presented at fig.2-2.
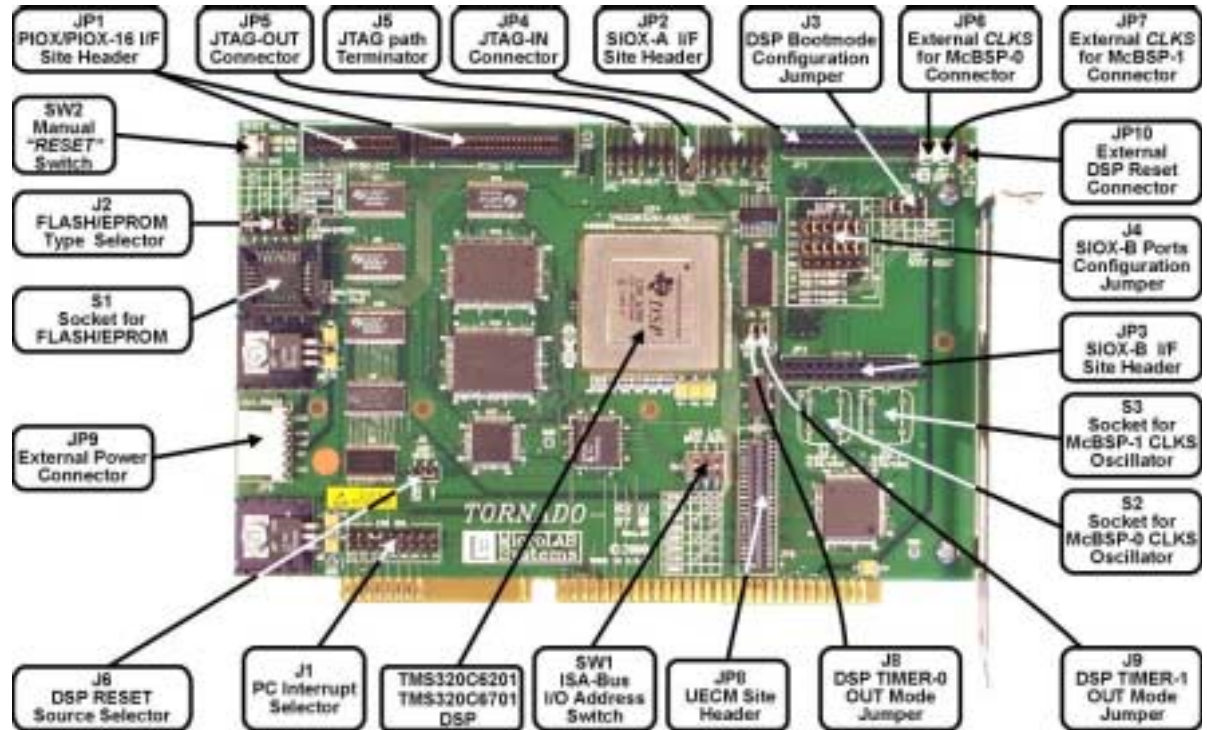
Fig.2-2a. Construction of *TORNADO-62/67* mainboard.
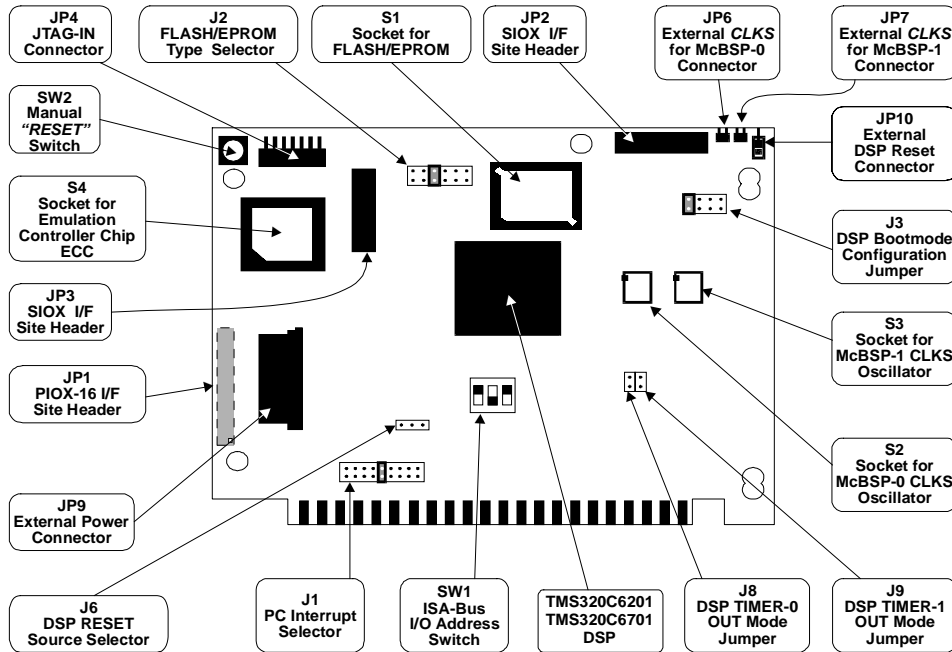
Fig.2-2b.   Construction of *TORNADO-62MX/67MX* mainboard.

TMS320C6x DSP

The on-board TMS320C6x DSP might be either 32-bit fixed-point TMS320C6201 DSP (1600 MIPS @ 200 MHz) or code-compatible 32-bit floating-point TMS320C6701 DSP (1000 MFLOPS @ 166 MHz) with VelociTI very-long instruction word (VLIW) on-chip architecture.

Synchronous Burst Static RAM (SBSRAM)

TORNADO-6x provides on-board synchronous burst static RAM (SBSRAM) for TMS320C6x DSP program and data memory areas. SBSRAM is mapped to CE-0 area of DSP' EMIF.

TORNADO-62/67 features up to 1Mx32 1ws on-board SBSRAM installed in two memory banks, whereas *TORNADO-62MX/67MX* features up to 512Kx32 1ws of on-board SBSRAM in one memory bank.

FLASH Memory for Stand-alone Operation

TORNADO-6x provides up to 1Mx8 on-board FLASH memory bank for program/data startup code during stand-alone operation. FLASH memory bank can accommodate either FLASH or EPROM memory chip, and features write protection facility for data safety.

Shared Bus (SB)

TORNADO-6x on-board SB delivers access to the on-board SBSRAM, FLASH and PIOX shared resources for both on-board TMS320C6x DSP and host ISA-bus memory interface. The SB address space comprises of SBSRAM memory area, FLASH memory area and I/O area, which is mapped into PIOX expansion interface. SB supports 8/16/32-bit data cycles. It is important to note, that all host accesses to the on-board SBSRAM, FLASH and PIOX resources are performed concurrently with the DSP running and without any DSP and host software overhead.

Host ISA-bus Interface

TORNADO-6x host ISA-bus interface was designed for DSP/system control and high-speed data transfer between host ISA-bus and on-board SBSRAM, FLASH, PIOX and HPI port of on-board TMS320C6x DSP. *TORNADO-6x* host ISA-bus interface includes:

- *ISA-bus memory interface*, which performs access to SBSRAM, FLASH and PIOX
- *ISA-bus I/O interface*, which provides *TORNADO-6x* system control and access to TMS320C6x on-chip HPI (host port interface).

Host ISA-bus memory interface is designed to access SB SBSRAM/FLASH/PIOX resources via 32Kx8 *shared memory page* (*SMP*) that is mapped into ISA-bus UMB memory address space. Once ISA-bus executes memory cycle within address range of *SMP*, then the on-board *TORNADO-6x* ISA-bus memory interface generates request to SB. Particular allocation of *SMP* onto SB address space is defined by *SB PAGE MAPPER* register from ISA-bus I/O interface. Host can access the SB data using 8/16/32-bit data cycles. Host ISA-bus memory interface has lowest SB access priority.

Base ISA-bus memory address for host ISA-bus memory is setup by host software and ISA-bus memory interface can be switched off in case *TORNADO-6x* board is not used.

ISA-bus base I/O address for ISA-bus I/O interface is configured by the on-board SW1 switch into one of eight predefined I/O address areas.

TMS320C6x HPI (host port interface)

TORNADO-6x host ISA-bus I/O interface also delivers access to TMS320C6x on-chip HPI, which comes as a secondary path for communication between host PC and on-board DSP along with on-board SBSRAM. HPI offers access from host PC to all TMS320C6x memory areas (both DSP on-chip and off-chip resources) and allows generation of mutual interrupts between DSP and host ISA-bus. However, unlike host-to-SBSRAM/FLASH/PIOX access, HPI does not support random access to DSP memory areas from host PC using standard ISA-bus memory cycle, and assumes that HPI memory address should be pre-latched into HPI address register prior HPI data access will be performed. However, the HPI address auto post-incrementing feature is available and simplifies data array upload/download. HPI is available only while TMS320C6x DSP is in the 'RUN' state (executing the program).

I/O Expansion Flag Controller (IOX)

TORNADO-6x has on-board I/O expansion flag controller (IOX), which provides extra DSP I/O ports in order to control the on-board TMS320C6x DSP environment. IOX area can be accessed by TMS320C6x DSP only, and is not available during host ISA-bus memory interface SB access cycles.

Serial I/O Expansion Interface (SIOX) sites

TORNADO-6x on-board SIOX interface sites are used for installation of AD/DA/DIO daughter-card modules and comprises of signals for TMS320C6x DSP on-chip McBSP serial ports, timers and interrupt control.

SIOX compatible daughter-card modules include a variety of speech/fax/modem AD/DA, telecom interfaces, audio AD/DA, DAT interface, multichannel instrumentation AD/DA/DIO modules, application specific I/O coprocessors, and many more.

Parallel I/O Expansion Interface (PIOX and PIOX-16) site

TORNADO-6x feature PIOX (*TORNADO-62/67* only) or PIOX-16 (*TORNADO-62MX/67MX* only) interface site for installation of high-speed AD/DA/DIO daughter-card modules. *TORNADO-6x* PIOX/PIOX-16 interface is allocated into TMS320C6x CE-3 memory area and is one of shared SB resources, i.e. can be accessed both by on-board DSP and host ISA-bus memory interface.

PIOX and PIOX-16 interfaces comprise of SB address/data/strobe signals and TMS320C6x DSP on-chip timers and interrupt control. The only difference between PIOX and PIOX-16 interfaces is that PIOX has 32-bit data and 20-bit address buses, whereas PIOX-16 features 16-bit data and address buses. PIOX site is designed to accommodate both 32-bit PIOX daughter-card modules, whereas PIOX-16 can accommodate only 16-bit PIOX-16 daughter-card modules.

PIOX/PIOX-16 compatible daughter-card modules include a variety of multichannel instrumentation AD/DA/DIO modules and many more. Moreover, PIOX daughter-card modules include DSP coprocessors and application specific I/O coprocessors for extending DSP performance of *TORNADO* DSP systems.

Stand-alone Operation

TORNADO-6x provide optional host-free stand-alone operation for embedded applications. This allows easy migration from target system software debugging using host PC to real system prototyping in embedded DSP application.

During stand-alone operation the external power may apply either from on-board dedicated external power connector or from ISA-bus, and source program/data code is loaded either from on-board FLASH/EPROM memory or HPI port of TMS320C6x DSP after DSP reset is released. The particular boot mode is defined by the on-board DSP Boot Mode jumpers. The on-board FLASH memory can be programmed via host ISA-bus memory interface while *TORNADO-6x* is installed into host PC. The HPI port is accessible via host ISA-bus I/O interface.

DSP Reset Controller (RC) and Reset Source Selector (RSS)

If *TORNADO-6x* is used for PC plug-in applications, then the on-board DSP reset source selector (RSS) connects the TMS320C6x DSP reset input to the corresponding output signal of host ISA-bus interface.

If *TORNADO-6x* is used for stand-alone operation, then RSS connects the TMS320C6x DSP reset input to the output of DSP reset controller (RC), which generates the DSP reset signal either from on-board DSP reset pushbutton, or from external DSP reset source, or from on-board power supervisory circuit, or from on-board watch-dog time (WDT). WDT feature is optional, and if enabled by the DSP software, it dramatically increases the DSP software reliability by means of automatic restarting DSP once the DSP software hangs-on or idles for more than 0.8 sec period.

Debugging of Resident TMS320C6x DSP Software

Resident TMS320C6x DSP software for *TORNADO-6x* can be debugged using TI XDS510 and MicroLAB' *MIRAGE-510DX* scan-path emulators. However, in order to minimize cost of debugging tools, the emulation controller chip (*ECC*) and emulation control daughter-card module (*UECMX*) options are available. *ECC* is designed to plug into the dedicated on-board socket of *TORNADO-62MX/67MX*, whereas *UECMX* is designed to plug into the dedicated site on *TORNADO-62/67*. Both *ECC* and *UECMX* are low cost replacement for XDS510 and *MIRAGE-510DX* emulators and run under the industry standard GoDSP TMS320C6x Code Composer IDE.

Debugging External TI TMS320 DSP Software with TORNADO-62/67 and UECMX

TORNADO-62/67 easily converts into universal scan-path emulator for any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP. This requires the *UECMX* daughter-card module installed onto *TORNADO-62/67* mainboard and optional external MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x/ C8x) pod attached to *UECMX*. The MPSD and JTAG pods are those used with MicroLAB' *MIRAGE-510DX* emulator. The *UECMX* runs under the industry standard TI HLL Debuggers and Code Composer IDE.

2.2   Shared Bus

The *TORNADO-6x* on-board shared bus (SB) architecture provides SBSRAM/PROGRAM, SBSRAM/DATA and I/O areas and supports 16-bit data cycles. SB comprises SBSRAM and PIOX-16 shared resources and is shared between the on-board TMS320C6x DSP and host ISA-bus memory interface.

SB Address Space

The SB address space is actually the address space for *TORNADO-6x* on-board TMS320C6x DSP with CE-0/1/3 memory areas. Table 2-1 specifies valid SB address areas.

Table 2-1. SB address areas and data ready wait times.

SB address areas	size (in bytes)	address range and wait time for *SB_READY* signal (SB data ready) after SB is granted	
		for on-board TMS320C6x DSP	*for host ISA-bus memory interface*
SBSRAM	4M (*TORNADO-62/67*) 2M (*TORNADO-62MX/67MX*)	0000000H..003FFFFFH 1ws (CE-0 memory area)	00000000..003FFFFFH @SBSRAM 1ws
FLASH/EPROM	4M (allocated on 32-bit words boundaries)	01000000H..013FFFFFH 26ws (CE-1 memory area) (the timing and 8-bit ROM mode should be programmed via EMIF CE-1 Space Control Register of TMS320C6x DSP)	00000000..003FFFFF @FLASH
PIOX I/O area	2M/PIOX (allocated as 32-bit words for *TORNADO-62/67*) 128K/PIOX-16 (allocated as 16-bit words on 32-bit boundaries for *TORNADO-62MX/67MX*)	03200000H..033FFFFFH (16ws + *PIOX_RDY*) (CE-3 memory area) 03200000H..0321FFFFH (16ws + *PIOX_RDY*) (CE-3 memory area) (the timing and 32-bit ASYNCHRONOUS ROM mode should be programmed via EMIF CE-3 Space Control Register of TMS320C6x DSP)	00000000..001FFFFF @IO (*PIOX_RDY* ,but not longer than 6µS timeout) 00000000..0003FFFF @IO (*PIOX_RDY* ,but not longer than 6µS timeout)

When accessed via host ISA-bus memory interface, the SB address space appears as a series of dual-access 32KB *shared memory pages* (*SMP*), which are mapped onto the predefined ISA-bus UMB (upper memory blocks) memory window by means of **SB PAGE MAPPER** register in host ISA-bus I/O interface. The SB can be accessed by host ISA-bus memory interface by means of random accesses to software variables or data arrays, which are allocated within *SMP*, or by means of block data transfers between PC main memory and *SMP* using either host i80x286 CPU MOVSB/MOVSW/etc instructions or host DMA controller.

SB Data Ready Signal

SB has internal **SB_READY** signal, which is generated by addressed device (SBSRAM/FLASH/PIOX) in order to acknowledge that SB data are valid after SB has been granted to the SB requestor. When SB is accessed by the on-board TMS320C6x DSP master, then **SB_READY** signal is internally connected to the *READY* pin of

TMS320C6x DSP, whereas for accesses from host ISA-bus memory interface the *SB_READY* signal is automatically processed by the SB access controller of ISA-bus memory interface.

SB Data Cycle Formats

SB supports 32/16/8-bit data cycles, which can be generated by both TMS320C6x DSP and host ISA-bus memory interface masters.

Although host ISA-bus is actually the 16-bit data bus, host ISA-bus memory interface of *TORNADO-6x* supports 32-bit SB access cycles. Once host ISA-bus cycle is addressing the SB area, then LSB/LSW or MSB/MSW are temporary stored in on-board register transceivers depending upon the memory read or memory write cycle is being performed correspondingly (see section 2.4).

SB Arbitration

When SB is requested by any of the SB masters (TMS320C6x DSP or host ISA-bus memory interface), then some time is required to resolve the arbitration. This normally takes about 2..6 TMS320C6x DSP clock cycles.

In case TMS320C6x DSP is requesting SB while SB is occupied by host ISA-bus memory interface, then the DSP should wait until host ISA-bus memory interface will release SB. After SB is granted to DSP, it is holded by DSP in order to access the SB resources at maximum speed without delays for arbitration between succeeding SB cycles.

In case host ISA-bus memory interface is requesting SB while SB is occupied by TMS320C6x DSP, then host ISA-bus memory interface must wait until DSP completes current SB access cycle and releases the SB.

When SB is requested by both DSP and host ISA-bus memory interface, then DSP has the highest SB access priority.

SB Locking

The SB arbiter supports *SB locking* by both SB masters in order to lock access to SB for processing of software semaphores or shared PIOX/PIOX-16 resources.

The SB locking by the on-board TMS320C6x DSP bus master is performed when DSP sets the *MLock* flag from I/O expansion flag area (IOX).

> **CAUTION**
>
> Time interval between setting and resetting *MLock* flag by the on-board TMS320C6x DSP should not exceed 6 μsec.

The SB locking by host ISA-bus memory interface master is performed by means of setting the *SB_GLOCK* or the *SB_LOCK* bits in *CONTROL REGISTER* of host ISA-bus I/O interface.

```
╔══════════════════════════════════════════════════════════════════╗
║                            CAUTION                                 ║
║                                                                    ║
║   Continuous SB locking by host ISA-bus memory interface by means  ║
║   of setting the SB_GLOCK and SB_LOCK bits can result in           ║
║   continuous halting of the on-board TMS320C6x DSP bus master      ║
║   and may lead to time distortions of real-time data processing.   ║
╚══════════════════════════════════════════════════════════════════╝
```

2.3   TMS320C6x DSP Environment

The *TORNADO-6x* DSP systems utilize state of art TMS320C6x ultra-high performance inter-compatible 32-bit fixed- and floating point DSP from TI:

- 1600 MIPS fixed-point TMS320C6201 DSP in *TORNADO-62/62MX* DSP systems
- 1000 MFLOPS floating-point TMS320C6701 DSP in *TORNADO-67/67MX* DSP systems.

TMS320C6x DSP Address Space

TORNADO-6x on-board TMS320C6x DSP supports three external memory address areas: SBSRAM (EMIF CE-0 area), FLASH/EPROM (EMIF CE-1 area) and IOX/PIOX (EMIF CE-3 area). The EMIF CE-2 area is reserved. Address areas for on-board TMS320C6x DSP and the corresponding EMIF registers settings are presented in table 2-2.

Table 2-2.   Address areas for TMS320C6x DSP in *TORNADO-6x* DSP systems.

Address area of TMS320C6x DSP	DSP address range (in bytes)	value at DSP RESET	access mode	EMIF CE space	memory type for EMIF CE space	wait states	fields of EMIF-CE Space Control Register
SBSRAM 1/2 DSP CLK	00000000H ..003FFFFFH (*TORNADO-6x*) 00000000H ..001FFFFFH (*TORNADO-6xMX*)	-	r/w	CE-0	SBSRAM	1ws	- (*EMIF-GCR* = 0x3078)
FLASH/EPROM	01000000H ..013FFFFFH	-	r/w (with write disable)	CE-1	8-bit ROM	35ws	*EMIF-CE1:* (0x8638d823) R/W_SETUP=8 R/W_STB=24 R/W_HLD=3
reserved	02000000H ..02FFFFFFH	-	-	CE-2	32-bit ASYNC	max	*EMIF-CE2* = 0xffffff23

				CE-3	32-bit ASYNC	12ws	*EMIF-CE3:* (0x31b3c623)
IOX area: *MH_RQ* register (DSP-to-Host request flag)	03000000H	-	w (write data is ignored)				R/W_SETUP=3 R/W_STB=6 R/W_HLD=3
IOX area: *Mlock* register (SB lock by DSP)	03000004H	0 (no SB Lock)	r/w (only bit D0 is valid)			12ws	
IOX area: *PXSX_RUN* register (software reset signals for SIOX/PIOX expansion interface sites)	03000008H	0 (software reset is OFF)	r/w (only bits D0..2 are valid)			12ws	
IOX area: *WDT_CLR* register (clear watch-dog timer)	03100000H	-	w (write data is ignored)			26ws (hardware controlled)	
IOX area: *WDT_EN* register (WDT enable for stand-alone operation)	03100004H	0 (WDT is disabled)	r/w (only bit D0 is valid)			12ws	
PIOX I/F (*TORNADO-62/67*)	03200000H ..033FFFFFH	-	r/w			(12ws + *PIOX_RDY*)	
PIOX-16 I/F (*TORNADO-6xMX*)	03200000H ..0321FFFFH	-	r/w			(12ws + *PIOX_RDY*)	

Notes:
1. IOX area denotes I/O Expansion Flag controller.
2. Other DSP memory and I/O areas are reserved. Do not use these areas.
3. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

CAUTION

SB address space for *TORNADO-6x* is the address space for 8-bit BYTE data words.

The 16-bit SB data words are allocated on the x2 odd address boundaries.

The 32-bit SB data words are allocated on x4 address boundaries.

SBSRAM Area

TORNADO-6x on-board SBSRAM operates at 1/2x of the DSP clock and might be used as external DSP program/data memory area and for DSP-to-PC communication via host ISA-bus memory interface.

SBSRAM is allocated to EMIF CE-0 space of TMS320C6x DSP, and its capacity differs for different *TORNADO-6x* DSP systems as the following:

- one or two banks (in accordance with the purchasing specifications) of up to 512Kx32 SBSRAM each, totally up to 1Mx32 SBSRAM for *TORNADO-62/67*
- one bank of up to 512Kx32 SBSRAM for *TORNADO-62MX/67MX*.

FLASH/EPROM Area

On-board FLASH/EPROM of *TORNADO-6x* is included for optional easy migration from PC plug-in application to stand-alone applications of *TORNADO-6x*.

FLASH/EPROM bank assumes installation of 5v only 128K..1Mx8 FLASH or EPROM chip in the PLCC-32 package into the dedicated S1 on-board PLCC-32 socket (see fig.2-2).

CAUTION

TORNADO-6x mainboards are designed to carry the FLASH 5v-only 128K..1Mx8 chips or EPROM 128K..1Mx8 chips in the PLCC-32 IC package.

Installation of other FLASH/EPROM chips than that specified in table 2-3 may result in damage of FLASH/EPROM chip and/or of *TORNADO-6x* hardware.

Once FLASH chip is installed, then it can be programmed by DSP software and via host ISA-bus memory interface. the EPROM chip, however, can be programmed in the external programmer only, and can be used for read-only program bootload purposes in *TORNADO-6x*.

The on-board J2 jumper set (jumpers J2-1..J2-6) are used to select the particular FLASH/EPROM chip type and to set the write protect features for the FLASH chips.

Table 2-3. FLASH/EPROM chip type selector.

FLASH/EPROM chip in PLCC-32 IC package	jumper configuration					
	J2-1	**J2-2**	**J2-3**	**J2-4**	**J2-5**	**J2-6**
Am29F010 128Kx8 FLASH *Am29F040 512Kx8 FLASH* *with WRITE ENABLE*	OFF	ON	OFF	ON	OFF	OFF
Am29F010 128Kx8 FLASH *Am29F040 512Kx8 FLASH* *with WRITE DISABLE*	OFF	ON	OFF	OFF	ON	OFF
27C010 128Kx8 EPROM *27C020 256Kx8 EPROM*	OFF	OFF	ON	OFF	ON	OFF
27C040 512Kx8 EPROM	OFF	OFF	ON	OFF	OFF	ON
27C080 1Mx8 EPROM	ON	OFF	OFF	OFF	OFF	ON

Notes:. 1. The highlighted configuration corresponds to the factory setting.
2. The recommended access time for the FLASH/EPROM chip is 100ns or less.

FLASH/EPROM is allocated into EMIF CE-1 space of TMS320C6x DSP, and, therefore the EMIF CE-1 Space Control Register must be configured to support 8-bit ROM memory type (other fields of EMIF CE-1 Space Control Register should be set in accordance with table 2-2). This is either done automatically by setting appropriate 8-bit ROM BOOT configuration with 1/2x CPU clock SBSRAM (J3 bootmode configuration BM#11) or should be done by user software when using other boot configurations.

> ### CAUTION
>
> TMS320C6x DSP allocates 8-bit FLASH/EPROM data words on 32-bit data word boundaries.

FLASH memory bank provides FLASH memory write protection by means of J2-2 and J2-3 jumpers in order to exclude unauthorized FLASH memory data update.

> ### CAUTION
>
> If J2-2 jumper is removed and J2-3 jumper is installed while the FLASH memory chip is installed, then the FLASH memory can be programmed either by DSP software or via host ISA-bus memory interface.
>
> If J2-3 jumper is installed and J2-2 jumper is removed while the FLASH memory chip is installed, then writing to FLASH memory is disabled.

If FLASH memory chip is bundled together with *TORNADO-6x* DSP system or is purchased from MicroLAB Systems, then *TORNADO-6x* supplied software utilities allow programming of the on-board FLASH memory via *TORNADO-6x* host ISA-bus memory interface.

> ### CAUTION
>
> If the FLASH chip type is other than that bundled as standard with *TORNADO-6x* DSP system, then the FLASH might be not programmed with software utilities for *TORNADO-6x*.

IOX Area

TMS320C6x DSP environment of *TORNADO-6x* features special I/O expansion (IOX) registers area, which is used for DSP environment control. IOX area can be accessed by the TMS320C6x DSP only and is not visible from host ISA-bus memory interface (however, it is visible via the DSP HPI port of host ISA-bus I/O interface). Details about IOX area are described in table 2-2 and below in this section.

IOX area is allocated into EMIF CE-3 space of TMS320C6x DSP, and comprises of the following registers:
- *MH_RQ* (DSP master-to-Host request) generator IOX register (write-only)
- *MLock* (SB lock by DSP) IOX register
- *PXSX_RUN* (software reset signals control for SIOX/PIOX expansion interface sites) IOX register
- *WDT_EN* (enable WDT feature) IOX register
- *WDT_CLR* (clear watchdog timer) generation (write-only) IOX register.

PIOX Area of TORNADO-62/67

TORNADO-62/67 provide 32-bit parallel I/O expansion interface (PIOX) site for compatible AD/DA/DIO daughter-card modules. PIOX area can be accessed both by the on-board TMS320C6x DSP and host ISA-bus memory interface. PIOX area occupies 512Kx32 address sub-space of EMIF CE-3 space of TMS320C6x DSP.

PIOX-16 Area of TORNADO-62MX/67MX

TORNADO-62MX/67MX provide 16-bit parallel I/O expansion interface (PIOX-16) site for compatible AD/DA/DIO daughter-card modules. PIOX-16 area can be accessed both by the on-board TMS320C6x DSP and host ISA-bus memory interface. PIOX-16 area occupies 64Kx16 address sub-space of EMIF CE-3 space of TMS320C6x DSP.

TMS320C6x DSP Reset Source Selector (RSS)

TORNADO-6x provides on-board J6 jumper (see fig.2-2 and fig.A-1), also known as the DSP reset source selector (RSS), in order to select the TMS320C6x DSP reset source signal. RSS allows selection of the DSP reset signal from either the corresponding output of host ISA-bus I/O interface during PC plug-in applications or from the output of DSP reset controller (RC) during stand-alone operation.

CAUTION

If J6 jumper is set to 1-2 position (see fig.2-2 or fig.A-1), then the DSP reset signal is connected to the output of DSP reset controller (RC) for *TORNADO-6x* *stand-alone operation*.

If J6 jumper is set to 2-3 position (see fig.2-2 or fig.A-1), then the DSP reset signal is connected to the output of host ISA-bus I/O interface for *TORNADO-6x* *PC plug-in applications*.

TMS320C6x DSP Reset Controller (RC)

TORNADO-6x on-board DSP reset controller (RC) generates TMS320C6x DSP reset signal during *TORNADO-6x* stand-alone operation (jumper J6 is set to 1-2 position) in the following conditions:
- external power is switched on
- on-board DSP reset pushbutton SW2 is pressed (refer to fig.2-2 and fig.A-1)
- external active DSP reset signal is applied via JP10 connector (refer to fig.2-2 and fig.A-1)
- WDT feature is enabled and the WDT output is active.

Watchdog Timer (WDT)

TORNADO-6x feature watchdog timer (WDT), which generates the TMS320C6x DSP reset (restart) pulse if WDT is not cleared by DSP software within every 0.8 sec. This feature is useful in *TORNADO-6x* stand-alone operation of *TORNADO-6x* for increasing software and system operation reliability.

The WDT timer should be periodically reset by the DSP software by means of writing to the *WDT_CLR* IOX port of the DSP environment (refer to table 2-2). Data written to *WDT_CLR* IOX port is ignored.

The WDT feature is valid in the DSP stand-alone mode only and is enabled by the *WDT_EN* IOX flag (see table 2-2) in case the J6 DSP reset source selector is set to 2-3 position (i.e. the DSP reset input is connected to the output of DSP reset controller).

WDT_EN flag can be set by TMS320C6x DSP software by means of writing to the *WDT_EN* I/O port in the IOX area. Note, that when writing or reading to/from the *WDT_EN* IOX register, only bit D0 is valid.

WDT_EN IOX Register (r/w)

x	x	x	x	x	x	x	x	WDT_EN (r/w, 0+)
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

When *WDT_EN* flag is set to logical '0' (this value is set as default on TMS320C6x DSP reset), then the WDT feature is disabled, and WDT output is ignored by the DSP reset controller.

When *WDT_EN* flag is set to logical '1', then the WDT feature is enabled and the WDT output will generate the DSP reset signal in accordance with the described above procedure.

TMS32C6x DSP Bootmode Configurations

The TMS320C6x DSP bootmode configuration is defined by the jumper set J3-1..J3-5 (see fig.2-2 or fig.A-1). Recommended bootmode configurations are presented in table 2-4. Not shown bootmode

Table 2-4. TMS320C6x DSP Bootmode Configurations.

Bootmode ID	Description	jumper J3-4	jumper J3-3	jumper J3-2	jumper J3-1
BM#3 (boot from SBSRAM)	*Corresponds to C6x DSP bootmode #3* *MAP-0 memory map (SBSRAM at address=0h) with automatic setting of EMIF CE-0 area configuration for SBSRAM after reset is released*	ON	ON	OFF	OFF
BM#6 (boot from HPI)	*Corresponds to C6x DSP bootmode #6* *MAP-0 memory map (SBSRAM at address=0h); requires optional setting of EMIF CE-0 area configuration for SBSRAM via HPI.*	ON	OFF	OFF	ON
BM#11 (boot from 8-bit FLASH)	*Corresponds to C6x DSP bootmode #11* *MAP-0 memory map (SBSRAM at address=0h) with automatic setting of EMIF CE-0 area configuration for SBSRAM and EMIF CE-1 area for FLASH after reset is released.*	OFF	ON	OFF	OFF

Notes:
1. 'ON' corresponds to installed jumper; 'OFF' corresponds to removed jumper.
2. Not shown bootmode configurations are reserved and are not recommended for usage.
3. Highlighted configuration corresponds to the factory setting.

Setting EMIF Control Registers of TMS320C6x DSP

In order to provide correct operation of *TORNADO-6x* on-board hardware, be sure to setup TMS320C6x on-chip *EMIF Control Registers (EMIF_GCR, EMIF_CE0_SCR, EMIF_CE1_SCR, EMIF_CE3_SCR)* in your TMS320C6x DSP software application as the following:

- the *EMIF Global Control Register (EMIF_GCR)* register of TMS320C6x DSP should be programmed to 0x3078 hex value. This corresponds to the following settings:
    - SSCLK is enabled at ½1/2x CPU clock rate
    - CLKOUT1 and CLKOUT2 are enabled
    - external HOLD is enabled
- the *EMIF CE0 Space Control Register (EMIF_CE0_SCR)* register of TMS320C6x DSP should be programmed to 0x40 hex value in order to configure the EMIF CE-0 space for SBSRAM operation.
- the *EMIF CE1 Space Control Register (EMIF_CE1_SCR)* register of TMS320C6x DSP should be programmed to 0x8638d82 hex value in order to interface to 8-bit FLASH memory. This corresponds to the following settings:
    - 32-bit asynchronous mode is selected
    - read/write setup is set to 8 DSP cycles (40ns)
    - read/write strobe length is set to 24 DSP cycles (120ns)
    - read/write hold is set to 3 DSP cycles (15ns)

- the *EMIF CE2 Space Control Register (EMIF_CE2_SCR)* register of TMS320C6x DSP should be left unconfigured with the reset default value. This EMIF area is not used.
- the *EMIF CE3 Space Control Register (EMIF_CE1_SCR)* register of TMS320C6x DSP should be programmed to 0x31b3c623 hex value in order to interface to external 32-bit IOX and PIOX hardware. This corresponds to the following settings, which are preconditioned to meet the worst timing requirements when addressing the *WDT_CLR* IOX flag register with 100ns minimum write strobe width:
    - 32-bit asynchronous mode is selected
    - read/write setup is set to 3 DSP cycles (15ns)
    - read/write strobe length is set to 6 DSP cycles (30ns) with on-board hardware strobe width extension to 100ns when the *WDT_CLR* (clear watchdog timer) generation (write-only) IOX register is selected
    - read/write hold is set to 3 DSP cycles (15ns)

TMS320C6x HPI (host port interface)

TORNADO-6x offers access from host ISA-bus I/O interface to TMS320C6x on-chip 32-bit HPI (host port interface). All HPI features are supported, including mutual interrupt generation between host ISA-bus I/O interface and TMS320C6x DSP. For details about TMS320C6x HPI refer to original TI documentation and see the corresponding ISA-bus I/O Interface section later in this chapter.

SB Locking by the on-board TMS320C6x DSP Master

SB locking technique is used for processing of software shared semaphores that can be allocated in on-board SBSRAM or PIOX shared resources.

SB locking/unlocking by the on-board TMS320C6x DSP master is performed by means of *MLock* IOX flag (see table 2-2). *MLock* flag can be set by TMS320C6x DSP software by means of writing to the *MLock* I/O port in the IOX area. Note, that when writing or reading to/from *MLock* IOX register, only bit D0 is valid.

MLock IOX Register (r/w)

x	x	x	x	x	x	x	x	Mlock (r/w, 0+)
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

When *MLock* flag is set to logical '0' (this value is set as default on TMS320C6x DSP reset), then there is no active SB locking from on-board TMS320C6x DSP, and both TMS320C6x DSP and host ISA-bus memory interface can access shared SB resources.

When *MLock* flag is set to logical '1', then there is active SB locking from on-board TMS320C6x DSP and SB access from host ISA-bus memory interface will be pending until SB will be unlocked by TMS320C6x DSP (*MLock* flag will be set to logical '0').

The SB lock-to-unlock time interval is not limited by *TORNADO-6x* hardware, however long duration of SB locking by DSP may cause timeout access faults for SB accesses by host ISA-bus memory interface.

The following is an example of C-code for TMS320C6x DSP that demonstrates processing of shared software semaphore using SB locking technique:

                    ...

```
unsigned * MLock = *(unsigned *) 0x03000004;          /* declare MLock I/O port */
int Sem;                                              /* declare software shared semaphore Sem */
                    ...
                    while (1)
                    {
                       *Mlock=1;              /* lock SB */
                       if (Sem==0) break;     /* verify for semaphore is free (Sem=0)*/
                       *Mlock =0;             /* if Sem is busy, then unlock SB and repeat */
                    }

                    Sem=1;                    /* semaphore is free, set it to Sem=1 */
                    *Mlock =0;                /* and unlock SB  */
                    ...
                    ...                       /* perform some critical data processing */
                    ...
                    *Mlock =1;                /* reset semaphore using SB locking */
                    Sem=0;
                    *Mlock =0;                /* unlock SB */
                    ...
```

Note that *TORNADO-6x* provides hardware timeout control for SB granting wait time for host ISA-bus memory access. This hardware timeout interval is setup to 6 µsec. In case host timeout condition will occur because SB is locked by DSP, then the *SB_ERROR* flag in *SYS_STATUS_FRG* flag register of host ISA-bus I/O interface will be set to the *SB_ERROR*=1 state. This will cancel current host-to-SB request and returned data will be undefined. *SB_ERROR* flag can generate active host PC interrupt and can be reset by host PC software.

CAUTION

Time interval between SB locking and unlocking by the on-board TMS320C6x DSP should not exceed 6 µsec in order to avoid timeout condition for host-to-SB access.

Generating DSP-to-Host Requests

TORNADO-6x supports attention request (interrupt request) from the on-board TMS320C6x DSP to host IBM PC CPU in order to synchronize between program execution in host and on-board DSP environments. Two methods for generation of DSP-to-host requests are supported in *TORNADO-6x*:

- *MH_RQ* (master to host request), that results in setting flag *MH_RQ* in *SYS_STATUS_FRG* flag register in host ISA-bus I/O interface. *MH_RQ* is generated when the on-board TMS320C6x DSP executes I/O write cycle to *MH_RQ* IOX register (see table 2-2). Data written has no meaning and is ignored. Generation of *MH_RQ* DSP-to-host request results in setting flag *MH_RQ* in *FLAG STATUS REGISTER* of host ISA-bus I/O interface into the *MH_RQ*=1 state and may generate active host PC interrupt request in case *MH_RQ_IE* bit in the *CONTROL REGISTER* from host ISA-bus I/O interface is set to the *MH_RQ_IE*=1 state.. The following is an example of C-code for TMS320C6x DSP that generates request to the host PC:

```
                    ...
unsigned * MH_RQ = *(unsigned *) 0x03000000;          /* declare MH-RQ I/O port */
```

```
...
*MH_RQ=0;                    /* DSP-to-host request is generated */
...
```

- *HPI_HINT* (host interrupt request via HPI), that results in setting bit *HINT* of HPIC register of TMS320C6x HPI and flag *HPI_HINT* in *SYS_STATUS_FRG* flag register of host ISA-bus I/O interface. *HPI_HINT* can generate active host PC interrupt request in case *HPI_HINT_IE* bit in *HPI_IE_FRG* flag register from host ISA-bus I/O interface is set to *HPI_HINT_IE*=1 state.

Processing Requests from Host PC

TORNADO-6x supports attention request (interrupt request) from host PC to TMS320C6x DSP in order to synchronize between the program execution in host and on-board DSP environments. Two methods for generation of host-to-DSP requests is supported in *TORNADO-6x*:

- *HM_RQ* (host-to-master request), that results in generation of active *INT3* external interrupt request for the on-board TMS320C6x DSP. In order to generate output *HM_RQ* flag, host PC software has to write any data into *SET_HM_RQ_FRG* flag register from host ISA-bus I/O interface. User software for the TMS320C6x DSP should provide processing of *INT3* hardware interrupt request in accordance with software requirements. This is the recommended method for generation of host-to-DSP request since it delivers compatibility with all other *TORNADO* DSP systems for PC.
- *HPI_DSPINT* (host-to-DSP interrupt via HPI), that results in setting bit *DSPINT* in HPIC register of TMS320C6x HPI and generation *HPIINT* on-chip interrupt request for TMS320C6x DSP. In order to generate *HPI_DSPINT* interrupt request to DSP, host PC software has to write 0x03030303 hex value to HPIC register of TMS320C6x DSP via host ISA-bus I/O interface. User software for the TMS320C6x DSP should provide processing of *HPIINT* interrupt request in accordance with software requirements. This is the *TORNADO-6x* specific method for generation of host-to-DSP request, and it is recommended for simulation of host-to-DSP communication via TMS320C6x DSP on-chip HPI.

External Hardware Interrupts for TMS320C6x DSP

TORNADO-6x on-board TMS320C6x DSP supports four external hardware interrupt requests *INT0...INT3* with the *INT0* request having the highest priority. These requests correspond to the following events:

- *INT0...INT2* interrupt requests can be generated by SIOX/PIOX/PIOX-16 daughter-card modules
- *INT3* is on-board wired for software request *HM_RQ* from host PC to TMS320C6x DSP.

TORNADO-6x hardware provides direct wiring of external interrupt request source signals to the corresponding *INT0...INT3* pins of TMS320C6x DSP chip. All *INT0...INT3* external interrupt request pins of TMS320C6x DSP are edge-triggered and allow pulse or static external interrupt request signals to applied to these input pins.

> **CAUTION**
>
> *TORNADO-6x* hardware is designed for external DSP interrupts *INT0..INT3* with inverse polarity inputs.
>
> The TMS320C6x DSP *External Interrupt Polarity Register* should be programmed to 0x0000000F value in order to support inverse polarity external interrupts requests.

SIOX Interface Sites

TORNADO-62/67 provides two serial I/O expansion interface (SIOX) sites (SIOX-A and SIOX-B) for compatible AD/DA/DIO daughter-card modules.

TORNADO-62MX/67MX provides one serial I/O expansion interface (SIOX) site (SIOX-A) for compatible AD/DA/DIO daughter-card modules. Site SIOX-A of *TORNADO-62MX/67MX* has two paralleled connectors for installation of AD/DA/DIO daughter-card module in either horizontal (recommended for installation into regular PC chassis) or vertical orientation (recommended for installation into MicroPC chassis).

SIOX comprises of the TMS320C6x DSP-on-chip McBSP-0/McBSP-1 serial ports control lines, DSP-on-chip timers TM-0/TM-1 input/output, *INT0..2* external interrupt requests and ±5v/±12v ISA-bus power supply lines. For details about SIOX sites refer to the corresponding section later in this chapter.

PIOX and PIOX-16 Interface Sites

TORNADO-62/67 provides one site for 32/16-bit parallel I/O expansion (PIOX/PIOX-16) site for compatible AD/DA/DIO and DSP coprocessor daughter-card modules.

TORNADO-62MX/67MX provides one site for 16-bit parallel I/O expansion (PIOX-16) site for compatible AD/DA/DIO daughter-card modules.

PIOX/PIOX-16 site comprises of the TMS320C6x DSP data and address buses, data strobes, DSP-on-chip timers TM-0/TM-1 input/output, *INT0..2* external interrupt requests and ±5v/±12v ISA-bus power supply lines. For details about PIOX/PIOX-16 sites refer to the corresponding section later in this chapter.

Generating Reset Signals for SIOX/PIOX Expansion Interface Sites

TORNADO-6x allows generation of individual reset signals for SIOX and PIOX/PIOX-16 expansion interface sites (refer to the corresponding sections earlier in this chapter) using the following logical conditions:
- all SIOX/PIOX reset signals are active in case on-board DSP is in the 'RESET' state
- the corresponding SIOX/PIOX reset signal(s) might be released only in case DSP is in the 'RUN' state and the corresponding bit(s) of *PXSX_RUN* IOX register is(are) set to logical '1' value by DSP software.

This allows correct initialization of the SIOX/PIOX daughter-card hardware and correct synchronization with the DSP software.

CAUTION

TORNADO-62/67 rev.2A hardware provides different on-board logic for generation of
SIOX/PIOX reset signals if compared to *TORNADO-62/67* rev.1.x hardware.

TORNADO-6x rev.1x generates common SIOX/PIOX reset signal using *XRESET* IOX
register, and this reset signal was generated as the logical OR between the DSP reset signal
and bit D0 of *XRESET* IOX register.

PXSX_RUN IOX register comprises of bits for individual 'RESET' control of PIOX/PIOX-16, SIOX-A and
SIOX-B (*TORNADO-62/67* only) interface sites.

PXSX_RUN IOX register might be set by the TMS320C6x DSP software only (refer to table 2-2). Note, that
when writing or reading to/from *PXSX_RUN* IOX register, only bits D0..2 are valid.

PXSX_RUN IOX Register (r/w)

x	x	x	x	x	x	SIOX-B_RUN (r/w, 0+) (TORNADO-62/67) x (TORNADO-62MX/67MX)	SIOX-A_RUN (r/w, 0+)	PIOX_RUN (r/w, 0+)
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

In case the DSP is in the 'RUN' state (refer to section 2.5 for more details), then the corresponding reset signals
for SIOX/PIOX expansion interface sites might be released by means of writing '1' value to the corresponding
bit of *PXSX_RUN* IOX flag register, and this will allow operation of the corresponding SIOX/PIOX daughter-
card hardware. Writing logical '0' to the corresponding bit of *PXSX_RUN* IOX flag register, which is also the
default value on the DSP reset condition, will set the corresponding reset signal for SIOX/PIOX expansion
interface sites.

External Power Connector for Stand-alone Operation

In case *TORNADO-6x* is used for stand-alone applications outside of host ISA-bus PC chassis, then the on-
board external power connector JP9 (see fig.2-2 and fig.A-1) provide connection to external power source. Note,
that although *TORNADO-6x* provides connection to external ±5v and ±12v power sources, only +5v power
source is actually required for operation of on-board *TORNADO-6x* hardware. Other power lines -5v and ±12v
are wired to PIOX/PIOX-16 and SIOX daughter-card sites.

2.4   Host ISA-bus Memory Interface

Host ISA-bus memory interface of *TORNADO-6x* is designed to transfer data between host IBM PC
environment and *TORNADO-6x* on-board SBSRAM/FLASH/PIOX SB resources without any software
overhead for both host PC and on-board TMS320C6x DSP.

Operation Description

The SB address space via host ISA-bus memory interface appears as a series of dual-access 32KB *shared memory pages* (*SMP*) that are mapped onto the ISA-bus UMB (upper memory blocks) memory window by means of *SB PAGE MAPPER* register from host ISA-bus I/O interface.

The SB can be accessed by host ISA-bus memory interface by means of random accesses to software variables or data arrays that are allocated within *SMP*, or by means of block data transfers between PC main memory and *SMP* using either host i80x86 CPU MOVSB/MOVSW/etc instructions or host DMA controller.

Host ISA-bus memory interface issues SB request and provides SB access using 8-/16/32-bit data cycles each time host PC performs ISA-bus memory read/write cycle within the ISA-bus *SMP* address range. Particular selection of the UMB area is performed by host software by programming the *ISA_MI_BADDR_FRG* flag register of host ISA-bus I/O interface.

SMP ISA-bus Memory Base Address

SMP ISA-bus memory base address can be set within the ISA-bus UMB (upper memory blocks) memory address range by means of programming the *ISA_MI_BADDR_FRG* flag register from *TORNADO-6x* host ISA-bus I/O interface (see section 2.5) in accordance with predefined configuration settings in table 2-5. Only three least significant bits of *ISA_MI_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes.

ISA_MI_BADDR_FRG Flag Register (r/w)

0	0	0	0	0	MI_BA2 (r/w, 0+)	MI_BA1 (r/w, 0+)	MI_BA0 (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-5.   ISA-bus memory base address for *SMP*.

ISA-bus memory base address for *SMP*	ISA-bus memory address range for *SMP*	bit settings for *ISA_MI_BADDR_FRG* flag register		
		bit#2 *MI_BA2*	*bit#1* *MI_BA1*	*bit#0* *MI_BA0*
SMP is switched OFF	-	0	0	0
B8000H	*B8000H ... BFFFFH*	0	0	1
C0000H	*C0000H ... C7FFFH*	0	1	0
C8000H	*C8000H ... CFFFFH*	0	1	1
D0000H	*D0000H ... D7FFFH*	1	0	0
D8000H	*D8000H ... DFFFFH*	1	0	1
E0000H	*E0000H ... E7FFFH*	1	1	0
E8000H	*E8000H ... EFFFFH*	1	1	1

Notes: 1. The highlighted configuration corresponds to power on default
value.

TORNADO-6x, as well as all other *TORNADO* DSP systems for ISA-bus hosts, offers software control for the *SMP* activity, i.e. switching *SMP* either 'ON' or 'OFF' in the ISA-bus memory address space.

CAUTION

SMP is activated and appears in ISA-bus memory address space after writing any non-zero value to *ISA_MI_BADDR_FRG* flag register in accordance with table 2-4.

SMP is deactivated and disappears from ISA-bus memory address space after writing the zero value o *ISA_MI_BADDR_FRG* flag register.

Software control over *SMP* activity in *TORNADO-6x* delivers optimal utilization of UMB area in host PC and allows multiple *TORNADO* DSP systems to share the same UMB area within one PC environment.

Addressing the SB data via Host ISA-bus Memory Interface

The host ISA-bus memory interface provides access to three SB address areas:
- *SBSRAM* area (or SRAM)
- *FLASH* memory area

- *PIOX or PIOX-16* I/O area.

Particular selection of the accessed SB address area as well as selection of *SMP* is performed by 16-bit *SB PAGE MAPPER* register from host ISA-bus I/O interface. For details about the *SB PAGE MAPPER* register programming please refer to subsection "SMP PAGE MAPPER Register" in section "Host ISA-bus I/O Interface" later in this chapter. The *SB PAGE MAPPER* register bit format is as the following:

SB PAGE MAPPER (LSB)   (r/w)

0	A21 (r/w, 0+)	A20 (r/w, 0+)	A19 (r/w, 0+)	A18 (r/w, 0+)	A17 (r/w, 0+)	A16 (r/w, 0+)	A15 (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

SB PAGE MAPPER (MSB)   (r/w)

SBA-1 (r/w, 0+)	SBA-0 (r/w, 0+)	0	0	0	0	0	0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Bits *A15..A21* select the particular *SMP*, which has the size 32KB, whereas bits *SBA-0..1* define the particular SB area in accordance with table 2-8.

CAUTION

TORNADO-6x provides relative byte addressing within the particular SB area (SBSRAM/FLASH/PIOX) for the SB data when SB is accessed by host ISA-bus memory interface (refer to table 2-1).

This means that although each of the SB address areas (SBSRAM, FLASH or PIOX/PIOX-16) has absolute 32-bit address within the TMS320C6x DSP environment, the corresponding address for host ISA-bus memory interface is set relative to the base address of this SB area with the SB area code specified in two upper bits of *SB PAGE MAPPER* register from host ISA-bus I/O interface.

The following are few examples for setting the SB address and *SB PAGE MAPPER* register when accessing the SB data from host ISA-bus memory interface:

- *Example 1*: TMS320C6x DSP address is 0x00020005 for accessing the location within the SBSRAM area. The corresponding address for host ISA-bus memory interface will be 0x0005 with the *SMP* #0x0004 and SB area @SBSRAM, i.e. the *SB PAGE MAPPER* should be programmed to the 0x0004 hex value.
- *Example 2*: TMS320C6x DSP address is 0x01100008 for accessing the location within the FLASH area. The corresponding address for host ISA-bus memory interface will be 0x0008 with the *SMP* #0x0010 and SB area @FLASH, i.e. the *SB PAGE MAPPER* should be programmed to the 0x4014 hex value.
- *Example 3*: TMS320C6x DSP address is 0x0380000A for accessing the location within the PIOX area. The corresponding address for host ISA-bus memory interface will be 0x000A with the *SMP* #0x0000 and SB area @PIOX, i.e. the *SB PAGE MAPPER* should be programmed to the 0xC000 hex value.

- *Example 4*: TMS320C6x DSP address is 0x03000004 for accessing the *Mlock* flag register. There is no way to access the DSP IOX area from host ISA-bus memory interface.

Accessing SB Data from PC Host Software via ISA-bus Memory Interface

Once *TORNADO-6x* host ISA-bus memory interface provides direct mapping of 32KB *SMP* onto ISA-bus UMB window, then the following host-to-SB data transfer techniques are applicable:
- *random access to variables or data arrays* allocated anywhere within the *SMP* by host PC software
- *block data transfers using MOVS/MOVSB/MOVSW instructions* of host PC i80x86 CPU
- *block data transfers under control of host PC DMA controller* using memory-to-memory or memory-to-port transfer cycles.

Timing Diagram Description for Host ISA-bus Memory Interface

The SB access from host ISA-bus memory interface is performed under hardware control of the on-board programmable *SB Access Controller* from ISA-bus interface of *TORNADO-6x*. Timing diagram for SB read cycle invoked by ISA-bus memory interface is presented at fig.2-3. Understanding of *SB Access Controller* operation is recommended for those applications, which require perfect evaluation of possible time delays when accessing the SB data from ISA-bus memory interface.
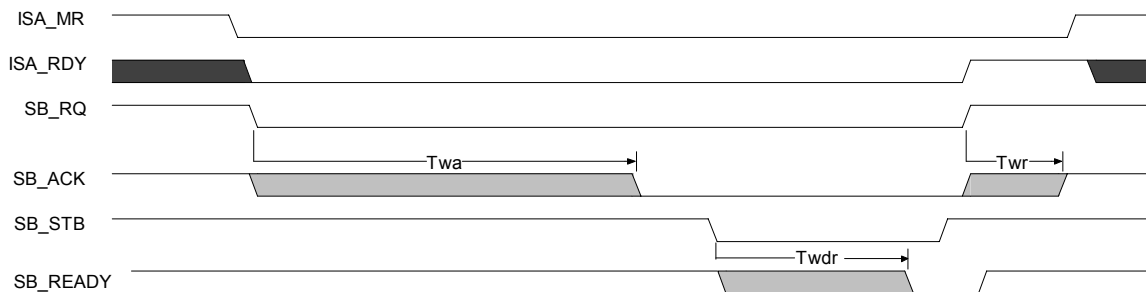

Fig.2-3. Timing diagram of SB read cycle invoked by ISA-bus memory interface.

> **CAUTION**
>
> Any host request to SB data will set the upcoming TMS320C6x DSP request to SB data (SBSRAM/FLASH/PIOX) to the pending condition upon host request is completed, and, therefore will introduce delays into real-time functionality of DSP software.
>
> Host ISA-bus memory interface of *TORNADO-6x* DSP System is designed to minimize these delays to a minimum of available.
>
> Host request to SB data will not introduce any time delays into operation of TMS320C6x DSP in case the latter is executing the program from on-chip cache or program memory while accessing the DSP on-chip data memory.

Any request to the *SMP* memory address space on the host ISA-bus (*ISA_MR*=0 or *ISA_MW*=0) will result in activation of host ISA-bus memory interface that will immediately generate request to SB arbiter (*SB_RQ*=0) and set ISA-bus data ready signal to 'NOT READY' state (*ISA_RDY*=0). Host ISA-bus interface will stay in this state until SB will be granted (*SB_ACK*=0) by SB arbiter. SB will be granted at least after T_{wa} delay. After that, the SB access cycle will be generated by host ISA-bus memory interface with *SB_STB* signal set to the *SB_STB*=0 state. Host ISA-bus memory interface will now wait for *SB_READY* signal comes true (*SB_READY*=0) in order to finish current SB access cycle. SB data ready signal *SB_READY* will come true (*SB_READY*=0) after T_{wdr} delay after *SB_STB* will come active (*SB_STB*=0). Wait time for *SB_READY* signal depends upon the SB address subspace selected (see table 2-1). Minimum wait time for *SB_READY* data ready signal is T_{wdr}=0ns and corresponds to access to the on-board SBSRAM area, whereas accesses to FLASH and PIOX areas require some wait-state time with further awaiting for *SB_READY* or *PIOX_READY* signal set to true. After *SB_READY* signal sets true, the *SB_RQ* signal is removed (*SB_RQ*=1) and *ISA_RDY* signal is set to *ISA_RDY* =1 state in order to finish current ISA-bus memory access cycle. *SB_ACK* signal will return to its inactive state (*SB_ACK*=1) within T_{wr} after *SB_RQ* will be removed (*SB_RQ*=1).

SB Access Timeout Control

TORNADO-6x provides hardware timeout control for wait times for SB granting and for *SB_READY* signals when SB is accessed by host ISA-bus memory interface. This is required in order to avoid idling and crashing of host PC environment while host waits for the SB granted during indefinite time period.

Hardware timeout for every of SB granting and SB data ready signals are set to 6 usec. Once SB granting timeout condition occurs, then the *SB_ERROR* bit in *SYS_STATUS_FRG* flag register from host ISA-bus I/O interface is set to the *SB_ERROR*=1 state. This will cancel current host-to-SB access and returned data will be undefined. The *SB_ERROR*=1 condition can generate interrupt reqeust to host PC in case *SB_ERROR_IE* bit of *CONTROL REGISTER* of host ISA-bus I/O interface is set to the '1' state.

The *SB_ERROR* bit can be reset by host software by writing to the *CLEAR_SB_ERROR_FRG* write-only flag register of host ISA-bus I/O interface.

Data Transfer Formats for Host SB Data Access Cycles

TORNADO-6x supports 8/16/32-bit SB data access cycles for both DSP and host ISA-bus memory interface.

Host ISA-bus memory interface offers special advanced features in order to minimize induced time delays into functionality of TMS320C6x DSP while the latter accesses the SB data.

Although PC can access *SMP* data using both from standard 8-bit or 16-bit ISA-bus memory cycles, special on-board hardware allows temporary storage of transferred data in order to reduce number of forwarded accesses to SB in case the accessed data format is either 16-bit or 32-bit data words.

The format of SB data cycle, when SB is accessed via host ISA-bus memory interface, can be by host software by means of programming the *SB_CCL* bit field {*SB_CCL-0*,*SB_CCL-1*} of *CONTROL REGISTER* from host ISA-bus I/O interface in accordance with table 2-6.

Table 2-6.   Data formats for host SB data transfer cycles.

Format of SB data cycle	*SB_CCL* bit field setting of *CONTROL REGISTER* from ISA-bus I/O interface		description
	SB_CCL-0	*SB_CCL-1*	
8-bit data cycle (power-on reset value)	0	0	Host SB data cycle is generated each time host PC CPU executes ISA-bus memory read/write cycle within *SMP* ISA-bus memory address range. Actual byte selection within the addressed SB 32-bit word is performed by ISA-bus address bits {*A0, A1*}. *SMP* appears as the 32KB linear byte space.
16-bit data cycle	1	0	Host SB data cycle is generated when host PC CPU performs either ISA-bus memory read cycle for even (*A0*=0) byte or ISA-bus memory write cycle for odd (*A0*=1) byte within the *SMP* ISA-bus memory address range. This cycle is also generated in case host PC CPU performs ISA-bus memory read/write cycle for 16-bit words allocated at the even (*A0*=0) address boundary. When this data cycle format is set and host PC CPU performs memory byte accesses to other bytes of *SMP*, then no SB data cycle is generated and data is read/written from/to the on-board bi-directional register transceivers. Actual 16-bit word selection within the addressed SB 32-bit word is performed by ISA-bus address bit *A1*. *SMP* appears as a linear 16Kx16 space of 16-bit words.
32-bit data cycle	0	1	SB data cycle is generated only when host CPU performs ISA-bus memory read of the least significant byte (*A0=A1=0*) or memory write of the most significant byte (*A0=A1=1*) of the 32-bit memory words within *SMP* ISA-bus memory address range. When host CPU accesses other bytes of the *SMP* then no SB data cycle is generated and data is read/written from/to the on-board bi-directional register transceivers. SB data are transferred as 32-bit data words. *SMP* appears as a linear 8Kx32 space of 32-bit words.
-	1	1	Reserved. Do not use.

Notes: 1. The highlighted configuration corresponds to default power on value.

Data format for host SB data access cycle can be changed by host software during *TORNADO-6x* operation and depends upon user requirements for host and resident DSP software.

8-bit data cycles are the recommended selection when host software either assumes *SMP* to appear as a linear set of bytes (as well as of 16-bit words or 32-bit words), or when host software may require access to any random selected byte of *SMP* data. In this case the SB data cycle is generated each time when host PC CPU or DMA controller perform ISA-bus *SMP* memory access cycle.

16-bit data cycles are the recommended selection when host software assumes *SMP* to appear as a linear set of either 16-bit words or 32-bit words. In this case the SB data cycle is generated when host PC CPU either reads even *SMP* memory bytes or writes to odd *SMP* memory bytes while other byte is stored in the on-board register transceiver. The 16-bit host data cycle format normally saves about 50% time required for equivalent 8-bit SB access cycles.

32-bit data cycles are the recommended selection when host software assumes *SMP* to appear as a linear set of 32-bit words. In this case the SB data cycle is generated when host PC CPU either reads least significant byte of 32-bit *SMP* memory words of writes to most significant byte of 32-bit *SMP* memory words while other bytes are stored in the on-board register transceiver. The 32-bit data cycle format normally saves about 75% time required for equivalent 8-bit SB access cycles.

SB Locking by ISA-bus Memory Interface

SB locking by ISA-bus memory interface is useful for preventing SB access from TMS320C6x DSP while processing shared semaphores allocated in SBSRAM/FLASH/PIOX shared SB resources.

SB locking by ISA-bus memory interface can be set by host PC software by means of programming either the *SB_GLOCK* bit or *SB_LOCK* bit of *CONTROL REGISTER* from ISA-bus I/O interface.

Timing diagrams of SB locking using *SB_GLOCK* and *SB_LOCK* bits are presented at fig. 2-4 and fig. 2-5.
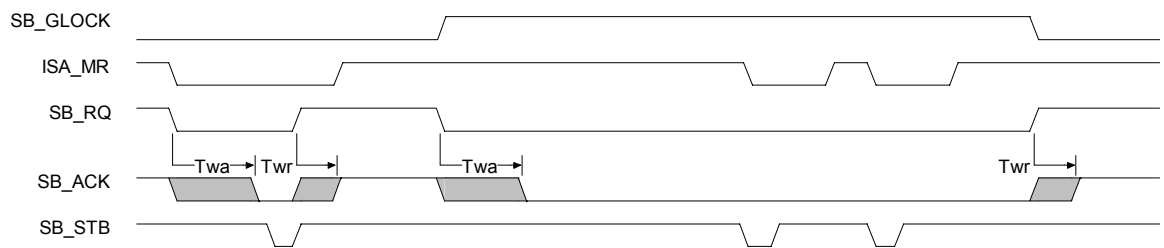
Fig.2-4. Timing diagram for SB access cycle invoked by ISA-bus memory interface with SB locking using *SB_GLOCK* bit.
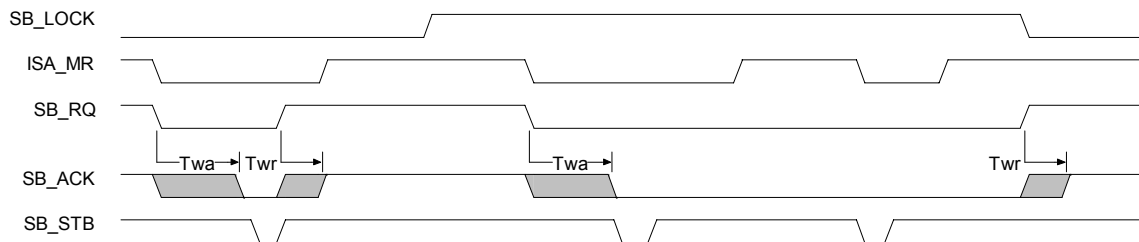
Fig.2-5. Timing diagram for SB access cycle invoked by ISA-bus memory interface with SB locking using *SB_LOCK* bit.

CAUTION

SB locking by ISA-bus memory interface using *SB_GLOCK* and *SB_LOCK* bits of *CONTROL REGISTER* from ISA-bus I/O interface should be used for short-time SB locking.

Continuous SB locking by ISA-bus memory interface using *SB_GLOCK* and *SB_LOCK* bits may result in continuous holding of TMS320C6x DSP (in case it requests access to SB data) and may lead to significant time distortions of real-time data processing.

2.5   Host ISA-bus I/O Interface

TORNADO-6x host ISA-bus I/O interface is designed for *TORNADO-6x* system control, accessing TMS320C6x DSP on-chip HPI from host software, and interrupt handshaking between host PC CPU and TMS320C6x DSP.

I/O Base Address of Host ISA-bus I/O Interface

Host ISA-bus I/O interface occupies sixteen 8-bit registers inside ISA-bus I/O address space. Base address of host ISA-bus I/O interface is defined by means of 3-button on-board DIP-switch SW1 (see fig.2-1) in accordance with predefined settings listed in table 2-7.

Table 2-7. ISA-bus I/O base address for host ISA-bus I/O interface.

ISA-bus I/O base address	ISA-bus I/O address range	button SW1-3	button SW1-2	button SW1-1
300H	*300H..30FH*	OFF	OFF	OFF
310H	*310H..31FH*	OFF	OFF	ON
320H	*320H..32FH*	OFF	ON	OFF
330H	*330H..33FH*	OFF	ON	ON
340H	*340H..34FH*	ON	OFF	OFF
350H	*350H..35FH*	ON	OFF	ON
360H	*360H..36FH*	ON	ON	OFF
370H	*370H..37FH*	ON	ON	ON

Note: 1. Highlighted configuration corresponds to the factory setting.

ISA-bus I/O Interface Registers

List of *TORNADO-6x* ISA-bus I/O interface registers is presented in table 2-8.

Table 2-8.   Register set of Host ISA-bus I/O interface.

register #	register address	access mode	reset value	description
#0	*BA+0*	r/w	0	*SB PAGE MAPPER* (*LSB*)
#1	*BA+1*	r/w	0	*SB PAGE MAPPER* (*MSB*)
#2	*BA+2*	r/w	0	*CONTROL REGISTER*
#3	*BA+3*	r/w	-	*FLAG DATA REGISTER* *or*
		r w	- -	*FLAG STATUS REGISTER* *FLAG CONTROL REGISTER*
#403H	*BA+0x403*	r/w	0	*FLAG SELECTOR REGISTER*
#4	*BA+4*			reserved (do not use)
#5	*BA+5*			reserved (do not use)
#6	*BA+6*			reserved (do not use)
#7	*BA+7*			reserved (do not use)
#8	*BA+8*	r/w	see TI documentation	HPIC (LSB of LSW) register (TMS320C6x HPI)
#9	*BA+9*	r/w	see TI documentation	HPIC (MSB of LSW) register (TMS320C6x HPI)
#0AH	*BA+0xA*	r/w	see TI documentation	HPIC (LSB of MSW) register (TMS320C6x HPI)
#0BH	*BA+0xB*	r/w	see TI documentation	HPIC (MSB of MSW) register (TMS320C6x HPI)
#0CH	*BA+0xC*	r/w	-	HPI Address Latch (LSB of LSW) register (HPIA), (TMS320C6x HPI)
#0DH	*BA+0xD*	r/w	-	HPI Address Latch (MSB of LSW) register (HPIA), (TMS320C6x HPI)
#0EH	*BA+0xE*	r/w	-	HPI Address Latch (LSB of MSW) register (HPIA), (TMS320C6x HPI)
#0FH	*BA+0xF*	r/w	-	HPI Address Latch (MSB of MSW) register (HPIA), (TMS320C6x HPI)

#408H	BA+0x408	r/w	-	HPI Data Latch (LSB of LSW) register (HPID_AI) with HPI address autoincrement facility (TMS320C6x HPI)
#409H	BA+0x409	r/w	-	HPI Data Latch (MSB of LSW) register (HPID_AI) with HPI address autoincrement facility (TMS320C6x HPI)
#40AH	BA+0x40A	r/w	-	HPI Data Latch (LSB of MSW) register (HPID_AI) with HPI address autoincrement facility (TMS320C6x HPI)
#40BH	BA+0x40B	r/w	-	HPI Data Latch (MSB of MSW) register (HPID_AI) with HPI address autoincrement facility (TMS320C6x HPI)
#40CH	BA+0x40C	r/w	-	HPI Data Latch (LSB of LSW) register (HPID) without HPI address autoincrement facility (TMS320C6x HPI)
#40DH	BA+0x40D	r/w	-	HPI Data Latch (MSB of LSW) register (HPID) without HPI address autoincrement facility (TMS320C6x HPI)
#40EH	BA+0x40E	r/w	-	HPI Data Latch (LSB of MSW) register (HPID) without HPI address autoincrement facility (TMS320C6x HPI)
#40FH	BA+0x40F	r/w	-	HPI Data Latch (MSB of MSW) register (HPID) without HPI address autoincrement facility (TMS320C6x HPI)

Notes:
1. '*BA*' denotes ISA-bus I/O base address of host ISA-bus I/O interface (table 2-6).
2. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.
3. '*LSB*' denotes Least Significant Byte; '*MSB*' denotes Most Significant Byte; '*LSW*' denotes Least Significant 16-bit Word; '*MSW*' denotes Most Significant 16-bit Word
4. All HPI registers access should be performed with bit *HWOB* of HPI HPIC register being set to *HWOB*=1 value. This correspond to the LSW first data transmission protocol for ISA-bus host.

SB PAGE MAPPER Register

Registers #0 and #1 of *TORNADO-6x* ISA-bus I/O interface are least significant byte (LSB) and most significant byte (MSB) of 16-bit *SB PAGE MAPPER* register, which is used to setup the *SMP* SB base address in for SBSRAM/FLASH/PIOX SB areas in 16Kx16 (32Kx8) increments. Reset value for *SB PAGE MAPPER* register is 0x0000.

SB PAGE MAPPER LSB register comprises of bits *A15..A21* for selection of particular *SMP* for host-to-SB access, whereas *SB PAGE MAPPER MSB* register comprises of bits *SBA-0..1* bits for the SB area selector in accordance with table 2-9.

All other bits of *SB PAGE MAPPER LSB* and *SB PAGE MAPPER MSB* registers are ignored on writing and read as zeros. The *A2..A14* bits of SB address for SB words within *SMP* are derived from ISA-bus memory address bits *ISA_A2..ISA_A14*, whereas address bits *ISA_A0..1* are used to select the particular byte within addressed 32-bit SB data word.

SB PAGE MAPPER (LSB) (r/w)

0	A21 (r/w, 0+)	A20 (r/w, 0+)	A19 (r/w, 0+)	A18 (r/w, 0+)	A17 (r/w, 0+)	A16 (r/w, 0+)	A15 (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

SB PAGE MAPPER (MSB) (r/w)

SBA-1 (r/w, 0+)	SBA-0 (r/w, 0+)	0	0	0	0	0	0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

CAUTION

SB address space for *TORNADO-6x* is the address space for 8-bit BYTE data words.

The 16-bit SB data words are allocated on the x2 odd address boundaries.

The 32-bit SB data words are allocated on x4 address boundaries.

CAUTION

TORNADO-6x provides relative byte addressing within the particular SB area (SBSRAM/FLASH/PIOX) for the SB data when SB is accessed by host ISA-bus memory interface (refer to table 2-1 and paragraph "Host ISA-bus Memory Interface" earlier in this chapter).

Particular SB area accessed is defined by bits *SBA-0..1* of *SB PAGE MAPPER MSB* register in accordance with table 2-9.

Table 2-9. SB Area Selector for Host-to-SB Accesses.

SB Area	*SBA-1* bit of SB PAGE MAPPER MSB register	*SBA-0* bit of SB PAGE MAPPER MSB register
SBSRAM area 1Mx32 for *TORNADO-62/67* 512Kx32 for *TORNADO-62MX/67MX*	0	0
SBSRAM/DATA area 1Mx8	0	1
reserved, do not use	1	0
PIOX area 512Kx32 for *TORNADO-62/67* *PIOX-16 area* 64Kx16 for *TORNADO-62MX/67MX*	1	1

Note: 1. Highlighted configuration corresponds to default power-on setting.

CONTROL REGISTER

Register #2 of *TORNADO-6x* ISA-bus I/O interface is known as **CONTROL REGISTER**. It is used for reset control of the on-board TMS320C6x DSP, for configuration of ISA-bus memory interface and for DSP-to-host interrupt communication.

CONTROL REGISTER (r/w)

SB_ERROR_IE *(r/w, 0+)*	MH_RQ_IE *(r/w, 0+)*	SB_CCL-1 *(r/w, 0+)*	SB_CCL-0 *(r/w, 0+)*	SB_LOCK *(r/w, 0+)*	SB_GLOCK *(r/w, 0+)*	0 *(reserved)*	M_GO *(r/w, 0+)*
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-10 contains detail description for bits and bit fields of **CONTROL REGISTER**. Note, that reserved bits of **CONTROL REGISTER** are ignored on writing and read as shown above.

Table 2-10. Bits and bit fields of *CONTROL REGISTER*.

bit/field of CONTROL REGISTER	power on default value	description
M_GO	0	*On-board TMS320C6x DSP reset line* control: • '0' corresponds to the RESET state for the on-board TMS320C6x DSP • '1' corresponds to GO (RUN) state for the on-board TMS320C6x DSP (i.e. the on-board DSP is in the program execution mode)
SB_GLOCK	0	*SB Global Lock*. With the *SB_GLOCK*=1 the SB access controller of ISA-bus memory interface generates immediate active SB locking.
SB_LOCK	0	*SB Lock*. With the *SB_LOCK*=1 the SB access controller of ISA-bus memory interface generates active SB locking starting from first next SB request cycle after the *SB_LOCK* bit is set to the *SB_LOCK*=1.
SB_CCL-1, SB_CCL-0	{0,0}	*SB Cycle format selector for Host-to-SB data transfers* : • {0,0} corresponds to 8-bit host SB data transfer cycle • {0,1} corresponds to 16-bit host SB data transfer cycle • {1,0} corresponds to 32-bit host SB data transfer cycle • {1,1} is reserved, do not use
MH_RQ_IE	0	*Master TMS320C6x DSP to Host Request Interrupt Enable*. If *MH_RQ_IE*=1 and *MH_RQ*=1, active interrupt request to host PC is generated. Host PC interrupt request is logical OR between (*MH_RQ_IE & MH_RQ*), (*SB_ERROR_IE & SB_ERROR*), (*HPI_ERROR_IE & HPI_ERROR*) and (*HPI_HINT_IE & HPI_HINT*) conditions.
SB_ERROR_IE	0	*SB Error Interrupt Enable*. If *SB_ERROR_IE*=1 and *SB_ERROR*=1, active interrupt request to host PC is generated. Host PC interrupt request is logical OR between (*MH_RQ_IE & MH_RQ*), (*SB_ERROR_IE & SB_ERROR*), (*HPI_ERROR_IE & HPI_ERROR*) and (*HPI_HINT_IE & HPI_HINT*) conditions.

Accessing the TMS320C6x DSP memory areas via DSP on-chip HPI

TORNADO-6x host ISA-bus I/O interface supports optional DSP-to-host communication via TMS320C6x DSP on-chip 32-bit host-port interface (HPI). Please refer to original TI documentation about details on TMS320C6x HPI.

> **CAUTION**
>
> The TMS320C6x DSP on-chip HPI port of *TORNADO-6x* DSP systems can operate only when DSP is in the 'RUN' state.

Along with the SB facility of *TORNADO-6x*, the TMS320C6x DSP on-chip HPI is another powerful data path for communication between DSP and host PC via full 32-bit DSP address space including all DSP on-chip memory areas.

> **CAUTION**
>
> *TORNADO-6x* provides absolute 32-bit byte addressing capabilities when accessing the TMS320C6x DSP memory areas via DSP on-chip HPI port (refer to original TI TMS320C6x documentation for details.)

Along with data transfer, mutual DSP-to-host (*HPI_HINT*) and host-to-DSP (*HPI_DSPINT*) interrupts via HPI are supported. On the host side, the *HPI_HINT* DSP-to-host interrupt can be individually masked and generate PC ISA-bus interrupt.

> **CAUTION**
>
> All host-to-HPI accesses to HPIC, HPIA and HPID_AI/HPID registers of TMS320C6x DSP HPI should be performed as to 32-bit I/O registers using two sequential 16-bit data words: LSW first, MSW last. Any violation of this may result in invalid data passed.
>
> Bit *HWOB* of HPIC register should be set to logical '1' prior any further data transfer will be performed via HPI and HPI address will be loaded. This corresponds to 16-bit LSW first communication via ISA-bus.

Timeout Control for Host-to-HPI Access

In accordance with TMS320C6x DSP specifications, the host-to-HPI access is allowed only in case the DSP is in the program execution mode, i.e. the DSP reset input is released. This is also true in case the HPI bootmode is selected (BM#6 from table 2-3) after the DSP reset input is released, since HPI bootload is performed with the DSP reset released although the DSP on-chip kernel is actually in the reset state.

All host-to-HPI data transfers are acknowledged with the *HPI_READY* hardware signal, which is an output from TMS320C6x DSP. Normally, *HPI_READY* signal comes true within several DSP cycles to confirm end of HPI data transfer.

In case the HPI is accessed while either the DSP is in the reset state or either DSP was placed into PD2 or PD3 conditions (by means of writing '1' to either of PD2 or PD3 bits of PRWD field of DSP on-chip CSR register), which results in DSP on-chip clock stopped, then this host-to-HPI access will be pended with *HPI_READY*

hardware signal set to false state until the DSP reset will be released. This might result in infinite host ISA-bus idling and crashing host PC environment unless special hardware timeout control for host-to-HPI access cycles was not used in all *TORNADO-6x* DSP systems.

In order to avoid host ISA-bus idling, *TORNADO-6x* host ISA-bus I/O interface features hardware timeout control for host-to-HPI accesses. The timeout interval for host-to-HPI access is equal to 6 μsec.

Once HPI timeout will occur, this will result in setting active *HPI_ERROR* flag (*HPI_ERROR*=1) in *SYS_STATUS_FRG* flag register. Furthermore, once *HPI_ERROR* flag is set, all succeeding host-to-HPI accesses will be canceled and returned data will be invalid until host will recognize and clear *HPI_ERROR* flag by means of writing to *CLEAR_HPI_ERROR_FRG* flag register.

CAUTION

If TMS320C6x DSP is in the RESET state or DSP software has set either of PD2 or PD3 bits of PRWD field DSP on-chip CSR register, then this will result in pending host-to-HPI access with 6 μsec host-to-HPI access timeout.

In this case the *HPI_ERROR* bit is set to '1' in *SYS_STATUS_FRG* flag register and the current host-to-HPI access will be cancelled.

All further host-to-HPI accessed will be ignored by *TORNADO-6x* Host ISA-bus I/O interface until *HPI_ERROR* flag will be cleared by host.

Note, that active state of *HPI_ERROR* flag may generate host interrupt in case *HPI_ERROR_IE* bit in *HPI_IE_FRG* flag register is set to *HPI_ERROR_IE*=1 state.

FLAG Registers

Registers #3 and #403H of *TORNADO-6x* ISA-bus I/O interface are used for auxiliary control (*flags*) of *TORNADO-6x*.

Optional flags (data bits and control signals) are comprised into a set of multiplexed 8-bit *flag registers*. Particular *flag register* is addressed by *FLAG SELECTOR REGISTER* (register #403H). Flags within a currently addressed (selected) *flag register* can be read/written using I/O read/write operation into *FLAG DATA REGISTER* (register #3).

FLAG SELECTOR REGISTER is available for I/O r/w operations has the following data format:

FLAG SELECTOR REGISTER   (read/write)

FSEL-7 (r/w, 0+)	FSEL-6 (r/w, 0+)	FSEL-5 (r/w, 0+)	FSEL-4 (r/w, 0+)	FSEL-3 (r/w, 0+)	FSEL-2 (r/w, 0+)	FSEL-1 (r/w, 0+)	FSEL-0 (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

List of available flag registers for *TORNADO-6x*, which can be addressed by *FLAG SELECTOR REGISTER*, is presented in table 2-11.

Table 2-11. Flag registers for *TORNADO-6x*.

code written to FLAG SELECTOR REGISTER	name of addressed flag register (register #3)	description
10H	r: SYS_STATUS_FRG w: SET_HM_RQ_FRG	In read mode indicates current status of main run-time system flags of *TORNADO-6x* (refer to subsection "*SYS_STATUS_FRG Flag Register*" later in this section). In write mode sets active *Host_to_Master_Request (HM_RQ)* via *INT3* external interrupt request input for TMS320C6x DSP. Data written to *SET_HM_RQ_FRG* register has no meaning and is ignored.
20H	r: SYS_STATUS_FRG w: CLEAR_MH_RQ_FRG	In read mode indicates current status of main run-time system flags of *TORNADO-6x* (refer to subsection "*SYS_STATUS_FRG Flag Register*" later in this section). In write mode clears active *Master_to_Host_Request (MH_RQ)* flag in *SYS_STATUS_FRG* flag register. *Master_to_Host_Request* flag can be set by resident TMS320C6x DSP software in order to set attention or interrupt request to host PC. Data written to *CLEAR_MH_RQ_FRG* register has no meaning and is ignored. Host PC should perform this operation in the end of corresponding procedure or interrupt handler (in case *MH_RQ_IE*=1) after *MH_RQ* interrupt source has been identified.
30H	r: SYS_STATUS_FRG w: CLEAR_SB_ERROR_FRG	In read mode indicates current status of main run-time system flags of *TORNADO-6x* (refer to subsection "*SYS_STATUS_FRG Flag Register*" later in this section). In write mode clears active *SB_ERROR* flag in *SYS_STATUS_FRG* flag register. Active *SB_ERROR* flag is set by timeout during host-to-SB access. Data written to *CLEAR_SB_ERROR_FRG* register has no meaning and is ignored. Host PC should perform this operation in the end of corresponding interrupt handler (in case *SB_ERROR_IE*=1) after *SB_ERROR* interrupt source has been identified. Also, host PC should perform this operation in the end of data transmission between host ISA-bus and SB in case active *SB_ERROR* flag is detected.
40H	w: CLEAR_HPI_ERROR_FRG	In write mode clears active *HPI_ERROR* flag in *SYS_STATUS_FRG* flag register. Active *HPI_ERROR* flag is set by timeout during host-to-HPI access. Data written to *CLEAR_HPI_ERROR_FRG* register has no meaning and is ignored. Host PC should perform this operation in the end of corresponding interrupt handler (in case *HPI_ERROR_IE*=1) after *HPI_ERROR* interrupt source has been identified. Also, host PC should perform this operation in the end of data transmission between host ISA-bus and HPI in case active *HPI_ERROR* flag is detected. This flag register is write-only

50H	r/w: HPI_IE_FRG	*HPI-to-Host Interrupt Enable Register*. This flag register sets interrupt enable masks for interrupting host PC on *HPI_ERROR* and *HPI_HINT* events. Host PC interrupt request is logical OR between (*MH_RQ_IE & MH_RQ*), (*SB_ERROR_IE & SB_ERROR*), (*HPI_ERROR_IE & HPI_ERROR*) and (*HPI_HINT_IE & HPI_HINT*) logic terms.
60H	r: DSP_STATUS_FRG	*DSP Status Register*. This flag register returns current state of *DSP_MLock*, *DSP_M_GO* and *DSP_PD* control signals from the TMS320C6x DSP environment.
E0H	r/w: ISA_MI_BADDR_FRG	*ISA-bus Memory Interface Base Address Register*. Sets ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-6x* in accordance with table 2-4. Sets/resets activity of host ISA-bus memory interface of *TORNADO-6x* within UMB area of ISA-bus memory address space. Only three least significant bits of this register are valid; all other bits are ignored and reads as zeros.
E2H	r/w: ISA_ECC_BADDR_FRG (*TORNADO-62MX/67MX* only)	*ECC ISA-bus I/O Base Address Register*. Sets ISA-bus I/O base address for *TORNADO-62MX/67MX* optional on-board emulation controller (*ECC*) in accordance with table 2-14. Sets/resets activity of *ECC* within ISA-bus I/O address space. Only three least significant bits of this register are valid; all other bits are ignored and reads as zeros.
F0H F1H	r: DEV_ID0_FRG r: DEV_ID1_FRG	*Device Identifier and S/N Registers #0/#1*. These registers are read only and contain LSB and MSB of device ID and s/n ID for *TORNADO-6x*

Notes: 1.   Unused codes for flag registers are reserved for future expansion.
2.   Access modes: *r* - read only; *w* - write only; *r/w* - read and write.

Once a desired flag register is selected by loading the corresponding code into *FLAG SELECTOR REGISTER* in accordance with table 2-11, current flags status can be obtained by reading *FLAG DATA REGISTER* (*FLAG STATUS REGISTER*), whereas flag settings can be performed by writing to *FLAG DATA REGISTER* (*FLAG CONTROL REGISTER*). Note, that *FLAG STATUS REGISTER* and *FLAG CONTROL REGISTER* are actually read and write denotification of *FLAG DATA REGISTER* that is available for both read and write operations. However, this makes useful sense since some of *TORNADO-6x* flag registers have different format for read and write operations.

Table 2-12. Bits of *SYS_STATUS_FRG* flag register for *TORNADO-6x*.

bit name	power on default value	description
SB_ACK	0	*SB Request Acknowledge. SB_ACK*=1 denotes that SB arbiter has granted SB access to host ISA-bus memory interface. *SB_ACK* flag can be read during active SB locking from host ISA-bus memory interface.
HPI_ERROR	0	*HPI Error (HPI_ERROR). HPI_ERROR*=1 denotes that 6 µsec timeout has been detected during host-to-HPI access. *HPI_ERROR* flag will keep staying in active *HPI_ERROR*=1 state until it will be reset by host PC software by means of writing to *CLEAR_HPI_ERROR_FRG* flag register. If *HPI_ERROR* flag has been set to active (*HPI_ERROR*=1) state, all succeeding host-to-HPI accesses from host ISA-bus memory interface of *TORNADO-6x* will be ignored and data returned will be undefined. If *HPI_ERROR_IE*=1 and *HPI_ERROR*=1, an active host PC CPU interrupt request is generated.
HPI_HINT	0	*DSP_to_Host Request_via_HPI (HPI_HINT). HPI_HINT*=1 denotes that TMS320C6x DSP has generated active request to host PC CPU via HPI. *HPI_HINT* flag will keep staying in active *HPI_HINT*=1 state until it will be reset by host PC software by means of writing 05050505H hex value to HPIC register of TMS320C6x DSP HPI. If *HPI_HINT_IE*=1 and *HPI_HINT*=1, then active host PC CPU interrupt request is generated.
MH_RQ	0	*Master_to_Host Request (MH_RQ). MH_RQ*=1 denotes that TMS320C6x DSP has generated active request to host PC CPU. *MH_RQ* flag will stay active (*MH_RQ*=1) until it will be reset by host PC software by writing to *CLEAR_MH_RQ_FRG* flag register. If *MH_RQ_IE*=1 and *MH_RQ*=1, then active host PC CPU interrupt request is generated.
SB_ERROR	0	*SB Error (SB_ERROR). SB_ERROR*=1 denotes that the 6 µsec timeout has been detected during SB access from host ISA-bus memory interface. *SB_ERROR* flag will stay active (*SB_ERROR*=1) until it will be reset by host PC software by means of writing to *CLEAR_SB_ERROR_FRG* flag register. If *SB_ERROR_IE*=1 and *SB_ERROR*=1, then active host PC CPU interrupt request is generated.

SYS_STATUS_FRG Flag Register

SYS_STATUS_FRG flag register is read-only and comprises of most important *TORNADO-6x* run-time system flags information:

SYS_STATUS_FRG Flag Register (read only)

SB_ERROR (r)	MH_RQ (r)	HPI_HINT (r)	0	0	0	HPI_ERROR (r)	SB_ACK (r)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Detail description for bits of *SYS_STATUS_FRG* flag register is presented in table 2-12.

HPI-to-Host Interrupt Enable Flag Register (HPI_IE_FRG)

HPI_IE_FRG flag register comprises of interrupt enable bit masks for generation of host PC interrupt on HPI events: active *HPI_HINT* HPI-to-host interrupt request and/or active *HPI_ERROR* flag. Format of *HPI_IE_FRG* flag register is as the following:

HPI_IE_FRG Flag Register (r/w)

0	0	HPI_HINT_IE (r/w, 0+)	0	0	0	HPI_ERROR_IE (r/w, 0+)	0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

In case *HPI_HINT_IE* bit is set to logical '1' and *HPI_HINT* flag is active (*HPI_HINT*=1) in *SYS_STATUS_FRG* flag register or HINT register of HPI, then this will result in generation of active host PC interrupt request. In case *HPI_HINT_IE* bit is set to logical '0', then no host PC interrupt will be generated when *HPI_HINT* flag will come active.

In case *HPI_ERROR_IE* bit is set to logical '1' and *HPI_ERROR* flag is active (*HPI_ERROR*=1) in *SYS_STATUS_FRG* flag register, then this will result in generation active host PC interrupt request. In case *HPI_ERROR_IE* bit is set to logical '0', then no host PC interrupt will be generated when *HPI_ERROR* flag will come active.

DSP_STATUS_FRG Flag Register

DSP_STATUS_FRG flag register comprises of most important TMS320C6x DSP control signals settings. It is available as read only register and has the following data format:

DSP_STATUS_FRG Flag Register (read only)

0	0	0	0	0	DSP_PD (r)	DSP_M_GO (r)	DSP_MLock (r)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Detail description for bits of *DSP_STATUS_FRG* flag register is presented in table 2-13.

Table 2-13. Bits of *DSP_STATUS_FRG* flag register for *TORNADO-6x*.

bit name	power on default value	description
DSP_MLock	0	*DSP MLock*. *DSP_MLock*=1 denotes that TMS320C6x DSP has set the SB lock request. The SB will be locked by DSP immediately in case there is no current host-to-SB request or immediately upon the current host-to-SB request will terminate.
DSP_M_GO	0	*DSP M_GO signal*. *DSP_M_GO*=0 denotes that TMS320C6x DSP is in the RESET state. *DSP_M_GO*=1 denotes that TMS320C6x DSP is in the GO (RUN) program execution mode. The *DSP M_GO* is not a simple return of *M_GO* from the *CONTROL REGISTER*. In case the J6 DSP RESET SELECTOR jumper is set to external DSP RESET source, then the *DSP_M_GO* returns the current value of external DSP RESET signal. In case the J6 DSP RESET SELECTOR jumper is set to host DSP RESET source, then the *DSP_M_GO* returns the current value of host *M_GO* from the *CONTROL REGISTER*. The *DSP M_GO* is useful for checking actual current RESET state of DSP, and to prevent host-to-HPI accesses while DSP is in the RESET state.
DSP_PD	0	*DSP Power Down*. *DSP_PD*=1 denotes that TMS320C6x DSP is either in the power down PD2 or PD3 state.

Flag Registers for Identifying TORNADO-6x DSP System

TORNADO-6x includes *DEV_ID0_FRG/DEV_ID1_FRG* read-only flag registers (see table 2-11), which contains code for identification of *TORNADO-6x* DSP systems and its serial number.

Usage of *DEV_ID0_FRG/DEV_ID1_FRG* flag registers in host PC software is recommended for those applications, which either require to be auto-configured for particular *TORNADO-6x* hardware, or should be protected from unauthorized duplication of software.

Generating Request to TMS320C6x DSP

TORNADO-6x can generate requests from host PC to TMS320C6x DSP in order to synchronize between programs execution in host and on-board DSP environments. Two methods for generation of host-to-DSP requests is supported in *TORNADO-6x*:

- *HM_RQ* (host to master request), that results in generation of active *INT3* external interrupt request for the on-board TMS320C6x DSP. In order to generate output *HM_RQ* flag, host PC software has to write to *SET_HM_RQ_FRG* flag register. This is the recommended method for generation of host-to-DSP request since it delivers compatibility with all other *TORNADO* DSP systems for PC.
- *HPI_DSPINT* (DSP interrupt via HPI), that results in setting bit *DSPINT* of HPIC register of TMS320C6x HPI. In order to generate *HPI_DSPINT* interrupt request to DSP, host PC software has to write 03030303H hex value to HPIC register of TMS320C6x DSP. This is the *TORNADO-6x*

specific method for generation of host-to-DSP request, and it is recommended for simulation of host-to-DSP communication via TMS320C6x DSP on-chip HPI.

Processing Request from TMS320C6x DSP

TORNADO-6x can generate requests from TMS320C6x DSP to host CPU in order to synchronize between program execution in host and on-board DSP environments. Two methods for generation of DSP-to-host requests is supported in *TORNADO-6x*:

- *MH_RQ* (master to host request), that results in setting flag *MH_RQ* in *SYS_STATUS_FRG* flag register. *MH_RQ* can generate active host PC interrupt request in case *MH_RQ_IE* bit in the *CONTROL REGISTER* is set to the *MH_RQ_IE*=1 state. *MH_RQ* will remain in active state *MH_RQ*=1 until it will be recognized and reset by host software. In order to reset the *MH_RQ* flag, host PC software has to write to *Clear_Master_to_Host_Request* flag register. This is the recommended method for generation of DSP-to-host request since it delivers compatibility with all other *TORNADO* DSP systems for PC.
- *HPI_HINT* (host interrupt request via HPI), that results in setting bit *HINT* of HPIC register of TMS320C6x HPI and flag *HPI_HINT* in *SYS_STATUS_FRG* flag register. *HPI_HINT* can generate active host PC interrupt request in case *HPI_HINT_IE* bit in *HPI_IE_FRG* flag register is set to *HPI_HINT_IE*=1 state. *HPI_HINT* will remain in active state *HPI_HINT*=1 until it will be recognized and reset by host software. In order to reset the *HPI_HINT* flag, host PC software has to write 05050505H hex value to HPIC register of TMS320C6x DSP. This is the *TORNADO-6x* specific method for generation of DSP-to-host request, and it is recommended for simulation of DSP-to-host communication via TMS320C6x DSP on-chip HPI.

Host Interrupts

Host ISA-bus I/O interface can generate active interrupts to host PC CPU in the following cases:

- when *SB_ERROR* flag is active (*SB_ERROR*=1) in *SYS_STATUS_FRG* flag register and *SB_ERROR_IE* bit in *CONTROL REGISTER* is set to *SB_ERROR_IE*=1 state
- when *MH_RQ* is active (*MH_RQ*=1) in *SYS_STATUS_FRG* flag register and *MH_RQ_IE* bit in *CONTROL REGISTER* is set to *MH_RQ_IE*=1 state
- when *HPI_ERROR* flag is active (*HPI_ERROR*=1) in *SYS_STATUS_FRG* flag register and *HPI_ERROR_IE* bit in *HPI_IE_FRG* flag register is set to *HPI_ERROR_IE*=1 state
- when *HPI_HINT* is active (*HPI_HINT*=1) in *SYS_STATUS_FRG* flag register or HINT register of HPI and *HPI_HINT_IE* bit in *HPI_IE_FRG* flag register is set to *HPI_HINT_IE*=1 state

Host ISA-bus interrupt request is generated as logical 'OR' of the above events. Decoding of interrupt source should be performed by host PC software by means of analyzing the contents of *SYS_STATUS_FRG* flag register.

Host PC interrupt request may be generated using one of nine available ISA-bus interrupt request lines. Particular PC interrupt line is selected by the on-board interrupt configuration jumper J1 (see fig.2-2). The following ISA-bus interrupt request lines are available: IRQ-3, IRQ-4, IRQ-5, IRQ-6, IRQ-7, IRQ-10, IRQ-11, IRQ-12 and IRQ-15.

Setting ISA-bus memory base address for Host ISA-bus Memory Interface

TORNADO-6x provides software setting of ISA-bus memory base address for host ISA-bus memory interface by means of writing to *ISA_MI_BADDR_FRG* flag register. Only three least significant bits of *ISA_MI_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes. Available settings for *ISA_MI_BADDR_FRG* flag register are presented in table 2-5.

ISA_MI_BADDR_FRG Flag Register (r/w)

0	0	0	0	0	MI_BA2 (r/w, 0+)	MI_BA1 (r/w, 0+)	MI_BA0 (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Setting ISA-bus I/O base address for ECC in TORNADO-62MX/67MX

TORNADO-62MX/67MX provides software setting of ISA-bus I/O base address for optional on-board emulation controller chip (*ECC*) by means of writing to *ISA_ECC_BADDR_FRG* flag register. Only three least significant bits of *ISA_ECC_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes. Available settings for *ISA_ECC_BADDR_FRG* flag register are presented in table 2-14.

ISA_ECC_BADDR_FRG Flag Register (r/w)

0	0	0	0	0	ECC_BA2 (r/w, 0+)	ECC_BA1 (r/w, 0+)	ECC_BA0 (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-14. ISA-bus I/O base address for *TORNADO-62MX/67MX* optional on-board emulation controller (*ECC*).

ISA-bus I/O base address for *ECC*	ISA-bus I/O address range for *ECC*	bit setting for *ISA_ECC_BADDR_FRG* flag register		
		bit#2 ECC_BA2	bit#1 ECC_BA1	bit#0 ECC_BA0
ECC is disconnected from host ISA-bus; attachment of external TI XDS510 or MicroLAB' MIRAGE-510DX emulator is allowed	-	0	x	x
[2)]240H	240H ... 25FH	1	0	0
280H	280H ... 29FH	1	0	1
320H	320H ... 33FH	1	1	0
340H	340H ... 35FH	1	1	1

Note: 1. Highlighted configuration corresponds to host power on default setting.
2. This configuration is used as default by *T6CC.EXE* software utility.

CAUTION

Attachment of external TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator to
TORNADO-62MX/67MX is allowed only in case the on-board emulation controller (*ECC*) is
either not installed or is programmed as 'disconnected' from ISA-bus (see table 2-14).

Attachment of external TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator to
TORNADO-62MX/67MX while the on-board emulation controller (*ECC*) is active is strongly
prohibited and may result in damaging emulator and/or *ECC*.

2.6   Parallel I/O Expansion Interface Site (PIOX and PIOX-16)

TORNADO-6x architecture provides expansion of the on-board I/O resources using 32-bit parallel I/O expansion interface (PIOX) for *TORNADO-62/67* or 16-bit parallel I/O expansion interface (PIOX-16) for *TORNADO-62MX/67MX*.

PIOX/PIOX-16 daughter-card sites are designed for compatible PIOX-16 daughter modules. PIOX/PIOX-16 daughter-card modules are installed above the *TORNADO-6x* mainboard (see fig.1-1 and fig.2-6) and are compatible with all *TORNADO* DSP systems for PC and all *TORNADO-E/EL* embedded DSP controllers.

Description

TORNADO-6x PIOX/PIOX-16 interfaces appear as either 512Kx32 (PIOX) or 64Kx16 (PIOX-16) I/O address sub-space of TMS320C6x DSP EMIF CE-3 address area, and can be accessed by both the on-board TMS320C6x DSP and host ISA-bus memory interface. PIOX/PIOX-16 include SB data/address buses, SB control signals, TMS320C6x DSP on-chip timers I/O pins and external interrupt inputs, DSP reset signal, and ISA-bus power supply lines.

PIOX supports 32-bit data bus and 8/16/32-bit data transfer cycles, whereas PIOX-16 supports 16-bit data transfer cycles only.

Installation of PIOX/PIOX-16 Daughter-card Modules onto TORNADO-6x Mainboard

Figure 2-6 shows installation of PIOX daughter-card modules onto *TORNADO-62/67* and *TORNADO-62MX/67MX* mainboard.
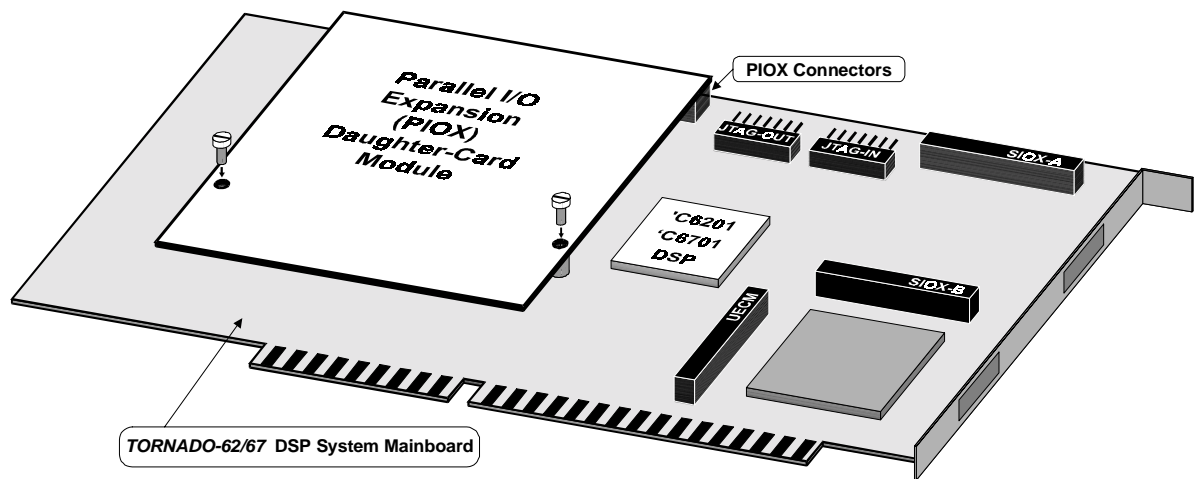
Fig.2-6a. Installation of PIOX daughter-card module onto *TORNADO-62/67* mainboard.
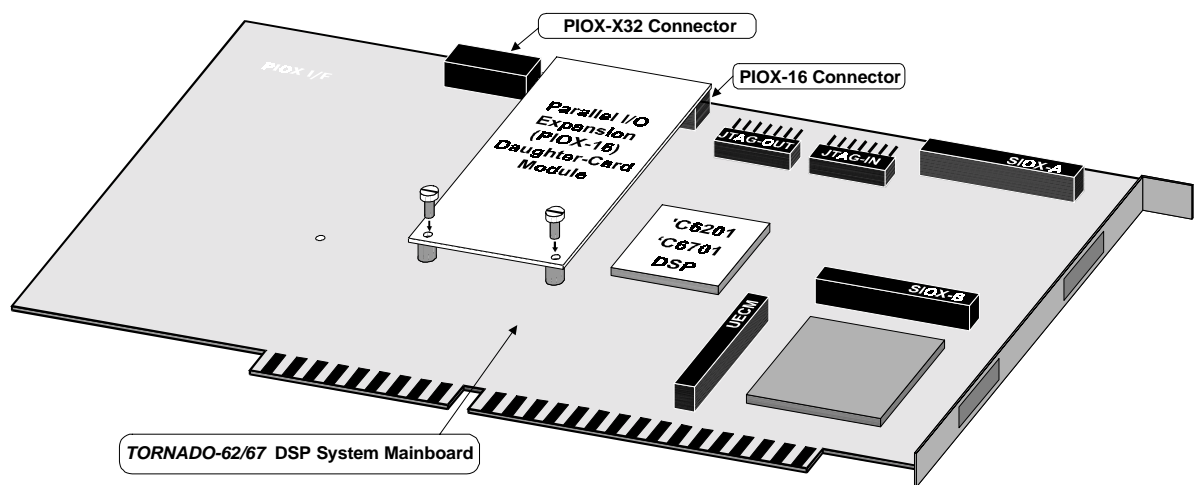
Fig.2-6b. Installation of PIOX-16 daughter-card module onto *TORNADO-62/67* mainboard.
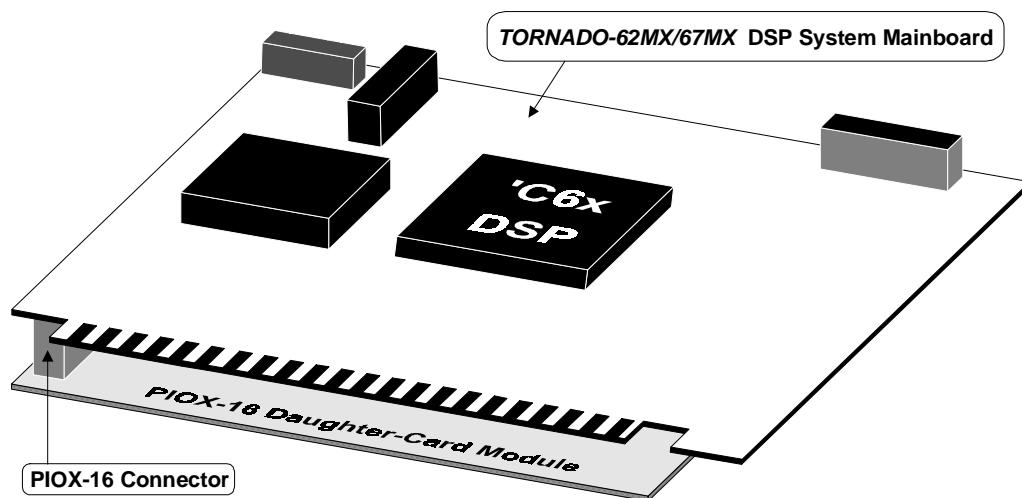
Fig.2-6c.   Installation of PIOX-16 daughter-card module onto *TORNADO-62MX/67MX* mainboard.

Accessing PIOX/PIOX-16 from TMS320C6x DSP Environment

PIOX/PIOX-16 can be accessed by on-board TMS320C6x DSP when addressing the corresponding sub-space of EMIF CE-3 address space (see table 2-2).

CAUTION

The EMIF CE-3 Space Control Register of TMS320C6x DSP should be programmed to 0x6336cc23 hex value in accordance with table 2-2 in order to meet requirements of *TORNADO-6x* hardware for PIOX/PIOX-16.

Minimum PIOX/PIOX-16 data transfer strobe width is 60ns with setup timing 30ns and hold timing 15ns. Data transfer acknowledgement is performed by means of asynchronous *PIOX_READY* signal.

Accessing PIOX/PIOX-16 from Host ISA-bus Memory Interface

PIOX/PIOX-16 can be accessed by host ISA-bus memory interface when *SBA-0..1* SB address space selector bits of *SB PAGE MAPPER MSB* register are set to {1,1} from host ISA-bus I/O interface.

CAUTION

PIOX/PIOX-16 area is accessed by host ISA-bus memory interface with default strobe width of 60ns and with further processing of *PIOX_READY* signal.

PIOX-16 Connector Pinout for TORNADO-62MX/67MX

TORNADO-62MX/67MX on-board PIOX-16 connector is a high-density DDK 50-pin DHB-series dual-row female connector with 0.05" pin pitch. Compatible PIOX-16 plugs for customer designed daughter-card modules are available from MicroLAB Systems upon request.

PIOX-16 connector pinout specification is presented at fig 2-7 whereas signal specifications are listed in table 2-15.

+5v	1	2	+5v
A16	3	4	A17
A14	5	6	A15
A12	7	8	A13
A10	9	10	A11
A8	11	12	A9
A6	13	14	A7
A4	15	16	A5
A2	17	18	A3
D14	19	20	D15
D12	21	22	D13
D10	23	24	D11
D8	25	26	D9
D6	27	28	D7
D4	29	30	D5
D2	31	32	D3
D0	33	34	D1
GND	35	36	GND
$\overline{STB}$	37	38	TM-0
$\overline{WE}$	39	40	TM-1
PIOX_READY	41	42	$\overline{IRQ\text{-}0}$
$\overline{RESET}$	43	44	$\overline{IRQ\text{-}1}$
	45	46	$\overline{IRQ\text{-}2}$
	47	48	
-5v	49	50	+12v
-12v			

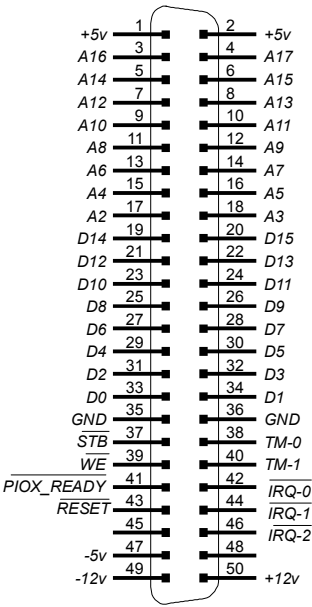*Fig.2-7.* PIOX-16 connector pinout (top view).

Table 2-15. PIOX-16 signal description.

Signal name	signal type	description
A2..A17	O	SB address bus.
D0..D15	I/O	SB data bus.

$\overline{STB}$	O	Active low PIOX-16 data transfer strobe ($\overline{STB}$ =0).
$\overline{WE}$	O	Active low PIOX-16 write enable signal ($\overline{WE}$ =0).
$\overline{PIOX\_READY}$	I	Active low PIOX-16 data ready acknowledge ($\overline{PIOX\_READY}$ =0) signal. Generated by PIOX-16 module in order to match the PIOX-16 SB cycle timing with timing requirements of memory and I/O devices used in PIOX-16 module.
TM-0	I/O/Z	Configured by on-board J8 jumper as either input for the TMS320C6x DSP on-chip Timer-0 (J8 jumper is not installed) or as output from the TMS320C6x DSP on-chip Timer-0 (J8 jumper is installed).
TM-1	I/O/Z	Configured by on-board J9 jumper as either input for the TMS320C6x DSP on-chip Timer-1 (J9 jumper is not installed) or as output from the TMS320C6x DSP on-chip Timer-1 (J9 jumper is installed).
$\overline{RESET}$	O	Active low reset signal ($\overline{RESET}$ =0) for the on-board PIOX/PIOX-16 expansion interface site, which is the output state of the *PIOX_RUN* bit from *PXSX_RUN* IOX register from the DSP environment (refer to table 2-2).
$\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, $\overline{IRQ\text{-}2}$	I	Active low external interrupt request lines for the on-board TMS320C6x DSP chip. These line are pulled up with the on-board resistor, so it is recommended to configure these external interrupt requests as inverse polarity external interrupt requests by means of programming the TMS320C6x DSP on-chip External Interrupt Polarity register to the 0x0000000F value. Both negative static and negative pulse interrupt requests are supported. Actual TMS320C6x DSP external interrupt requests (*EXT_INT4...EXT_INT6*) will be generated on the falling edge (1→0) of $\overline{IRQ\text{-}0}$ .. $\overline{IRQ\text{-}2}$ signals.
GND		Ground.
+5v		+5v power (from ISA-bus).
+12v		+12v power (from ISA-bus).
-5v		-5v power (from ISA-bus).
-12v		-12v power (from ISA-bus).

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

PIOX Connector Pinout for TORNADO-62/67

TORNADO-62MX/67MX on-board PIOX connector comprises of the PIOX-16 connector and PIOX 32-bit add-on connector. This allows accommodation of either PIOX-16 daughter-card module for high-speed AD/DA/DIO applications or 32-bit PIOX DSP Coprocessor daughter-card module.

PIOX-16 connector is described in the above section "*PIOX-16 Connector Pinout for TORNADO-62MX/67MX*".

The PIOX add-on connector is a high-density DDK 30-pin DHB-series dual-row female connector with 0.05" pin pitch. Compatible PIOX-16 plugs for customer designed daughter-card modules are available from MicroLAB Systems upon request.

PIOX connector pinout specification is presented at fig 2-8. As a part of PIOX, the PIOX-16 signal specifications are listed in table 2-15, whereas signal specifications for PIOX add-on connector are listed in table 2-16.
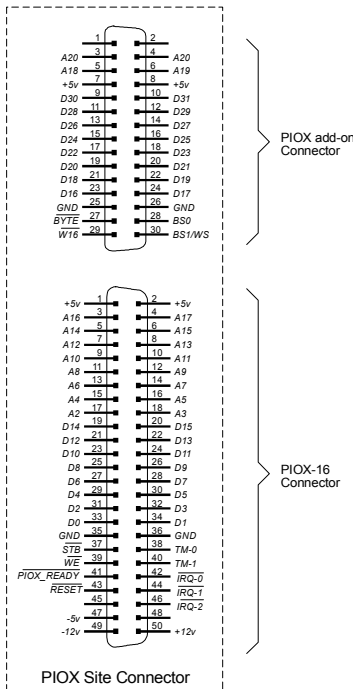
Fig.2-8. PIOX connector pinout (top view).

Table 2-16. PIOX 32-bit add-on connector signal description.

Signal name	signal type	description
A18..A20	O	Extra SB address lines.
D16..D31	I/O	16-bit MSW of SB data bus.
$\overline{BYTE}$	O	Defines 8-bit (byte) SB data cycle ($\overline{BYTE}$ =0). The byte selection signals *BS0/BS1* define actual byte #0..#3 (byte #0 is LSB) inside 32-bit SB data word, which will be selected with active $\overline{STB}$ signal. If none of $\overline{BYTE}$ and $\overline{W16}$ signals is active, then current SB access cycle has 32-bit data format.

$\overline{W16}$	O	Defines 16-bit (halfword) SB data cycle ($\overline{W16}$=0). The halfword selection signal *W0* define actual halfword #0/#1 (halfword #0 is LSW) inside 32-bit SB data word, which will be selected with active $\overline{STB}$ signal. If none of $\overline{BYTE}$ and $\overline{W16}$ signals is active, then current SB access cycle has 32-bit data format.
BS0		Least significant bit of byte selection signals (*BS0*, *BS1*) for 8-bit SB data cycle. Valid during valid $\overline{BYTE}$=0 signal only.
BS1/WS		Most significant bit of byte selection signals (*BS0*, *BS1*) for 8-bit SB data cycle ($\overline{BYTE}$=0) or 16-bit halfword selection signal (*WS*) for 16-bit SB data cycle ($\overline{W16}$=0).
GND		Ground.
+5v		+5v power (from ISA-bus).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

PIOX Data Transfer Cycles

PIOX interface site of *TORNADO-62/67* supports 8/16/32-bit PIOX data access cycles. Particular type PIOX data access cycle is defined by $\overline{BYTE}$ and $\overline{W16}$ PIOX signals as the following:

- { $\overline{BYTE}$=0, $\overline{W16}$=1} state corresponds to *byte (8-bit) PIOX data access cycle*. Selection of particular byte (#0..#3) within addressed 32-bit data word id performed by (*BS0*, *BS1*) byte selection signals.
- { $\overline{BYTE}$=1, $\overline{W16}$=0} state corresponds to *16-bit half-word PIOX data access cycle*. Selection of particular 16-bit half-word (#0..#1) within addressed 32-bit data word id performed by *BS1/W0* signals. Signal *BS0* is ignored.
- { $\overline{BYTE}$=1, $\overline{W16}$=1} state corresponds to *32-bit word PIOX data access cycle*. (*BS0*, *BS1*) signals are ignored in this mode.
- { $\overline{BYTE}$=0, $\overline{W16}$=0} state is reserved.

PIOX-16 Data Transfer Cycles

PIOX-16 interface site of *TORNADO-6x* supports 16-bit data transfer cycles only, and, therefore PIOX-16 connector does not contain the cycle definition signals.

Data Transfer Strobe for PIOX/PIOX-16

The PIOX/PIOX-16 data transfer timing is presented at fig.2-9. This data transfer timing is known as the industry standard MOTO mode and assumes usage of data strobe signal and write enable signal.
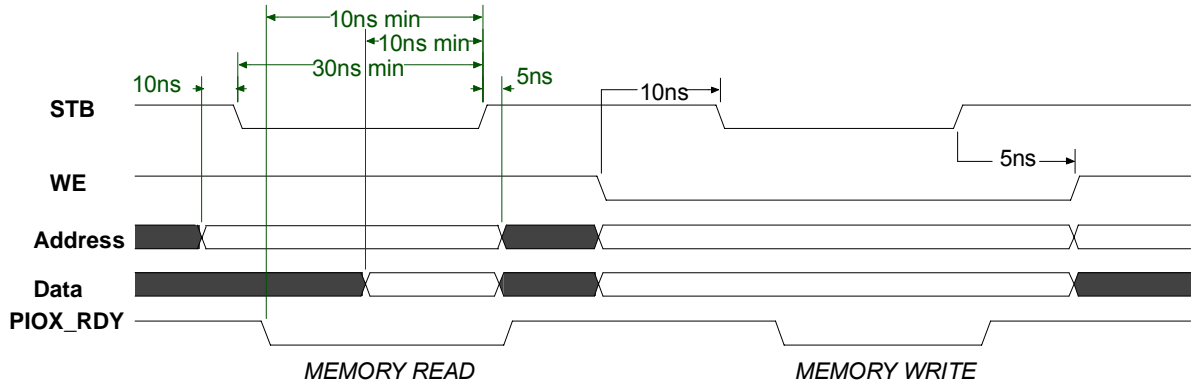
Fig.2-9. Timing diagram of PIOX/PIOX-16 data transfer strobe.

Generating Reset Signal for PIOX/PIOX-16 Expansion Interface Site

TORNADO-6x allows generation of individual reset signal for PIOX/PIOX-16 expansion interface site (refer to the corresponding sections earlier in this chapter) using the following logical conditions:

- PIOX/PIOX-16 reset signal is active in case the on-board DSP is in the 'RESET' state
- reset signal for PIOX/PIOX-16 expansion site can be released only in case DSP is in the 'RUN' state and bit *PIOX_RUN* of *PXSX_RUN* IOX register is set to logical '1' value by DSP software.

This allows correct initialization of the PIOX/PIOX-16 daughter-card hardware and correct synchronization with the DSP software.

CAUTION

TORNADO-6x rev.2A hardware provides different on-board logic for generation of SIOX/PIOX reset signals if compared to *TORNADO-6x* rev.1.x hardware.

TORNADO-6x rev.1x generates common SIOX/PIOX reset signal using *XRESET* IOX register, and this reset signal was generated as the logical OR between the DSP reset signal and bit D0 of *XRESET* IOX register.

PIOX reset signal can be released by the TMS320C6x DSP software by means of writing logical '1' value to the *PIOX_RUN* bit of *PXSX_RUN* IOX register (refer to table 2-2 and to the corresponding subsection in section "TMS320C6x DSP Environment" earlier in this chapter), and this will allow operation of the PIOX/PIOX-16 daughter-card hardware. Writing logical '0' to the *PIOX_RUN* bit of *PXSX_RUN* IOX register, which is the default value on the DSP reset, will set the PIOX reset signal active.

Physical Dimensions for PIOX/PIOX-16 Daughter-card Modules

Physical dimensions for PIOX and PIOX-16 daughter-card modules are presented at fig.2-10. This information is intended for those *TORNADO* customers, who need to design customized PIOX or PIOX-16 daughter-card modules.
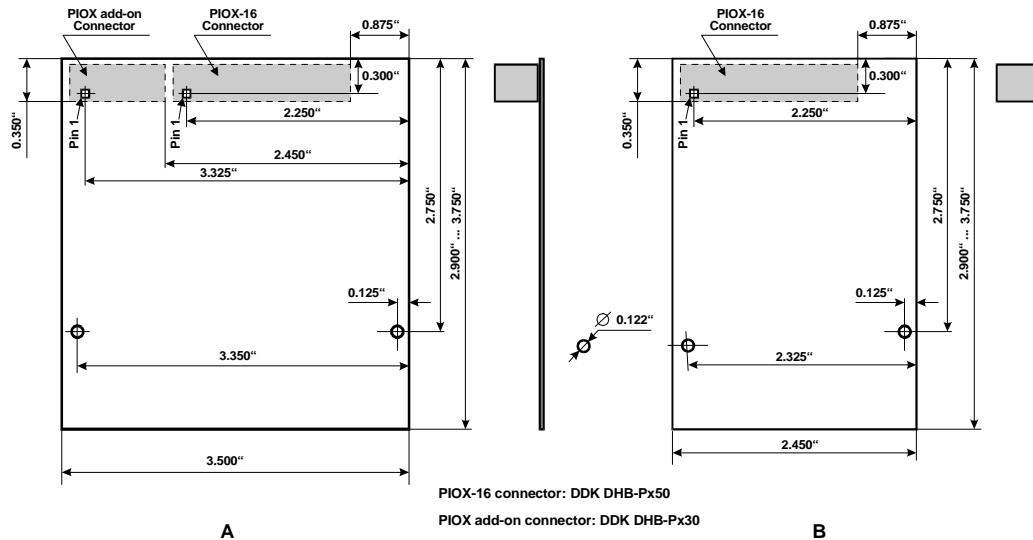

Fig.2-10.   Physical dimensions for PIOX (A) and PIOX-16 (B) daughter-card modules.

2.7   Serial I/O Expansion Interface Sites (SIOX)

TORNADO-6x architecture provides expansion of the on-board TMS320C6x I/O resources via on-board serial I/O expansion interface sites (SIOX) (refer to fig.1-1 and fig.2-2), which are designed to carry compatible daughter-card modules.

TORNADO-62/67 provides two on-board SIOX sites (SIOX-A and SIOX-B), whereas *TORNADO-62MX/67MX* offers one on-board SIOX site.

On-board SIOX sites of *TORNADO-6x* are compatible with SIOX sites for all *TORNADO* DSP systems for PC and *TORNADO-E/EL/SX* stand-alone DSP controllers.

Available SIOX daughter-cards for *TORNADO* include a variety of AD/DA/DIO daughter-cards for telecommunication, speech and audio signal processing, industrial and instrumentation applications, and many more.

Description

Each SIOX site (SIOX-A and SIOX-B) comprises of signals for SIO-0 and SIO-1 serial ports, TMS320C6x DSP on-chip TM-0/1 timers and interrupts control, as well as DSP reset signal and ISA-bus power supply lines (fig.2-11).
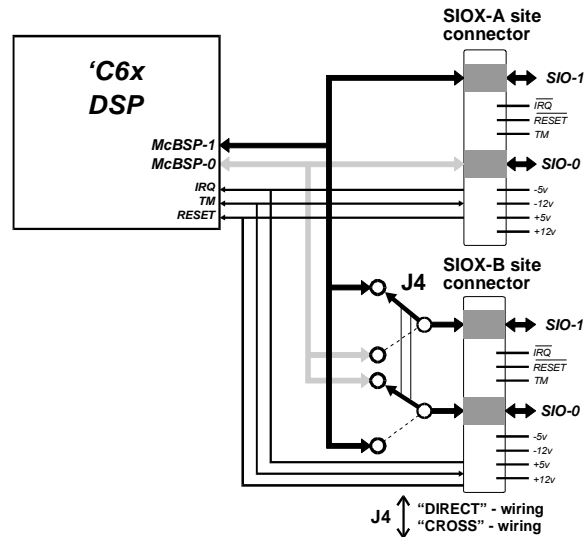
Fig.2-11a. SIOX sites connection diagram for *TORNADO-62/67*.
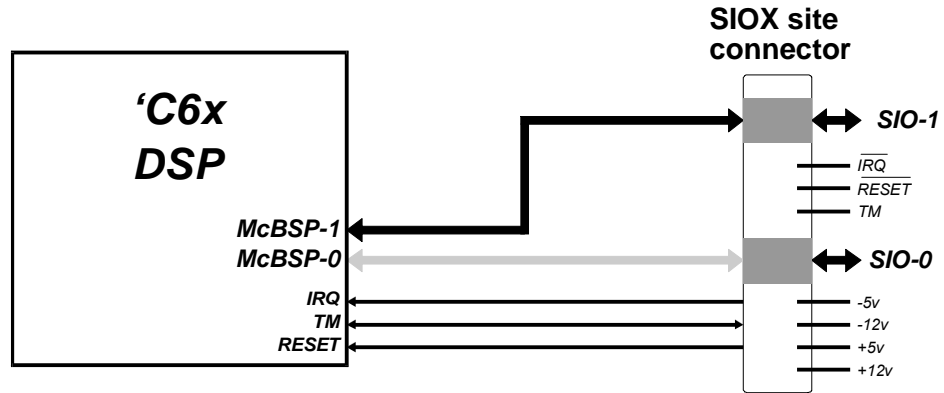
Fig.2-11b. SIOX sites connection diagram for *TORNADO-62MX/67MX*.

The SIO-0 and SIO-1 ports of SIOX-A site of *TORNADO-62/67* and of SIOX site of *TORNADO-62MX/67MX* are connected to the TMS320C6x DSP on-chip McBSP-0 and McBSP-1 serial ports correspondingly.

However, the SIO-0 and SIO-1 ports of SIOX-B site of *TORNADO-62/67* are connected either to the TMS320C6x DSP on-chip McBSP-0 and McBSP-1 serial ports correspondingly (direct connection) or vise-versa (cross-wire connection).

Maximum throughoutput of SIO-0/1 serial ports of SIOX sites on *TORNADO-6x* DSP systems is 200Mbit/s.

External analog and digital I/O signals for installed SIOX daughter-card modules should be attached by means of the SIOX on-module I/O connector via rear panel of host PC.

Installation of SIOX Daughter-card Modules onto TORNADO-6x Mainboard

Figure 2-12 shows installation of SIOX daughter-card modules onto *TORNADO-62/67* and *TORNADO-62MX/67MX* mainboard.

CAUTION

The on-board area for SIOX-B site of *TORNADO-62/67* is shared with the on-board area for *UECMX* emulation control daughter-card module. Either SIOX-B or *UECMX* daughter-card module can be installed onto *TORNADO-62/67* mainboard.
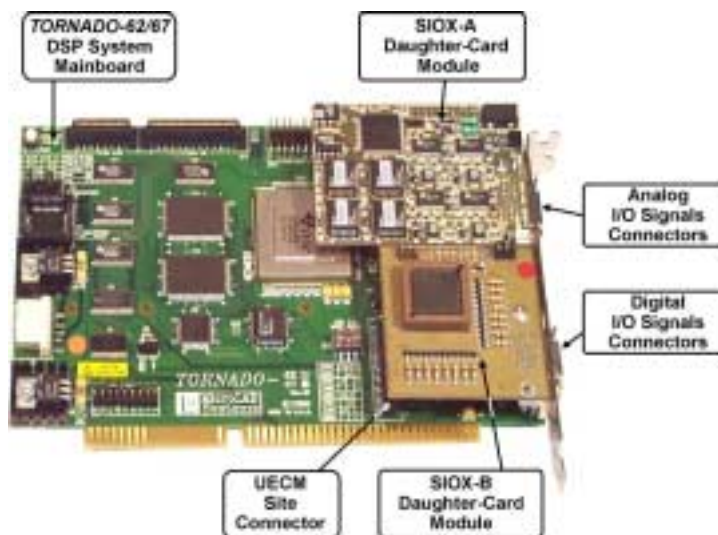
Fig.2-12a. TORNADO-62/67 mainboard with SIOX-A and SIOX-B daughter-card modules.
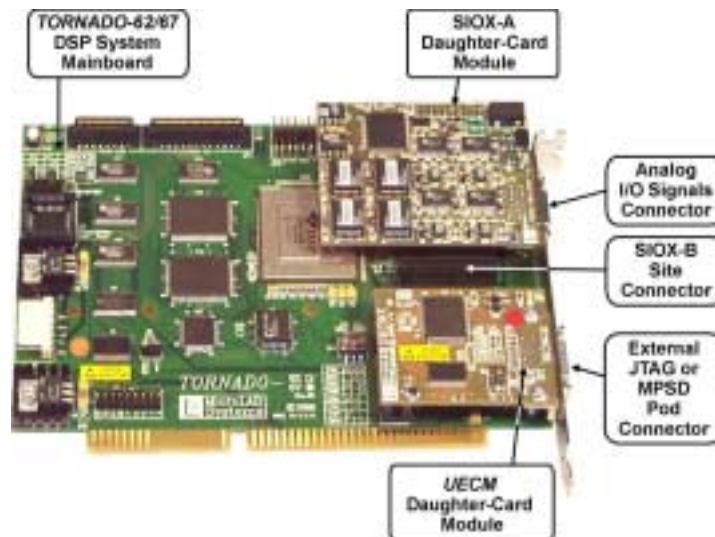
Fig.2-12b. TORNADO-62/67 mainboard with SIOX-A and UECMX daughter-card modules.

CAUTION

The SIOX site on *TORNADO-62MX/67MX* mainboard is identical to SIOX-A site of *TORNADO-62/67* and appears as two on-board parallel SIOX sites. Installation of SIOX daughter-card module is allowed into anyone of these SIOX sites, however only one SIOX daughter-card module can be installed at a time.

The horizontal SIOX site is used for installation of compatible SIOX daughter-card module in case the *TORNADO-62MX/67MX* mainboard is installed into the standard desktop PC with external peripherals connection via rear panel of PC chassis.

The vertical SIOX site is used for installation of compatible SIOX daughter-card module in case the *TORNADO-62MX/67MX* mainboard is installed into industrial MicroPC chassis and the external peripherals connects via top panel of MicroPC™ chassis.
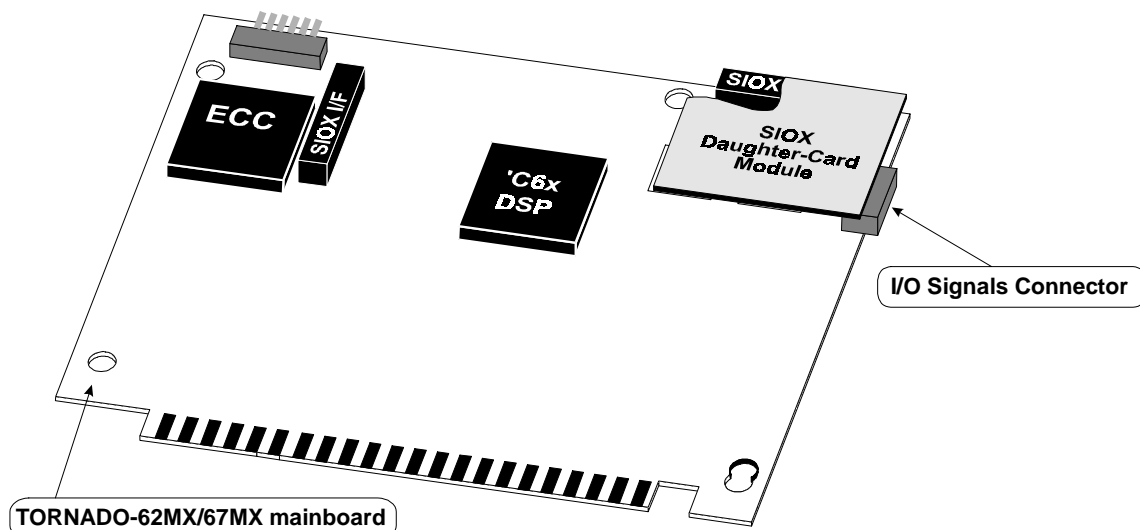
Fig.2-12c. TORNADO-62MX/67MX mainboard with SIOX daughter-card module for installation into standard desktop PC chassis.

Fig.2-12d. TORNADO-62MX/67MX mainboard with SIOX daughter-card module for installation into industrial MicroPC™ chassis.
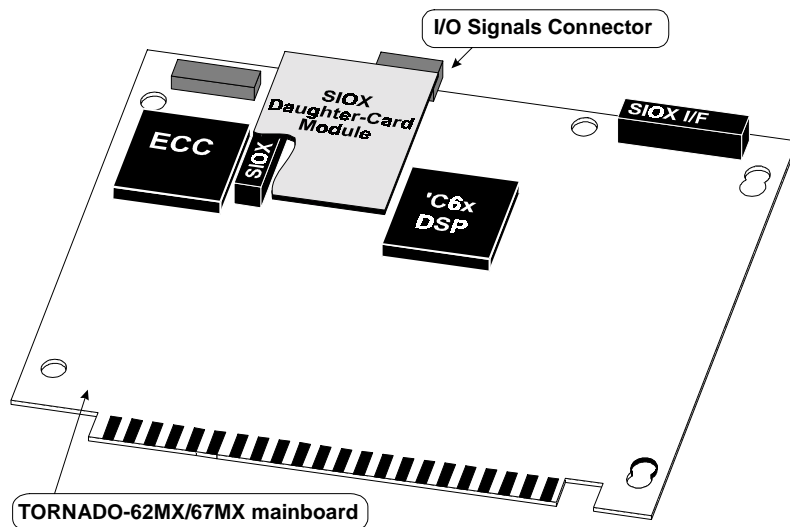
SIOX site connector

SIOX site connector is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. SIOX connector pinout is presented at fig.2-13 and signal specifications are listed in table 2-17.
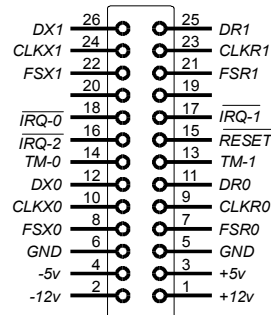
Fig.2-13. SIOX connector pinout (top view).

Table 2-17. SIOX signal specification.

SIOX signal name	signal type	description
SIO-0 port control		
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX site. For SIOX-A site of *TORNADO-6x* DSP systems these signals correspond to the TMS320C6x DSP on-chip McBSP-0 serial port transmitter and are wired directly to its pins. For SIOX-B site of *TORNADO-6x* DSP systems these signals might be configured by on-board J4 jumper set to connect to the transmitter of either McBSP-0 or McBSP-1 serial port of TMS320C6x DSP.
DR0 FSR0 CLKR0	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX site. For SIOX-A site of *TORNADO-6x* DSP systems these signals correspond to the TMS320C6x DSP on-chip McBSP-0 serial port receiver and are wired directly to its pins. For SIOX-B site of *TORNADO-6x* DSP systems these signals might be configured by on-board J4 jumper set to connect to the receiver of either McBSP-0 or McBSP-1 serial port of TMS320C6x DSP.
SIO-1 port control		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX site. For SIOX-A site of *TORNADO-6x* DSP systems these signals correspond to the TMS320C6x DSP on-chip McBSP-0 serial port transmitter and are wired directly to its pins. For SIOX-B site of *TORNADO-6x* DSP systems these signals might be configured by on-board J4 jumper set to connect to the transmitter of either McBSP-0 or McBSP-1 serial port of TMS320C6x DSP.
DR1 FSR1 CLKR1	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX site. For SIOX-A site of *TORNADO-6x* DSP systems these signals correspond to the TMS320C6x DSP on-chip McBSP-0 serial port receiver and are wired directly to its pins. For SIOX-B site of *TORNADO-6x* DSP systems these signals might be configured by on-board J4 jumper set to connect to the receiver of either McBSP-0 or McBSP-1 serial port of TMS320C6x DSP.

DSP Timers, Reset and Interrupt Requests		
TM-0	I/O/Z	Configured by on-board J8 jumper as either input for the TMS320C6x DSP on-chip Timer-0 (J8 jumper is not installed) or as output from the TMS320C6x DSP on-chip Timer-0 (J8 jumper is installed).
TM-1	I/O/Z	Configured by on-board J9 jumper as either input for the TMS320C6x DSP on-chip Timer-1 (J9 jumper is not installed) or as output from the TMS320C6x DSP on-chip Timer-1 (J9 jumper is installed).
$\overline{RESET}$	O	Active low reset signal ($\overline{RESET}$ =0) for the on-board SIOX-A or SIOX-B expansion interface site, which is the output state of the corresponding *SIOX-A_RUN* or *SIOX-B_RUN* bit from *PXSX_RUN* IOX register from the DSP environment (refer to table 2-2).
$\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, $\overline{IRQ\text{-}2}$	I	Active low external interrupt request lines for the on-board TMS320C6x DSP chip. These line are pulled up with the on-board resistor, so it is recommended to configure these external interrupt requests as inverse polarity external interrupt requests by means of programming the TMS320C6x DSP on-chip External Interrupt Polarity register to the 0x0000000F value. Both negative static and negative pulse interrupt requests are supported. Actual TMS320C6x DSP external interrupt requests (*EXT_INT4...EXT_INT6*) will be generated on the falling edge (1→0) of $\overline{IRQ\text{-}0}$ .. $\overline{IRQ\text{-}2}$ signals.
Power Supplies		
GND		Ground.
+5v		+5v power (from ISA-bus).
+12v		+12v power (from ISA-bus).
-5v		-5v power (from ISA-bus).
-12v		-12v power (from ISA-bus).

Note: 1.   Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
               1.   All logical signal levels and load currents correspond to that for CMOS/TTL signals.

Correspondence between SIO-0/SIO-1 ports of SIOX-A site and TMS320C6x DSP on-chip McBSP serial ports

The SIO-0 and SIO-1 ports of SIOX-A site of *TORNADO-62/67* and of SIOX site of *TORNADO-62MX/67MX* are connected to the TMS320C6x DSP on-chip McBSP-0 and McBSP-1 serial ports correspondingly.

Configuring SIO-0/SIO-1 ports of SIOX-B site for TORNADO-62/67

The SIO-0 and SIO-1 ports of SIOX-B site of *TORNADO-62/67* might be connected either to the TMS320C6x DSP on-chip McBSP-0 and McBSP-1 serial ports correspondingly ("direct" connection) or vise-versa ("cross-wire" connection).

This delivers flexibility in selection of the DSP serial ports for application, simplifies software design and allows simultaneous installation of two SIOX daughter-card modules onto *TORNADO-6x* board, most of which utilize only SIO-0 serial port of SIOX interface.

In *TORNADO-62/67* DSP systems the selection between SIO-0/1 ports of SIOX-B site and TMS320C6x DSP on-chip McBSP-0/1 serial ports is configured by means of the on-board jumper array J4 (refer to fig.2-1a and fig.A-1). Only two configurations are available: "direct"-wiring (McBSP-0 → SIO-0, McBSP-1 → SIO-1) and "cross"-wiring (McBSP-1 → SIO-0, McBSP-0 → SIO-1). Available installations of the J4 jumper set are presented at figure 2-14.
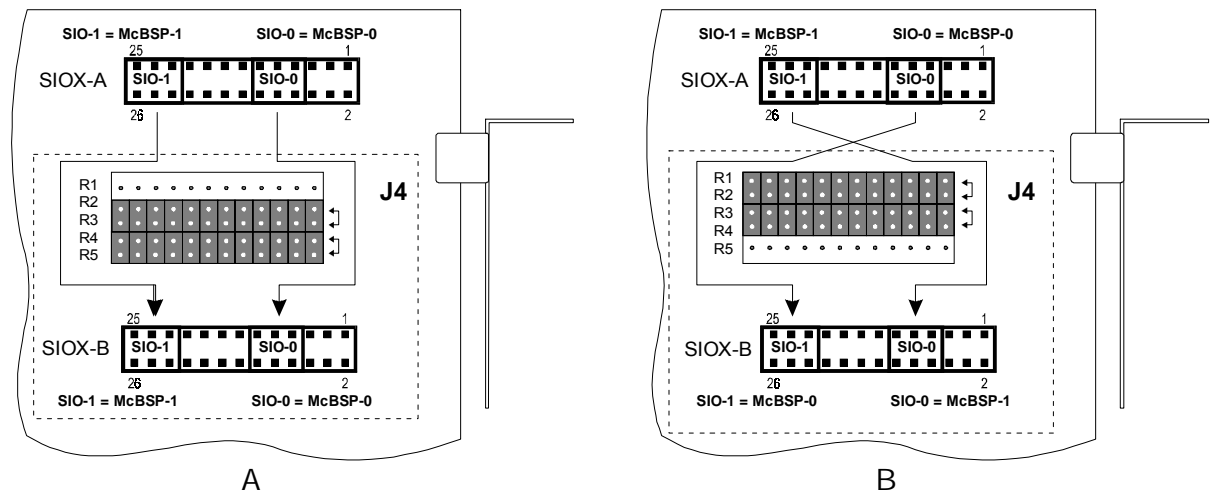
Fig. 2-14. "Direct" (A) and "cross" (B) wiring configurations of SIO-0/1 ports for SIOX-B site for *TORNADO-62/67*.

Generating Reset Signals for SIOX-A/B Expansion Interface Sites

TORNADO-6x allows generation of individual reset signals for SIOX-A and SIOX-B expansion interface sites (refer to the corresponding sections earlier in this chapter) using the following logical conditions:

- SIOX-A/B reset signals are active in case the on-board DSP is in the 'RESET' state
- reset signal(s) for SIOX-A/B expansion site can be released only in case DSP is in the 'RUN' state and the corresponding bit(s) *SIOX-A_RUN* and *SIOX-B_RUN* of *PXSX_RUN* IOX register is(are) set to the logical '1' value by DSP software.

This allows correct initialization of the SIOX-A/B daughter-card hardware and correct synchronization with the DSP software.

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CAUTION

TORNADO-6x rev.2A hardware provides different on-board logic for generation of
SIOX/PIOX reset signals if compared to *TORNADO-6x* rev.1.x hardware.

TORNADO-6x rev.1x generates common SIOX/PIOX reset signal using *XRESET* IOX
register, and this reset signal was generated as the logical OR between the DSP reset signal
and bit D0 of *XRESET* IOX register.

</div>

SIOX-A reset signal can be released by the TMS320C6x DSP software by means of writing logical '1' value to
the *SIOX-A_RUN* bit of *PXSX_RUN* IOX register (refer to table 2-2 and to the corresponding subsection in
section "TMS320C6x DSP Environment" earlier in this chapter), and this will allow operation of the SIOX-A
daughter-card hardware. Writing logical '0' to *SIOX-A_RUN* bit of *PXSX_RUN* IOX register, which is the
default value on the DSP reset, will set the SIOX-A reset signal active.

SIOX-B reset signal can be released by the TMS320C6x DSP software by means of writing logical '1' value to
the *SIOX-B_RUN* bit of *PXSX_RUN* IOX register (refer to table 2-2 and to the corresponding subsection in
section "TMS320C6x DSP Environment" earlier in this chapter), and this will allow operation of the SIOX-B
daughter-card hardware. Writing logical '0' to *SIOX-B_RUN* bit of *PXSX_RUN* IOX register, which is the
default value on the DSP reset, will set the SIOX-B reset signal active.

Connecting External Clocks to McBSP-0/McBSP-1 Serial Ports

TORNADO-6x DSP systems allow connection of external clock source to the DSP on-chip McBSP-0 and
McBSP-1 serial ports. These clocks are known as CLKS-0 and CLKS-1 signals in accordance with TI
TMS320C6x specifications. Usage of CLKS-0/1 external clocks for the DSP on-chip McBSP-0/1 serial ports
delivers outstanding flexibility in generation of virtually any data transfer frequency for the McBSP-0/1 serial
ports in order to meet the requirements of any application.

External clock source signals CLKS-0/1 for each of the McBSP-0/1 serial ports independently are available via
either of the following signal sources:
- via JP6 (for McBSP-0 port) and JP7 (for McBSP-1 port) on-board connectors (refer to fig.2-1a and
  fig.A-1)
- via 5v TTL/CMOS crystal generators in the DIP-8 package, which might be installed into the S2 (for
  McBSP-0 port) and S3 (for McBSP-1 port) on-board sockets (refer to fig.2-1a and fig.A-1).

Details of JP6/JP7 connector specifications and location of the S2/S3 crystal generators sites for connection of
clock source signals CLKS-0/1 for McBSP-0/1 serial ports are shown at figure 2-15.

Selection of the CLKS-0/1 source clock as the timing source clock for the McBSP-0/1 instead of DSP clock is
performed by means of programming the DSP on-chip McBSP-0/1 control registers. Refer to original TI
TMS320C6x documentation for getting more information on programming the McBSP serial ports.

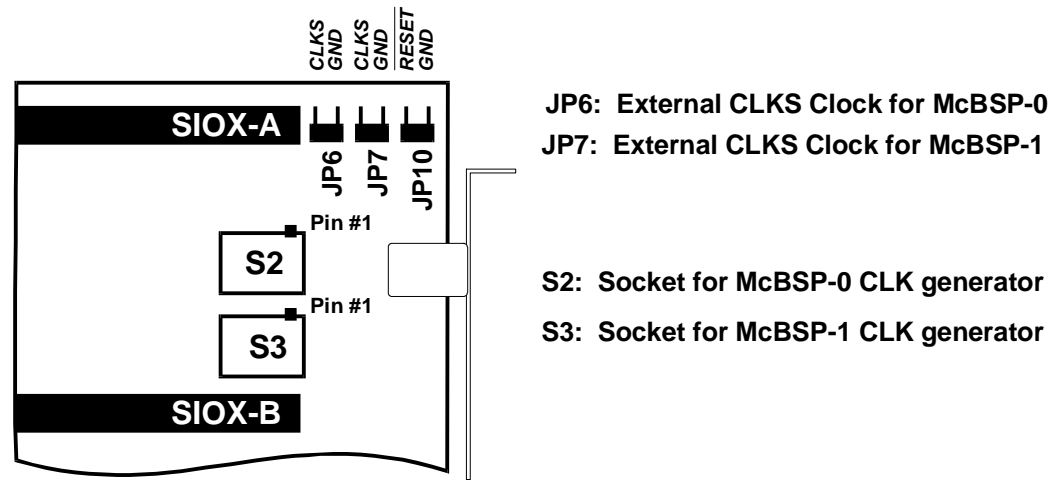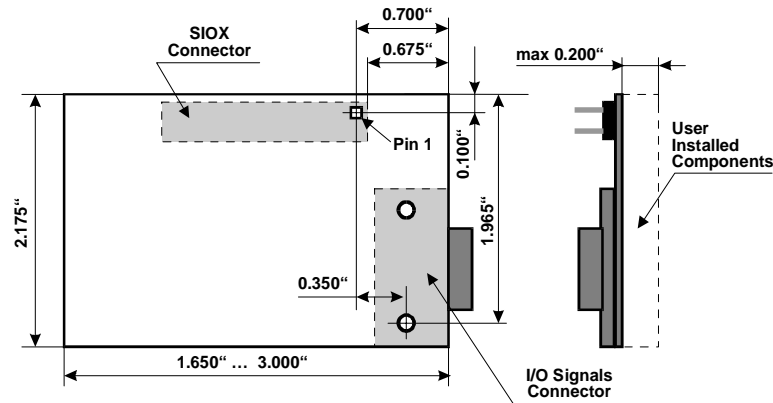*Fig. 2-15.* McBSP-0/McBSP-1 External Clock Connectors and Crystal Generators Sites.

Physical Dimensions for SIOX Daughter-card Modules

Physical dimensions for SIOX daughter-card module are presented at fig.2-16. This information is intended for those *TORNADO* customers, who need to design customized SIOX daughter-card modules.

Fig.2-16. Physical dimensions for SIOX daughter-card modules.

2.8   Emulation Tools for *TORNADO-6x*

TORNADO-6x uses scan-path emulation technique for the on-board TMS320C6x DSP in order to debug resident TMS320C6x DSP environment and software. Compatible scan-path emulation tools, which can be used with *TORNADO-6x* are as the following:

- external TI XDS510 and MicroLAB' *MIRAGE-510DX* universal JTAG scan-path emulators
- low cost emulation controller chip (*ECC*) for *TORNADO-62MX/67MX*, which plugs into the dedicated on-board socket on *TORNADO-62MX/67MX* mainboard
- low cost universal emulation control daughter-card module (*UECMX*) for *TORNADO* DSP systems, which plugs into the dedicated site on *TORNADO-62/67*. *UECMX* converts *TORNADO-62/67* DSP system into universal emulator for all TI TMS320 DSP if used with optional external buffer pod, which is compatible with *MIRAGE-510DX* emulator.
- TI HLL Debuggers and GoDSP Code Composer IDE as the debugging environments for TMS320 DSPs, which run with all of the above emulator tools (*ECC*, *UECMX* , TI XDS510 and MicroLAB' *MIRAGE-510DX* universal scan-path emulators).

CAUTION

The DSP must be released from the 'RESET' state and placed into the 'RUN' state prior running TI C6x HLL Debugger or GoDSP C6x Code Composer IDE for debugging the on-board C6x DSP chip of *TORNADO-6x* DSP system via JTAG path (use *-cr0* command line option of *T6CC.EXE* software utility).

It is recommended that the *T6CC.EXE* software utility will be invoked with the *-r* command line option just after the host power on or after any software trouble situation. This will guarantee that the DSP will be put into known state after the DSP will be released from the 'RESET' state prior running the TI C6x HLL Debugger or GoDSP C6x Code Composer IDE.

TORNADO-62/67 on-board JTAG path for connection to external JTAG emulator

TORNADO-62/67 on-board JTAG path for connection to external TI XDS510 or MicroLAB' *MIRAGE-510DX* JTAG emulator is presented at figure 2-17 (see also fig. 2-1 and fig. A-1) and comprises of JTAG-IN connector (JP4), TMS320C6x JTAG port, JTAG-OUT connector (JP5) and JTAG path terminating jumper (J5).
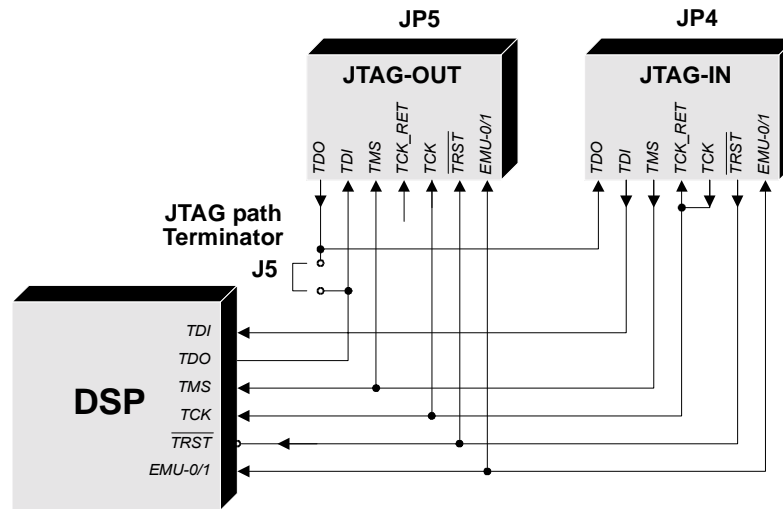
Fig. 2-17. On-board JTAG path for connection external JTAG emulator to *TORNADO-62/67*.

The on-board JTAG-IN connector should be used for connection of either external JTAG emulator or for connection to the JTAG-OUT connector of 'previous' JTAG device in the JTAG path.

The on-board JTAG-OUT connector should be used in case another JTAG device(s) is(are) included in the same JTAG path 'after' *TORNADO-62/67* board. In this case, the succeeding JTAG device should connect to JTAG-OUT connector of *TORNADO-62/67* using JTAG EXTENSION CABLE in the daisy-chain manner. Last JTAG device should terminate JTAG path and return JTAG *TDO* signal back to the emulator, which is connected to the first JTAG device in JTAG path. JTAG devices, included into the JTAG path together with *TORNADO-62/67* board, might include any JTAG supporting devices without any restrictions (logic, FPGA, other DSPs, etc). However the debugger JTAG path configuration file for JTAG emulator must accurately specify all JTAG devices in JTAG path.

CAUTION

The *TORNADO-62/67* on-board J5 jumper is used for termination of JTAG path on *TORNADO-62/67*.

J5 jumper should set to ON (installed) once *TORNADO-62/67* is either the only or the last JTAG device in JTAG path.

J5 jumper should set to OFF (removed) once two or more JTAG devices are included into JTAG path, and *TORNADO-62/67* is not the last JTAG device in JTAG path.

> **CAUTION**
>
> In case *TORNADO-62/67* is used with other JTAG devices connected to the JTAG-OUT connector, then the succeeding JTAG devices should use the JTAG default *TCK* clock source, which outcomes from the JTAG-OUT connector of *TORNADO-62/67*.

Using external JTAG emulator with single TORNADO-62/67 board

If external TI XDS510 or MicroLAB' *MIRAGE-510DX* JTAG emulator is used for debugging single *TORNADO-62/67* board, then this emulator should connect to the dedicated on-board JTAG-IN connector on *TORNADO-62/67* mainboard with the J5 JTAG terminator jumper installed and the JTAG-OUT connector left unconnected (fig. 2-18). In this case the debugger JTAG path configuration file for JTAG emulator should be normally omitted (refer to your debugger user's guide for details how to handle the JTAG path configuration file).
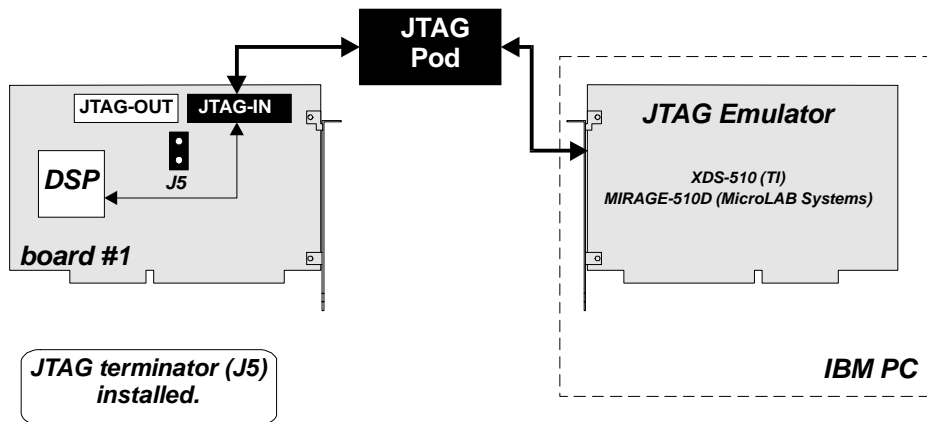
Fig. 2-18. Connection of external JTAG emulator to single *TORNADO-62/67* board.

Using external JTAG emulator with multiple TORNADO-62/67 boards

If either TI XDS510 or MicroLAB' *MIRAGE-510DX* universal JTAG emulator is used for debugging either multiple *TORNADO-62/67* boards or *TORNADO-62/67* board with other JTAG devices (other *TORNADO* boards, FPGA, other DSPs) in the same JTAG path, then this emulator should connect to the on-board JTAG-IN connector (JP4) of the 'first' *TORNADO-62/67* board in JTAG-path (see fig. 2-19).

The on-board JTAG-OUT connector (JP5) of the 'first' and 'intermediate' boards should connect to the 'next' JTAG device in the JTAG path using JTAG EXTENSION CABLE in the daisy-chain manner.

The 'last' JTAG device in JTAG path should terminate JTAG path via J5 JTAG terminator jumper and return the JTAG *TDO* signal back to JTAG emulator, which is connected to the first JTAG device in JTAG path.

The debugger JTAG path configuration file for JTAG emulator must accurately specify all JTAG devices in the JTAG path (refer to your debugger user's guide for details how to handle the JTAG path configuration file).

Fig. 2-19. Connection of external JTAG emulator to multiple *TORNADO-62/67* boards.

TORNADO-62/67 on-board JTAG path for UECMX emulator daughter-card module

UECMX is actually the low-cost replacement for external TI XDS510 and MicroLAB' *MIRAGE-510DX* universal JTAG emulators, however it does not require external JTAG pod for connection to *TORNADO-62/67* board via JTAG-IN connector. Instead, the on-board *TORNADO-62/67* hardware provides direct connection of the *UECMX* JTAG port to the on-board TMS320C6x DSP in case *UECMX* is installed and configured for operation with on-board DSP. Therefore, all available JTAG-path configurations for *UECMX* is are similar to that with external JTAG emulator.

TORNADO-62/67 on-board JTAG path for connection to low-cost MicroLAB' *UECMX* universal JTAG emulator daughter-card module for *TORNADO* DSP systems is presented at figure 2-20 (see also fig. 2-1 and fig. A-1) and comprises of *UECMX* site header connector (JP8), TMS320C6x JTAG port, JTAG-OUT connector (JP5) and JTAG path terminating jumper (J5).
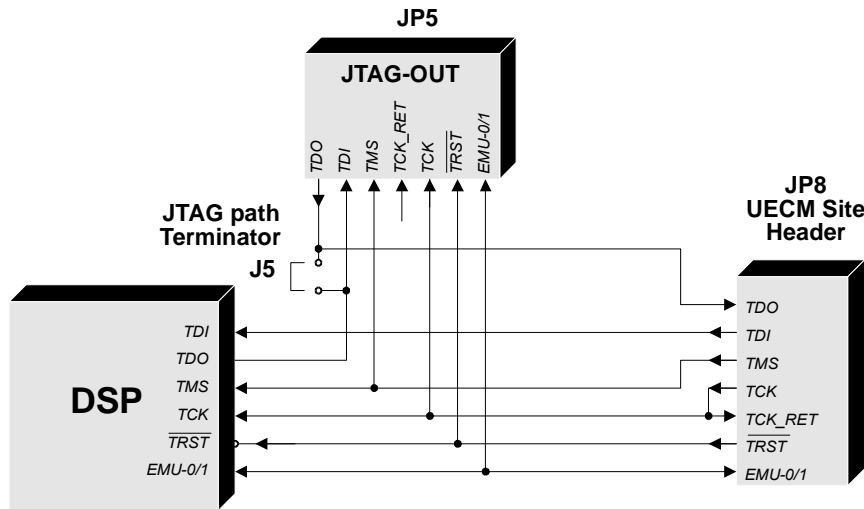
Fig. 2-20. On-board JTAG path for connection *UECMX* to *TORNADO-62/67*.

UECMX might be configured to connect either to the on-board TMS320C6x DSP or to any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP via optional MPSD or JTAG pod. This configuration is performed by the *T6CC.EXE* software utility, which is included with the *TORNADO-62/67* board (see chapter 4).

UECMX runs under the industry standard TI C6x HLL Debugger and GoDSP C6x Code Composer IDE, when it is configured for debugging the *TORNADO-62/67* on-board C6x DSP environment, and runs under any of TI C2xx, C3x, C4x, C5x, C54x, C6x, C8x HLL Debuggers or any of C2xx/C5x, C3x/C4x, C54x and C6x Code Composer IDE, when it is used for emulation of external TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP via optional MPSD or JTAG pod.

CAUTION

Once *UECMX* is installed onto *TORNADO-62/67* mainboard and configured for connection to the on-board DSP, then the on-board hardware disconnects the JTAG-IN (JP4) connector from on-board JTAG-path.

In this case the external TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator, which is connected to JTAG-IN connector *TORNADO-62/67* is ignored and its operation does not effect the functionality of *TORNADO-62/67* board.

Using UECMX with single TORNADO-62/67 board

If *UECMX* is used for debugging single *TORNADO-62/67* board, then *UECMX* should install onto this board to the dedicated *UECMX* site header (JP8) on *TORNADO-62/67* mainboard with the J5 JTAG terminator jumper installed and the JTAG-OUT connector left unconnected (fig. 2-21). In this case the debugger JTAG path configuration file for *UECMX* should be normally omitted (refer to your debugger user's guide for details how to handle the JTAG path configuration file).
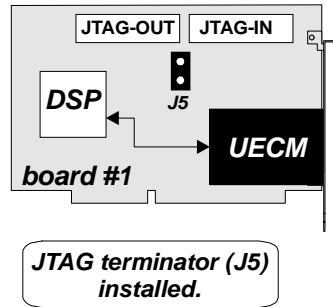
Fig. 2-21. Connection of *UECMX* to single *TORNADO-62/67* board.

Using UECMX with multiple TORNADO-62/67 boards

If *UECMX* is used for debugging either multiple *TORNADO-62/67* boards or *TORNADO-62/67* board with other JTAG devices (other *TORNADO* boards, FPGA, other DSPs) in the same JTAG path, then *UECMX* should install onto the 'first' *TORNADO-62/67* board in JTAG-path (see fig. 2-22).

The on-board JTAG-OUT connector (JP5) of the 'first' and 'intermediate' boards should connect to the 'next' JTAG device in the JTAG path using JTAG EXTENSION CABLE in the daisy-chain manner.

The 'last' JTAG device in JTAG path should terminate JTAG path via J5 JTAG terminator jumper and return the JTAG *TDO* signal back to JTAG emulator, which is connected to the first JTAG device in JTAG path.

The debugger JTAG path configuration file for JTAG emulator must accurately specify all JTAG devices in the JTAG path (refer to your debugger user's guide for details how to handle the JTAG path configuration file).
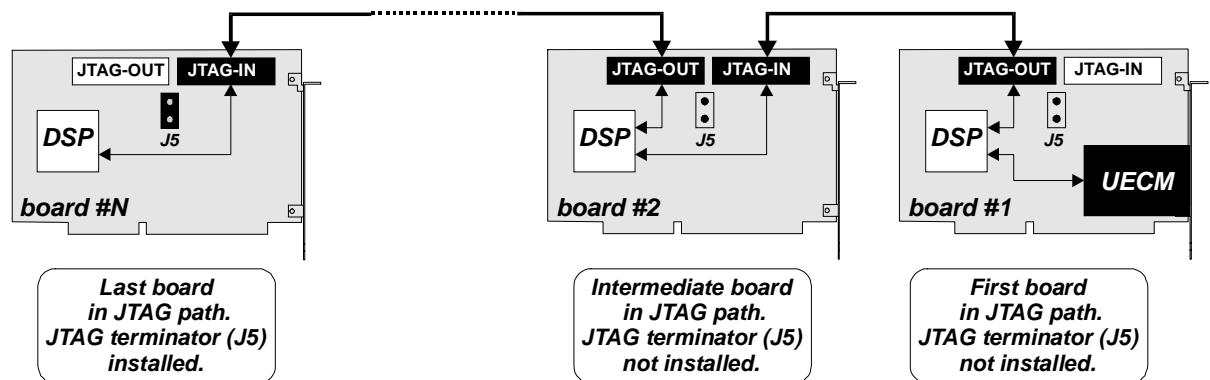

Fig. 2-22. Connection of *UECMX* to multiple *TORNADO-62/67* boards.

Using UECMX for emulation external TI TMS320 DSPs

UECMX also converts *TORNADO-62/67* into universal scan-path emulator for any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP. This feature requires optional external MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x) pod connected to *UECMX*. This optional external pod also connects to target TMS320 DSP. The MPSD and JTAG pods for *UECMX* are the pods used with MicroLAB' *MIRAGE-510DX* emulator.
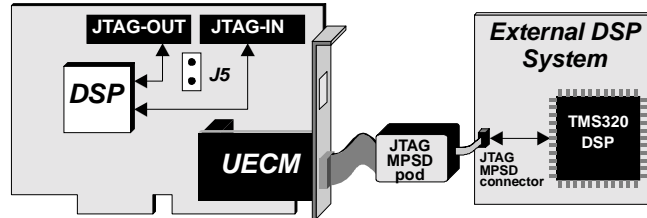

Fig. 2-23. Connection of *UECMX* to external TMS320 DSP via optional MPSD or JTAG path.

When *UECMX* is configured for emulation of any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP via optional MPSD or JTAG pod, then it may run under any of TI C2xx, C3x, C4x, C5x, C54x, C6x, C8x HLL Debuggers or any of C2xx/C5x, C3x/C4x, C54x and C6x Code Composer IDE.

CAUTION

Once *UECMX* is installed onto *TORNADO-62/67* mainboard and configured for connection to external TMS320 DSP via optional MPSD or JTAG pod, then the on-board hardware disconnects *UECMX* from on-board JTAG-path and configures the on-board JTAG-path for connection to external TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator via JTAG-IN (JP4) connector.

This allows any of single- or multi- board JTAG-path device configurations in accordance with the described above for external TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator.

TORNADO-62MX/67MX on-board JTAG-path

The on-board JTAG path of *TORNADO-62MX/67MX* (fig.2-24) comprises of JTAG-IN connector (JP4), TMS320C6x DSP and the *ECC* (emulation control chip, also known as TBC) socket site (S4).
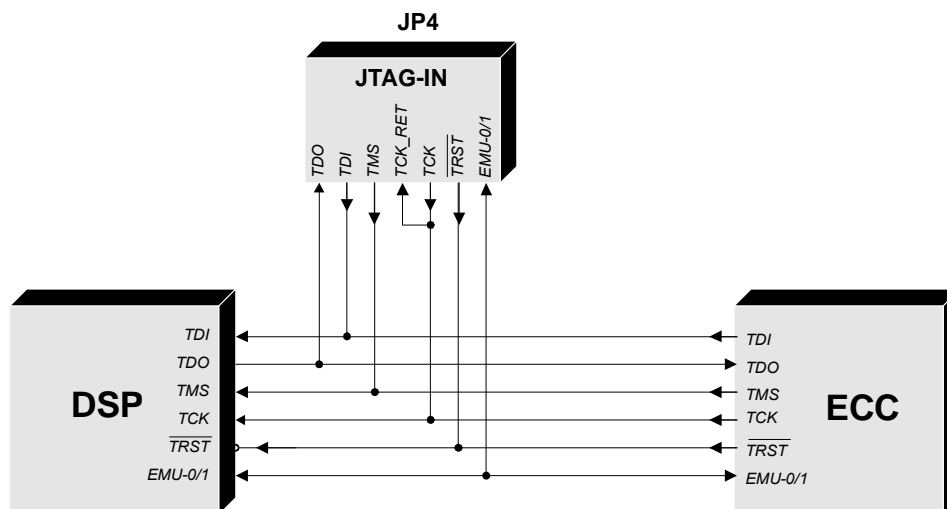
Fig. 2-24. On-board JTAG path of *TORNADO-62MX/67MX*.

JTAG-IN connector is designed for connection of external TI XDS510 or MicroLAB' *MIRAGE-510DX* JTAG emulator, and is actually parallel with optional on-board *ECC*.

CAUTION

If TI XDS510 or MicroLAB' *MIRAGE-510DX* universal scan-path emulator is being used with *TORNADO-62MX/67MX*, then the emulation controller chip (*ECC*) should be switched off, and vise-versa.

Connection of external XDS510 and *MIRAGE-510DX* emulators to the *TORNADO-62MX/67MX* on-board JTAG-IN connector while *ECC* is installed and is configured to connect to the on-board TMS320C6x DSP is strongly prohibited and may result in damage of either *ECC* or external XDS510 and *MIRAGE-510DX* emulators.

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CAUTION

JTAG path of *TORNADO-62MX/67MX* does not provide the dedicated JTAG 'multiprocessor-chaining' hardware (JTAG-OUT connector and JTAG path terminator).

When either of external JTAG emulator or *ECC* is used for emulation the *TORNADO-62MX/67MX* on-board TMS320C6x DSP, then JTAG 'multiprocessor-chain' mode is not allowed as standard with this JTAG connection.

Should the user consider to use *TORNADO-62MX/67MX* in JTAG 'multiprocessor-chain' while emulating the on-board TMS320C6x DSP, then optional external JTAG-path IN/OUT splitter is required. Call MicroLAB Systems for details.

</div>

Using external JTAG emulator with TORNADO-62MX/67MX

If external TI XDS510 or MicroLAB' *MIRAGE-510DX* JTAG emulator is considered for debugging the *TORNADO-62MX/67MX* on-board TMS320C6x DSP environment, then this emulator should connect to the dedicated on-board JTAG-IN connector on *TORNADO-62MX/67MX* mainboard (see fig.2-1, fig.2-25 and fig. A-1).
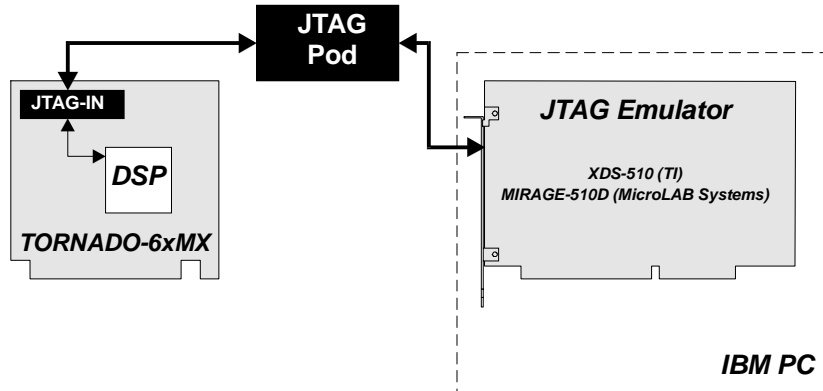

Fig. 2-25. Connection of external JTAG emulator to *TORNADO-62MX/67MX*.

CAUTION

If TI XDS510 or MicroLAB' *MIRAGE-510DX* universal scan-path emulator is being used with *TORNADO-62MX/67MX*, then the emulation controller chip (*ECC*) should be switched off.

Connection of external XDS510 and *MIRAGE-510DX* emulators to the *TORNADO-62MX/67MX* on-board JTAG-IN connector while *ECC* is installed and is configured to connect to the on-board TMS320C6x DSP is strongly prohibited and may result in damage of either *ECC* or external XDS510 and *MIRAGE-510DX* emulators.

Using ECC for emulation the TORNADO-62MX/67MX on-board TMS320C6x DSP

In case *TORNADO-62MX/67MX* is used inside the closed computer package, or external TI XDS510 or MicroLAB' *MIRAGE-510DX* universal JTAG emulator is not available, then optional *ECC* (emulation controller chip, also known as TBC) is recommended for emulation of *TORNADO-62MX/67MX* on-board TMS320C6x DSP.

ECC is a low-cost replacement for external TI XDS510 and MicroLAB' *MIRAGE-510DX* universal JTAG emulators and installs into the dedicated S4 socket on *TORNADO-62MX/67MX* mainboard (fig.2-26). *ECC* does not require external JTAG pod for connection to *TORNADO-62MX/67MX* board via JTAG-IN connector. Instead, the on-board *TORNADO-62MX/67MX* hardware provides direct connection of the *ECC* JTAG port to the on-board TMS320C6x DSP in case *ECC* is installed.
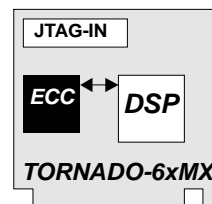

Fig. 2-26. Connection of *ECC* to *TORNADO-62MX/67MX* on-board TMS320C6x DSP.

ECC runs under the industry standard TI TMS320C6x HLL Debugger and GoDSP TMS320C6x Code Composer IDE.

Note, that *ECC* might be activated and allocated into the host PC-bus I/O area by means of the *T6CC.EXE* software utility, which is included with the *TORNADO-62/67* board (see chapter 4).

CAUTION

Once *ECC* is installed, then the external XDS510 or *MIRAGE-510DX* emulator should be disconnected from the JTAG-IN connector of *TORNADO-62MX/67MX*.

Connection of external XDS510 and *MIRAGE-510DX* emulators to the *TORNADO-62MX/67MX* on-board JTAG-IN connector while *ECC* is installed and is configured to connect to the on-board TMS320C6x DSP is strongly prohibited and may result in damage of either *ECC* or external XDS510 and *MIRAGE-510DX* emulators.

2.9   Software Development Tools

TMS320C6x DSP is now an industry standard DSP and is supported by a variety of software development tools from multiple 3rd party vendors.

Compilers and Debuggers

Software development for *TORNADO-6x* is supported by TI TMS320C6x DSP Optimizing C Compiler and Assembly Language Tools.

Debugging of TMS320C6x DSP resident software for *TORNADO-6x* is supported by C6000 Code Composer Studio IDE from Texas Instruments Inc (*www.ti.com*). C6000 Code Composer Studio IDE requires either on-board optional emulation controller chip (*ECC*) installed for *TORNADO-62MX/67MX* or *UECMX* emulation control daughter-card module installed for *TORNADO-62/67*, which may ship together with *TORNADO-6x* DSP system.

Hypersignal RIDE Visual DSP Algorithm Development and Simulation Tool

TORNADO-6x DSP systems are supported by DSP algorithm development tools from Hyperception Inc (Hypersignal Block Diagram, RIDE and Code Generator). Hypersignal RIDE is the visual real-time integrated DSP algorithm development and simulation environment for Windows 95/NT, and allows design entry using high-level function blocks (FIR, FFT, math, etc). The designed DSP algorithm is compiled and loaded into *TORNADO-6x* during design process in order to evaluate the algorithm parameters for real-time execution and to benefit from the ultra-high performance of *TORNADO-6x* DSP systems.

Real-time Multitasking Operating Systems (RTOS)

TORNADO-6x is supported by multiple RTOS that provide multitasking capabilities:
- *VIRTUOSO* from Eonic Systems Inc (*www.eonic.com*) is an industry standard high-performance RTOS and provides full feature multitasking support. It comes standard with capabilities for host file, keyboard and screen text/graphics I/O from DSP environment via *TORNADO-6x* host ISA-bus interface, and is available with a wide selection of function libraries for DSP, math, matrix, 2D, etc. computations.
- *NUCLEUS PLUS* from Accelerated Technology Inc (*www.atinucleus.com*) is an industry standard single-processor high-performance RTOS and provides full feature multitasking support. It features

- low cost and comes standard with source codes. Available options include *NUCLEUS FILE*, *NUCLEUS NET*, and *NUCLEUS DBUG+* that also come in source codes.
- *SPOX* from Spectron Microsystems Inc (*www.spectron.com*) is an industry standard RTOS for DSP that provides multitasking support. It is available with a selection of function libraries for DSP, math, matrix, etc. computations.

Application Software Tools for TORNADO-6x

Application specific tools for *TORNADO-6x* DSP system include a variety of function libraries for DSP, math, vector, image, etc computation, as well as function libraries for vocoder/fax/modem applications and audio multimedia.

Chapter 3. Installation and Configuration

This chapter includes instructions for configuring and installation of *TORNADO-6x* DSP system into host ISA-bus PC.

3.1 Setting I/O Base Address for Host ISA-bus I/O Interface

You have to setup ISA-bus I/O base address for host ISA-bus I/O interface of *TORNADO-6x* prior installation of *TORNADO-6x* board into ISA-bus slot of host PC. This procedure should be done while host PC power is switched off.

I/O base address for host ISA-bus I/O interface of *TORNADO-6x* is configured by means of on-board 3-button DIP-switch SW1 (refer to fig.2-2 and fig.A-1) in accordance with configuration setting in table 2-7.

CAUTION

When setting I/O base address for host ISA-bus I/O interface be sure to check I/O base address for other hardware installed in your host PC in order to avoid I/O address conflicts on ISA-bus.

TORNADO-6x is shipped from factory with I/O base address for host ISA-bus I/O interface in accordance with default settings from table 2-7.

3.2 Setting Interrupt Request Line for Host PC

Setting of host PC interrupt request line is optional procedure for *TORNADO-6x* and should be performed in accordance with requirements of application software that you use together with *TORNADO-6x*. This procedure should be done while host PC power is switched off.

Setting of host PC interrupt request line is provided via on-board host PC interrupt request jumper J1 (refer to fig.2-2 and fig.A-1). See section 2.5 for details about *TORNADO-6x* host PC interrupt support. *TORNADO-6x* is shipped from factory without PC interrupt request jumper installed.

CAUTION

When setting host CPU interrupt request line be sure to check interrupt requests for other hardware installed in your host PC in order to avoid interrupt request conflicts on ISA-bus.

3.3   Installation of *TORNADO-6x* Mainboard into Host PC

After I/O base address for host ISA-bus I/O interface of *TORNADO-6x* has been configured and host PC interrupt request line has been setup, you can now install *TORNADO-6x* board into 16-bit ISA-bus slot of host PC and screw on-board *TORNADO-6x* mounting bracket to rear panel of host PC. Afterthat, you can safely switch on power of host PC and load operating system of your PC.

3.4   Setting Memory Base Address for Host ISA-bus Memory Interface

After *TORNADO-6x* has been installed into host PC, the PC power has been switched on, and PC operating system (DOS or Windows) has been loaded, you can proceed with configuring ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-6x*.

It is recommended to use *T6CC.EXE* software utility for configuring ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-6x* at DOS prompt.

Setting host PC software environment for accessing host ISA-bus memory interface of TORNADO-6x

Prior you will start working with *TORNADO-6x* host ISA-bus memory interface, you have to configure host PC software environment in accordance with table 2-5 in order it can properly communicate with host ISA-bus memory interface of *TORNADO-6x*.

If memory base address of *TORNADO-6x* host ISA-bus memory interface should be set to *D8000H* hex value, then this requires including the following line into CONFIG.SYS file of host DOS or WINDOWS operating system:

Device=C:\DOS\EMM386.EXE noems x=D800-DFFF

or

Device=C:\WINDOWS\EMM386.EXE noems x=D800-DFFF

The "*x=D800-DFFF*" option for the *EMM386.EXE* memory driver informs *EMM386.EXE* memory driver to reserve the *D8000H..DFFFFH* UMB area, so it will might be used for communication with *TORNADO-6x* host ISA-bus memory interface.

Should you need to set different memory base address of *TORNADO-6x* host ISA-bus memory interface in accordance with table 2-5, then you should setup appropriate "*x=*" option for *EMM386.EXE* memory driver in CONFIG.SYS file. Please refer to documentation for DOS and WINDOWS operating system for details.

CAUTION

In case you have PCI PnP cards with UMB mapped memory-based PCI host interface (above 640KB and below 1MB of PC memory address space) installed into your PC along with *TORNADO-31x* board(s), then you have to reserve appropriate UMB area space for *TORNADO-31x* host ISA-bus memory interface via host PC build-in PCI BIOS on PC boot.

Setting memory base address for host ISA-bus memory interface of TORNADO-6x

You have to invoke *T6CC.EXE* software utility with *-imXXXXX* command line option in order to setup ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-6x* at DOS prompt in accordance with table 2-5.

The following example sets *D8000H* memory base address for host ISA-bus memory interface of *TORNADO-6x*:

> *T6CC -imD8000*

In case I/O base address of host ISA-bus I/O interface of *TORNADO-6x* differs from default value specified in table 2-7, then you have also specify *-ipXXX* command line option (where *XXX* denotes I/O base address of host ISA-bus I/O interface for *TORNADO-6x*) in DOS command line when invoking *T6CC.EXE* software utility.

The following example shows how to invoke *T6CC.EXE* software utility for *TORNADO-6x* DSP system with I/O base address for host ISA-bus I/O interface being configured to 300H value:

> *T6CC -imD8000 -ip300*

Switching Off host ISA-bus memory interface of TORNADO-6x

The following example shows how to switch off host ISA-bus memory interface of *TORNADO-6x* DSP system:

> *T6CC -im0*

CAUTION

When setting memory base address for host ISA-bus memory interfaces be sure to check memory base address for other hardware installed in your host PC in order to avoid memory address conflicts on ISA-bus.

3.5 Installation of Emulation Controller (ECC) onto *TORNADO-62MX/67MX* Mainboard

Installation of emulation controller chip (*ECC*) onto *TORNADO-62MX/67MX* board should be performed while host PC power off.

Installation of ECC

In order to install emulation controller chip (*ECC*) into the S4 socket onto *TORNADO-62MX/67MX* board follow recommendations below (see fig. 3-1):

- switch off power of host PC
- remove *TORNADO-62MX/67MX* board from host PC ISA-bus slot
- take *ECC* by your fingers in such way that its front (labeling) surface is turned at you
- adjust *ECC* to be parallel to surface of the corresponding S4 PLCC-44 socket on *TORNADO-62MX/67MX* board
- orient *ECC* in such way, that the key corner of its PLCC-44 package would match the corresponding corner of on-board S4 PLCC-44 socket
- safely insert *ECC* into on-board S4 PLCC-44 socket
- safely plug and fix *ECC* in the on-board S4 PLCC-44 socket
- install *TORNADO-62MX/67MX* install into 8-bit ISA-bus slot of host PC
- switch on power of host PC

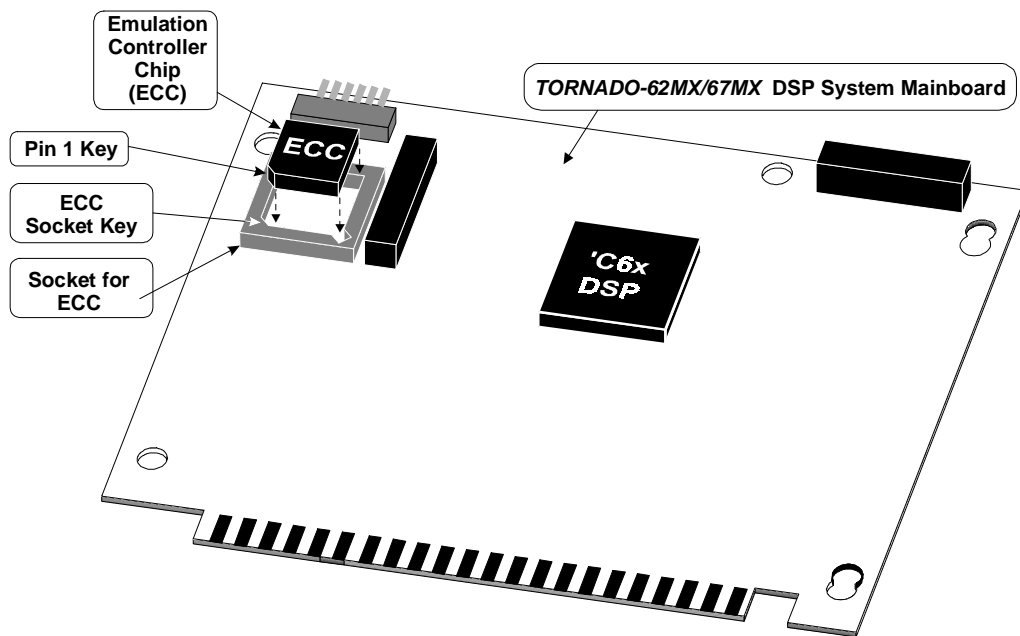*Fig.3-1.*   Installation of emulation controller chip (*ECC*) onto *TORNADO-62MX/67MX* board.

Setting I/O Base Address for ECC

You have to invoke *T6CC.EXE* software utility with *-epXXX* command line option in order to setup ISA-bus I/O base address for *ECC* at DOS prompt in accordance with table 2-14.

The following example sets *240H* I/O base address for *ECC*:

                                         T6CC -ep240

In case I/O base address of host ISA-bus I/O interface of *TORNADO-62MX/67MX* differs from the default value in table 2-7, then you have also specify the *-ipXXX* command line option (where *XXX* denotes I/O base address of host ISA-bus I/O interface for *TORNADO-62MX/67MX*) in DOS command line when invoking *T6CC.EXE* software utility.

The following example shows how to invoke *T6CC.EXE* software utility for *TORNADO-62MX/67MX* DSP system with I/O base address for host ISA-bus I/O interface being configured to 300H value:

<div align="center">*T6CC -ep240 -ip300*</div>

Switching ECC Out from ISA-bus I/O Address Space

The following example demonstrates how to switch *ECC* out from ISA-bus I/O address space:

<div align="center">*T6CC -ep0*</div>

CAUTION

When setting I/O base address for *ECC* be sure to check I/O base address for other hardware installed in your host PC in order to avoid I/O address conflicts on ISA-bus.

3.6 Installation of *UECMX* Daughter-Card Module onto *TORNADO-62/67* Mainboard

You have to install *UECMX* module as a daughter-card module (see fig.1-1) into the dedicated on-board connector of *TORNADO-62/67* mainboard (see fig.2-2a and fig.A-1a).

CAUTION

Once you install the *UECMX* daughter-card module onto the *TORNADO-62/67* mainboard, you cannot use SIOX-1 site for installation of SIOX AD/DA/DIO daughter-card modules.

In order to install *UECMX* module onto *TORNADO-62/67* mainboard you have to follow the instructions below (see fig.3-2):
- slant the *UECMX* module
- insert the on-module connector for active buffer pod into the corresponding hole in the *TORNADO-62/67* mounting bracket
- plug in the *UECMX* male header into the dedicated female connector on *TORNADO-62/67* mainboard
- setup the ISA-bus I/O base address for the *UECMX* module using the on-module DIP-switch in accordance with the "*UECMX/ECC* User's Guide".
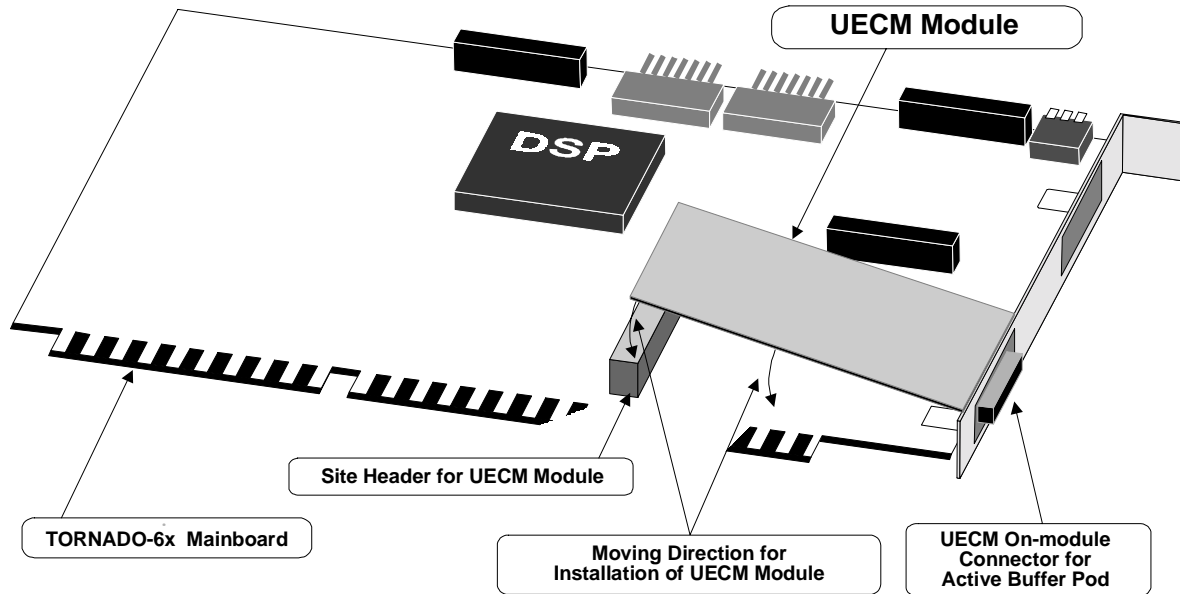
Fig.3-2. Installation of *UECMX* daughter-card module onto *TORNADO-62/67* mainboard.

The *UECMX* can connect both to the on-board TMS320C6x DSP and any external
TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP via optional external buffer pod.

Configuring UECMX to connect to the on-board TMS320C6x DSP JTAG path

After power-on, the *UECMX* is connect to the on-board TMS320C6x DSP JTAG path. You do not need to use
any external JTAG pod for this configuration.

CAUTION

When using the *UECMX* daughter-card module to emulate the on-board TMS320C6x DSP, be
sure to set properly the on-board JTAG path terminating jumper J5 in accordance with figure
2-16.

If you want to configure *UECMX* to connect to the on-board TMS320C6x DSP, then you should use the
T6CC.EXE software utility with '*-ei*' command line option. If *UECMX* is allocated at the I/O base address that
differs from the 240H I/O base address, then use '*-epXXX*' command line option for specifying the I/O base
address for *UECMX* (default is the '*-ep240*' configuration).

The following command line configures the *UECMX*, which is allocated at 280H I/O base address, to connect to
the on-board TMS320C6x DSP JTAG path:

T6CC -ei -ep280

Using UECMX for emulation of external TMS320 DSP

If you want to use *UECMX* to emulate any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP, you have to use optional MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x) external buffer pod for connection between the *UECMX* and external TMS320 DSP.

In order to configure the *UECMX* to connect to external TMS320 DSP, you can use the *T6CC.EXE* software utility with '*-EX*' command line option and the '*-epXXX*' command line option for specifying the I/O base address for *UECMX* (default is the '*-epXXX*' configuration).

The following command line configures the *UECMX* (allocated at 280H I/O base address) to connect to external TMS320 DSP via optional external buffer MPSD or JTAG pod:

T6CC -ex -ep280

3.7 Installation of FLASH/EPROM chip onto *TORNADO-6x* Mainboard

Installation of FLASH/EPROM chip (see fig.2-2 and fig.A-1) onto *TORNADO-6x* board should be performed while host PC power off.

CAUTION

TORNADO-6x mainboards are designed to carry the FLASH 5v-only 128K..1Mx8 chips or EPROM 128K..1Mx8 chips in the PLCC-32 IC package.

Installation of other FLASH/EPROM chips than that specified in table 2-3 may result in damage of FLASH/EPROM chip and/or of *TORNADO-6x* hardware.

CAUTION

You have to set the on-board J2 jumper in accordance with table 2-3 in order to meet the installed FLASH/EPROM chip type.

Installation of FLASH/EPROM chip

In order to FLASH/EPROM into the *TORNADO-6x* S1 on-board socket follow the recommendations below (see fig. 3-3):
- switch off power of host PC
- remove *TORNADO-6x* board from host PC ISA-bus slot
- take FLASH/EPROM chip by your fingers in such way that its front (labeling) surface is turned at you

- adjust FLASH /EPROM chip to be parallel to surface of the S1 PLCC-32 socket on *TORNADO-6x* board
- orient FLASH/EPROM chip in such way, that the key corner of its PLCC-32 package would match the corresponding corner of on-board S1 PLCC-32 socket
- safely insert FLASH/EPROM chip into the on-board S1 PLCC-32 socket
- safely plug and fix FLASH/EPROM chip in the on-board S1 PLCC-32 socket
- set J2 jumper in accordance with table 2-3 to meet the installed FLASH/EPROM chip type
- install *TORNADO-62MX/67MX* install into 16-bit ISA-bus slot of host PC
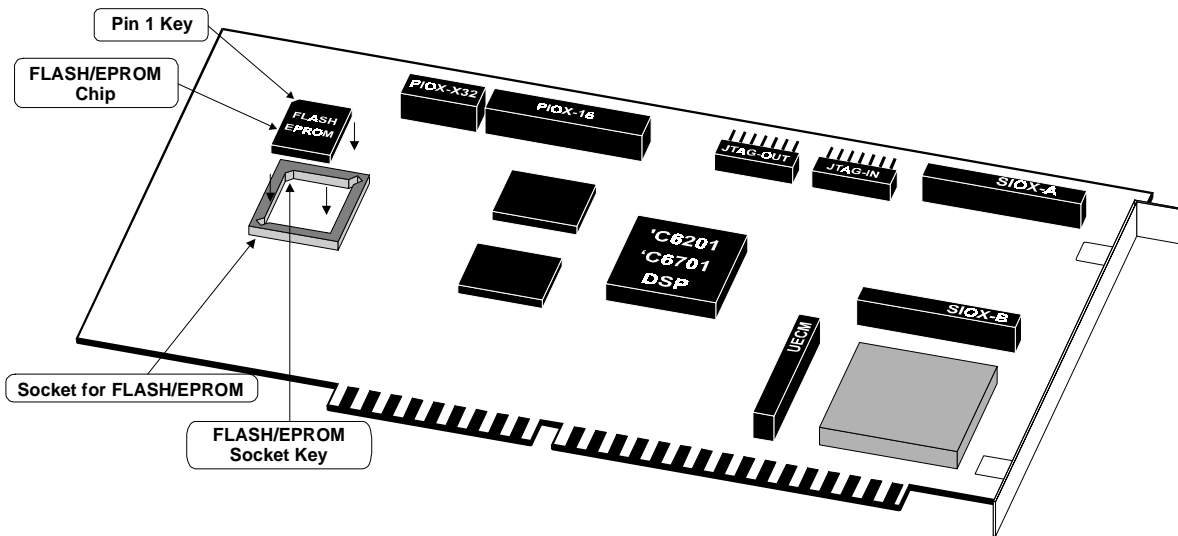- switch on power of host PC

Fig.3-3.   Installation of FLASH/EPROM chip onto *TORNADO-6x* mainboard.

Chapter 4.   Utility Software

This chapter contains description of utility software for *TORNADO-6x* DSP system.

4.1   *T6CC.EXE* Control Center Utility

T6CC.EXE ("*TORNADO-6x* Control Center") utility is a DOS command line control software tool for *TORNADO-6x* that delivers easy and powerful user control for *TORNADO-6x* hardware. *T6CC.EXE* utility features the following functionality:

- display and set all registers of *TORNADO-6x* host ISA-bus I/O interface
- read/write from/to the on-board SB areas (SBSRAM, FLASH and PIOX/PIOX-16) via *TORNADO-6x* host ISA-bus memory interface
- access to all DSP memory areas via the DSP on-chip HPI port
- configure the *ECC* emulation controller for *TORNADO-62MX/67MX* and *UECMX* emulation control daughter-card module for *TORNADO-62/67.*

T6CC.EXE utility must be invoked from DOS prompt with up to ten command line options:

<div align="center">

T6CC [-*option1*] [-*option2*] [-*option3*] *...*

</div>

Each command line option corresponds to specific *TORNADO-6x* hardware control operation. The following is a list of available command line options for *T6CC.EXE* utility.

System Control via CONTROL REGISTER

-c	Display and interpret contents of *CONTROL REGISTER*.
-cc	Display current setting for host SB data cycle format, which is specified by {*SB_CCL-0,SB_CCL-1*} bit field of *CONTROL REGISTER*.
-ccb	Set 8-bit (byte) format for host SB data cycle. Corresponds to setting of {*SB_CCL-0,SB_CCL-1*} bit field of the *CONTROL REGISTER* to the {0,0} state.
-cch	Set 16-bit (halfword) format for host SB data cycle. Corresponds to setting of {*SB_CCL-0,SB_CCL-1*} bit field of *CONTROL REGISTER* to the {1,0} state.
-ccw	Set 32-bit (word) format for host SB data cycle. Corresponds to setting of {*SB_CCL-0,SB_CCL-1*} bit field of *CONTROL REGISTER* to the {0,1} state.
-cg	Display current state of *SB_GLOCK* bit (global SB locking by host ISA-bus memory interface) of *CONTROL REGISTER*.
-cg0	Clear *SB_GLOCK* bit of *CONTROL REGISTER* and unlock SB.
-cg1	Set *SB_GLOCK* bit of *CONTROL REGISTER* for immediate active SB locking.

-cl	Display current state of *SB_LOCK* bit (SB locking by host ISA-bus memory interface) of *CONTROL REGISTER*.
-cl0	Clear *SB_LOCK* bit of *CONTROL REGISTER* and unlock SB.
-cl1	Set *SB_LOCK* bit of *CONTROL REGISTER* and issue active SB locking during nearest SB access from host ISA-bus memory interface.
-cie	Display current state of *SB_ERROR_IE* bit (host interrupt enable on SB error) of *CONTROL REGISTER*.
-cie0	Clear *SB_ERROR_IE* bit of *CONTROL REGISTER* and disable host interrupts on SB error.
-cie1	Set *SB_ERROR_IE* bit of *CONTROL REGISTER* and enable host interrupts on SB error.
-cim	Display current state of *MH_RQ_IE* bit (host interrupt enable on requests from TMS320C6x DSP) of *CONTROL REGISTER*.
-cim0	Clear *MH_RQ_IE* bit of *CONTROL REGISTER* and disable host interrupts on requests from TMS320C6x DSP.
-cim1	Set *MH_RQ_IE* bit of *CONTROL REGISTER* and enable host interrupts on requests from TMS320C6x DSP.
-cr	Display current state of reset signal for TMS320C6x DSP, which is specified by *M_GO* bit of *CONTROL REGISTER*.
-cr0	Remove reset signal for TMS320C6x DSP, i.e. put DSP into "RUN" state. This option sets *M_GO* bit to '1' of *CONTROL REGISTER*.
-cr1	Apply reset signal for TMS320C6x DSP, i.e. put DSP into "RESET" state. This option clears *M_GO* bit of *CONTROL REGISTER*.

Flag Registers Control

-fsr	Display contents of *FLAG SELECTOR REGISTER*.
-fsrXX	Select flag register #*XX (hex)*, i.e. load *XX* 8-bit hex data into *FLAG SELECTOR REGISTER*.
-fr	Display contents of currently selected flag register (display *FLAG STATUS REGISTER*). The number of currently selected flag register is defined by the contents of *FLAG SELECTOR REGISTER*.
-frXX	Loads *XX* 8-bit hex data into the currently selected flag register (load *FLAG CONTROL REGISTER*). The number of currently selected flag register is defined by the contents of *FLAG SELECTOR REGISTER*..
-frs	Display and interpret contents of *SYS_STATUS_FRG* flag register.
-fe	Display current state of *SB_ERROR* flag from *SYS_STATUS_FRG* flag register.

-fe0	Clear *SB_ERROR* flag, i.e. write to *CLEAR_SB_ERROR_FRG* flag register.
-fb	Display current state of *SB_ACK* flag from *SYS_STATUS_FRG* flag register.
-fh	Display current state of *MH_RQ* flag from *SYS_STATUS_FRG* flag register.
-fh0	Clear *MH_RQ* flag, i.e. write to *CLEAR_MH_RQ_FRG* flag register.
-fhh	Display current state of *HPI_HINT* DSP-to-host interrupt request via HPI from *SYS_STATUS_FRG* flag register.
-fhe	Display current state of *HPI_ERROR* flag from *SYS_STATUS_FRG* flag register.
-fhe0	Clear *HPI_ERROR* flag, i.e. write to *CLEAR_HPI_ERROR_FRG* flag register.
-fm1	Generate interrupt request to TMS320C6x DSP, i.e. write to *SET_HM_RQ_FRG* flag register.
-fhi	Display and interpret contents of *HPI_IE_FRG* flag register.
-fhie	Display current state of *HPI_ERROR_IE* bit (host interrupt enable on *HPI_ERROR*) of *HPI_IE_FRG* flag register.
-fhie0	Clear *HPI_ERROR_IE* bit of *HPI_IE_FRG* flag register and disable host interrupts on *HPI_ERROR*.
-fhie1	Set *HPI_ERROR_IE* bit of *HPI_IE_FRG* flag register and enable host interrupts on *HPI_ERROR*.
-fhih	Display current state of *HPI_HINT_IE* bit (host interrupt enable on *HPI_HINT*) of *HPI_IE_FRG* flag register.
-fhih0	Clear *HPI_HINT_IE* bit of *HPI_IE_FRG* flag register and disable host interrupts on *HPI_HINT*.
-fhih1	Set *HPI_HINT_IE* bit of *HPI_IE_FRG* flag register and enable host interrupts on *HPI_HINT*.
-fds	Display and interpret contents of *DSP_STATUS_FRG* flag register.
-fdsm	Display current state of *MLock* flag from *DSP_STATUS_FRG* flag register.
-fdsr	Display current state of *DSP_M_GO* flag from *DSP_STATUS_FRG* flag register.
-fdsp	Display current state of *DSP_PD* flag from *DSP_STATUS_FRG* flag register.
-frdi	Display *TORNADO-6x* device ID and s/n, i.e. display contents of *DEV_ID0_FRG* and *DEV_ID1_FRG* flag registers.

SB Access Control

-ba

Display contents of *SB PAGE MAPPER* register that defines *SMP* SB base address for host-to-SB access.

-balA@Z

Load *SB PAGE MAPPER* register with *SMP* SB base address that corresponds to *A* six digit hex SB address within the *Z* SB area ('S' - for SBSRAM area, 'F' - for FLASH area, and 'I' - for I/O area).

-bdSA,EA@Z

Display 32-bit SB data words. *SA* and *EA* parameters specify six digit hex SB starting and ending addresses correspondingly within the *Z* SB area ('S' - for SBSRAM area, 'F' - for FLASH area, and 'I' - for I/O area). Final contents of *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *EA* address.

-bdSA,EA@bZ

Display 8-bit SB data words (bytes). *SA* and *EA* parameters specify six digit hex SB starting and ending addresses correspondingly within the *Z* SB area ('S' - for SBSRAM area, 'F' - for FLASH area, and 'I' - for I/O area). Final contents of *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *EA* address.

-bdSA,EA@hZ

Display 16-bit SB data words. *SA* and *EA* parameters specify six digit hex SB starting and ending addresses correspondingly within the *Z* SB area ('S' - for SBSRAM area, 'F' - for FLASH area, and 'I' - for I/O area). Final contents of *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *EA* address.

-bwA,X@Z

Write 32-bit *X* hex data word at *A* six digit hex SB address. *A* parameter defines six digit SB address within the *Z* SB area ('S' - for SBSRAM area, 'F' - for FLASH area, and 'I' - for I/O area). *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *A* address.

-bwA,X@bZ

Write 8-bit *X* hex data word (byte) at *A* six digit hex SB address. *A* parameter defines six digit SB address within the *Z* SB area ('S' - for SBSRAM area, 'F' - for FLASH area, and 'I' - for I/O area). *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *A* address.

-bwA,X@hZ

Write 16-bit *X* hex data word at *A* six digit hex SB address. *A* parameter defines six digit SB address within the *Z* SB area ('S' - for SBSRAM area, 'F' - for FLASH area, and 'I' - for I/O area). *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *A* address.

HPI Access Control

-hc

Display and interpret contents of HPIC register of TMS320C542 DSP.

-hch0

Clear *HINT* bit of HPIC register (DSP-to-host interrupt request via HPI) of TMS320C6x DSP.

-hcd1

Set *DSPINT* bit of HPIC register (host-to-DSP interrupt request via HPI) of TMS320C6x DSP.

-hdSA,EA	Display 32-bit data words within the *SA...EA* hex HPI address range of TMS320C6x DSP.
-hwA,X	Write 32-bit *X* hex data word at *A* hex HPI memory address of TMS320C6x DSP.

Setting I/O and Memory Base Addresses for Host ISA-bus Interface

-im	Display ISA-bus memory base for host ISA-bus memory interface of *TORNADO-6x* in accordance with table 2-5 (display and interpret contents of *ISA_MI_BADDR_FRG* flag register).
-imXXXXX	Set *XXXXX* hex ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-6x* in accordance with table 2-5 (load *ISA_MI_BADDR_FRG* flag register). If *T6CC.EXE* utility is invoked with *-bd* or *-bw* command line options and option *-im* is not specified (or *ISA_MI_BADDR_FRG* flag register was not loaded previously), then the default *D8000H* ISA-bus memory base address will be used for host ISA-bus memory interface during host-to-SB access, and option *-im0* will be automatically executed on exit from *T6CC.EXE* utility in order to deactivate host ISA-bus memory interface afterthat.
-im0	Deactivates host ISA-bus memory interface of *TORNADO-6x*, i.e. removes it from ISA-bus memory address on exit from *T6CC.EXE* utility.
-ipXXX	Specifies *XXX* hex I/O base address for host ISA-bus I/O interface. If this option is omitted, then default factory setting in accordance with table 2-7 will is used.

Control for Emulation Controller (ECC) and Emulation Daughter-card Module (UECMX)

-ep	Display current ISA-bus I/O base for *ECC* for *TORNADO-62MX/67MX* in accordance with table 2-14 (display and interpret contents of *ISA_ECC_IO_BADDR_FRG* flag register).
-epXXX	Set *XXX* hex I/O base address for *ECC* for *TORNADO-62MX/67MX* in accordance with table 2-14 and activate it, i.e. include ECC into ISA-bus I/O address space and connect it to scan-path interface of TMS320C6x DSP. For *TORNADO-62/67* with *UECMX* installed, this option specified the I/O base address for *UECMX*. Once *T6CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB' MIRAGE-510DX emulator is not allowed for *TORNADO-62MX/67MX* unless *T6CC.EXE* utility will be invoked with *-ex* command line option.
-ei	Set default I/O base address for *ECC* for *TORNADO-62MX/67MX* in accordance with table 2-14 and activate *ECC*, i.e. include ECC into ISA-bus I/O address space and connect it to scan-path interface of TMS320C6x DSP. In case *D_OPTIONS* DOS system variable for TI TMS320C6x C Source Debugger is set and its list includes *-pXXX* option, then *XXX* hex I/O address will be used as default I/O base address for *ECC* instead of that

in accordance with table 2-14. For *TORNADO-62/67* with *UECMX* installed, this option configures *UECMX* to connect to the on-board TMS320C6x JTAG path. Once *T6CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB' MIRAGE-510DX emulator is not allowed to *TORNADO-62MX/67MX* and is ignored for *TORNADO-62/67* unless *T6CC.EXE* utility will be invoked with *-ex* command line option.

-ep0   Deactivates *ECC* controller for *TORNADO-62MX/67MX*, i.e. remove *ECC* from ISA-bus I/O address space and disconnect it from scan-path interface of TMS320C6x DSP. Once *T6CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB' MIRAGE-510DX emulator is allowed to *TORNADO-62MX/67MX*.

-ex   For *TORNADO-62MX/67MX* this option is identical to '*-ep0*' command line option, i.e. it removes *ECC* from ISA-bus I/O address space and disconnects it from scan-path interface of on-board TMS320C6x DSP. For *TORNADO-62/67* with *UECMX* installed this option configures *UECMX* to connect to external TMS320 DSP via optional MPSD or JTAG pod. Once *T6CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB' MIRAGE-510DX emulator is allowed to *TORNADO-6x*.

-er   Perform software reset of *ECC* or *UECMX*. Recommended on invocation and exit from TI TMS320C6x HLL Debugger or GoDSP TMS320C6x Code Composer IDE.

General System Control Options

-r   Perform software reset of *TORNADO-6x* host ISA-bus interface. All registers of host ISA-bus interface are put into default states, the *ECC* chip of *TORNADO-62MX/67MX* is reset, DSP is put into 'RESET' state, all error flags are reset, and all host interrupt enable masks are reset.
                    Also, the <B 0x00000000> program code is written into the reset vector location of DSP interrupt table (default address 0x00000000 after DSP reset), which guarantees that DSP will be put into known state after the DSP reset line will be released prior running the TI C6x HLL Debugger or C6000 Code Composer Studio IDE via DSP JTAG interface.

Utility Options

-p   Set page-by-page display mode. The "ESC" keypress terminates display output whereas any other keypress results in the next page display.

-?   Display list of available options for *T6CC.EXE* utility program. Help list is also displayed when *T6CC.EXE* utility program is invoked without command line options.

T6CC.EXE utility processes command line options in accordance with the following priority list:

1. *CONTROL REGISTER* control options
2. *FLAG STATUS REGISTER* and *FLAG CONTROL REGISTER* control options
3. HPI control options
4. *ECC* control options
5. SB access control options.

T6CC.EXE utility returns DOS *exit code* in case it is invoked with *-im*, *-c*, *-cg*, *-cl*, *-cie*, *-cim*, *-fsr*, *-fr*, *-frs*, *-fe*, *-fb, -fds, -fdsm, -fdsr, -fdsp, -fh, -fhh, -fhe, -fhi, -fhie* and *-fhih* command line options, which correspond to display of contents of registers, bits and flags of *TORNADO-6x* host ISA-bus interface. The exit code returned corresponds to current value or contents of last displayed bit, bit field, flag or register. Exit code is useful when *T6CC.EXE* utility is integrated into DOS batch (.BAT) file that provides conditional processing. Exit code of *T6CC.EXE* utility program can be analyzed using succeeding '*IF ERRORLEVEL*' DOS batch file commands. The following example of DOS batch file performs conditional processing of *SB_ERROR* flag of *TORNADO-6x*:

```
...
T6CC -fed
IF ERRORLEVEL 1  T6CC -fe0
...
```

When multiple data display options for the *T6CC.EXE* utility are specified, then the returned exit code will correspond to the last processed data display command line option.

In case error is detected by *T6CC.EXE* utility, then the exit code '255' is returned. If *T6CC.EXE* utility is invoked without any data display command line options and no errors is detected, than the exit code '0' is returned.

4.2   Uploading TMS320C6x COFF-files via Host ISA-bus Memory Interface

Uploading of TI TMS320C6x COFF-files (output .OUT files from TI TMS320C6x C/Assembler compilers) into *TORNADO-6x* on-board SB areas and TMS320C6x DSP on-chip environment can be performed by means of *T6COFF.EXE* software utility, that is included with utility software for *TORNADO-6x*. *T6COFF.EXE* utility loads TI TMS320C6x COFF-file into *TORNADO-6x* environment via host ISA-bus memory interface without utilization of emulation controller *ECC* or *UECMX* emulation control daughter-card module.

COFF-file can be uploaded into the *TORNADO-6x* environment using different modes:
- *standard mode*, i.e. when data is uploaded to on-board SB areas via host ISA-bus memory interface without affecting TMS320C6x DSP chip reset line and SB locking
- *reset mode*, i.e. when data is uploaded to on-board SB areas and TMS320C6x DSP on-chip environment via host ISA-bus memory interface while holding TMS320C6x DSP in 'RESET' state
- *global SB locking mode*, i.e. when data is uploaded to on-board SB areas via host ISA-bus memory interface using global SB locking
- *SB locking mode*, i.e. when data is uploaded to on-board SB areas via host ISA-bus memory interface using the SB locking.

All modes except for *reset mode* provide uploading of COFF-file into SB areas only. However, these modes do not effect reset signal for TMS320C6x DSP, and data can be uploaded in parallel with TMS320C6x DSP running.

Reset mode provides uploading of COFF‑file into both on-board SB areas and TMS320C6x DSP on-chip environment (including DSP on-chip memory and peripherals). This is performed by means of using run-time TMS320C6x loader that is loaded into on-board SBSRAM and then removed automatically by *T6COFF.EXE* utility each time loader recognizes that COFF‑file data section should be loaded into the DSP on-chip resources.

Uploading of COFF‑file into *TORNADO-6x* is performed by invoking *T6COFF.EXE* utility from DOS command line:

<div align="center">

T6COFF   FILENAME[.OUT] [-*option1*] [-*option2*] [-*option3*] ...

</div>

If file extension is missed for source *FILENAME* COFF‑file, then .OUT extension is assumed. The following is list of command line options for *T6COFF.EXE* utility, which are grouped into several functional groups.

Upload Mode Control

-lr	Set *RESET* mode for uploading of COFF‑file. COFF‑file is uploaded while holding TMS320C6x DSP in 'RESET' state by means of clearing the *M_GO* bit of *CONTROL REGISTER*. This mode is used for uploading of source program/data modules and supports uploading into both on-board SB areas and TMS320C6x DSP on-chip memory and peripherals. TMS320C6x DSP can be placed into the 'RUN' state on exit from *T6COFF.EXE* utility using *-cr0* command line option. The *-lr* option is assumed as default if none of *-lg*, *-ll* and *-ln* options is specified.
-lg	Set *GLOBAL SB LOCKING* mode for uploading of COFF‑file. COFF‑file is uploaded into on-board SB areas while holding SB locking by means of setting *SB_GLOCK* bit of *CONTROL REGISTER*. TMS320C6x DSP will not be able to access SB areas until uploading will be finished. TMS320C6x DSP on-chip resources cannot be loaded in this mode. This mode is normally used for uploading of shared data into on-board SB areas while TMS320C6x DSP is executing a program.
-ll	Set *SB LOCKING* mode for uploading of COFF‑file. COFF‑file is uploaded into on-board SB areas while holding SB locking by means of setting *SB_LOCK* bit of *CONTROL REGISTER*. TMS320C6x DSP will not be able to access SB areas until uploading will be finished. TMS320C6x DSP on-chip resources cannot be loaded in this mode. This mode is normally used for uploading of shared data into on-board SB areas while TMS320C6x DSP is executing a program.
-ln	Set *STANDARD* mode for uploading of COFF‑file. COFF‑file is uploaded without affecting the 'RESET' state of TMS320C6x DSP and without SB locking. TMS320C6x DSP will be able to access on-board SB areas during uploading of COFF‑file. The on-board TMS320C6x DSP on-chip resources cannot be loaded during this mode. This mode is normally used for uploading of run-time program or data into on-board SB areas while on-board TMS320C6x DSP chip is executing a program.
-xi	Exclude uploading of TMS320C6x DSP on-chip memory and peripherals when using the *RESET* mode for uploading. This option should be used together with *-lr* option only.

Restarting DSP on Exit

-cr0
Restart TMS320C6x DSP on exit from *T6COFF.EXE* utility. This option corresponds to toggling *M_GO* bit from *CONTROL REGISTER*.

Viewing Directory of COFF-file

-d
List directory (sections loading information) for COFF-file. COFF-file will be not loaded into *TORNADO-6x* environment an all other command line options specified will be ignored.

Setting Base Addresses of ISA-bus Memory and I/O Interfaces

-imXXXXX
Set *XXXXX* hex ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-6x* in accordance with table 2-5 (load *ISA_MI_BADDR_FRG* flag register). If *T6CC.EXE* utility is invoked with *-bd* or *-bw* command line options and option *-im* is not specified (or *ISA_MI_BADDR_FRG* flag register was not loaded previously), then the default *D8000H* ISA-bus memory base address will be used for host ISA-bus memory interface during host-to-SB access, and option *-im0* will be automatically executed on exit from *T6CC.EXE* utility in order to deactivate host ISA-bus memory interface afterthat.

-im0
Deactivates host ISA-bus memory interface of *TORNADO-6x*, i.e. removes it from ISA-bus memory address on exit from *T6CC.EXE* utility.

-ipXXX
Specifies *XXX* hex I/O base address for host ISA-bus I/O interface. If this option is omitted, then default factory setting in accordance with table 2-7 will is used.

Utility Options

-?
Display list of available options for *T6COFF.EXE* utility. Help list is also displayed when *T6COFF.EXE* utility is invoked without command line options and parameters.

In case no errors are detected by *T6COFF.EXE* utility, then exit code '0' will be returned, otherwise exit code '1' will be generated.

CAUTION

If *T6COFF.EXE* utility is used with *-lr* command line option (or when *-lg*, *-ll* and *-ln* options are not specified) and if either emulation controller (*ECC*) or *UECMX* emulation control daughter-card module is installed or any of TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator is attached, then the following error message may appear:

error: missing DSP handshaking

This error message states that the TMS320C6x DSP cannot be initialized correctly during uploading of TMS320C6x DSP on-chip memory or peripherals. This problem is caused by DSP on-chip execution controller that is locked by attached emulator or *ECC/UECMX*.

In order to avoid this problem you have to reset the *ECC/UECMX* or attached emulator. The emulator can be reset using the supplied software reset utility, whereas *ECC/UECMX* can be reset by invoking *T6CC.EXE* utility program with the *-er* command line option.

Appendix A.   On-board Jumpers, Connectors and Sockets.

This Appendix includes a summarized description for the *TORNADO-6x* on-board configuration jumpers, connectors, switches and sockets.

The layout for the *TORNADO-6x* on-board configuration jumpers, connectors, switches and sockets is presented at fig.A-1. Fig.A-1a contains information for the *TORNADO-62/67* layout, whereas fig.A-1b contains information for the *TORNADO-62/67* layout.
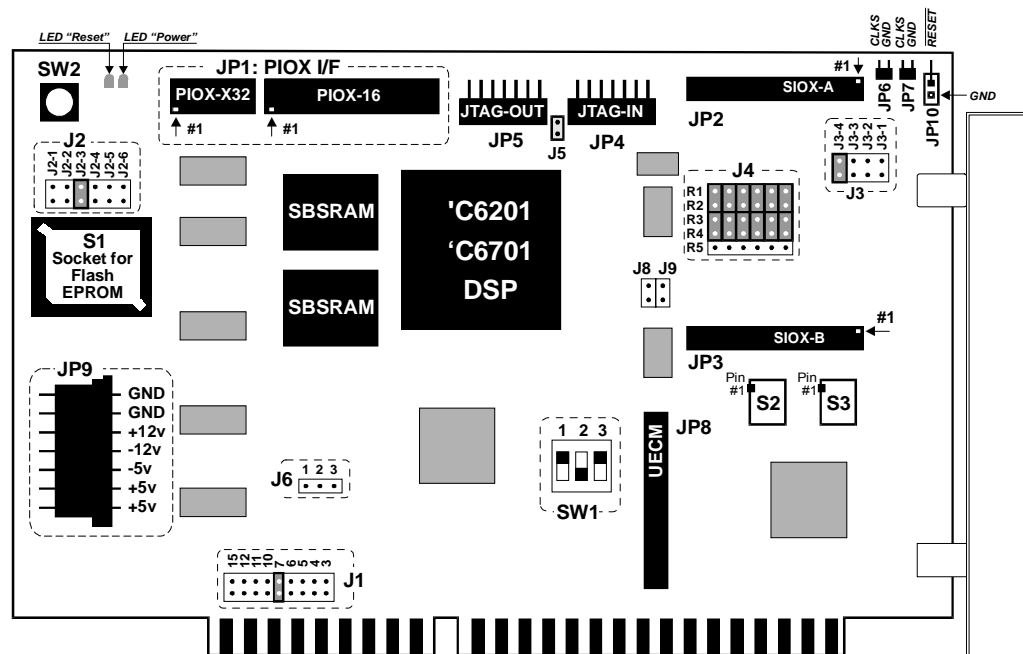

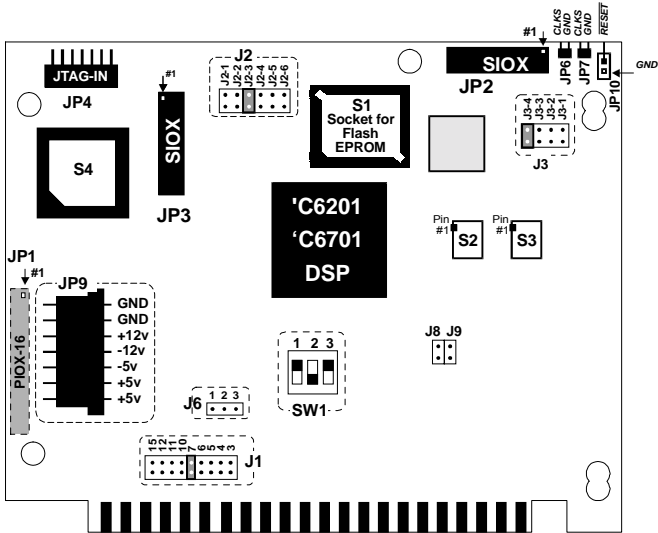*Fig.A-1a.*   On-board layout for *TORNADO-62/67*.

Fig.A-1b. On-board layout for *TORNADO-62MX/67MX*.

On-board Switches

All on-board switches for *TORNADO-6x* DSP systems are summarized in table A-1.

Table A-1. On-board switches for *TORNADO-6x*.

switch ID	switch function description	reference information
SW1	ISA -bus I/O base address for host ISA-bus I/O interface.	Section 2.5 and table 2-7.
SW2	Manual reset for the on-board TMS320C6x DSP in case DSP is used in stand-alone operation.	Section 2.3.

On-board Configuration Jumpers

All on-board configuration jumpers for *TORNADO-6x* DSP systems are summarized in table A-2.

Table A-2. On-board configuration jumpers for *TORNADO-6x*.

jumper ID	jumper function description	reference information
J1	Host ISA-bus interrupt request line selector.	Sections 2.5 and 3.2.

J2 *(J2-1..J2-6)*	FLASH/EPROM chip type selector.	Sections 2.3 and 3.7; table 2-3.
J3	TMS320C6x DSP Bootmode configuration.	Section 2.3 and table 2-4.
J4 *(J4-R1..J4-R5)*	SIOX-B site ports configurator ("direct" or "cross-wiring" selector) for *TORNADO-62/67*.	Section 2.7 and fig.2-14.
J5	JTAG path terminator.	Section 2.8 and fig.2-17..2-23.
J6	DSP Reset source selector.	Section 2.3.
J8	TMS320C6x DSP Timer-0 IN/OUT mode for SIOX-A/B and PIOX/PIOX-16.	Sections 2.6 and 2.7; tables 2-15 and 2-17.
J9	TMS320C6x DSP Timer-1 IN/OUT mode for SIOX-A/B and PIOX/PIOX-16.	Sections 2.6 and 2.7; tables 2-15 and 2-17.

On-board Connectors

All on-board connectors for *TORNADO-6x* DSP systems are summarized in table A-3.

Table A-3. On-board connectors and headers for *TORNADO-6x*.

connector ID	connector function description	reference information
JP1	PIOX/PIOX-16 expansion interface site header.	Section 2.6, fig.2-7 and fig. 2-8.
JP2 JP3	SIOX-A/B expansion interface sites headers.	Section 2.7 and fig.2-13.
JP4 JP5	JTAG-IN and JTAG-OUT connectors	Section 2.8 and fig.2-17..2-26.
JP6	External clock (CLKS) for McBSP-0 of TMS320C6x DSP.	Section 2.7 and fig.2-15.
JP7	External clock (CLKS) for McBSP-1 of TMS320C6x DSP.	Section 2.7 and fig.2-15.
JP8	UECMX site header.	Sections 2.8 and 3-6; fig.2-20..2-23
JP9	External power connector for stand-alone operation.	Section 2.3.
JP10	External DSP Reset connector for stand-alone operation.	Section 2.3.

On-board Sockets

All on-board sockets for *TORNADO-6x* DSP systems are summarized in table A-4.

Table A-4.   On-board sockets for *TORNADO-6x*.

socket ID	switch function description	reference information
S1	PLCC-32 socket for FLASH/EPROM (5v power supply).	Section 2.3.
S2	DIP-8 socket for TTL/CMOS 5v crystal generator for external clock source of McBSP-0 serial port of TMS320C6x DSP.	Section 2.7 and fig.2-15.
S3	DIP-8 socket for TTL/CMOS 5v crystal generator for external clock source of McBSP-1 serial port of TMS320C6x DSP.	Section 2.7 and fig.2-15.
S4	PLCC-44 socket for *ECC* (emulation controller chip) for local emulation of TMS320C6x DSP.	Section 2.8; fig.2-24 and 2-26.

Appendix B.   Glossary of Terms.

This Glossary contains definition for terms and other synchronism used along in this databook.

A

B

Bootmode Configuration
TMS320C6x DSP bootmode, which is defined by on-board jumper J3. Refer to section 2.3 for more details.

C

CLEAR_HPI_ERROR_FRG
Write-only flag register of host ISA-bus I/O interface, which clears the *HPI_ERROR* flag bit (HPI access timeout) in *SYS_STASTUS_FRG* flag register of host ISA-bus I/O interface. Refer to section 2.5 for more details.

CLEAR_MH_RQ_FRG
Write-only flag register of host ISA-bus I/O interface, which clears the *MH_RQ* flag bit (DSP-to-host interrupt request) in *SYS_STASTUS_FRG* flag register of host ISA-bus I/O interface. Refer to sections 2.4 and 2.5 for more details.

CLEAR_SB_ERROR_FRG
Write-only flag register of host ISA-bus I/O interface, which clears the *SB_ERROR* flag bit in *SYS_STASTUS_FRG* flag register of host ISA-bus I/O interface. Refer to sections 2.4 and 2.5 for more details.

COFF
Common object file format files, which are output from the TI TMS320 DSP compiler tools. These files are loaded to the DSP environment either via JTAG emulator or via host ISA-bus interface using *T6COFF.EXE* software utility. Refer to section 4.2 for more details.

CONTROL REGISTER
Register of host ISA-bus I/O interface, which controls the DSP reset signal, SB access cycles format, SB locking mechanism and some interrupt enable masks. Refer to section 2.5 for more details.

D

DEV_ID0_FRG and DEV_ID1_FRG

Read-only flag registers of host ISA-bus I/O interface, which contains device ID for *TORNADO-6x* DSP system. Refer to section 2.5 for more details.

DSP_STATUS_FRG

Read-only flag register of host ISA-bus I/O interface, which comprises of flag bits of current DSP status. Refer to section 2.5 for more details.

E

ECC

Emulation Controller Chip (also known as TBC), which is used for emulation control of TMS320C6x DSP via DSP on-chip JTAG port. Refer to section 2.8 and to TI documentation for more details.

F

FLAG DATA REGISTER

Register of host ISA-bus I/O interface, which contains read/write data for particular flag register, which is selected by the *FLAG SELECTOR REGISTER*. Refer to section 2.5 for more details.

FLAG SELECTOR REGISTER

Register of host ISA-bus I/O interface, which selects particular flag register for further read/write via *FLAG DATA REGISTER*. Refer to section 2.5 for more details.

G

H

HM_RQ

Host-to-DSP interrupt request, which is generated when host writes to the *SET_HM_RQ_FRG* flag register of host ISA-bus I/O interface. Refer to sections 2.3 and 2.5 for more details.

Host ISA-bus interface

TORNADO-6x on-board host ISA-bus interface, which comprises of host ISA-bus memory interface and host ISA-bus I/O interface. Refer to sections 2.4 and 2.5 for more details.

HPI

TMS320C6x DSP on-chip Host Port Interface, which is used for access to entire DSP environment from host PC. Refer to section 2.5 and to TI TMS320C6x documentation for more details.

HPI Access Timeout

> Timeout condition when host ISA-bus I/O interface accesses TMS320C6x DSP on-chip Host Port Interface, which sets *HPI_ERROR* flag bit in *SYS_STATUS_FRG* flag registers. Refer to section 2.5 and to TI TMS320C6x documentation for more details.

HPI_IE_FRG

> HPI-to-host interrupt enable register of host ISA-bus I/O interface. Refer to section 2.5 for more details.

HPI_HINT

> DSP-to-Host interrupt request source via DSP on-chip HPI port. Refer to sections 2.3 and 2.5 for more details.

HPI Address Latch (HPIA)

> 16-bit LSW/MSW DSP on-chip HPI Address Register, which is mapped to host ISA-bus I/O interface. Refer to section 2.5 and TI TMS320C6x DSP documentation for more details.

HPIC

> 16-bit LSW/MSW DSP on-chip HPI Control Register, , which is mapped to host ISA-bus I/O interface. Refer to section 2.5 and TI TMS320C6x DSP documentation for more details.

HPID_AI

> 16-bit LSW/MSW DSP on-chip HPI Data Register with address post-increment feature, , which is mapped to host ISA-bus I/O interface. Refer to section 2.5 and TI TMS320C6x DSP documentation for more details.

HPID

> 16-bit LSW/MSW DSP on-chip HPI Data Register, , which is mapped to host ISA-bus I/O interface. Refer to section 2.5 and TI TMS320C6x DSP documentation for more details.

HPI_ERROR

> Flag bit in *SYS_STASTUS_FRG* flag register of host ISA-bus I/O interface, which indicates that the timeout condition has been occurred for host-to-HPI access via host ISA-bus I/O interface. Refer to sections 2.4 and 2.5 for more details.

I

INT-0, INT-1, INT-2,

> External hardware DSP interrupt request from SIOX and PIOX/PIOX-16 daughter-card sites, which can generate active DSP interrupt request. Refer to sections 2.3, 2.6 and 2.7 for more details.

IOX Area

> DSP mapped I/O registers. Refer to section 2.3 for more details.

IOX Controller

On-board hardware, which is mapped to the DSP environment and is used for generation of optional signal and control of the DSP environment. Refer to section 2.3 for more details.

ISA_ECC_BADDR_FRG

Flag register from host ISA-bus I/O interface, which defines I/O base address of the ECC for host ISA-bus I/O interface. Refer to sections 2.5 and 2.8 for more details.

ISA_MI_BADDR_FRG

Flag register from host ISA-bus I/O interface, which defines SMP ISA-bus memory base address within the UMB area of host PC environment. Refer to sections 2.4 and 2.5 for more details.

J

JTAG

Joint Test Action Group interface, which is a part of the TMS320C2xx/C4x/C5x/C54x/C6x/C8x DSP on-chip hardware and is used for debugging the DSP hardware/software using external JTAG emulators (TI XDS510 and MicroLAB' *MIRAGE-510DX*).

JTAG-IN, JTAG-OUT

On-board input and output connectors, which are used for connection to external JTAG emulator and to the next device/board in JTAG path correspondingly. Refer to section 2.8 for more details.

K

L

M

MH_RQ

DSP-to-Host interrupt request source, which is generated when DSP writes to the *MH_RQ* IOX register. Refer to sections 2.3 and 2.5 for more details.

MicroPC

Industrial PC form-factor from Octagon Systems Inc.

MLock

IOX flag, which might be set by DSP software in order to lock SB. Refer to section 2.3 for more details.

MPSD

Modular Port Scan Device interface, which is a TI proprierity and is a part of the TMS320C3x DSP on-chip hardware and is used for debugging the DSP hardware/software using external MPSD emulators (TI XDS510 and MicroLAB' *MIRAGE-510DX*).

N

O

P

PIOX

Parallel I/O eXpansion interface site for compatible daughter-card modules (DCM). Refer to section 2.6 for more details.

Pod

Electronic device, which connects PC plug-in JTAG/MPSD emulator board with JTAG/MPSD interface of target external TMS320 DSP.

PXSX_RUN

IOX register, which offers control over reset signals for SIOX and PIOX/PIOX-16 daughter-card sites. Refer to section 2.3 for more details.

Q

R

Reset Controller (RC)

On-board DSP reset hardware, which generates the DSP reset signal during stand-alone operation. Refer to section 2.3 for more details.

Reset Source Selector (RSS)

On-board jumper, which configures the DSP reset source signal either from the output of host ISA-bus I/O interface or from the on-board DSP reset controller (RC). Refer to section 2.3 for more details.

S

SBSRAM

Synchronous burst static RAM, which is a part of on-board DSP environment. Refer to section 2.3 for more details.

Shared Bus (SB)

TORNADO-6x on-board data bus, which connects on-board SBSRAM, FLASH, and PIOX resources with DSP and host ISA-bus memory interface bus masters. SB offers shared access to the on-board SBSRAM, FLASH and PIOX shared resources for the on-board TMS320C6x DSP and host ISA-bus memory interface. Host ISA-bus memory interface can provide access to SBSRAM, FLASH and PIOX both in random and block data transfer modes in parallel with DSP operation and almost without consuming the DSP time. Refer to section 2.2 for more details.

SB Access Timeout

Timeout condition for host-to-SB access via host ISA-bus memory interface, which generates active *SB_ERROR* flag bit in *SYS_STASTUS_FRG* flag register of host ISA-bus I/O interface. Refer to sections 2.2 and 2.4 for more details.

SB_CCL

Data bit filed of *CONTROL REGISTER* from host ISA-bus I/O interface, which defines data access format for host-to-SB access cycles. Refer to section 2.4 and 2.5 for more details.

SB Data Cycles Format

Data bus width for SB access cycles. This is 8/16/32-bit data formats for DSP access cycles and host ISA-bus memory interface cycles. Refer to section 2.2 and 2.4 for more details.

SB_ERROR

Flag bit in *SYS_STASTUS_FRG* flag register of host ISA-bus I/O interface, which indicates that the timeout condition has been occurred for host-to-SB access via host ISA-bus memory interface. Refer to sections 2.4 and 2.5 for more details.

SB_GLOCK

Bit of *CONTROL REGISTER* from host ISA-bus I/O interface, which allows immediate SB locking by host ISA-bus memory interface. Refer to sections 2.4 and 2.5 for more details.

SB Locking

SB acquisition feature, which offers monopoly access to SB for either DSP or host ISA-bus memory interface and prevents another SB master to access SB. Refer to sections 2.2 and 2.4 for more details.

SB_LOCK

Bit of *CONTROL REGISTER* from host ISA-bus I/O interface, which allows the deferred SB locking by host ISA-bus memory interface. Refer to sections 2.4 and 2.5 for more details.

SB PAGE MAPPER

SB base address register from host ISA-bus I/O interface, which defines base address for 32KB SMP page for further host-to-SB access from host ISA-bus memory interface. Refer to sections 2.4 and 2.5 for more details.

SET_HM_RQ_FRG

Write-only flag register of host ISA-bus I/O interface, which generates *HM_RQ* host-to-DSP interrupt request. Refer to sections 2.3 and 2.5 for more details.

SIOX

Serial I/O eXpansion interface sites for compatible daughter-card modules (DCM). Refer to section 2.7 for more details.

SMP

Shared memory page mechanism, which is used for host-to-SB access from host ISA-bus memory interface. SMP size is set to 32KB for *TORNADO-6x* DSP systems. Refer to sections 2.2 and 2.4 for more details.

SMP ISA-bus Memory Base Address

Host ISA-bus memory base address for SMP of host ISA-bus memory interface, which is mapped to the UMB area of host PC environment using *ISA_MI_BADDR_FRG* flag register from *TORNADO-6x* host ISA-bus I/O interface. Refer to sections 2.4 and 2.5 for more details.

Stand-Alone Operation

Means that *TORNADO-6x* board is not installed into host PC ISA-bus slot and external power is applied via on-board dedicated power connector. Host ISA-bus interface is not utilized in stand-alone operation. Refer to section 2.3 for more details.

SYS_STATUS_FRG

Read-only flag register of host ISA-bus I/O interface, which comprises of flag bits of most important *TORNADO-6x* control signal. Refer to section 2.5 for more details.

T

T6CC.EXE

TORNADO-6x Control center software utility. Refer to section 4.1 for more details.

T6COFF.EXE

TORNADO-6x COFF loader software utility. Refer to section 4.2 for more details.

U

UECMX

Universal Emulator Control daughter-card Module for *TORNADO* DSP Systems for ISA-bus and *MIRAGE-510DX* emulator.

UMB
>   Upper memory blocks area (below 1MB and higher than 640KB) of host PC memory.

V

W

WDT
>   Watch-dog timer, which is the part of on-board DSP environment. Refer to section 2.3 for more details.

WDT_CLR
>   DSP IOX register, which provides reset of watch-dog timer. Refer to section 2.3 for more details.

WDT_EN
>   DSP IOX register, which enables the WDT feature for stand-alone operation. Refer to section 2.3 for more details.

X

Y

Z