TORNADO-54x

High Performance 16-bit Fixed-Point TMS320C54x DSP Systems
and Emulators for host ISA-bus PC

User's Guide

covers:
TORNADO-542L
TORNADO-548/549

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About this Document

This user's guide contains description for *TORNADO-54x* (*TORNADO-542L* and *TORNADO-548/549*) 16-bit fixed-point digital signal processing (DSP) systems and emulators for host ISA-bus PC, which utilize Texas Instruments (TI) TMS320C54x DSP.

This document does not include detail description neither for TI TMS320C54x DSP nor for the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C54x DSP. CPU and Peripherals.*** Texas Instruments Inc, SPRU131D, USA, 1997.
2. ***TMS320C54x DSP. Mnemonic Instruction Set.*** Texas Instruments Inc, SPRU172, USA, 1996.
3. ***TMS320C54x DSP. Algebraic Instruction Set.*** Texas Instruments Inc, SPRU179A, USA, 1997.
4. ***TMS320C54x Optimizing C Compiler User`s Guide.*** Texas Instruments Inc, SPRU103B, USA, 1997.
5. ***TMS320C54x Assembly Language Tools User`s Guide.*** Texas Instruments Inc, SPRU102B, USA, 1997.

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Chapter 1.   Introduction

This chapter contains general description for *TORNADO-54x* DSP systems product line, which comprises of *TORNADO-542L* and *TORNADO-548/549* DSP systems.

CAUTION

Here and further in this document the '*TORNADO-54x*' notation denotes the supplied information is applicable to all *TORNADO-54x* DSP systems (*TORNADO-542L* and *TORNADO-548/549* products).

Should information be a product specific, then the name of the corresponding product (*TORNADO-542L* or *TORNADO-548/549*) will be highlighted.

1.1   General Information

TORNADO-54x are high performance fixed point DSP system boards and emulators for host ISA-bus PC computers. *TORNADO-54x* are designed to plug into 16-bit ISA-bus slot of host PC and feature flexible modular system architecture in order to meet requirements for multiple applications while keeping a cost of project to a minimum.

TORNADO-54x DSP systems comprise of *TORNADO-542L* and *TORNADO-548/549* and feature 100% compatible host ISA-bus interface and TMS320C54x DSP environment. *TORNADO-548/549* features extended memory capacity and enchanced emulation facility.
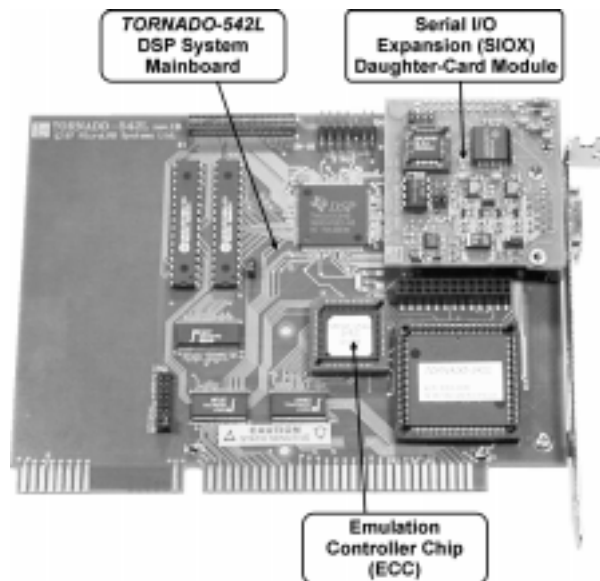
Fig.1-1.a.   TORNADO-542L DSP system board with SIOX and PIOX-16 daughter card modules and *ECC* emulation controller.
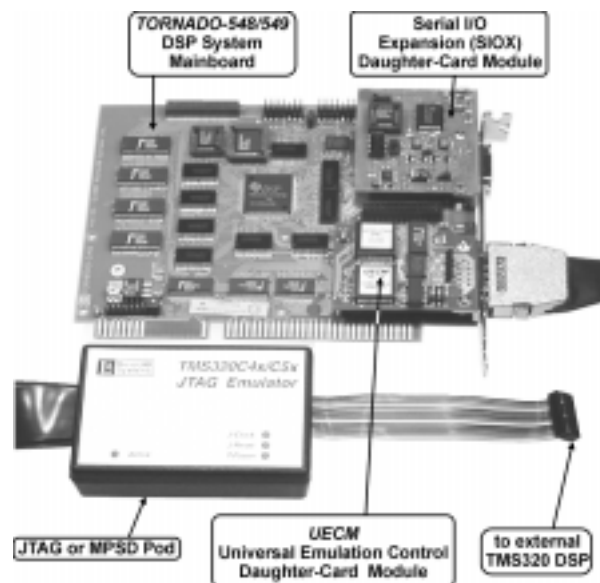
Fig.1-1b.   TORNADO-548/549 DSP system board with SIOX and PIOX-16 daughter card modules, *UECM* emulation control daughter card module and external JTAG pod.

The following are some applications for *TORNADO-54x* DSP systems:
- *real-time DSP and signal acquisition*
- *speech signal processing and acoustics*
- *fax and modem communication*

- *audio signal processing*
- *multimedia*
- *instrumentation and industrial*
- *universal emulator for TI C2xx/C3x/C4x/C5x/C54x/C6x DSP (TORNADO-548/549 only with UECM and external MPSD/JTAG pod)*
- *evaluation and education*
- many more ...

TORNADO-54x utilize TMS320C54x 16-bit fixed point DSP (40 MIPS TMS320C542 in *TORNADO-542L*, 66/80 MIPS TMS320LC548 in *TORNADO-548* and 100 MIPS TMS320VC549 in *TORNADO-549*. The on-board static RAM (SRAM) for program and data includes 128Kx16 (*TORNADO-542L*) and 256Kx16 (*TORNADO-548/549*). On-board SRAM is splitted into program and data memory banks each having 64Kx16 (*TORNADO-542L*) and 128Kx16 (*TORNADO-548/549*) capacity.

TORNADO-54x have on-board shared bus (SB) architecture that shares access to SRAM and PIOX-16 shared resources between the on-board TMS320C54x DSP and host ISA-bus memory interface. Host ISA-bus memory interface can provide access to SRAM/PIOX-16 both in random and block data transfer modes in parallel with DSP operation and almost without consuming the DSP time.

TORNADO-54x feature optional facility for installation of serial I/O expansion (SIOX) daughter card modules from a variety of AD/DA and digital I/O SIOX modules for real-time instrumentation, industrial and speech, telecommunication and audio signal processing applications.

TORNADO-54x feature optional facility for installation of parallel I/O expansion (PIOX-16) daughter card modules from a variety of AD/DA and digital I/O PIOX-16 daughter cards modules for high-speed real-time instrumentation, industrial and speech, telecommunication and audio signal processing applications.

TORNADO-54x offer access to HPI (host port interface) of on-board TMS320C54x DSP from host ISA-bus I/O interface. Along with host ISA-bus memory interface this provides a second data path for communication between host and DSP.

TORNADO-54x use scan-path emulation control for the on-board TMS320C54x DSP in order to debug resident TMS320C54x DSP software. Scan-path emulation control of the on-board TMS320C54x DSP is available either via external TI XDS510 or MicroLAB' *MIRAGE-510D* scan-path emulators, or by means of optional *emulation controller chip (ECC)* for *TORNADO-542L* that plugs into dedicated on-board socket, or by means of optional *emulation control daughter card module (UECM)* for *TORNADO-548/549* that plugs into dedicated on-board daughter card site. Both *ECC* and *UECM* are low cost replacements for TI XDS510 and MicroLAB's *MIRAGE-510D* scan-path emulators and run under identical industry standard TI TMS320C54x HLL Debugger and GoDSP C54x Code Composer IDE. Furthermore, *UECM* allows optional connection to external MPSD and JTAG pods (which are the pods used with MicroLAB's *MIRAGE-510D* scan-path emulator) in order to emulate any external TI C2xx/C3x/C4x/C5x/C54x/C6x DSP. This converts *TORNADO-548/549* into universal emulator for TI DSP.

TORNADO-54x software development tools include TI TMS320C54x DSP C compiler and Assembly language tools.

TORNADO-54x are supported by a variety of industry standard 3rd party DSP software tools, that include real-time operating systems (RTOS), digital filter design tools, DSP/vector/math function libraries, vocoder/fax/modem function libraries, and many more...

TORNADO-54x provide unique burn-in device serial codes, that can be read by host software and used for hardware copyright protection of software tools for software vendors and DSP system integrators.

1.2   Host PC Specifications

TORNADO-54x require that host ISA-bus IBM PC configuration should be at least 80386SX CPU and provides at least one 16-bit ISA-bus slot.

In order to learn configuration requirements for host PC running TMS320C54x DSP software development and debugging tools, refer to the corresponding documentation from TI and Go DSP Corp as well as to MicroLAB' "*UECM/ECC User's Guide*".

1.3   Technical Specification

The following are the technical specifications for *TORNADO-54x* system specified for the temperature +25°Ñ of the environment.

Parameter description	*parameter value*
power supply voltage	+5V for *TORNADO-54x* board,
	optional ±5V/±12V for SIOX/PIOX daughter card modules
power consumption (no *ECC* or *UECM* installed)	+5V@1.8A
DSP performance	40 MIPS (*TORNADO-542L*)
	66/80 MIPS (*TORNADO-548*)
	100 MIPS (*TORNADO-549*)
dimensions	160x110 mm
operating temperature	+10..+45°C
I/O expansion interfaces	two sites (SIOX-A and SIOX-B) for TORNADO/SIOX daughter-card module.
	One site for TORNADO/PIOX-16 daughter-card module.
host ISA-bus interface:	
number of 8-bit I/O ports in host ISA-bus I/O interface	16
size of ISA-bus memory page in the UMB memory address area for SB access via host ISA-bus memory interface	32Kx8

host timeout control time for SB grant, SB ready and HPI ready	>4 us
host IRQ lines	IRQ 3, 4, 5, 6, 7, 10, 11, 12, 15

on-board SRAM:

SRAM capacity	128Kx16 0ws (*TORNADO-542L*) 256Kx16 1ws (*TORNADO-548/549*)
Program memory area	64Kx16 (*TORNADO-542L*) 2x64Kx16 (*TORNADO-548/549*)
Data memory area	64Kx16 (*TORNADO-542L*) 4x32Kx16 (*TORNADO-548/549*)

Chapter 2. System Architecture and Construction

This chapter contains description for *TORNADO-54x* system architecture, construction, host ISA-bus interface, and SIOX/PIOX-16 I/O expansion sites.

2.1   *TORNADO-54x* System Architecture

TORNADO-54x DSP system mainboards install into 16-bit ISA-bus slot of host PC (fig.1-1). *TORNADO-542L* and *TORNADO-548/549* system architectures are presented at fig.2-1.
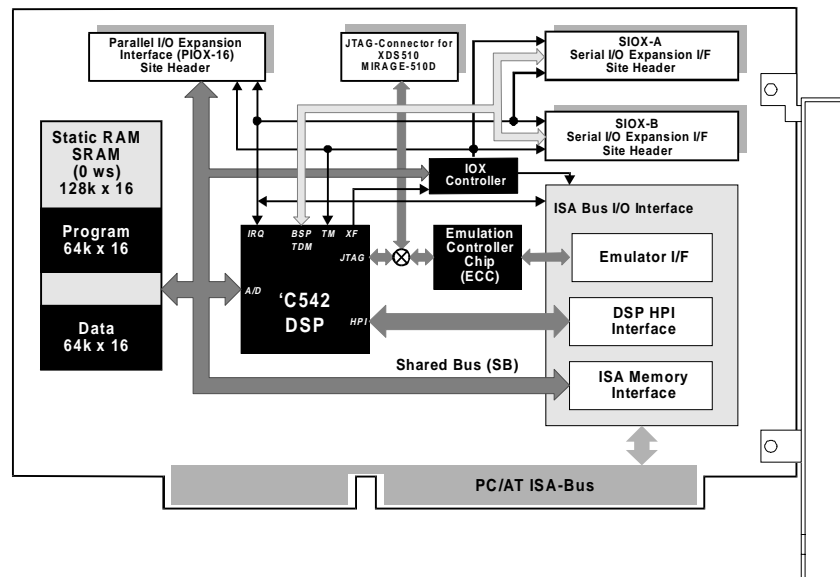
Fig.2-1a.   Architecture of *TORNADO-542L* mainboard.
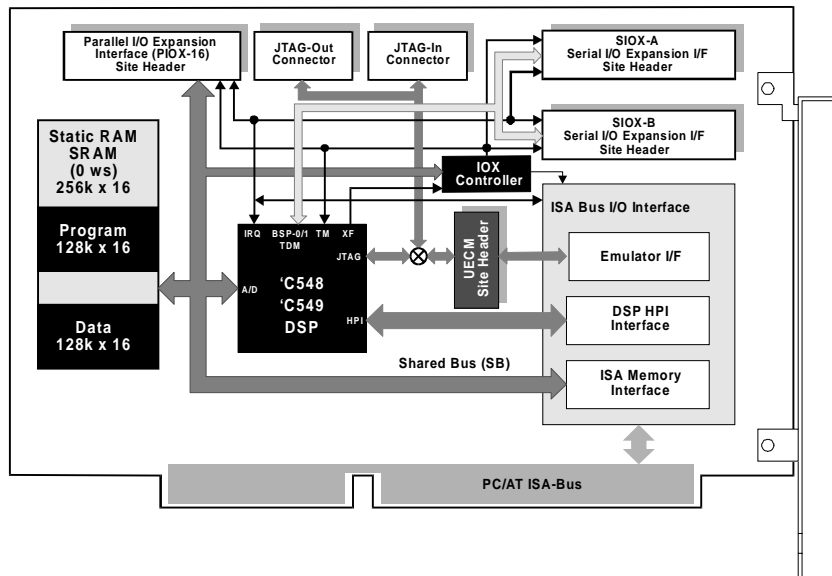
Fig.2-1b.   Architecture of *TORNADO-548/549* mainboard.

Main components of *TORNADO-54x* mainboard are:
- *TMS320C542 (**TORNADO-542L**), TMS320LC548 (**TORNADO-548**) or TMS320VC549 (**TORNADO-549**) 16-bit fixed point DSP*
- *on-board SRAM comprising of PROGRAM and DATA memory areas*
- *host ISA-bus memory and I/O interfaces*
- *I/O expansion flag controller (IOX)*
- *serial I/O expansion interface (SIOX) site*
- *16-bit parallel I/O expansion interface (PIOX-16) site*
- *emulation controller chip (ECC) for **TORNADO-542L** or site for universal emulation control daughter-card module (UECM) for **TORNADO-548/549.***

The on-board TMS320C54x DSP, SRAM, PIOX-16 and host ISA-bus memory interface are linked together by means of the on-board *Shared Bus (SB)*. SB shares SRAM/PIOX-16 resources between two 'bus masters', that can execute SB access cycles: the on-board TMS320C54x DSP and host ISA-bus memory interface. On-board SB arbitration assumes that TMS320C54x DSP bus master has highest SB access priority whereas ISA-bus memory interface is designed to access SB in-parallel with DSP internal operation, without any DSP and host software overhead and almost without consuming the DSP time.

Constructions for *TORNADO-542L* and *TORNADO-548/549* mainboards are presented at fig.2-2.
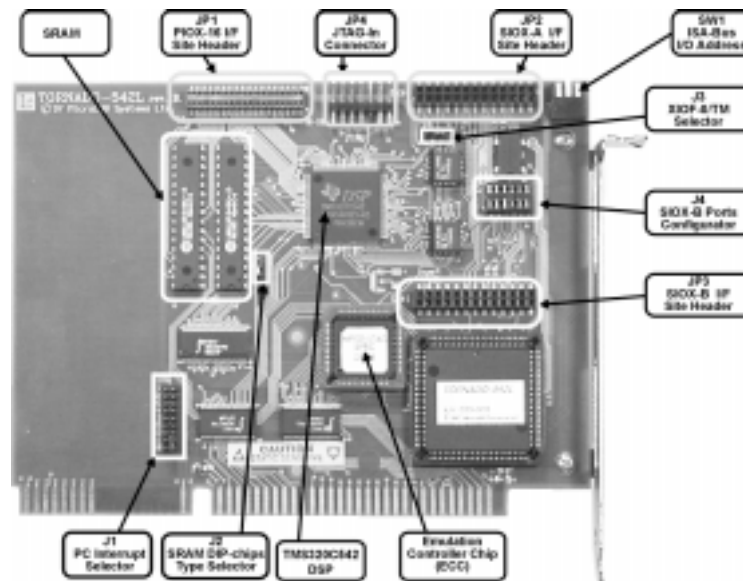
Fig.2-2a. Construction of *TORNADO-542L* mainboard.
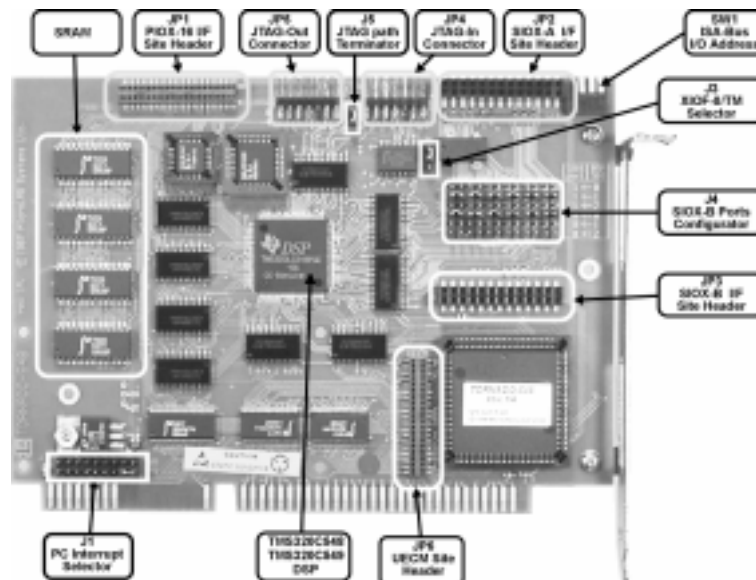
Fig.2-2b. Construction of *TORNADO-548/549* mainboard.

TMS320C54x DSP

The on-board TMS320C542 DSP (*TORNADO-542L*), TMS320LC548 DSP (*TORNADO-548*) or TMS320VC549 DSP (*TORNADO-549*) is 16-bit fixed point DSP chip with on-chip Harvard architecture delivering 40 MIPS, 66/80 MIPS or 100MIPS of peak performance correspondingly.

Static RAM (SRAM) for Program and Data

TORNADO-54x provides on-board static RAM (SRAM) for TMS320C54x DSP program and data memory areas.

TORNADO-542L features 128Kx16 0ws of on-board SRAM that comprises of PROGRAM and DATA memory areas each having 64Kx16 SRAM capacity.

TORNADO-548/549 features 256Kx16 1ws of on-board SRAM that comprises of 128Kx16 PROGRAM and 128Kx16 DATA memory areas. The 128Kx16 PROGRAM memory area is organized as two 64Kx16 memory pages (PMEM-pages #0 and #1), so build-in extended program memory addressing capabilities of TMS320LC548/VC549 DSP should be used to address this program memory. The 128Kx16 DATA memory is organized as four pages of 32Kx16 with each page mapped into the upper (off-chip) half of TMS320LC548/VC549 data memory address space. *TORNADO-548/549* provides on-board extended data memory addressing hardware (extended data memory page register (*XDMPR*)) in order to switch between these data memory pages from the DSP software.

Shared Bus (SB)

TORNADO-54x on-board SB delivers access to the on-board SRAM and PIOX-16 shared resources for both on-board TMS320C54x DSP and host ISA-bus memory interface. The SB address space comprises of SRAM/PROGRAM memory area, SRAM/DATA memory area and I/O area, which is mapped into PIOX-16 expansion interface. SB supports 16-bit data cycles. It is important to note, that all host accesses to the on-board SRAM and PIOX-16 resources are performed concurrently with the DSP running and without any DSP and host software overhead.

Host ISA-bus Interface

TORNADO-54x host ISA-bus interface was designed for DSP/system control and high-speed data transfer between host ISA-bus and on-board SRAM/PIOX-16 and HPI port of on-board TMS320C54x DSP. *TORNADO-54x* host ISA-bus interface includes:
- *ISA-bus memory interface* that performs access to SRAM and PIOX-16
- *ISA-bus I/O interface* that provides *TORNADO-54x* system control and access to TMS320C54x on-chip HPI (host port interface).

Host ISA-bus memory interface can access SB SRAM/PIOX-16 resources via 32Kx8 *shared memory page* (*SMP*) that is mapped into ISA-bus UMB memory address space. Once ISA-bus executes memory cycle within address range of *SMP*, then the on-board *TORNADO-54x* ISA-bus memory interface generates request to SB. Particular allocation of *SMP* onto SB address space is defined by *SB PAGE MAPPER* register from ISA-bus I/O interface. Host can access the SB data using 16-bit data cycles. Host ISA-bus memory interface has lowest SB access priority.

Base ISA-bus memory address for host ISA-bus memory is setup by host software and can be switched off in case *TORNADO-54x* board is not used.

ISA-bus base I/O address for ISA-bus I/O interface is configured by the on-board SW1 DIP-switch into one of eight predefined I/O address areas.

TMS320C54x HPI (host port interface)

TORNADO-54x host ISA-bus I/O interface also delivers access to TMS320C54x on-chip HPI, which comes as a second data path for communication between host PC and on-board DSP along with on-board SRAM. HPI offers access from host PC to TMS320C54x on-chip HPI shared memory area and allows generation of mutual interrupts. However, unlike access to on-board SRAM, HPI does not support random access to HPI memory from host PC using standard ISA-bus memory cycle, and assumes that HPI memory address should be pre-latched into HPI address register prior HPI data access will be performed. However, the HPI address auto post-incrementing feature is available and simplifies data array upload/download.

I/O Expansion Flag Controller (IOX)

TORNADO-54x has on-board I/O expansion flag controller (IOX) that provides some extra I/O ports used by the on-board TMS320C54x DSP environment. These I/O ports include DSP-to-Host interrupt request output (*MH_RQ*), SB lock by DSP output (*MLock*), two I/O expansion flags (*XIOF-0* and *XIOF-0*) and extended data memory page register (*XDMPR,* for *TORNADO-548/549* only). IOX controller is accessible by on-board TMS320C54x DSP only using I/O ports access instructions with the DSP XF output flag is set to logical '1'.

Serial I/O Expansion Interface (SIOX) sites

TORNADO-54x on-board SIOX interface sites are used for installation of AD/DA/DIO daughter card modules and comprises of signals for TMS320C54x DSP on-chip serial ports (BSP and TDM), timer and interrupt control, and XIOF-0/1 I/O flags.

SIOX compatible daughter card modules include a variety of multichannel instrumentation AD/DA/DIO modules, telecommunication codecs, speech and stereo-audio codecs, DAT interface, and many more.

Parallel I/O Expansion Interface (PIOX-16) site

TORNADO-54x PIOX-16 interface site is used for installation of AD/DA/DIO daughter card modules and comprises of SB signals, *XIOF-0/1* I/O flags and TMS320C54x DSP on-chip timer and interrupt control. *TORNADO-54x* PIOX-16 interface is allocated into TMS320C54x I/O address area and can be accessed both by on-board DSP and host ISA-bus memory interface.

PIOX-16 compatible daughter card modules include a variety of multichannel instrumentation AD/DA/DIO modules and many more.

Debugging of resident TMS320C54x DSP Software

Resident TMS320C54x DSP software for *TORNADO-54x* can be debugged using TI XDS510 and MicroLAB' *MIRAGE-510D* scan-path emulators. However, in order to minimize cost of debugging tools, the emulation controller chip (*ECC*) can be plugged into the dedicated on-board socket of *TORNADO-542L* or universal emulation control daughter-card module (*UECM*) can be plugged into the dedicated site on *TORNADO-548/549*. Both *ECC* and *UECM* are low cost replacement for XDS510 and *MIRAGE-510D* emulators and run under identical industry standard TI TMS320C54x HLL Debugger and GoDSP TMS320C54x Code Composer IDE.

Debugging of external TI TMS320 DSP Software with TORNADO-548/549 and UECM

TORNADO-548/549 easily converts into universal scan-path emulator for any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP. This requires the *UECM* daughter-card modules installed onto *TORNADO-548/549* mainboard and optional external MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x) pod attached to *UECM*. The MPSD and JTAG pods are the pods used with MicroLAB' *MIRAGE-510D* emulator. The *UECM* runs under the industry standard TI HLL Debuggers and GoDSP Code Composer IDE.

2.2　　Shared Bus

The *TORNADO-54x* on-board shared bus (SB) architecture provides SRAM/PROGRAM, SRAM/DATA and I/O areas and supports 16-bit data cycles. SB comprises SRAM and PIOX-16 shared resources and is shared between the on-board TMS320C54x DSP and host ISA-bus memory interface.

SB Address Space

The SB address space is actually the address space for *TORNADO-54x* on-board TMS320C54x DSP. Table 2-1 specifies valid SB address areas.

Table 2-1. SB address areas and data ready wait times.

SB address areas	address range (in 16-bit word units)	wait time for **SB_READY** signal (SB data ready) after SB is granted for	
		on-board TMS320C54x DSP	*host ISA-bus memory interface*
SRAM/PROGRAM memory area	0000H...FFFFH @PROG (*TORNADO-542L*) 00000H...1FFFFH @PROG (*TORNADO-548/549*)	0ws (should be programmed via PROGRAM field of SWWSR for *TORNADO-542L*) 1ws (should be programmed via PROGRAM field of SWWSR for *TORNADO-548/549*)	0ws (*TORNADO-542L*) 1ws (*TORNADO-548/549*)
SRAM/DATA memory area	2800H...FFFFH @DATA (*TORNADO-542L*) 8000H...FFFFH @DATA (4 overlapped memory pages for *TORNADO-548/549* on-board DSP; memory page is selected by *XDMPR*) 08000H...0FFFFH 18000H...1FFFFH 28000H...2FFFFH 38000H...3FFFFH @DATA (for host ISA-bus memory I/F of *TORNADO-548/549*)	0ws (should be programmed via DATA field of SWWSR for *TORNADO-542L*) 1ws (should be programmed via DATA field of SWWSR for *TORNADO-548/549*)	0ws (*TORNADO-542L*) 1ws (*TORNADO-548/549*)
PIOX I/O area	0000H...FFFFH @I/O	(2ws + *PIOX_RDY*) (should be programmed via I/O field of SWWSR)	(1ws + *PIOX_READY*), but not longer than 4µS timeout

The SB address space in host ISA-bus memory interface appears as a series of dual-access 32KB *shared memory pages* (SMP) that are mapped onto the predefined ISA-bus UMB (upper memory blocks) memory window by means of SB PAGE MAPPER register in host ISA-bus I/O interface. The SB can be accessed by host ISA-bus memory interface by means of random accesses to software variables or data arrays that are allocated within SMP, or by means of block data transfers between PC main memory and SMP using either host i80x286 CPU MOVSB/MOVSW/etc instructions or host DMA controller.

SRAM area for TORNADO-542L

TORNADO-542L allows user to install up to 128Kx16 0ws of on-board SRAM using two 8K/32K/64K/128Kx8 SRAM DIP chips in DIP-28 and DIP-32 packages with 15ns access time. The on-board J2 jumper (see fig.2-2 and fig A-1) should be set in accordance with particular type of SRAM chips installed.

CAUTION

On-board J2 jumper for *TORNADO-542L* should be set to 1-2 position in case the 32K/64K/128Kx8 SRAM DIP-32 chips are installed.

On-board J2 jumper for *TORNADO-542L* should be set to 2-3 position in case the 8Kx8 SRAM DIP-28 chips are installed.

TORNADO-542L on-board hardware automatically splits the on-board installed SRAM capacity into two PROGRAM and DATA memory areas each having equal SRAM capacity. For example, for 128Kx16 SRAM installed, the PROGRAM and DATA memory areas will equal to 64Kx16 SRAM capacity each, whereas for 32Kx16 SRAM installed this results to 16Kx16 PROGRAM and DATA memory areas.

CAUTION

Table 2-1 shows the SRAM/PROGRAM and SRAM/DATA memory area address ranges for *TORNADO-542L* with 128Kx16 SRAM installed. This covers full address range for PROGRAM and DATA memory areas of TMS320C542 DSP.

In case the installed SRAM has smaller capacity (i.e. 8K/32K/64Kx16), then the SRAM/PROGRAM and SRAM/DATA memory areas will appear as overlapped memory pages in the PROGRAM and DATA memory areas of TMS320C54x DSP. In this case the recommended allocation for SRAM/PROGRAM and SRAM/DATA memory pages will be allocation at the most high memory page addresses, i.e. the highest memory page address must fit to 0FFFFH PROGRAM and 0FFFFH DATA memory address of TMS320C54x DSP.

SRAM area for TORNADO-548/549

TORNADO-548/549 features 256Kx16 1ws of on-board SRAM that comprises of 128Kx16 PROGRAM and 128Kx16 DATA memory areas. The 128Kx16 PROGRAM memory area is organized as two 64Kx16 memory pages (PMEM-pages #0 and #1), so build-in extended program memory addressing capabilities of TMS320LC548/VC549 DSP should be used to address this program memory. The 128Kx16 DATA memory is organized as four pages of 32Kx16 with each page mapped into the upper (off-chip) half of TMS320LC548/VC549 data memory address space. *TORNADO-548/549* provides on-board extended data memory addressing hardware (extended data memory page register (*XDMPR*)) in order to switch between these data memory pages from the DSP software.

SB Data Ready Signal

SB has internal *SB_READY* signal that is generated by passive addressed device (SRAM or PIOX-16) in order to acknowledge that SB data are valid after SB is granted to requesting SB master. When SB is accessed by the on-board TMS320C54x DSP master, the *SB_READY* signal is logically connected to the *READY* pin of TMS320C54x DSP, whereas for accesses from host ISA-bus memory interface the *SB_READY* signal is automatically processed by the SB access controller of ISA-bus memory interface.

SB Data Cycle Formats

SB supports 16-bit data cycles only. The on-board TMS320C54x DSP master provides only 16-bit SB data cycles whereas host ISA-bus memory interface can perform 8-bit or 16-bit ISA-bus memory cycles. In case host ISA-bus memory interface executes 8-bit ISA-bus cycle while accessing the SB areas, then LSB or MSB are temporary stored in on-board register transceivers depending upon the memory read or memory write cycle is being performed correspondingly (see section 2.4).

SB Arbitration

When SB is requested by any of the SB masters (TMS320C54x DSP or host ISA-bus memory interface), then some time is required to resolve the arbitration. This normally takes about 1-2 TMS320C54x DSP clock cycles.

In case TMS320C54x DSP is requesting SB while SB is occupied by host ISA-bus memory interface, then the DSP should wait until host ISA-bus memory interface will release SB. After SB is granted to DSP, it is holded by DSP in order to provide 0ws (*TORNADO-542L*) or 1ws (*TORNADO-548/549*) for all further SB accesses.

In case host ISA-bus memory interface is requesting SB while SB is occupied by TMS320C54x DSP, then host ISA-bus memory interface has to wait until DSP will complete current SB access cycle and release SB.

When SB is requested by both DSP and host ISA-bus memory interface, then DSP has the highest SB access priority.

SB Locking

The SB arbiter supports program *SB locking* in order to lock the SB access for processing of program semaphores or shared PIOX-16 resources.

The SB locking by the on-board TMS320C54x DSP bus master is performed when DSP set *MLock* flag in I/O expansion flag area (IOX).

CAUTION

Time interval between setting and resetting *MLock* flag by the on-board TMS320C54x DSP should not exceed 4 μsec.

The SB locking by host ISA-bus memory interface master is performed by means of setting the *SB_GLOCK* or the *SB_LOCK* bits of *CONTROL REGISTER* by host ISA-bus I/O interface.

CAUTION

Continuous SB locking by host ISA-bus memory interface by means of setting the
SB_GLOCK and *SB_LOCK* bits can result in continuous halting of the on-board
TMS320C54x DSP bus master and may lead to time distortions of real-time data processing.

2.3   TMS320C54x DSP Environment

The *TORNADO-54x* DSP systems utilize state of art TMS320C54x high-performance 16-bit fixed point DSP
from TI:

- 40 MIPS TMS320C542 DSP in *TORNADO-542L* DSP system
- 66/80 MIPS TMS320LC548 and 100MIPS TMS320VC549 DSP in *TORNADO-548/549* DSP
  systems.

TMS320C54x DSP Address Space

TMS320C54x DSP supports three external address spaces (areas): program area, data area and I/O area. Each
area can be accessed by a specific set of instructions. Address areas for on-board TMS320C54x DSP are
presented in table 2-2.

Table 2-2. Address areas for TMS320C54x DSP in *TORNADO-54x* DSP systems.

Address area of TMS320C54x DSP	value by TMS320C54x DSP RESET	access mode	address range (in 16-bit words)	wait states
SRAM/PROGRAM area, which is the shared resource of the on-board SB and can be accessed by both TMS320C54x DSP and host ISA-bus memory interface	-	r/w	0000H...FFFFH @PROG (*TORNADO-542L*) 00000H...1FFFFH @PROG (*TORNADO-548/549*)	0ws/SWS-M (*TORNADO-542L*) 1ws/SWS-M (*TORNADO-548/549*)
SRAM/DATA area, which is the shared resource of the on-board SB and can be accessed by both TMS320C54x DSP and host ISA-bus memory interface	-	r/w	2800H...FFFFH @DATA (*TORNADO-542L*) page #0: 8000H..FFFFH @*XDMPR*=0 @DATA page #1: 8000H..FFFFH @*XDMPR*=1 @DATA page #2: 8000H..FFFFH @*XDMPR*=2 @DATA page #3: 8000H..FFFFH @*XDMPR*=3 @DATA (*TORNADO-548/549*)	0ws/SWS-M (*TORNADO-542L*) 1ws/SWS-M (*TORNADO-548/549*)
IOX area: *XDMPR* register (extended data memory page register), *TORNADO-548/549* only	0 (extended data memory page#0 is selected)	r/w	2000H @I/O while XF=1 (only bits D0/D1 are valid)	2ws/SWS-IO
IOX area: *XIOF* register (I/O expansion flags data)	0	r/w	4000H @I/O while XF=1 (only bits D0/D1 are valid)	2ws/SWS-IO
IOX area: *XIOF-DIR* register (I/O expansion flags direction)	0 (*XIOF-0/1* are inputs)	r/w	4001H @I/O while XF=1 (only bits D0/D1 are valid)	2ws/SWS-IO
IOX area: *MH_RQ* register (DSP_master-to-Host request flag)	-	w	8000H @I/O while XF=1 (data written is ignored)	2ws/SWS-IO
IOX area: *Mlock* register (SB lock by DSP_master flag)	0 (no SB Lock)	r/w	8001H @I/O while XF=1 (only bit D0 is valid)	2ws/SWS-IO
PIOX-16 area	-	r/w	0000H...FFFFH @I/O while XF=0	2ws/SWS-IO + *PIOX_READY*

Notes: 1. '*XF*' denotes XF output of TMS320C54x DSP.

2.   *IOX* area denotes I/O Expansion Flag controller, that is accessible with I/O cycles while XF=1.
3.   *'SWS-M'* denotes recommended number of software wait states programmed in the PROGRAM and DATA fields of TMS320C54x on-chip SWWSR register. The XPA bit of SWWSR register for TMS320LC548/VC549 DSP of *TORNADO-548/549* DSP system should be set to logical '0'.
4.   *'SWS-IO'* denotes recommended number of software wait states programmed in the I/O field of TMS320C54x on-chip SWWSR register.
5.   Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

PROGRAM and DATA SRAM Areas

TORNADO-54x on-board PROGRAM and DATA memory areas reside in the on-board SRAM, which has the following capacity:
- 128Kx16 0ws SRAM in *TORNADO-542L*
- 256Kx16 1ws SRAM in *TORNADO-548/549*.

Each PROGRAM and DATA memory area occupies one half of total SRAM capacity as the following:
- 64Kx16 program memory area and 64Kx16 data memory area (only 2800H..FFFFH data address space for TMS320C542 DSP is accessible) for *TORNADO-542L*
- 2x64Kx16 program memory area (pages #0 and #1 of extended program memory address space of TMS320LC548/VC549 DSP) and 4x32Kx16 data memory area (four overlapped pages of data memory in 8000H..FFFFH data address area of TMS320LC548/VC549 DSP, which are selected by the on-board *XDMPR* register) for *TORNADO-548/549*.

IOX Area

TMS320C54x DSP environment of *TORNADO-54x* features special I/O expansion (IOX) flags area that is allocated into I/O area. IOX area is used for DSP environment control and includes several I/O registers. IOX area is available during TMS320C54x DSP I/O accesses with the DSP' XF output flag set to logical '1'. IOX area can be accessed only by TMS320C54x DSP and is not visible from host ISA-bus memory interface.

IOX area includes:
- *MH_RQ* (DSP master-to-Host request) generation register
- *MLock* (SB lock by DSP) flag register
- *XIOF-0/1* (I/O expansion flags #0/#1) control registers.
- *XDMPR* (extended data memory page register) in *TORNADO-548/549* DSP system only.

All IOX area registers are accessible with two software wait states programmed via SWWSR register of TMS320C54x DSP. Details about IOX area are described below in this section.

PIOX-16 Area

TORNADO-54x provides 16-bit parallel I/O expansion interface (PIOX-16) site for compatible AD/DA/DIO daughter card modules. PIOX-16 occupies 64Kx16 of DSP I/O address space and is available during TMS320C54x DSP I/O accesses with the DSP' XF output flag set to '0'. PIOX-16 area can be accessed both by the on-board TMS320C54x DSP and host ISA-bus memory interface.

Setting SWWSR and BSCR Control Registers of TMS320C54x DSP

In order to benefit of full performance of TMS320C54x DSP and to provide correct operation of on-board hardware, be sure to setup TMS320C54x on-chip *SWWSR/BSCR* peripheral access control registers in your TMS320C54x DSP software as the following:

- the *SWWSR* register (software programmable wait state generator) of TMS320C54x DSP should be programmed to 0200H hex value for *TORNADO-542L* DSP system and to 2209H hex value for *TORNADO-548/549* DSP system. This corresponds to the following settings:
  - on-board SRAM/PROGRAM memory area is accessed with 0ws in *TORNADO-542L* and with 1ws in *TORNADO-548/549*
  - on-board SRAM/DATA memory area is accessed with 0ws in *TORNADO-542L* and with 1ws in *TORNADO-548/549*
  - IOX I/O area is accessed with 2ws (accessible from TMS320C54x DSP environment only)
  - PIOX-16 I/O area is accessed with 2ws and further awaiting for *PIOX_READY* signal
- the *BSCR* register (programmable memory bank switching) should be programmed to 0000H hex value

TMS320C54x HPI (host port interface)

TORNADO-54x offers access from host ISA-bus I/O interface to TMS320C54x on-chip HPI (host port interface). All HPI features are supported, including mutual interrupt generation between host ISA-bus I/O interface and TMS320C54x DSP. For details about TMS320C54x HPI refer to original TI documentation and see the corresponding section later in this chapter.

Extended Data Memory Addressing with XDMPR register in TORNADO-548/549

TORNADO-548/549 allows the on-board TMS320LC548/VC549 DSP to address data memory beyond conventional 0000H..FFFFH@DATA data memory address range for TMS320LC548/VC549 DSP.

The extended data memory addressing for TMS320LC548/VC549 DSP in *TORNADO-548/549* DSP system is performed by means of two-bit external extended data memory page register (*XDMPR*), which selects between four available overlapped external data memory pages while TMS320LC548/VC549 DSP addresses data memory within the 8000H..FFFFH@DATA data memory address range. The *XDMPR* can be accessed by TMS320LC548/VC549 DSP only via IOX area (I/O access cycles while DSP' XF flag is set to logical '1').

The extended data memory addressing for TMS320LC548/VC549 DSP in *TORNADO-548/549* DSP system operates as the following:
- while data memory within 0000H..7FFFH@DATA data memory address range is addressed by TMS320LC548/VC549 DSP, then the DSP on-chip RAM is selected
- once data memory within 8000H..FFFFH@DATA data memory address range is addressed by TM320C548 DSP, then external SRAM/DATA area is selected. Page #0 of external SRAM/DATA area is selected while *XDMPR*=0. Correspondingly, page #0 of external SRAM/DATA area is selected while *XDMPR*=1, page #2 - while *XDMPR*=2, and page #3 - while *XDMPR*=3. The reset value of *XDMPR* is '0' in order to provide compatibility with *TORNADO-542L* DSP system.

The *XDMPR* can be accessed by TMS320LC548/VC549 DSP during I/O access cycles at 2000H@I/O I/O address while DSP' XF flag is set to logical '1'. The *XDMPR* is available during both read/write I/O cycles and has the following data format:

XDMPR Register (r/w)

x	x	x	x	x	x	x	x	x	x	x	x	x	x	XDMP-1	XDMP-0
bit-15	bit-14	bit-13	bit-12	bit-12	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XIOF-0 and XIOF-1 I/O Flags

XIOF-0/1 I/O flags are used for expansion of I/O facilities of on-board TMS320C54x DSP and are wired to on-board PIOX-16 interface site and SIOX interface sites for direct control of compatible daughter card modules. Each of *XIOF-0/1* I/O flags can be independently programmed by TMS320C54x DSP as input or output flag. *XIOF-0/1* I/O flags can be accessed from TMS320C54x DSP environment only via IOX area (I/O access cycles while DSP' XF flag is set to logical '1').

XIOF-0/1 I/O flags control facility occupies two registers in IOX area:
- *XIOF-DIR* register (*XIOF* flags direction register)
- *XIOF-DATA* register (*XIOF* flags data register).

XIOF-DIR register configures direction for *XIOF-0/1* I/O flags and can be accessed by TMS320C54x DSP when it performs I/O access cycle to 4001H I/O port in IOX area (while DSP' on-chip XF flag is set to logical '1') and has the following data format:

XIOF-DIR Register (r/w)

x	x	x	x	x	x	x	x	x	x	x	x	x	x	XIOF-1/ DIR	XIOF-0/ DIR
bit-15	bit-14	bit-13	bit-12	bit-12	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Logical '0' for *XIOF-0/DIR* and *XIOF-1/DIR* bits corresponds to configuring corresponding *XIOF-0/1* I/O flag as input, whereas logical '1' corresponds to configuring corresponding *XIOF-0/1* I/O flag as output. *XIOF-0/DIR* and *XIOF-1/DIR* bits of *XIOF-DIR* register defaults to '0' during DSP reset.

XIOF-DATA register specifies current state of *XIOF-0/1* I/O flags and can be accessed by TMS320C54x DSP when it performs I/O access cycle to 4000H I/O port in IOX area (while DSP' on-chip XF flag is set to logical '1') and has the following data format:

XIOF-DATA Register (r/w)

x	x	x	x	x	x	x	x	x	x	x	x	x	x	XIOF-1	XIOF-0
bit-15	bit-14	bit-13	bit-12	bit-12	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Note, that when any of *XIOF-0/1* I/O flag is configured as input, then writing to corresponding bit of *XIOF-DATA* register is ignored, however data written will be hold in *XIOF-DATA* register and will appear on *XIOF-0/1* output as soon as it will be configured as output.

SB Locking by the on-board TMS320C54x DSP Master

SB locking technique is used for processing of software shared semaphores that can be allocated in on-board SRAM or PIOX shared resources.

SB locking/unlocking by the on-board TMS320C54x DSP master is performed by means of *MLock* IOX flag (see table 2-2). *MLock* flag can be set by TMS320C54x DSP when it performs I/O access cycle to 8001H I/O port in IOX area (while DSP' on-chip XF flag is set to logical '1'). Note, that when writing or reading to/from *MLock* IOX register, only bit D0 is valid.

When *MLock* flag is set to logical '0' (this value is set as default on TMS320C54x DSP reset), then there is no active SB locking from on-board TMS320C54x DSP, and both TMS320C54x DSP and host ISA-bus memory interface can access shared SB resources.

When *MLock* flag is set to logical '1', then there active SB locking from on-board TMS320C542 DSP and SB access from host ISA-bus memory interface will be pending until SB will be unlocked by TMS320C54x DSP (*MLock* flag will be set to logical '0').

The SB lock-to-unlock time interval is not limited by *TORNADO-54x* hardware, however long duration of SB locking by DSP may cause timeout access faults for SB accesses by host ISA-bus memory interface.

The following is an example of C-code for TMS320C54x DSP that demonstrates processing of software shared semaphore using SB locking technique:

```
                    ...
ioport unsigned port8001;              /* declare MLock I/O port */
#define SET_XF1      asm(" ssbx xf")   /* declare MACROS to set XF=1 */
int Sem;                               /* declare software shared semaphore Sem */
                    ...
                    SET_XF1;
                    while (1)
                    {
                      port8001=1;      /* lock SB */
                      if (Sem==0) break;  /* verify for semaphore is free (Sem=0)*/
                      port8001=0;      /* unlock SB and repeat */
                    }

                    Sem=1;             /* semaphore is free, set it to Sem=1 */
                    port8001=0;        /* and unlock SB  */
                    ...
                    ...                /* perform some critical data processing */
                    ...
                    port8001=1;        /* reset semaphore using SB locking */
                    Sem=0;
                    port8001=0;        /* unlock SB */
                    ...
```

Note that *TORNADO-54x* provide hardware timeout control for SB granting wait time. This hardware timeout interval is setup to 6 μsec. In case timeout will occur due to SB locking by DSP, the *SB_ERROR* flag in *FLAG STATUS REGISTER* of host ISA-bus I/O interface will be set to the *SB_ERROR*=1 state. This will result in cancellation of all further SB requests from host ISA-bus memory interface until the *SB_ERROR* flag will be reset to the *SB_ERROR*=0 state by host PC software.

CAUTION

Time interval between SB locking and unlocking by the on-board TMS320C54x DSP should
not exceed 4 μsec to avoid timeout on host-to-SB access.

Generating DSP-to-host requests

TORNADO-54x supports attention request (interrupt request) from the on-board TMS320C54x DSP to host
IBM PC CPU in order to synchronize between program execution in host and on-board DSP environments.
Two methods for generation of DSP-to-host requests are supported in *TORNADO-54x*:

- *MH_RQ* (master to host request), that results in setting flag *MH_RQ* in *SYS_STATUS_FRG* flag
  register in host ISA-bus I/O interface. *MH_RQ* is generated when the on-board TMS320C54x DSP
  executes I/O write cycle to *MH_RQ* IOX register (see table 2-2), i.e. when TMS320C54x DSP when
  performs I/O write cycle at 8000H I/O port in IOX area (while DSP' on-chip XF flag is set to logical
  '1'). Data written has no meaning and is ignored. Generation of *MH_RQ* DSP-to-host request
  results in setting flag *MH_RQ* in *FLAG STATUS REGISTER* of host ISA-bus I/O interface into
  the *MH_RQ*=1 state and may generate active host PC interrupt request in case *MH_RQ_IE* bit in the
  CONTROL REGISTER from host ISA-bus I/O interface is set to the *MH_RQ_IE*=1 state.. The
  following is an example of C-code for TMS320C54x DSP that generates request to the host PC:

```
              ...
ioport unsigned port8000;              /* declare MH-RQ I/O port */
#define SET_XF1        asm(" ssbx xf")  /* declare MACROS to set XF=1 */


              ...
              SET_XF1;
              port8000=0;              /* DSP-to-host request is generated */
              ...
```

- *HPI_HINT* (host interrupt request via HPI), that results in setting bit *HINT* of HPIC register of
  TMS320C54x HPI and flag *HPI_HINT* in *SYS_STATUS_FRG* flag register of host ISA-bus I/O
  interface. *HPI_HINT* can generate active host PC interrupt request in case *HPI_HINT_IE* bit in
  HPI_IE_FRG flag register from host ISA-bus I/O interface is set to *HPI_HINT_IE*=1 state.

Processing request from host PC

TORNADO-54x supports attention request (interrupt request) from host PC to TMS320C54x DSP in order to
synchronize between the program execution in host and on-board DSP environments. Two methods for
generation of host-to-DSP requests is supported in *TORNADO-54x*:

- *HM_RQ* (host to master request), that results in generation of active *INT3* external interrupt request
  for the on-board TMS320C54x DSP. In order to generate output *HM_RQ* flag, host PC software has
  to write any data into *SET_HM_RQ_FRG* flag register from host ISA-bus I/O interface. User
  software for the TMS320C54x DSP should provide processing of *INT3* hardware interrupt request in
  accordance with software requirements. This is the recommended method for generation of host-to-
  DSP request since it delivers compatibility with all other *TORNADO* DSP systems for PC.

- *HPI_DSPINT* (host-to-DSP interrupt via HPI), that results in setting bit *DSPINT* in HPIC register of TMS320C54x HPI and generation *HPIINT* on-chip interrupt request for TMS320C54x DSP. In order to generate *HPI_DSPINT* interrupt request to DSP, host PC software has to write 0505H hex value to HPIC register of TMS320C54x DSP via host ISA-bus I/O interface. User software for the TMS320C54x DSP should provide processing of *HPIINT* interrupt request in accordance with software requirements. This is the *TORNADO-54x* specific method for generation of host-to-DSP request, and it is recommended for simulation of host-to-DSP communication via TMS320C54x DSP on-chip HPI.

External hardware interrupts for TMS320C54x DSP

TORNADO-54x on-board TMS320C54x DSP supports four external hardware interrupt requests *INT0...INT3* with the *INT0* request having the highest priority. These requests correspond to the following events:
- *INT0...INT2* interrupt requests can be generated by SIOX/PIOX-16 daughter modules
- *INT3* is on-board wired for software request *HM_RQ* from host PC to TMS320C54x DSP.

TORNADO-54x hardware provides direct wiring of external interrupt request source signals to the corresponding *INT0...INT3* pins of TMS320C54x DSP chip. All *INT0...INT3* external interrupt request pins of TMS320C54x DSP are edge-triggered (active interrupt is generated on falling edge) and allow pulse (τ_P>40ns) or static external interrupt request signals to applied to these input pins.

SIOX interface sites

TORNADO-54x provides two serial I/O expansion interface (SIOX) sites (SIOX-A and SIOX-B) for compatible AD/DA/DIO daughter card modules.

SIOX comprises of the TMS320C54x DSP-on-chip BSP/TDM serial ports control lines (BSP/TDM/BSP1 for *TORNADO-548/549*), DSP-on-chip timer output, *XIOF-0/1* I/O flags, *INT0..2* external interrupt requests and ±5v/±12v ISA-bus power supply lines. For details about SIOX sites refer to the corresponding section later in this chapter.

2.4   Host ISA-bus Memory Interface

Host ISA-bus memory interface of *TORNADO-54x* is designed to transfer data between host IBM PC environment and *TORNADO-54x* on-board SRAM/PIOX-16 SB resources without any software overhead for both host PC and on-board TMS320C54x DSP.

The SB address space in host ISA-bus memory interface appears as a series of dual-access 32KB *shared memory pages* (*SMP*) that are mapped onto the ISA-bus UMB (upper memory blocks) memory window by means of *SB PAGE MAPPER* register in host ISA-bus I/O interface. The SB can be accessed by host ISA-bus memory interface by means of random accesses to software variables or data arrays that are allocated within *SMP*, or by means of block data transfers between PC main memory and *SMP* using either host i80x286 CPU MOVSB/MOVSW/etc instructions or host DMA controller.

Host ISA-bus memory interface issues SB request and provides SB access using 16-bit data cycles each time host PC performs ISA-bus memory read/write cycle within the ISA-bus *SMP* address range. Particular selection of the UMB area is performed by host software by programming the *ISA_MI_BADDR_FRG* flag register of host ISA-bus I/O interface.

SMP ISA-bus Memory Base Address

SMP ISA-bus memory base address can be set within the ISA-bus UMB (upper memory blocks) memory address range by means of programming the *ISA_MI_BADDR_FRG* flag register from *TORNADO-54x* host ISA-bus I/O interface (see section 2.5) in accordance with predefined configuration settings in table 2-3. Only three least significant bits of *ISA_MI_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes.

ISA_MI_BADDR_FRG Flag Register (r/w)

0	0	0	0	0	MI_BA2	MI_BA1	MI_BA0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-3.   ISA-bus memory base address for *SMP*.

ISA-bus memory base address for *SMP*	ISA-bus memory address range for *SMP*	bit settings for *ISA_MI_BADDR_FRG* flag register		
		bit#2 MI_BA2	bit#1 MI_BA1	bit#0 MI_BA0
SMP is switched OFF	-	0	0	0
B8000H	B8000H ... BFFFFH	0	0	1
C0000H	C0000H ... C7FFFH	0	1	0
C8000H	C8000H ... CFFFFH	0	1	1
D0000H	D0000H ... D7FFFH	1	0	0
D8000H	D8000H ... DFFFFH	1	0	1
E0000H	E0000H ... E7FFFH	1	1	0
E8000H	E8000H ... EFFFFH	1	1	1

Notes: 1. The highlighted configuration corresponds to power on default value.

TORNADO-54x, as well as all other *TORNADO* DSP systems for ISA-bus hosts, offers software control for the *SMP* activity, i.e. switching *SMP* to either 'ON' or 'OFF' state in ISA-bus memory address space.

CAUTION

SMP is activated and appears in ISA-bus memory address space after loading any non-zero value to *ISA_MI_BADDR_FRG* flag register in accordance with table 2-3.

SMP is disactivated and disappears from ISA-bus memory address space after loading the zero value o *ISA_MI_BADDR_FRG* flag register.

Software control over *SMP* activity in *TORNADO-54x* delivers rational usage of deficit UMB area in host PC and allows multiple *TORNADO* DSP systems to operate within one PC environment.

Software Applications for ISA-bus Memory Interface

Once *TORNADO-54x* host ISA-bus memory interface provides direct mapping of 32KB *SMP* onto ISA-bus UMB window, the following host-to-SB data transfer techniques are applicable:
- *random access to variables or data arrays* allocated within the *SMP* by host PC software
- *block data transfers using MOVS/MOVSB/MOVSW instructions* of host PC i80x86 CPU
- *block data transfers under control of host PC DMA controller* using memory-to-memory or memory-to-port transfer cycles.

Operation Description for ISA-bus Memory Interface

The SB access from host ISA-bus memory interface is performed under hardware control of the on-board programmable *SB Access Controller* from ISA-bus interface of *TORNADO-54x*. Timing diagram for SB read cycle invoked by ISA-bus memory interface is presented at fig.2-3.
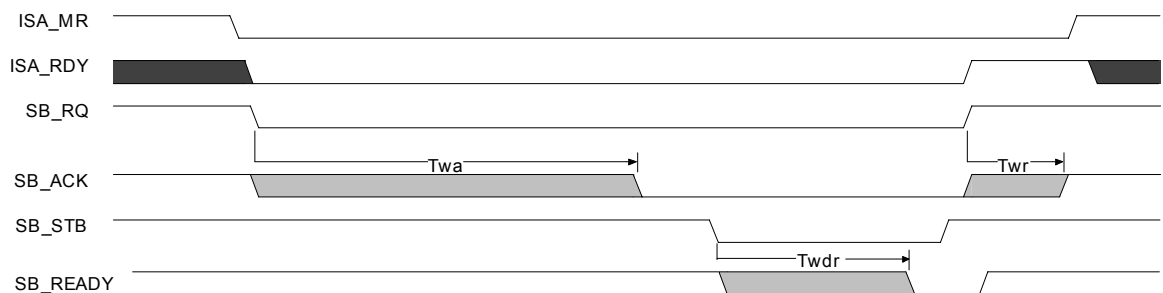
Fig.2-3. Timing diagram of SB read cycle invoked by ISA-bus memory interface.

Any request to the *SMP* memory address space on the host ISA-bus (*ISA_MR*=0 or *ISA_MW*=0) will result in activation of host ISA-bus memory interface that will immediately generate request to SB arbiter (*SB_RQ*=0) and set ISA-bus data ready signal to 'NOT READY' state (*ISA_RDY*=0). Host ISA-bus interface will stay in this state until SB will be granted (*SB_ACK*=0) by SB arbiter. SB will be granted at least after T_{wa}=50ns delay. After that, the SB access cycle will be generated by host ISA-bus memory interface with *SB_STB* signal set to the *SB_STB*=0 state. Host ISA-bus memory interface will now wait for *SB_READY* signal comes true

(SB_READY=0) in order to finish current SB access cycle. SB data ready signal SB_READY will come true (SB_READY=0) after T_{wdr} delay after SB_STB will come active (SB_STB=0). Wait time for SB_READY signal depends upon the SB address subspace selected (see table 2-1). Minimum wait time for SB_READY data ready signal is T_{wdr}=0ns and corresponds to accessing on-board SRAM area, whereas accesses PIOX-16 interface require at least 1ws with further awaiting for $PIOX\_READY$ signal sets true. After SB_READY signal sets true, the SB_RQ signal is removed (SB_RQ=1) and ISA_RDY signal is set to ISA_RDY =1 state in order to finish current ISA-bus memory access cycle. SB_ACK signal will return to its inactive state (SB_ACK=1) within T_{wr}=25ns after SB_RQ will be removed (SB_RQ=1).

SB Access Timeout Control

TORNADO-54x provides hardware timeout control for wait times for SB granting and for SB_READY signals when SB is accessed by host ISA-bus memory interface. This is required in order to avoid idling and crashing of host PC environment.

Hardware timeout for both SB granting and SB data ready are set to 6 usec. Once SB granting timeout occurs, the SB_ERROR bit in *CONTROL REGISTER* from host ISA-bus I/O interface is set to SB_ERROR=1 state. This will cancel all succeeding SB requests from host ISA-bus memory interface until SB_ERROR bit will be reset by host software. However, there is no error bit set in case of SB data ready timeout.

Data Formats for Host SB Data Access Cycles

TORNADO-54x supports only 16-bit SB data access cycles for both DSP and host ISA-bus memory interface.

However, PC can access SMP using both 8-bit and 16-bit ISA-bus memory cycles. In case 16-bit ISA-bus memory cycle is generated within SMP address space, then this will result in immediate generation of SB request and SB access cycle on SB grant. However, when 8-bit ISA-bus memory cycle is generated within SMP address space, then SB request will be generated only in case MSB (most significant byte) is accessed during ISA-bus memory write cycle or LSB (least significant byte) is accessed during ISA-bus memory read cycle. The corresponding LSB for memory write cycle is taken from the on-board register transceiver, that keeps LSB data since previous access to LSB during ISA-bus memory write cycle. Similar, the corresponding MSB will be latched in on-board register transceiver during memory read from LSB, and will be read later when ISA-bus memory read cycle to MSB will be generated.

SB Locking by ISA-bus Memory Interface

SB locking is used in order to lock SB access when processing software shared semaphores allocated in SRAM/PIOX-16 SB resources.

SB locking by ISA-bus memory interface may be set by means of setting either the SB_GLOCK bit or SB_LOCK bit of *CONTROL REGISTER* from ISA-bus I/O interface.

Timing diagrams of SB locking using SB_GLOCK and SB_LOCK bits are presented at fig. 2-4 and fig. 2-5.
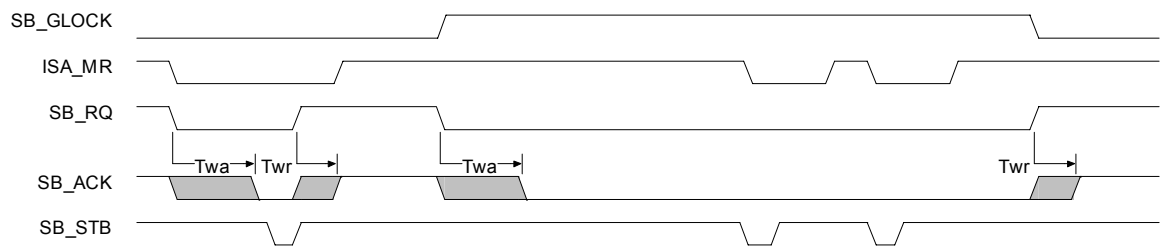
Fig.2-4. Timing diagram for SB access cycle invoked by ISA-bus memory interface with SB locking using *SB_GLOCK* bit.
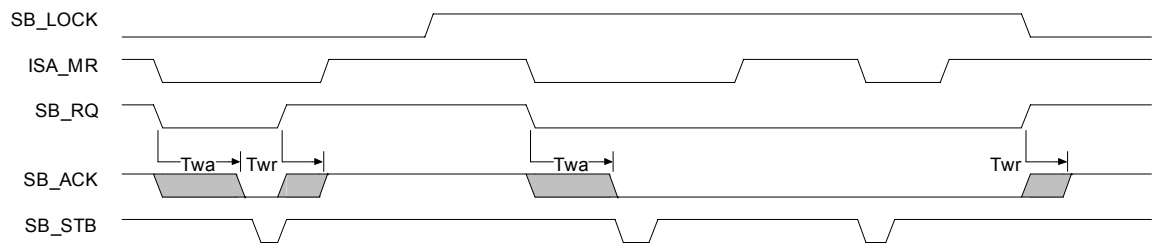
Fig.2-5. Timing diagram for SB access cycle invoked by ISA-bus memory interface with SB locking using *SB_LOCK* bit.

CAUTION

SB locking by ISA-bus memory interface using *SB_GLOCK* and *SB_LOCK* bits of *CONTROL REGISTER* from ISA-bus I/O interface should be used for short-time SB locking.

Continuous SB locking by ISA-bus memory interface using *SB_GLOCK* and *SB_LOCK* bits may result in continuous holding of TMS320C54x DSP (in case it requests access to SB data) and may lead to significant time distortions of real-time data processing.

2.5   Host ISA-bus I/O Interface

TORNADO-54x host ISA-bus I/O interface should be used for *TORNADO-54x* system control, accessing TMS320C54x DSP on-chip HPI, and interrupt handshaking between host PC CPU and TMS320C54x DSP.

I/O Base Address of Host ISA-bus I/O Interface

Host ISA-bus I/O interface occupies sixteen 8-bit registers inside ISA-bus I/O address space. Base address of host ISA-bus I/O interface is defined by means of 3-button on-board DIP-switch SW1 (see fig.2-2) in accordance with predefined settings listed in table 2-4.

Table 2-4. ISA-bus I/O base address for host ISA-bus I/O interface.

ISA-bus I/O base address for Host ISA-bus I/O interface	ISA-bus I/O address range	button SW1-3	button SW1-2	button SW1-1
300H	*300H..30FH*	OFF	OFF	OFF
310H	*310H..31FH*	OFF	OFF	ON
320H	*320H..32FH*	OFF	ON	OFF
330H	*330H..33FH*	OFF	ON	ON
340H	*340H..34FH*	ON	OFF	OFF
350H	*350H..35FH*	ON	OFF	ON
360H	*360H..36FH*	ON	ON	OFF
370H	*370H..37FH*	ON	ON	ON

Note: 1. Highlighted configuration corresponds to the factory setting.

ISA-bus I/O Interface Registers

List of *TORNADO-54x* ISA-bus I/O interface registers is presented in table 2-5.

Table 2-5. Register set of Host ISA-bus I/O interface.

register #	register address	access mode	reset value	description
#0	*BA*+0	r/w	0	*SB PAGE MAPPER* (*LSB*)
#1	*BA*+1	r/w	0	*SB PAGE MAPPER* (*MSB*)
#2	*BA*+2	r/w	10H	*CONTROL REGISTER*
#3	*BA*+3	r/w	-	*FLAG DATA REGISTER* *or*
		r w	- -	*FLAG STATUS REGISTER* *FLAG CONTROL REGISTER*
#403	*BA*+403H	r/w	0	*FLAG SELECTOR REGISTER*
#4	*BA*+4			reserved (do not use)
#5	*BA*+5			reserved (do not use)
#6	*BA*+6			reserved (do not use)
#7	*BA*+7			reserved (do not use)
#8	*BA*+8	r/w	see TI documentation	HPIC (LSB) register (TMS320C54x HPI)
#9	*BA*+9	r/w	see TI documentation	HPIC (MSB) register (TMS320C54x HPI)
#10	*BA*+10	r/w	-	HPI Data Latch (LSB) register (HPIDAI) with HPI address autoincrement facility (TMS320C54x HPI)
#11	*BA*+11	r/w	-	HPI Data Latch (MSB) register (HPIDAI) with HPI address autoincrement facility (TMS320C54x HPI)
#12	*BA*+12	r/w	-	HPI Address Latch (LSB) register (HPIA), (TMS320C54x HPI)
#13	*BA*+13	r/w	-	HPI Address Latch (MSB) register (HPIA), (TMS320C54x HPI)
#14	*BA*+14	r/w	-	HPI Data Latch (LSB) register (HPID) without HPI address autoincrement facility (TMS320C54x HPI)
#15	*BA*+15	r/w	-	HPI Data Latch (MSB) register (HPID) without HPI address autoincrement facility (TMS320C54x HPI)

Notes: 1.   '*BA*' denotes ISA-bus I/O base address of host ISA-bus I/O interface in
accordance with table 2-5.

2.   Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.
3.   All HPI registers access should be performed with bit *BOB* of HPI HPIC register being set
      to *BOB*=1 value. This correspond to LSB first data transmission protocol for ISA-bus host.

SB PAGE MAPPER Register

Registers #0 and #1 of *TORNADO-54x* ISA-bus I/O interface are least significant byte (LSB) and most significant byte (MSB) of 16-bit *SB PAGE MAPPER* register, which is used to setup the *SMP* SB base address in PROGRAM/DATA/IO SB areas in 16Kx16 (32Kx8) increments. Reset value for *SB PAGE MAPPER* register is 0.

SB PAGE MAPPER LSB register comprises of bits *A14..A15* for *TORNADO-542L* and of bits *A14..A17* for *TORNADO-548/549* of SB address and *I/O* and *D/P* SB area selector bits. All other bits of *SB PAGE MAPPER LSB* and *SB PAGE MAPPER MSB* registers are ignored on writing and read as zeros. The *A0..A13* bits of SB address for 16-bit SB words within *SMP* are derived from ISA-bus memory address bits *ISA_A1..ISA_A14*, whereas address bit *ISA_A0* is used to select particular byte within addressed 16-bit *SMP* SB word.

SB PAGE MAPPER (LSB) (r/w)

0	0	0	0	0 (*TORNADO-542L*) *A17* (*TORNADO-548/549*)	0 (*TORNADO-542L*) *A16* (*TORNADO-548/549*)	A15	A14
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

SB PAGE MAPPER (MSB) (r/w)

I/O	D/P	0	0	0	0	0	0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Particular SB area accessed is defined by bits *I/O* and *D/P* of *SB PAGE MAPPER MSB* register in accordance with table 2-6.

Table 2-6. SB Area Selector for Host-to-SB Accesses.

SB Area	*I/O* bit of SB PAGE MAPPER MSB register	*D/P* bit of SB PAGE MAPPER MSB register
SRAM/PROGRAM area 64Kx16 for *TORNADO-542L* 2x64Kx16 for *TORNADO-548/549*	0	0
SRAM/DATA area 64Kx16 for *TORNADO-542L* 4x32Kx16 for *TORNADO-548/549*	0	1
PIOX-16 area (64Kx16)	1	x

Note: 1. Highlighted configuration corresponds to default power-on setting.

It is important to note some specifics of extended memory addressing for *TORNADO-548/549* DSP system.

CAUTION

If SRAM/PROGRAM area (2x64Kx16) of *TORNADO-548/549* is selected, then bits *A14..A16* of *SB PAGE MAPPER LSB* are used, and bit *A17* is ignored.

If SRAM/DATA area (4x32Kx16) of *TORNADO-548/549* is selected, then all *A14..A17* bits of *SB PAGE MAPPER LSB* are used, however actual SB access is performed only if bit *A14*=1, i.e. the addressed SRAM/DATA area corresponds to the TMS320LC548/VC549 DSP off-chip data memory.

CONTROL Register

Register #2 of *TORNADO-54x* ISA-bus I/O interface is called *CONTROL REGISTER*. It used for reset control of on-board TMS320C54x DSP, for configuration of ISA-bus memory interface and for DSP-to-host interrupt communication.

CONTROL REGISTER (r/w)

SB_ERRO R IE	MH_RQ_IE	0 (reserved)	1 (reserved)	SB_LOCK	SB_GLOCK	0 (reserved)	M_GO
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-7 contains detail description for bits and bit fields of *CONTROL REGISTER*. Note, that some bits of *CONTROL REGISTER* are reserved for compatibility with other *TORNADO* DSP systems, and are ignored on writing and read as shown above.

Table 2-7. Bits and bit fields of *CONTROL REGISTER*.

bit of CONTROL REGISTER	power on default state	description
M_GO	0	*On-board TMS320C54x DSP reset line* control: ● '0' corresponds to the RESET state for the on-board TMS320C54x DSP ● '1' corresponds to RESET OFF for the on-board TMS320C54x DSP (i.e. the on-board DSP is in the program execution mode)
SB_GLOCK	0	*Shared Bus Global Lock.* With the *SB_GLOCK*=1 the SB access controller of ISA-bus memory interface generates active SB locking.
SB_LOCK	0	*Shared Bus Lock.* With the *SB_LOCK*=1 the SB access controller of ISA-bus memory interface generates active SB locking starting from first next SB request cycle after the *SB_LOCK* bit is set to the *SB_LOCK*=1.
MH_RQ_IE	0	*Master TMS320C54x DSP to Host Request Interrupt Enable.* If *MH_RQ_IE*=1 and *MH_RQ*=1, active interrupt request to host PC is generated. Host PC interrupt request is logical OR between (*MH_RQ_IE & MH_RQ*), (*SB_ERROR_IE & SB_ERROR*), (*HPI_ERROR_IE & HPI_ERROR*) and (*HPI_HINT_IE & HPI_HINT*) logic terms.
SB_ERROR_IE	0	*SB Error Interrupt Enable.* If *SB_ERROR_IE*=1 and *SB_ERROR*=1, active interrupt request to host PC is generated. Host PC interrupt request is logical OR between (*MH_RQ_IE & MH_RQ*), (*SB_ERROR_IE & SB_ERROR*), (*HPI_ERROR_IE & HPI_ERROR*) and (*HPI_HINT_IE & HPI_HINT*) logic terms.

Accessing TMS320C54x DSP on-chip HPI

TORNADO-54x host ISA-bus I/O interface supports optional DSP-to-host communication via TMS320C54x DSP on-chip HPI (refer to original TI documentation about details on TMS320C54x HPI).

Along with SB SRAM, TMS320C54x DSP HPI is a another data path for communication between DSP and host via DSP on-chip 2Kx16 shared RAM area mapped into 1000H..17FFH data memory address space. Along with data communication, mutual DSP-to-host (*HPI_HINT*) and host-to-DSP (*HPI_DSPINT*) interrupts are supported. On host side, the *HPI_HINT* DSP-to-host interrupt can be individually masked and generate PC ISA-bus interrupt.

> **CAUTION**
>
> All host-to-HPI accesses to HPIC, HPIDAI, HPIA and HPID registers of TMS320C54x DSP HPI should be performed as to 16-bit I/O registers only. Any violation of this may result in invalid data passed.
>
> Bit *BOB* of HPIC register should be set to logical '1' prior any further data transfer will be performed via HPI and HPI address will be loaded. This corresponds to LSB first communication via ISA-bus.

Timeout Control for Host-to-HPI Access

Normally, when TMS320C54x DSP is running while *SMODE* bit of HPIC register is set to logical '1' (this corresponds to shared mode for accessing HPI shared RAM area), or when *SMODE* bit of HPIC register is set to logical '0' (this corresponds to host-only mode for accessing HPI shared RAM area), then HPI will respond immediately and will set its *HPI_READY* hardware signal to true state almost without any wait states on PC host ISA-bus I/O interface side.

However, in case *SMODE* bit of HPIC register is set to logical '1' and HPI is accessed by host ISA-bus I/O interface after TMS320C54x DSP has executes either *IDLE 2* or *IDLE 3* instruction (which results in DSP on-chip clock stopped), this host-to-HPI access will be pended with *HPI_READY* hardware signal set to false state until DSP clock will recover after receiving valid DSP interrupt. This may result in host ISA-bus idling and crashing host PC environment.

In order to avoid host ISA-bus idling, *TORNADO-54x* host ISA-bus I/O interface features hardware timeout control for host-to-HPI accesses. The timeout interval for host-to-HPI access is equal to 4 µsec.

Once HPI timeout will occur, this will result in setting active *HPI_ERROR* flag (*HPI_ERROR*=1) in *SYS_STATUS_FRG* flag register. Furthermore, once *HPI_ERROR* flag is set, all succeeding host-to-HPI accesses will be canceled and returned data will be invalid until host will recognize and clear *HPI_ERROR* flag by means of writing to *CLEAR_HPI_ERROR_FRG* flag register.

> **CAUTION**
>
> If *SMODE* bit of HPIC register is set to logical '1' and HPI is accessed by host ISA-bus I/O interface after TMS320C54x DSP has executes either *IDLE 2* or *IDLE 3* instruction, this will result in pending host-to-HPI access and may cause 6 µsec host-to-HPI access timeout, which will result in setting *HPI_ERROR* flag in *SYS_STATUS_FRG* flag register and cancellation all succeeding host-to-HPI accesses until *HPI_ERROR* flag will be cleared by host.

Note, that active state of *HPI_ERROR* flag may generate host interrupt in case *HPI_ERROR_IE* bit in *HPI_IE_FRG* flag register is set to *HPI_ERROR_IE*=1 state.

FLAG Registers

Registers #3 and #403 of *TORNADO-54x* ISA-bus I/O interface are used for auxiliary control (*flags*) of *TORNADO-54x*.

Flags are comprised into a set of multiplexed 8-bit *flag registers*. Particular *flag register* is addressed by *FLAG SELECTOR REGISTER* (register #403). Flags within a currently addressed (selected) *flag register* can be read/written using I/O read/write operation into *FLAG DATA REGISTER* (register #3).

FLAG SELECTOR REGISTER is available for I/O r/w operations has the following data format:

FLAG SELECTOR REGISTER (r/w)

FSEL-7	FSEL-6	FSEL-5	FSEL-4	FSEL-3	FSEL-2	FSEL-1	FSEL-0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

List of available flag registers for *TORNADO-54x*, which can be addressed by *FLAG SELECTOR REGISTER*, is presented in table 2-8.

Table 2-8. Flag registers for *TORNADO-54x.*

code written to FLAG SELECTOR REGISTER	name of addressed flag register (register #3)	description
10H	r: SYS_STATUS_FRG w: SET_HM_RQ_FRG	In read mode indicates current status of major run-time systems flags of *TORNADO-54x* (refer to subsection "*SYS_STATUS_FRG Flag Register*" later in this section). In write mode sets active *Host_to_Master_Request (HM_RQ)* via *INT3* external interrupt request input for TMS320C54x DSP. Data written to *SET_HM_RQ_FRG* register has no meaning and is ignored.
20H	r: SYS_STATUS_FRG w: CLEAR_MH_RQ_FRG	In read mode indicates current status of major run-time systems flags of *TORNADO-54x* (refer to subsection "*SYS_STATUS_FRG Flag Register*" later in this section). In write mode clears active *Master_to_Host_Request (MH_RQ)* flag in *SYS_STATUS_FRG* flag register. *Master_to_Host_Request* flag can be set by resident TMS320C54x DSP software in order to set attention or interrupt request to host PC. Data written to *CLEAR_MH_RQ_FRG* register has no meaning and is ignored. Host PC should perform this operation in the end of corresponding procedure or interrupt handler (in case *MH_RQ_IE*=1) after *MH_RQ* interrupt source has been identified.
30H	r: SYS_STATUS_FRG w: CLEAR_SB_ERROR_FRG	In read mode indicates current status of major run-time systems flags of *TORNADO-54x* (refer to subsection "*SYS_STATUS_FRG Flag Register*" later in this section). In write mode clears active *SB_ERROR* flag in *SYS_STATUS_FRG* flag register. Active *SB_ERROR* flag is set by timeout during host-to-SB access. Data written to *CLEAR_SB_ERROR_FRG* register has no meaning and is ignored. Host PC should perform this operation in the end of corresponding interrupt handler (in case *SB_ERROR_IE*=1) after *SB_ERROR* interrupt source has been identified. Also, host PC should perform this operation in the end of data transmission between host ISA-bus and SB in case active *SB_ERROR* flag is detected.
40H	w: CLEAR_HPI_ERROR_FRG	In write mode clears active *HPI_ERROR* flag in *SYS_STATUS_FRG* flag register. Active *HPI_ERROR* flag is set by timeout during host-to-HPI access. Data written to *CLEAR_HPI_ERROR_FRG* register has no meaning and is ignored. Host PC should perform this operation in the end of corresponding interrupt handler (in case *HPI_ERROR_IE*=1) after *HPI_ERROR* interrupt source has been identified. Also, host PC should perform this operation in the end of data transmission between host ISA-bus and HPI in case active *HPI_ERROR* flag is detected. This flag register is write-only

50H	r/w: HPI_IE_FRG	*HPI-to-Host Interrupt Enable Register*. This flag register sets interrupt enable masks for interrupting host PC on *HPI_ERROR* and *HPI_HINT* events. Host PC interrupt request is logical OR between (*MH_RQ_IE & MH_RQ*), (*SB_ERROR_IE & SB_ERROR*), (*HPI_ERROR_IE & HPI_ERROR*) and (*HPI_HINT_IE & HPI_HINT*) logic terms.
60H	r: DSP_STATUS_FRG	*DSP Status Register*. This flag register returns current state of *DSP_Mlock* and *DSP_M_GO* control signals from the TMS320C54x DSP environment. This register is provided for compatibility with *TORNADO* multiprocessor DSP systems
E0H	r/w: ISA_MI_BADDR_FRG	*ISA-bus Memory Interface Base Address Register*. Sets ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-54x* in accordance with table 2-3. Sets/resets activity of host ISA-bus memory interface of *TORNADO-54x* within UMB area of ISA-bus memory address space. Only three least significant bits of this register are valid; all other bits are ignored and reads as zeros.
E2H	r/w: ISA_ECC_BADDR_FRG (*TORNADO-542L* only)	*ECC ISA-bus I/O Base Address Register*. Sets ISA-bus I/O base address for *TORNADO-542L* optional on-board emulation controller (*ECC*) in accordance with table 2-10. Sets/resets activity of *ECC* within ISA-bus I/O address space. Only three least significant bits of this register are valid; all other bits are ignored and reads as zeros.
F0H F1H	r: DEV_ID0_FRG r: DEV_ID1_FRG	*Device Identifier and S/N Registers #0/#1*. These registers are read only and contain LSB and MSB of unique device and s/n identifier for *TORNADO-54x*

Notes: 1.   Unused codes for flag registers are reserved for future expansion.
              2.   Access modes: *r* - read only; *w* - write only; *r/w* - read and write.

Once a desired flag register is selected by loading the corresponding code into *FLAG SELECTOR REGISTER* in accordance with table 2-8, current flags status can be obtained by reading *FLAG DATA REGISTER* (*FLAG STATUS REGISTER*), whereas flag settings can be performed by writing to *FLAG DATA REGISTER* (*FLAG CONTROL REGISTER*). Note, that *FLAG STATUS REGISTER* and *FLAG CONTROL REGISTER* are actually read and write denotification of *FLAG DATA REGISTER* that is available for both read and write operations. However, this makes useful sense since some of *TORNADO-54x* flag registers have different format for read and write operations.

Table 2-9. Bits of *SYS_STATUS_FRG* flag register for *TORNADO-54x*.

bit name	power on default value	description
SB_ACK	0	*SB Request Acknowledge. SB_ACK*=1 denotes that SB arbiter has granted SB access to host ISA-bus memory interface. *SB_ACK* flag can be read during active SB locking from host ISA-bus memory interface. It is used for diagnostic purpose only.
HPI_ERROR	0	*HPI Error (HPI_ERROR). HPI_ERROR*=1 denotes that 6 μsec timeout has been detected during host-to-HPI access. *HPI_ERROR* flag will keep staying in active *HPI_ERROR*=1 state until it will be reset by host PC software by means of writing to *CLEAR_HPI_ERROR_FRG* flag register. If *HPI_ERROR* flag has been set to active (*HPI_ERROR*=1) state, all succeeding host-to-HPI accesses from host ISA-bus memory interface of *TORNADO-54x* will be ignored and data returned will be undefined. If *HPI_ERROR_IE*=1 and *HPI_ERROR*=1, an active host PC CPU interrupt request is generated.
HPI_HINT	0	*DSP_to_Host Request_via_HPI (HPI_HINT). HPI_HINT*=1 denotes that TMS320C54x DSP has generated active request to host PC CPU via HPI. *HPI_HINT* flag will keep staying in active *HPI_HINT*=1 state until it will be reset by host PC software by means of writing 0909H hex value to HPIC register of TMS320C54x DSP HPI. If *HPI_HINT_IE*=1 and *HPI_HINT*=1, then active host PC CPU interrupt request is generated.
MH_RQ	0	*Master_to_Host Request (MH_RQ). MH_RQ*=1 denotes that TMS320C54x DSP has generated active request to host PC CPU. *MH_RQ* flag will keep staying in active *MH_RQ*=1 state until it will be reset by host PC software by means of writing to *CLEAR_MH_RQ_FRG* flag register. If *MH_RQ_IE*=1 and *MH_RQ*=1, then active host PC CPU interrupt request is generated.
SB_ERROR	0	*SB Error (SB_ERROR). SB_ERROR*=1 denotes that the 4.2 μsec timeout has been detected during previous SB access from host ISA-bus memory interface. *SB_ERROR* flag will keep staying in active *SB_ERROR*=1 state until it will be reset by host PC software by means of writing to *CLEAR_SB_ERROR_FRG* flag register. If *SB_ERROR* flag is set active (*SB_ERROR*=1), all succeeding host-to-SB requests from host ISA-bus memory interface of *TORNADO-54x* will be ignored and data returned will be undefined. If *SB_ERROR_IE*=1 and *SB_ERROR*=1, an active host PC CPU interrupt request is generated.

SYS_STATUS_FRG Flag Register

SYS_STATUS_FRG flag register comprises of major *TORNADO-54x* run-time system flags settings. It is available as read only register and has the following data format:

SYS_STATUS_FRG Flag Register   (read only)

SB_ERROR	MH_RQ	HPI_HINT	0	0	0	HPI_ERROR	SB_ACK
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Detail description for bits of *SYS_STATUS_FRG* flag register is presented in table 2-9.

HPI-to-Host Interrupt Enable Flag Register (HPI_IE_FRG)

HPI_IE_FRG flag register comprises of interrupt enable bit masks for generation of host PC interrupt on HPI events: active *HPI_HINT* HPI-to-host interrupt request and/or active *HPI_ERROR* flag. Format of *HPI_IE_FRG* flag register is as the following:

HPI_IE_FRG Flag Register   (r/w)

0	0	HPI_HINT_IE	0	0	0	HPI_ERROR_IE	0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

In case *HPI_HINT_IE* bit is set to logical '1' and *HPI_HINT* flag is active (*HPI_HINT*=1) in *SYS_STATUS_FRG* flag register or HINT register of HPI, then this will result in generation of active host PC interrupt request. In case *HPI_HINT_IE* bit is set to logical '0', then no host PC interrupt will be generated when *HPI_HINT* flag will come active.

In case *HPI_ERROR_IE* bit is set to logical '1' and *HPI_ERROR* flag is active (*HPI_ERROR*=1) in *SYS_STATUS_FRG* flag register, then this will result in generation active host PC interrupt request. In case *HPI_ERROR_IE* bit is set to logical '0', then no host PC interrupt will be generated when *HPI_ERROR* flag will come active.

DSP_STATUS_FRG Flag Register

DSP_STATUS_FRG flag register is provided for compatibility with *TORNADO* multi-DSP systems and comprises of most important TMS320C54x DSP control signals settings. It is available as read only register and has the following data format:

DSP_STATUS_FRG Flag Register   (read only)

0	0	0	0	0	0	DSP_M_GO	DSP_MLock
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

The *DSP_M_GO* bit is actually the returned value of *M_GO* bit from the *CONTROL REGISTER*, whereas the *DSP_MLock* bit indicates the SB locking by on-board TMS320C54x DSP master (see section 2.3 "TMS320C54x DSP Environment" earlier in this chapter). The *DSP_MLock*=1 denotes that TMS320C54x DSP has set the SB lock request. The SB will be locked by DSP immediately in case there is no current host-to-SB request or immediately upon the current host-to-SB request will terminate.

Flag Registers for Identifying TORNADO-54x DSP System

TORNADO-54x includes *DEV_ID0_FRG/DEV_ID1_FRG* read-only flag registers (see table 2-8), which contains unique code for identification of *TORNADO-54x* DSP systems and its serial number.

Usage of *DEV_ID0_FRG/DEV_ID1_FRG* flag registers in host PC software is recommended for those applications that require to be protected from unauthorized duplication of software.

Generating Request to TMS320C54x DSP

TORNADO-54x can generate requests from host PC to TMS320C54x DSP in order to synchronize between programs execution in host and on-board DSP environments. Two methods for generation of host-to-DSP requests is supported in *TORNADO-54x*:

- *HM_RQ* (host to master request), that results in generation of active *INT3* external interrupt request for the on-board TMS320C54x DSP. In order to generate output *HM_RQ* flag, host PC software has to write to *SET_HM_RQ_FRG* flag register. This is the recommended method for generation of host-to-DSP request since it delivers compatibility with all other *TORNADO* DSP systems for PC.
- *HPI_DSPINT* (DSP interrupt via HPI), that results in setting bit *DSPINT* of HPIC register of TMS320C54x HPI. In order to generate *HPI_DSPINT* interrupt request to DSP, host PC software has to write 0505H hex value to HPIC register of TMS320C54x DSP. This is the *TORNADO-54x* specific method for generation of host-to-DSP request, and it is recommended for simulation of host-to-DSP communication via TMS320C54x DSP on-chip HPI.

Processing Request from TMS320C54x DSP

TORNADO-54x can generate requests from TMS320C54x DSP to host CPU in order to synchronize between program execution in host and on-board DSP environments. Two methods for generation of DSP-to-host requests is supported in *TORNADO-54x*:

- *MH_RQ* (master to host request), that results in setting flag *MH_RQ* in *SYS_STATUS_FRG* flag register. *MH_RQ* can generate active host PC interrupt request in case *MH_RQ_IE* bit in the *CONTROL REGISTER* is set to the *MH_RQ_IE*=1 state. *MH_RQ* will remain in active state *MH_RQ*=1 until it will be recognized and reset by host software. In order to reset the *MH_RQ* flag, host PC software has to write to *Clear_Master_to_Host_Request* flag register. This is the recommended method for generation of DSP-to-host request since it delivers compatibility with all other *TORNADO* DSP systems for PC.
- *HPI_HINT* (host interrupt request via HPI), that results in setting bit *HINT* of HPIC register of TMS320C54x HPI and flag *HPI_HINT* in *SYS_STATUS_FRG* flag register. *HPI_HINT* can generate active host PC interrupt request in case *HPI_HINT_IE* bit in *HPI_IE_FRG* flag register is set to *HPI_HINT_IE*=1 state. *HPI_HINT* will remain in active state *HPI_HINT*=1 until it will be recognized and reset by host software. In order to reset the *HPI_HINT* flag, host PC software has to write 0909H hex value to HPIC register of TMS320C54x DSP. This is the *TORNADO-54x* specific method for generation of DSP-to-host request, and it is recommended for simulation of DSP-to-host communication via TMS320C54x DSP on-chip HPI.

Host Interrupts

Host ISA-bus I/O interface can generate active interrupts to host PC CPU in the following cases:
- when *SB_ERROR* flag is active (*SB_ERROR*=1) in *SYS_STATUS_FRG* flag register and *SB_ERROR_IE* bit in *CONTROL REGISTER* is set to *SB_ERROR_IE*=1 state

- when *MH_RQ* is active (*MH_RQ*=1) in *SYS_STATUS_FRG* flag register and *MH_RQ_IE* bit in *CONTROL REGISTER* is set to *MH_RQ_IE*=1 state
- when *HPI_ERROR* flag is active (*HPI_ERROR*=1) in *SYS_STATUS_FRG* flag register and *HPI_ERROR_IE* bit in *HPI_IE_FRG* flag register is set to *HPI_ERROR_IE*=1 state
- when *HPI_HINT* is active (*HPI_HINT*=1) in *SYS_STATUS_FRG* flag register or HINT register of HPI and *HPI_HINT_IE* bit in *HPI_IE_FRG* flag register is set to *HPI_HINT_IE*=1 state

Host ISA-bus interrupt request is generated as logical 'OR' of the above events. Decoding of interrupt source should be performed by host PC software by means of analyzing the contents of *SYS_STATUS_FRG* flag register.

Host PC interrupt request may be generated using one of nine available ISA-bus interrupt request lines. Particular PC interrupt line is selected by the on-board interrupt configuration jumper J3 (see fig.2-2). The following ISA-bus interrupt request lines are available: IRQ-3, IRQ-4, IRQ-5, IRQ-6, IRQ-7, IRQ-10, IRQ-11, IRQ-12 and IRQ-15.

Setting ISA-bus memory base address for Host ISA-bus Memory Interface

TORNADO-54x provides software setting of ISA-bus memory base address for host ISA-bus memory interface by means of writing to *ISA_MI_BADDR_FRG* flag register. Only three least significant bits of *ISA_MI_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes. Available settings for *ISA_MI_BADDR_FRG* flag register are presented in table 2-3.

ISA_MI_BADDR_FRG Flag Register (r/w)

0	0	0	0	0	MI_BA2	MI_BA1	MI_BA0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Setting ISA-bus I/O base address for ECC in TORNADO-542L

TORNADO-542L provides software setting of ISA-bus I/O base address for optional on-board emulation controller chip (*ECC*) by means of writing to *ISA_ECC_BADDR_FRG* flag register. Only three least significant bits of *ISA_ECC_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes. Available settings for *ISA_ECC_BADDR_FRG* flag register are presented in table 2-10.

ISA_ECC_BADDR_FRG Flag Register (r/w)

0	0	0	0	0	ECC_BA2	ECC_BA1	ECC_BA0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-10. ISA-bus I/O base address for *TORNADO-542L* optional on-board emulation controller (*ECC*).

ISA-bus I/O base address for *ECC*	ISA-bus I/O address range for *ECC*	bit setting for *ISA_ECC_BADDR_FRG* flag register		
		bit#2 ECC_BA2	*bit#1 ECC_BA2*	*bit#0 ECC_BA2*
ECC is disconnected from host ISA-bus; attachment of external TI XDS510 or MicroLAB' MIRAGE-510D emulator is allowed	-	0	x	x
[2)]*240H*	*240H ... 25FH*	1	0	0
280H	*280H ... 29FH*	1	0	1
320H	*320H ... 33FH*	1	1	0
340H	*340H ... 35FH*	1	1	1

Note: 1. Highlighted configuration corresponds to host power on default setting.
           2. This configuration is used as default by *T54CC.EXE* software utility.

CAUTION

Attachment of external TI XDS510 or MicroLAB' *MIRAGE-510D* emulator to *TORNADO-542L* is allowed only in case on-board emulation controller (*ECC*) is either not installed or is software 'disconnected' from ISA-bus (see table 2-10).

Attachment of external TI XDS510 or MicroLAB' *MIRAGE-510D* emulator to *TORNADO-542L* while the on-board emulation controller (*ECC*) is active is strongly prohibited and may result in damaging emulator and/or *ECC*.

2.6   Parallel I/O Expansion Interface (PIOX-16)

TORNADO-54x architecture provides expansion of the on-board I/O resources using 16-bit parallel I/O expansion interface (PIOX-16) and compatible PIOX-16 daughter modules. PIOX-16 is designed to carry compatible daughter card modules above *TORNADO-54x* mainboard (see fig.1-1 and fig.2-2) and is compatible with all *TORNADO-3x/4x/6x* DSP systems and *TORNADO-E3x/E6x* embedded DSP controllers.

Description

PIOX-16 appears as 64Kx16 I/O address space of *TORNADO-54x* on-board SB and can be accessed by both the on-board TMS320C54x DSP and host ISA-bus memory interface. It includes SB control signals, TMS320C54x DSP on-chip timer and external interrupt inputs, DSP reset signal, and *XIOF-0/1* I/O flags from DSP IOX area..

PIOX-16 provides data transfer timing using data strobe and write enable signals, and generates data ready signal *PIOX_READY*. PIOX-16 supports 16-bit SB access cycles only.

Installation of PIOX-16 daughter-card modules onto TORNADO-54x mainboard

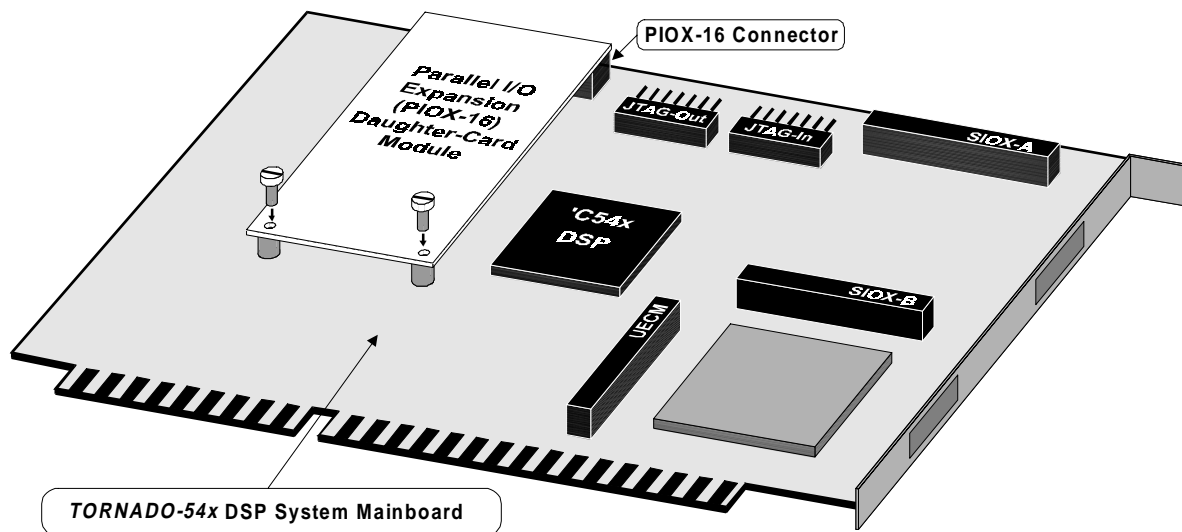Figure 2-6 shows installation of PIOX daughter-card modules onto *TORNADO-62/67* and *TORNADO-62MX/67MX* mainboard.

Fig.2-6.   Installation of PIOX-16 daughter-card module onto *TORNADO-54x* mainboard.

Accessing PIOX-16 from TMS320C54x software

PIOX-16 can be accessed by on-board TMS320C54x DSP during I/O access cycles while DSP XF flag is set to logical '0'.

> **CAUTION**
>
> The I/O field of DSP on-chip SWWSR register should be programmed to 02H in order to set two software wait states with further processing of *PIOX_READY* signal when accessing PIOX-16.

Accessing PIOX-16 from Host ISA-bus Memory Interface

PIOX-16 can be accessed by host ISA-bus memory interface when *I/O* bit of *SB PAGE MAPPER MSB* register from host ISA-bus I/O interface is set to logical '1'.

> **CAUTION**
>
> PIOX-16 area is accessed by host ISA-bus memory interface with one hardware wait state and with further processing of *PIOX_READY* signal.

PIOX-16 Connector Pinout

On-board PIOX-16 connector is a high-density DDK 50-pins DHB-series dual row female connector with 0.05" pin pitch. Compatible PIOX-16 plugs for user designed PIOX-16 daughter-card modules are available upon request from MicroLAB Systems Ltd.

PIOX-16 pinout specification is presented at fig 2-7 whereas signal specification is listed in table 2-11.
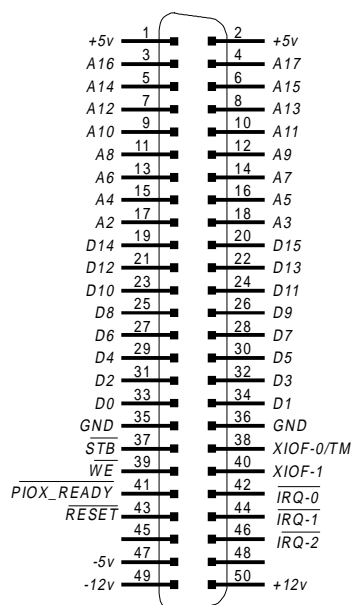
Fig.2-7. PIOX-16 connector pinout (top view).

Table 2-11. PIOX-16 signal specification.

Signal name	signal type	description
A0..A15	O	SB address bus.
D0..D15	I/O	SB data bus.
$\overline{STB}$	O	Active low PIOX-16 data transfer strobe.
$\overline{WE}$	O	Active low PIOX-16 write enable.
$\overline{PIOX\_READY}$	I	PIOX-16 data ready acknowledge ($\overline{PIOX\_READY}$=0) signal. Generated by PIOX-16 module in order to match the PIOX-16 SB cycle timing with timing requirements of memory and I/O devices used in PIOX-16 module.
XIOF-0/TM	I/O/Z	Configured by the on-board J3 jumper as either *XIOF-0* I/O flag from TMS320C54x DSP IOX area or DSP on-chip timer output (TM). If J3 jumper is in the 2-3 state (see fig.A-1), then this pin is configured as *XIOF-0* I/O flag, then it can be configured by DSP as input or output general purpose pin. If J3 jumper is in the 1-2 state, then this pin is configured as DSP on-chip timer output, i.e. it wires non-buffered DSP on-chip timer pin signal to this connector pin.

XIOF-1	I/O/Z	*XIOF-1* I/O flag from TMS320C54x DSP IOX area. It can be configured by DSP as input or output general purpose pin.
$\overline{RESET}$	O	Reset signal ($\overline{RESET}$ =0) for the on-board TMS320C54x DSP chip.
$\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, $\overline{IRQ\text{-}2}$	I	Hardware interrupt request lines ($\overline{IRQ\text{-}0}$ has the highest priority) for the on-board TMS320C54x DSP chip. Both static and one-shot (with the pulse length longer than 50 ns) are supported. Actual hardware interrupt requests (*INT0...INT2*) will be generated on the falling edge (1→0) of $\overline{IRQ\text{-}0}$ ..$\overline{IRQ\text{-}2}$ signals.
GND		Ground.
+5v		+5v power (from ISA-bus).
+12v		+12v power (from ISA-bus).
-5v		-5v power (from ISA-bus).
-12v		-12v power (from ISA-bus).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

Data Transfer Timing for PIOX-16

PIOX-16 data transfer timing is presented at fig.2-8. This data transfer timing is known as MOTO mode and assumes usage of data strobe signal and write enable signal.
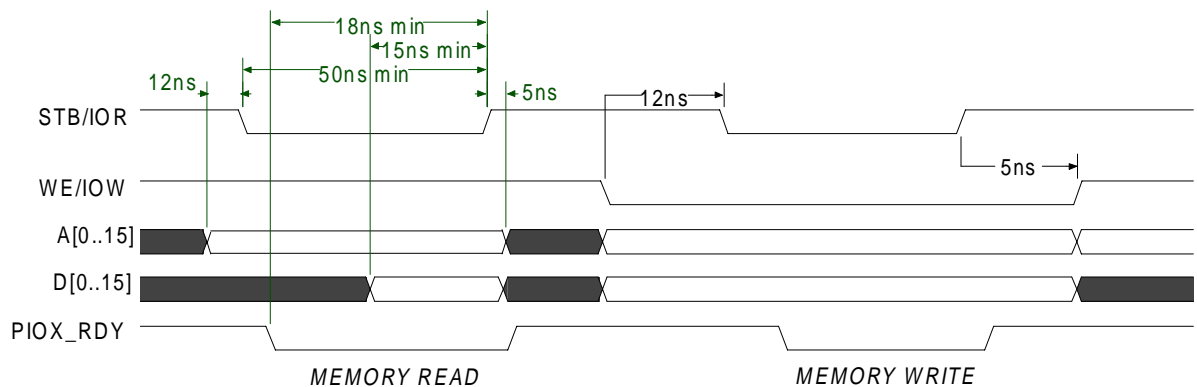

Fig.2-8. PIOX-16 data transfer timing diagram.

Physical Dimensions for PIOX-16 Daughter-card Modules

Physical dimensions for PIOX-16 daughter-card modules are presented at fig. 2-9. This information is intended for those *TORNADO* customers, who need to design customized PIOX-16 daughter-card modules.
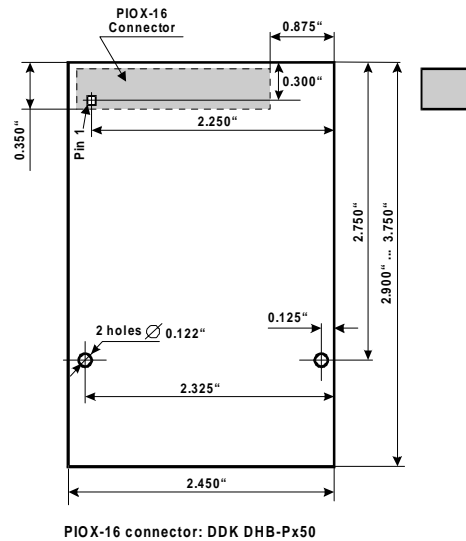

PIOX-16 connector: DDK DHB-Px50

Fig.2-9.   Physical dimensions for PIOX-16 daughter-card modules.

2.7   Serial I/O Expansion Interfaces (SIOX-A/B)

TORNADO-54x architecture provides expansion of the on-board TMS320C54x I/O resources via two serial I/O expansion interface sites (SIOX-A and SIOX-B), which are designed to carry compatible daughter card modules (see fig.1-1 and fig.2-2). SIOX interface sites of *TORNADO-54x* is compatible with SIOX interface sites for *TORNADO-3x/54x/6x* DSP systems and stand-alone *TORNADO-E/EL/SX* DSP controllers.

Available SIOX daughter cards for *TORNADO-3x/54x* DSP systems include a variety of AD/DA/DIO daughter cards for telecommunication, speech and audio signal processing, industrial and instrumentation applications, and many more.

CAUTION

The *TORNADO-548/549* on-board area for SIOX-B site is shared with the on-board area for *UECM* emulation control daughter-card module. Only one of SIOX-B or *UECM* daughter cards can be installed simultaneously onto *TORNADO-548/549* mainboard.

Description

Each of SIOX-A/B interface sites comprises of signals for SIO-0 and SIO-1 serial ports, TMS320C54x DSP on-chip timer and interrupts control, as well as optional *XIOF-0/1* I/O flags, DSP reset signal and ISA-bus power supply lines (fig.2-10).
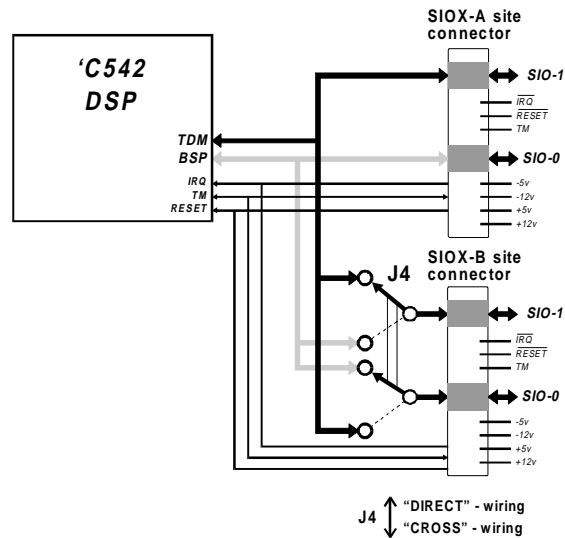
Fig.2-10a. SIOX sites connection diagram for *TORNADO-542L*.
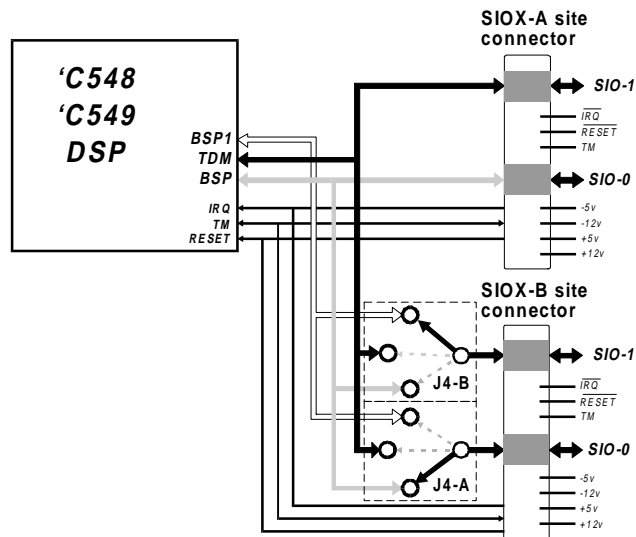
Fig.2-10b. SIOX sites connection diagram for *TORNADO-548/549*.

The SIO-0 and SIO-1 ports of SIOX-A and SIOX-B sites may connect to the TMS320C54x DSP on-chip buffered serial port (BSP) and time division multiplexed serial port (TDM). The SIOX-B site in *TORNADO-548/549* DSP system can also be configured to connect SIO-0 and SIO-1 ports to the TMS320LC548/VC549 on-chip BSP1 port. Maximum throughoutput of serial ports is 20 Mbit/sec for *TORNADO-542L* and 50 Mbit/sec for *TORNADO-548/549*. See subsection below for more details.

External analog and digital I/O signals for installed SIOX daughter cards should be attached by means of the SIOX daughter card on-board I/O connector via rear panel of host PC.

Installation of SIOX Daughter-card Modules onto TORNADO-54x Mainboard

Figure 2-11 shows installation of SIOX daughter-card modules onto *TORNADO-54x* and *TORNADO-62MX/67MX* mainboard.
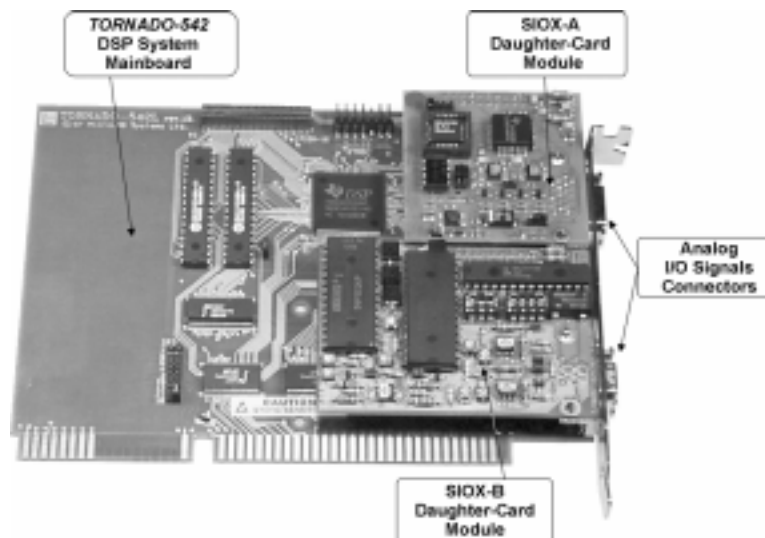

Fig.2-11a. TORNADO-542L mainboard with SIOX-A and SIOX-B daughter-card modules.

CAUTION

The on-board area for SIOX-B site of *TORNADO-548/549* is shared with the on-board area for *UECM* emulation control daughter-card module. Either SIOX-B or *UECM* daughter-card module can be installed onto *TORNADO-548/549* mainboard.

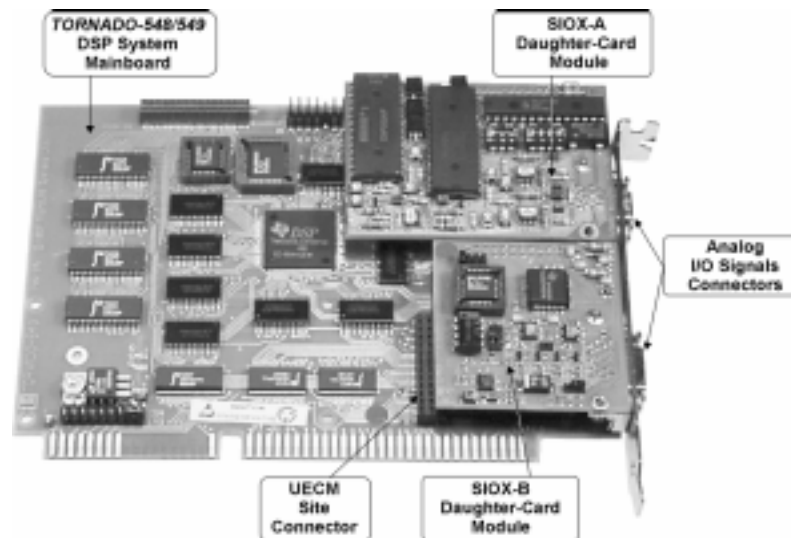*Fig.2-11b. TORNADO-548/549* mainboard with SIOX-A and SIOX-B daughter-card modules.

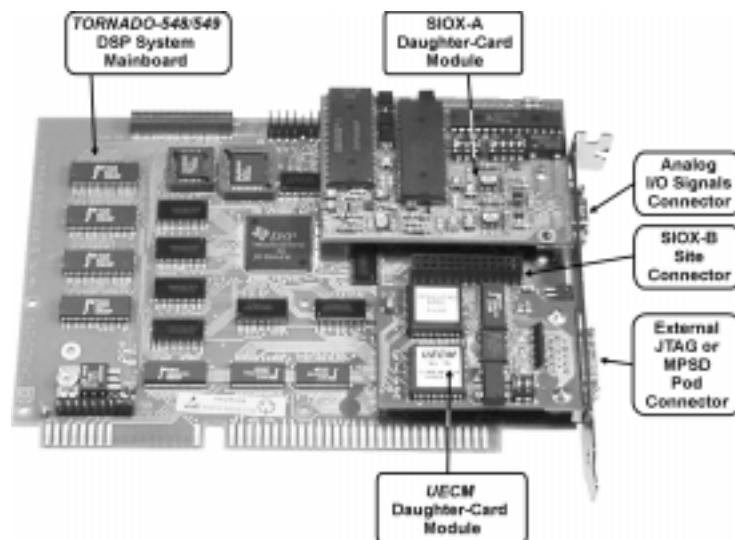*Fig.2-11c. TORNADO-548/549* mainboard with SIOX-A and UECM daughter-card modules.

SIOX site connector

SIOX sites connector is and industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. SIOX connector pinout is presented at fig.2-12 and signal specifications are listed in table 2-12.
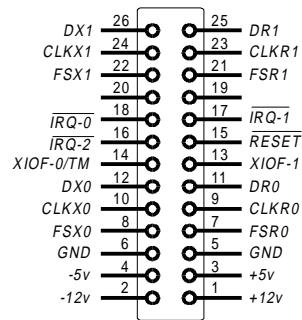
Fig.2-12. SIOX connector pinout (top view).

Table 2-12. SIOX signal specification.

SIOX signal name	signal type	description
SIO-0 port control		
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX site. For SIOX-A site of *TORNADO-54x* DSP systems these signals correspond to the TMS320C54x DSP on-chip BSP serial port transmitter and are wired directly to pins *BDX, BFSX, BCLKX* of TMS320C54x DSP. For SIOX-B site of *TORNADO-54x* DSP systems these signals might be configured by on-board jumpers to connect to the transmitter of any of the TMS320C54x DSP on-chip BSP/TDM/BSP1 serial ports.
DR0 FSR0 CLKR0	I I I	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX site. For SIOX-A site of *TORNADO-54x* DSP systems these signals correspond to the TMS320C54x DSP on-chip BSP serial port receiver and are wired directly to pins *BDR, BFSR, BCLKR* of TMS320C54x DSP. For SIOX-B site of *TORNADO-54x* DSP systems these signals might be configured by on-board jumpers to connect to the receiver of any of the TMS320C54x DSP on-chip BSP/TDM/BSP1 serial ports.
SIO-1 port control		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX site. For SIOX-A site of *TORNADO-54x* DSP systems these signals correspond to the TMS320C54x DSP on-chip TDM serial port transmitter and are wired directly to pins *TDX, TFSX, TCLKX* of TMS320C54x DSP. For SIOX-B site of *TORNADO-54x* DSP systems these signals might be configured by on-board jumpers to connect to the transmitter of any of the TMS320C54x DSP on-chip BSP/TDM/BSP1 serial ports.
DR1 FSR1 CLKR1	I I/O I	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX site. For SIOX-A site of *TORNADO-54x* DSP systems these signals correspond to the TMS320C54x DSP on-chip TDM serial port receiver and are wired directly to pins *TDR, TFSR, TCLKR* of TMS320C54x DSP. For SIOX-B site of *TORNADO-54x* DSP systems these signals might be configured by on-board jumpers to connect to the receiver of any of the TMS320C54x DSP on-chip BSP/TDM/BSP1 serial ports.

Timers/IO, DSP Reset and Interrupt Requests		
XIOF-0/TM	I/O/Z	Configured by on-board J3 jumper as either *XIOF-0* I/O flag from TMS320C54x DSP IOX area or DSP on-chip timer output (TM). If J3 jumper is in the 2-3 state (see fig.A-1), then this pin is configured as *XIOF-0* I/O flag, then it can be configured by DSP as input or output general purpose pin. If J3 jumper is in the 1-2 state, then this pin is configured as DSP on-chip timer output, i.e. it wires non-buffered DSP on-chip timer pin signal to this connector pin.
XIOF-1	I/O/Z	*XIOF-1* I/O flag from TMS320C54x DSP IOX area. It can be configured by DSP as input or output general purpose pin.
$\overline{RESET}$	O	Reset signal ($\overline{RESET}$ =0) for TMS320C54x DSP.
$\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, $\overline{IRQ\text{-}2}$	I	Hardware interrupt request lines ($\overline{IRQ\text{-}0}$ has the highest priority) for the on-board TMS320C54x DSP chip. Both static and one-shot (with the pulse length longer than 50 ns) are supported. Actual hardware interrupt requests (*INT0...INT2*) will be generated on the falling edge (1→0) of $\overline{IRQ\text{-}0}$ .. $\overline{IRQ\text{-}2}$ signals.
Power Supplies		
GND		Ground.
+5v		+5v power (from ISA-bus).
+12v		+12v power (from ISA-bus).
-5v		-5v power (from ISA-bus).
-12v		-12v power (from ISA-bus).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
1. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

Correspondence between SIO-0/SIO-1 ports of SIOX-A site and TMS320C54x DSP on-chip BSP/TDM serial ports

SIOX-A site of *TORNADO-54x* provides fixed connection of SIO-0 port of SIOX-A site to the TMS320C54x DSP on-chip BSP port and fixed connection of SIO-1 port of SIOX-A site to the TMS320C54x DSP on-chip TDM port.

Correspondence between SIO-0/SIO-1 ports of SIOX-B site and TMS320C54x DSP on-chip BSP/TDM/BSP1 serial ports

SIOX-B site of *TORNADO-54x* DSP systems provides flexible wiring of SIO-0 and SIO-1 ports to the TMS320C54x DSP on-chip BSP/TDM serial ports (BSP/TDM/BSP1 serial ports for *TORNADO-548/549*). This delivers flexibility in selection of the DSP serial ports for application, simplifies software design and allows simultaneous installation of two SIOX daughter card modules onto *TORNADO-54x* board, most of which utilize only SIO-0 serial port of SIOX interface.

Configuring SIO-0/SIO-1 ports of SIOX-B site for TORNADO-542L

Selection between SIO-0/1 ports of SIOX-B site and TMS320C542 DSP on-chip BSP/TDM serial ports for *TORNADO-542L* DSP system is performed by means of on-board jumper array J4 (see fig.2-13a). Only two combinations are available: "direct"-wiring (BSP->SIO-0, TDM->SIO-1) and "cross"-wiring (TDM->SIO-0, BSP->SIO-1).
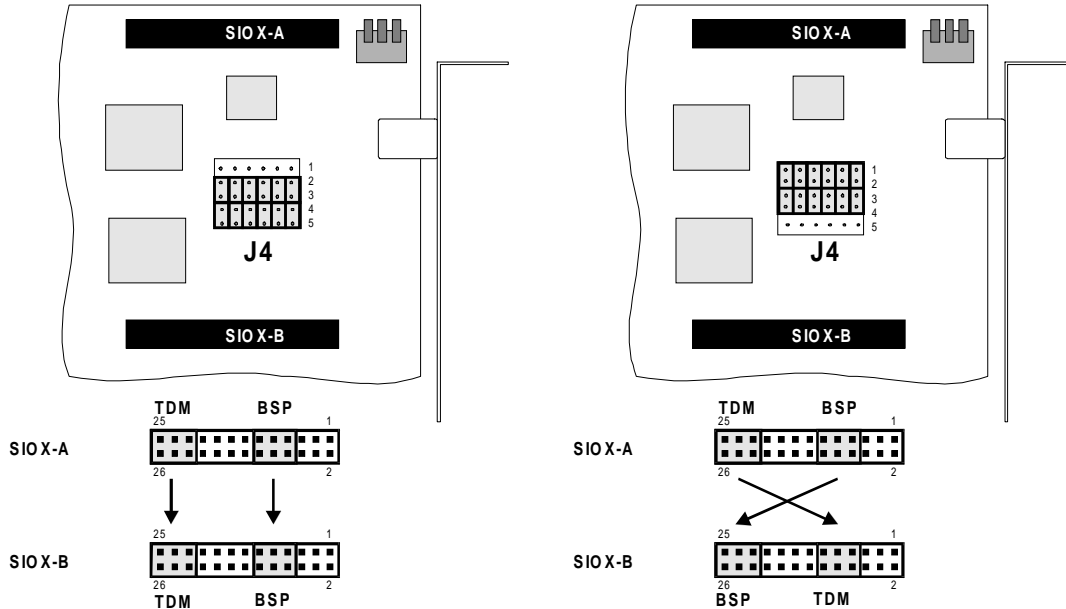
Fig. 2-13a. "Direct" (A) and "cross" (B) wiring configurations of SIO-0/1 ports for SIOX-B site for
TORNADO-542L.

Configuring SIO-0/SIO-1 ports of SIOX-B site for TORNADO-548/549

In *TORNADO-548/549* DSP system selection between SIO-0/1 ports of SIOX-B site and TMS320LC548/VC549 DSP on-chip BSP/TDM/BSP1 serial ports is performed by means of on-board jumper arrays J4-A and J4-B (see fig.2-13b). Independent configurations for SIO-0 (using J4-A jumper array) and SIO-1 (using J4-B jumper array) ports are supported, i.e. each of SIO-0/1 ports can connect to any of the TMS320LC548/VC549 DSP on-chip BSP/TDM/BSP1 serial ports. This delivers more flexibility than that with *TORNADO-542L* DSP system.
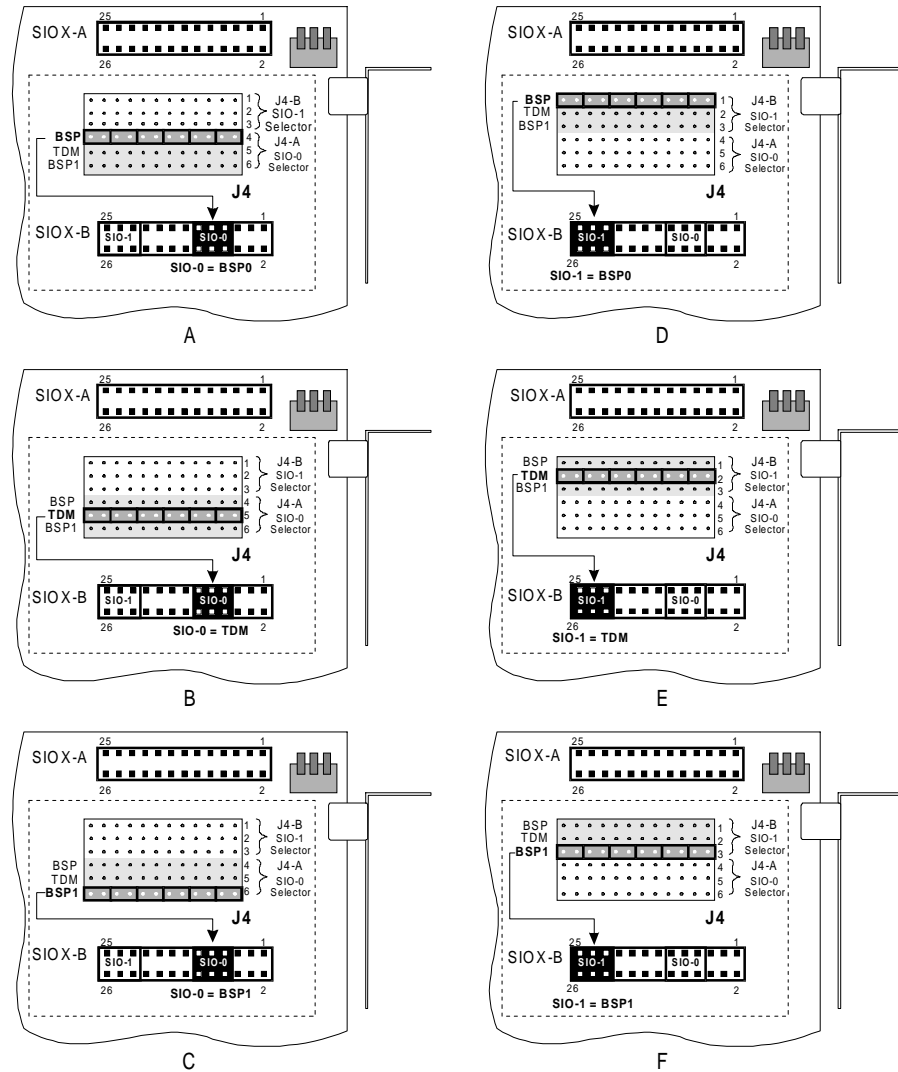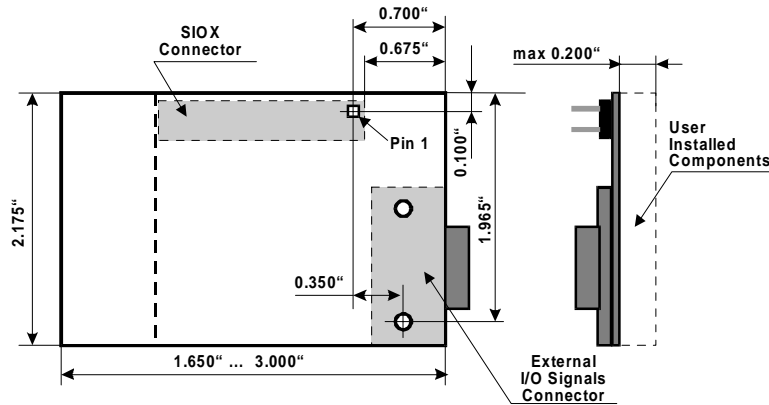
Fig. 2-13b. Configurations of SIO-0/1 ports for SIOX-B site for *TORNADO-548/549*.

Physical Dimensions for SIOX Daughter-card Modules

Physical dimensions for SIOX daughter-card module are presented at fig.2-14. This information is intended for those *TORNADO* customers, who need to design customized SIOX daughter-card modules.

Fig.2-14.   Physical dimensions for SIOX daughter-card modules.

2.8   Scan-path Emulation Tools for *TORNADO-54x*

TORNADO-54x uses scan-path emulation technique for the on-board TMS320C54x DSP in order to debug resident TMS320C54x DSP environment and software. Compatible scan-path emulation tools, which can be used with *TORNADO-54x* are as the following:

- TI XDS510 and MicroLAB' *MIRAGE-510D* universal scan-path emulators
- low cost emulation controller chip (*ECC*) for *TORNADO-542L*, which plugs into the dedicated on-board socket on *TORNADO-542L* mainboard
- low cost emulation control daughter card module (*UECM*) for *TORNADO* DSP systems, which plugs into the dedicated site on *TORNADO-548/549*. The *UECM* converts *TORNADO-548/549* DSP system into universal emulator for all TI TMS320 DSP if used with optional external buffer pod.

Using TI XDS510 and MicroLAB' MIRAGE-510D emulator with TORNADO-548/549

If TI XDS510 or MicroLAB' *MIRAGE-510D* universal scan-path emulator is used for debugging the *TORNADO-548/549* on-board TMS320LC548/VC549 DSP environment, then this emulator should connect to the dedicated on-board JTAG-IN connector on *TORNADO-548/549* mainboard (see fig. 2-2, fig. A-1 and fig. 2-15).
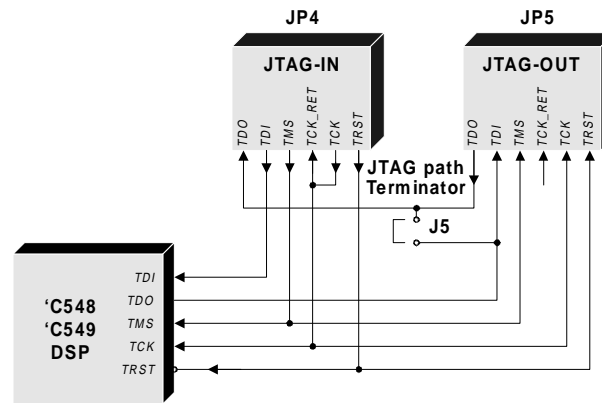
Fig. 2-15. On-board JTAG scan-path for *TORNADO-548/549*.

The on-board JTAG-OUT connector should be used once another JTAG device(s) is(are) included in the same JTAG path 'after' *TORNADO-548/549* board. In this case, the succeeding JTAG device should connect to JTAG-OUT connector of *TORNADO-548/549* using JTAG EXTENSION CABLE in the daisy-chain manner. Last JTAG device should terminate JTAG path and return JTAG *TDO* signal back to the emulator, which is connected to the first JTAG device in JTAG path.

CAUTION

The *TORNADO-548/549* on-board J5 jumper is used for termination of JTAG path on *TORNADO-548/549*.

J5 jumper should set to ON (installed) once *TORNADO-548/549* is either the only or the last JTAG device in JTAG path.

J5 jumper should set to OFF (removed) once two or more JTAG devices are included into JTAG path, and *TORNADO-548/549* is not the last JTAG device in JTAG path.

CAUTION

In case *TORNADO-548/549* is used with other JTAG devices connected to the JTAG-OUT connector, then the succeeding JTAG devices should use the JTAG default *TCK* clock source, which outcomes from the JTAG-OUT connector of *TORNADO-62/67*.

Using TI XDS510 and MicroLAB' MIRAGE-510D emulator with TORNADO-542L

If TI XDS510 or MicroLAB' *MIRAGE-510D* universal scan-path emulator is considered for debugging the *TORNADO-542L* on-board TMS320C542 DSP environment, then this emulator should connect to the dedicated on-board JTAG (JTAG-IN) connector on *TORNADO-542L* mainboard (see fig.2-2 and fig.A-1).


CAUTION

JTAG path of *TORNADO-542L* for connection of external TI XDS510 or MicroLAB' *MIRAGE-510D* emulators includes only one JTAG (JTAG-IN) connector (see fig.2-2 and fig. A-1), and there is no dedicated JTAG 'multiprocessor-chaining' hardware (JTAG-OUT connector and JTAG path terminator) on *TORNADO-542L*.

When external emulator connects to JTAG connector on *TORNADO-542L* board, then JTAG 'multiprocessor-chain' mode is not allowed as standard with this JTAG connection.

Should the user consider to use *TORNADO-542L* in JTAG 'multiprocessor-chain' mode with external JTAG emulator, then optional external JTAG-path IN/OUT splitter is required. Call MicroLAB Systems for details.

CAUTION

If TI XDS510 or MicroLAB' *MIRAGE-510D* universal scan-path emulator is being used with *TORNADO-542L*, then the emulation controller chip (*ECC*) should be switched off.

Using ECC and UECM for emulation the on-board TMS320C54x DSP

Both *ECC* and *UECM* are low cost replacements for XDS510 and *MIRAGE-510D* emulators and run under identical industry standard GoDSP TMS320C54x Code Composer IDE.

Emulation control chip (*ECC*) installs into the dedicated socket on *TORNADO-542L* mainboard, whereas *UECM* emulation control daughter card module installs into the dedicated daughter card site onto *TORNADO-548/549* mainboard.

Once *ECC* and *UECM* are used, then there is no need to connect external XDS510 and *MIRAGE-510D* emulators to the *TORNADO-548/549* on-board JTAG or JTAG-IN connectors.

CAUTION

Since J5 JTAG path terminating jumper is included into the *TORNADO-548/549* on-board JTAG path, then you have to follow the same instructions for setting J5 jumper in case the UECM daughter-card module is installed (see the corresponding subsection earlier in this section).

Using UECM for emulation external TI TMS320 DSP

UECM converts *TORNADO-548/549* into universal scan-path emulator for any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP. This optional external MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x) pod attached to *UECM*. The MPSD and JTAG pods are the pods used with MicroLAB' *MIRAGE-510D* emulator. The debuggers used for debugging external TI TMS320 DSP are the TI HLL Debuggers and GoDSP Code Composer IDE.

2.9   Software Development Tools

TMS320C54x DSP is now an industry standard DSP and is supported by a variety of software development tools from multiple 3rd party vendors.

Compilers and Debuggers

Software development for *TORNADO-54x* is supported by TI TMS320C54x DSP Optimizing C Compiler and Assembly Language Tools.

Debugging of TMS320C54x DSP resident software for *TORNADO-54x* is supported by TI HLL Debugger (*www.ti.com*) and TMS320C54x Code Composer IDE from GoDSP Corp (*www.go-dsp.com*). Both debuggers require either on-board optional emulation controller chip (*ECC*) installed for *TORNADO-542L* or *UECM* emulation control daughter-card module installed for *TORNADO-548/549*, which may ship together with *TORNADO-54x* DSP system.

Real-time Multitasking Operating Systems (RTOS)

TORNADO-54x is supported by multiple RTOS that provide multitasking capabilities:
- *VIRTUOSO* from Eonic Systems Inc (*www.eonic.com*) is an industry standard high-performance RTOS and provides full feature multitasking support. It comes standard with capabilities for host file, keyboard and screen text/graphics I/O from DSP environment via *TORNADO-54x* host ISA-bus interface, and is available with a wide selection of function libraries for DSP, math, matrix, 2D, etc. computations.
- *NUCLEUS PLUS* from Accelerated Technology Inc (*www.atinucleus.com*) is an industry standard single-processor high-performance RTOS and provides full feature multitasking support. It features low cost and comes standard with source codes. Available options include *NUCLEUS FILE*, *NUCLEUS NET*, and *NUCLEUS DBUG+* that also come in source codes.

- *SPOX* from Spectron Microsystems Inc (*www.spectron.com*) is an industry standard RTOS for DSP that provides multitasking support. It is available with a selection of function libraries for DSP, math, matrix, etc. computations.

Application Software Tools for TORNADO-54x

Application specific tools for *TORNADO-54x* DSP system include a variety of function libraries for DSP, math, vector, image, etc computation, as well as function libraries for vocoder/fax/modem applications and audio multimedia.

Chapter 3. Installation and Configuration

This chapter includes instructions for configuring and installation of *TORNADO-54x* DSP system into host ISA-bus PC.

3.1   Setting I/O Base Address for Host ISA-bus I/O Interface

You have to setup ISA-bus I/O base address for host ISA-bus I/O interface of *TORNADO-542L* prior installation of *TORNADO-54x* board into ISA-bus slot of host PC. This procedure should be done while host PC power is switched off.

I/O base address for host ISA-bus I/O interface of *TORNADO-54x* is configured by means of on-board DIP-switch SW1 (see fig.2-2 and fig.A-1) in accordance with configuration setting in table 2-4.

> **CAUTION**
>
> When setting I/O base address for host ISA-bus I/O interface be sure to check I/O base address for other hardware installed in your host PC in order to avoid I/O address conflicts on ISA-bus.

TORNADO-54x is shipped from factory with I/O base address for host ISA-bus I/O interface in accordance with default settings from table 2-4.

3.2   Setting Interrupt Request Line for Host PC

Setting of host PC interrupt request line is optional procedure for *TORNADO-54x* and should be performed in accordance with requirements of application software that you use together with *TORNADO-54x*. This procedure should be done while host PC power is switched off.

Setting of host PC interrupt request line is provided via on-board host PC interrupt request jumper J1 (see fig.2-2 and fig.A-1). See section 2.5 for details about *TORNADO-54x* host PC interrupt support. *TORNADO-54x* is shipped from factory without PC interrupt request jumper installed.

CAUTION

When setting host CPU interrupt request line be sure to check interrupt requests for other
hardware installed in your host PC in order to avoid interrupt request conflicts on ISA-bus.

3.3   Installation of *TORNADO-54x* Mainboard into Host PC

After I/O base address for host ISA-bus I/O interface of *TORNADO-54x* has been configured and host PC
interrupt request line has been setup, you can now install *TORNADO-54x* board into 16-bit ISA-bus slot of
host PC and screw on-board *TORNADO-54x* mounting bracket to rear panel of host PC. Afterthat, you can
safely switch on power of host PC and load operating system of your PC.

3.4   Setting Memory Base Address for Host ISA-bus Memory Interface

After *TORNADO-54x* has been installed into host PC, the PC power has been switched on, and DOS has been
loaded, you can proceed with configuring ISA-bus memory base address for host ISA-bus memory interface of
TORNADO-54x.

It is recommended to use *T54CC.EXE* software utility for configuring ISA-bus memory base address for host
ISA-bus memory interface of *TORNADO-54x* at DOS prompt.

Setting host PC software environment for accessing host ISA-bus memory interface of TORNADO-54x

Prior you will start working with *TORNADO-54x* host ISA-bus memory interface, you have to configure host
PC software environment in order it can properly communicate with host ISA-bus memory interface of
TORNADO-54x.

If memory base address of *TORNADO-54x* host ISA-bus memory interface should be set to *D8000H* hex
value, then this requires including the following line into CONFIG.SYS file of host DOS or WINDOWS
operating system:

Device=C:\DOS\EMM386.EXE noems x=D800-DFFF

or

Device=C:\WINDOWS\EMM386.EXE noems x=D800-DFFF

The "*x=D800-DFFF*" option for the *EMM386.EXE* memory driver informs *EMM386.EXE* memory driver to
reserve the *D8000H..DFFFFH* UMB area, so it will might be used for communication with *TORNADO-54x*
host ISA-bus memory interface.

Should you need to setup different memory base address of *TORNADO-54x* host ISA-bus memory interface in accordance with table 2-3, then you should setup appropriate "*x=*" option for *EMM386.EXE* memory driver in CONFIG.SYS file. Please refer to documentation for DOS and WINDOWS operating system for details.

Setting memory base address for host ISA-bus memory interface in TORNADO-54x

You have to invoke *T54CC.EXE* software utility with *-imXXXXX* command line option in order to setup ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-542L* at DOS prompt in accordance with table 2-3.

The following example sets *D8000H* memory base address for host ISA-bus memory interface of *TORNADO-54x*:

<p align="center">T54CC -imD8000</p>

In case I/O base address of host ISA-bus I/O interface of *TORNADO-54x* differs from default value specified in table 2-4, then you have also specify *-ipXXX* command line option (where *XXX* denotes I/O base address of host ISA-bus I/O interface for *TORNADO-54x*) in DOS command line when invoking *T54CC.EXE* software utility. The following example demonstrates how to invoke *T54CC.EXE* software utility for *TORNADO-54x* DSP system with I/O base address for host ISA-bus I/O interface being configured to 300H value:

<p align="center">T54CC -imD8000 -ip300</p>

Switching Off host ISA-bus memory interface of TORNADO-54x

The following example demonstrates how to switch off host ISA-bus memory interface of *TORNADO-54x* DSP system:

<p align="center">T54CC -im0</p>

CAUTION

When setting memory base address for host ISA-bus memory interfaces be sure to check memory base address for other hardware installed in your host PC in order to avoid memory address conflicts on ISA-bus.

3.5 Installation of Emulation Controller (ECC) onto *TORNADO-542L* Mainboard

Installation of emulation controller chip (*ECC*) onto *TORNADO-542L* board should be performed while host PC power off.

Installation of ECC

In order to install emulation controller chip (*ECC*) onto *TORNADO-542L* board follow recommendations below (see fig. 3-1):

- switch off power of host PC
- remove *TORNADO-542L* board from host PC ISA-bus slot
- take *ECC* by your fingers in such way that its front (labeling) surface is turned at you
- adjust *ECC* to be parallel to surface of the corresponding PLCC-44 socket on *TORNADO-542L* board
- orient *ECC* in such way, that the key corner of its PLCC-44 package would match the corresponding corner of on-board PLCC-44 socket
- safely insert *ECC* into on-board PLCC-44 socket
- safely plug and fix *ECC* in the on-board PLCC-44 socket
- install *TORNADO-542L* into 16-bit ISA-bus slot of host PC
- switch on power of host PC
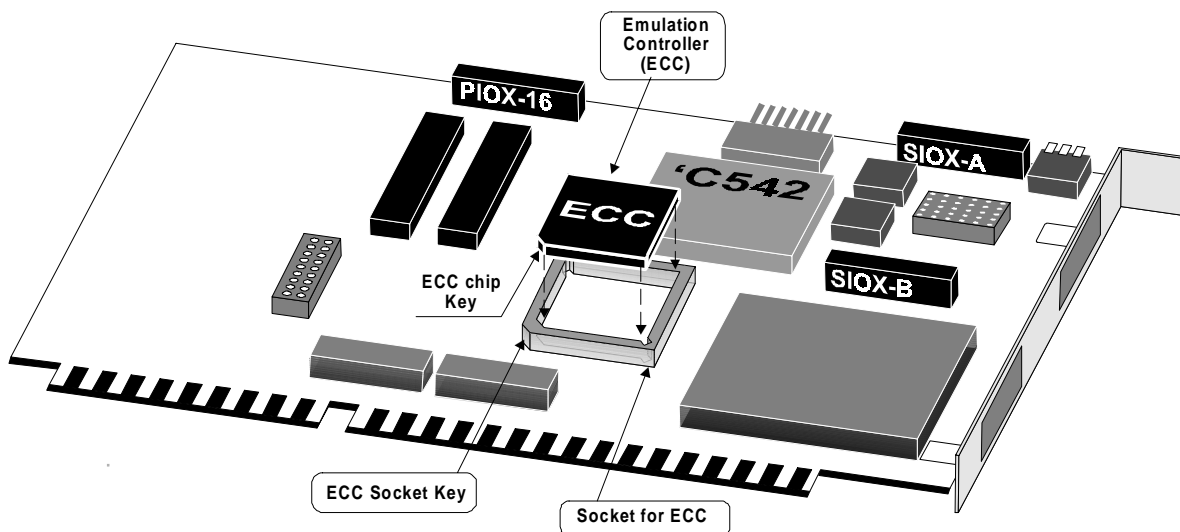
Fig.3-1.   Installation of emulation controller chip (*ECC*) onto *TORNADO-542L* board.

Setting I/O Base Address for ECC

You have to invoke *T54CC.EXE* software utility with *-epXXX* command line option in order to setup ISA-bus I/O base address for *ECC* at DOS prompt in accordance with table 2-10.

The following example sets *240H* I/O base address for *ECC*:

T54CC -ep240

In case I/O base address of host ISA-bus I/O interface of *TORNADO-542L* differs from default value specified in table 2-4, then you have also specify *-ipXXX* command line option (where *XXX* denotes I/O base address of

host ISA-bus I/O interface for *TORNADO-542L*) in DOS command line when invoking *T54CC.EXE* software utility. The following example demonstrates how to invoke *T54CC.EXE* software utility for *TORNADO-542L* DSP system with I/O base address for host ISA-bus I/O interface being configured to 300H value:

<div align="center">

T54CC -ep240 -ip300

</div>

Switching ECC Out from ISA-bus I/O Address Space

The following example demonstrates how to switch *ECC* out from ISA-bus I/O address space:

<div align="center">

T54CC -ep0

</div>

CAUTION

When setting I/O base address for *ECC* be sure to check I/O base address for other hardware installed in your host PC in order to avoid I/O address conflicts on ISA-bus.

3.6   Installation of *UECM* Daughter-Card Module onto *TORNADO-548/549* Mainboard

You have to install *UECM* module as a daughter-card module (see fig.1-1) into the dedicated on-board connector of *TORNADO-548/549* mainboard (see fig.2-2 and fig.A-1).

CAUTION

Once you install the *UECM* daughter card module onto the *TORNADO-548/549* mainboard, you cannot use SIOX-B site for installation of SIOX AD/DA/DIO daughter-card modules.

In order to install *UECM* module onto *TORNADO-548/549* mainboard you have to follow the instructions below (see fig.3-2):

- slant *UECM* module
- insert the on-module connector for active buffer pod into the corresponding hole in the *TORNADO-548/549* mounting bracket
- plug in the *UECM* male header into the dedicated female connector on *TORNADO-548/549* mainboard
- setup the ISA-bus I/O base address for the *UECM* module using the on-module DIP-switch in accordance with the "*UECM/ECC* User's Guide".
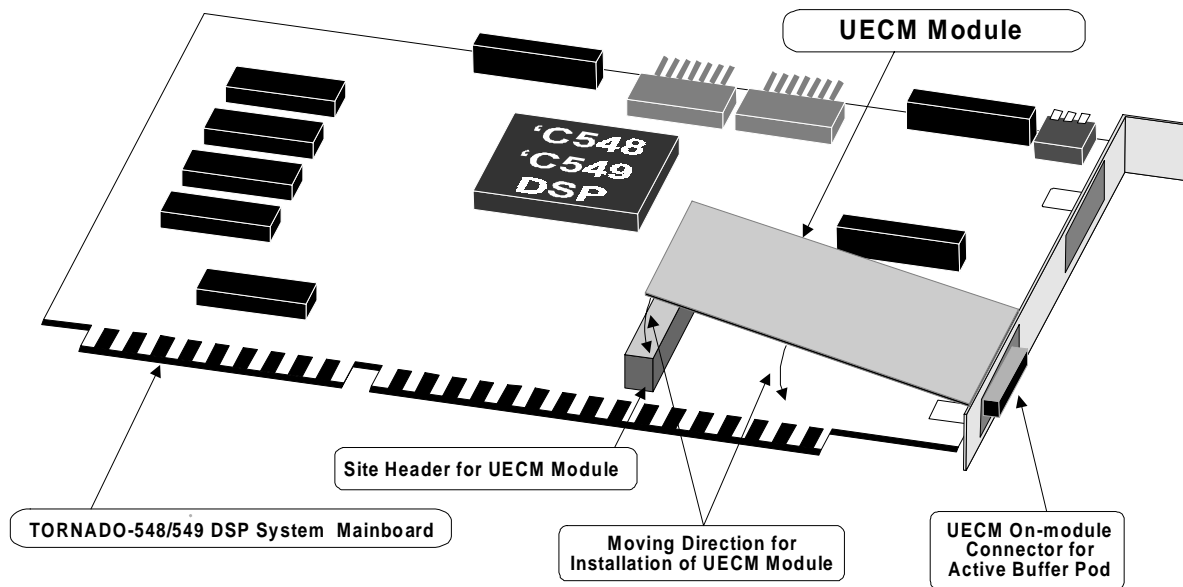
Fig.3-2.   Installation of *UECM* daughter card module onto *TORNADO-548/549* mainboard.

The *UECM* can connect both to the on-board TMS320LC548/VC549 DSP and any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP via optional external buffer pod.

Configuring UECM to connect to the on-board TMS320LC548/VC549 DSP JTAG path

After power-on, the *UECM* is connect to the on-board TMS320LC548/VC549 DSP JTAG path. You do not need to use any external JTAG pod for this configuration.

CAUTION

When using the *UECM* daughter card module to emulate the on-board
TMS320LC548/VC549 DSP, be sure to set properly the on-board JTAG path terminator
jumper J5 in accordance with figure 2-15.

If you want to setup this connection again, you should use the *T54CC.EXE* software utility with '*-ei*' command line option. If *UECM* is allocated at the I/O base address that differs from the 240H I/O base address, then use '*-epXXX*' command line option for specifying the I/O base address for *UECM* (default is the '*-ep240*' configuration).

The following command line configures the *UECM*, which is allocated at the 280H I/O base address, to connect to the on-board TMS320LC548/VC549 DSP JTAG path:

T54CC -ei -ep280

Using UECM for emulation of external TMS320 DSP

If you want to use *UECM* to emulate any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP, you have to use optional MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x) external buffer pod for connection between the *UECM* and external TMS320 DSP.

In order to configure the *UECM* to connect to external TMS320 DSP, you can use the *T54CC.EXE* software utility with '*-EX*' command line option and the '*-epXXX*' command line option for specifying the I/O base address for *UECM* (default is the '*-epXXX*' configuration).

The following command line configures the *UECM* (allocated at the 280H I/O base address) to connect to external TMS320 DSP via optional external buffer MPSD or JTAG pod:

T54CC -ex -ep280

Chapter 4.   Utility Software

This chapter contains description of utility software for *TORNADO-54x* DSP system.

4.1   *T54CC.EXE* Control Center Utility

T54CC.EXE ("*TORNADO-54x* Control Center") utility is a DOS command line control tool for *TORNADO-54x* that delivers simple and powerful user control for *TORNADO-54x* hardware. *T54CC.EXE* utility features the following functionality:

- display and set all registers of *TORNADO-54x* host ISA-bus I/O interface
- read/write from/to on-board SRAM (Program/Data memory areas) and PIOX-16 I/O area via *TORNADO-54x* host ISA-bus memory interface
- access to the HPI port of TMS320C54x DSP
- configure the *ECC* emulation controller for *TORNADO-542L* and *UECM* emulation control daughter card module for *TORNADO-548/549.*

T54CC.EXE utility should be invoked from DOS with up to ten command line options specified:

<p align="center">T54CC [-option1] [-option2] [-option3] ...</p>

Each command line option corresponds to specific *TORNADO-54x* hardware control operation. The following is a list of available command line options for *T54CC.EXE* utility.

System Control via CONTROL REGISTER

-c	Display and interpret contents of *CONTROL REGISTER*.
-cg	Display current state of *SB_GLOCK* bit (global SB locking by host ISA-bus memory interface) of *CONTROL REGISTER*.
-cg0	Clear *SB_GLOCK* bit of *CONTROL REGISTER* and unlock SB.
-cg1	Set *SB_GLOCK* bit of *CONTROL REGISTER* for immediate active SB locking.
-cl	Display current state of *SB_LOCK* bit (SB locking by host ISA-bus memory interface) of *CONTROL REGISTER*.
-cl0	Clear *SB_LOCK* bit of *CONTROL REGISTER* and unlock SB.
-cl1	Set *SB_LOCK* bit of *CONTROL REGISTER* and issue active SB locking during nearest SB access from host ISA-bus memory interface.
-cie	Display current state of *SB_ERROR_IE* bit (host interrupt enable on SB error) of *CONTROL REGISTER*.
-cie0	Clear *SB_ERROR_IE* bit of *CONTROL REGISTER* and disable host interrupts on SB error.
-cie1	Set *SB_ERROR_IE* bit of *CONTROL REGISTER* and enable host interrupts on SB error.

-cim	Display current state of *MH_RQ_IE* bit (host interrupt enable on requests from TMS320C54x DSP) of *CONTROL REGISTER*.
-cim0	Clear *MH_RQ_IE* bit of *CONTROL REGISTER* and disable host interrupts on requests from TMS320C54x DSP.
-cim1	Set *MH_RQ_IE* bit of *CONTROL REGISTER* and enable host interrupts on requests from TMS320C54x DSP.
-cr	Display current state of reset signal for TMS320C54x DSP, which is specified by *M_GO* bit of *CONTROL REGISTER*.
-cr0	Remove reset signal for TMS320C54x DSP, i.e. put DSP into "RUN" state. This option sets *M_GO* bit of *CONTROL REGISTER*.
-cr1	Apply reset signal for TMS320C54x DSP, i.e. put DSP into "RESET" state. This option clears *M_GO* bit of *CONTROL REGISTER*.

Flag Registers Control

-fsr	Display contents of *FLAG SELECTOR REGISTER*.
-fsrXX	Select flag register #*XX (hex)*, i.e. load *XX* 8-bit hex data into *FLAG SELECTOR REGISTER*.
-fr	Display contents of currently selected flag register (display *FLAG STATUS REGISTER*). The number of currently selected flag register is defined by the contents of *FLAG SELECTOR REGISTER*.
-frXX	Loads *XX* 8-bit hex data into the currently selected flag register (load *FLAG CONTROL REGISTER*). The number of currently selected flag register is defined by the contents of *FLAG SELECTOR REGISTER*..
-frs	Display and interprete contents of *SYS_STATUS_FRG* flag register.
-fe	Display current state of *SB_ERROR* flag from *SYS_STATUS_FRG* flag register.
-fe0	Clear *SB_ERROR* flag, i.e. write to *CLEAR_SB_ERROR_FRG* flag register.
-fb	Display current state of *SB_ACK* flag from *SYS_STATUS_FRG* flag register.
-fh	Display current state of *MH_RQ* flag from *SYS_STATUS_FRG* flag register.
-fh0	Clear *MH_RQ* flag, i.e. write to *CLEAR_MH_RQ_FRG* flag register.
-fhh	Display current state of *HPI_HINT* DSP-to-host interrupt request via HPI from *SYS_STATUS_FRG* flag register.
-fhe	Display current state of *HPI_ERROR* flag from *SYS_STATUS_FRG* flag register.

-fhe0	Clear *HPI_ERROR* flag, i.e. write to *CLEAR_HPI_ERROR_FRG* flag register.
-fm1	Generate interrupt request to TMS320C54x DSP, i.e. write to *SET_HM_RQ_FRG* flag register.
-fhi	Display and interpret contents of *HPI_IE_FRG* flag register.
-fhie	Display current state of *HPI_ERROR_IE* bit (host interrupt enable on *HPI_ERROR*) of *HPI_IE_FRG* flag register.
-fhie0	Clear *HPI_ERROR_IE* bit of *HPI_IE_FRG* flag register and disable host interrupts on *HPI_ERROR*.
-fhie1	Set *HPI_ERROR_IE* bit of *HPI_IE_FRG* flag register and enable host interrupts on *HPI_ERROR*.
-fhih	Display current state of *HPI_HINT_IE* bit (host interrupt enable on *HPI_HINT*) of *HPI_IE_FRG* flag register.
-fhih0	Clear *HPI_HINT_IE* bit of *HPI_IE_FRG* flag register and disable host interrupts on *HPI_HINT*.
-fhih1	Set *HPI_HINT_IE* bit of *HPI_IE_FRG* flag register and enable host interrupts on *HPI_HINT*.
-frdi	Display *TORNADO-54x* device ID and s/n, i.e. display contents of *DEV_ID0_FRG* and *DEV_ID1_FRG* flag registers.

SB Access Control

-ba	Display contents of *SB PAGE MAPPER* register that defines *SMP* SB base address for host-to-SB access.
-balA@Z	Load *SB PAGE MAPPER* register with *SMP* SB base address that corresponds to *A* five digit hex SB address of 16-bit SB data word in *Z* SB area ('P' - for program area, 'D' - for data area, and 'I' - for I/O area).
-bdSA,EA@Z	Display 16-bit SB data. *SA* and *EA* parameters specify five digit hex SB starting and ending addresses for 16-bit SB data words correspondingly in *Z* SB area ('P' - for program area, 'D' - for data area, and 'I' - for I/O area). Final contents of *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *EA* address.
-bwA,XXXX@Z	Write 16-bit *XXXX* hex data word at *A* five digit hex SB address. *A* parameter defines SB address of 16-bit SB word in *Z* SB area ('P' - for program area, 'D' - for data area, and 'I' - for I/O area). *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *A* address. (see section 2.4)

HPI Access Control

-hc	Display and interprete contents of HPIC register of TMS320C542 DSP.

-hch0	Clear *HINT* bit of HPIC register (DSP-to-host interrupt request via HPI) of TMS320C54x DSP.
-hcd1	Set *DSPINT* bit of HPIC register (host-to-DSP interrupt request via HPI) of TMS320C54x DSP.
-hdSA,EA	Display HPI shared memory data of TMS320C54x DSP within the *SA...EA* hex HPI address range.
-hwA,XXXX	Write 16-bit *XXXX* hex data word at *A* hex HPI shared memory address of TMS320C54x DSP.

Setting I/O and Memory Base Addresses for Host ISA-bus Interface

-im	Display ISA-bus memory base for host ISA-bus memory interface of *TORNADO-54x* in accordance with table 2-3 (display and interpret contents of *ISA_MI_BADDR_FRG* flag register).
-imXXXXX	Set *XXXXX* hex ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-54x* in accordance with table 2-3 (load *ISA_MI_BADDR_FRG* flag register). If *T54CC.EXE* utility is invoked with *-bd* or *-bw* command line options and option *-im* is not specified (or *ISA_MI_BADDR_FRG* flag register was not loaded previously), then the default *D8000H* ISA-bus memory base address will be used for host ISA-bus memory interface during host-to-SB access, and option *-im0* will be automatically executed on exit from *T54CC.EXE* utility in order to deactivate host ISA-bus memory interface afterthat.
-im0	Deactivates host ISA-bus memory interface of *TORNADO-54x*, i.e. removes it from ISA-bus memory address on exit from *T54CC.EXE* utility.
-ipXXX	Specifies *XXX* hex I/O base address for host ISA-bus I/O interface. If this option is omitted, then default factory setting in accordance with table 2-4 will is used.

Control for Emulation Controller (ECC) and Emulation Daughter-card Module (UECM)

-ep	Display current ISA-bus I/O base for *ECC* for *TORNADO-542L* in accordance with table 2-10 (display and interpret contents of *ISA_ECC_IO_BADDR_FRG* flag register).
-epXXX	Set *XXX* hex I/O base address for *ECC* for *TORNADO-542L* in accordance with table 2-10 and activate it, i.e. include ECC into ISA-bus I/O address space and connect it to scan-path interface of TMS320C542 DSP. For *TORNADO-548/549* with *UECM* installed, this option specified the I/O base address for *UECM*. Once *T54CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB' MIRAGE-510D emulator is not allowed for

	TORNADO-542L unless *T54CC.EXE* utility will be invoked with *-ex* command line option.
-ei	Set default I/O base address for *ECC* for *TORNADO-542L* in accordance with table 2-10 and activate *ECC*, i.e. include ECC into ISA-bus I/O address space and connect it to scan-path interface of TMS320C542 DSP. In case *D_OPTIONS* DOS system variable for TI TMS320C54x C Source Debugger is set and its list includes *-pXXX* option, then *XXX* hex I/O address will be used as default I/O base address for *ECC* instead of that in accordance with table 2-10. For *TORNADO-548/549* with *UECM* installed, this option configures *UECM* to connect to the on-board TMS320LC548/VC549 JTAG path. Once *T54CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB' MIRAGE-510D emulator is not allowed to *TORNADO-542L* and is ignored for *TORNADO-548/549* unless *T54CC.EXE* utility will be invoked with *-ex* command line option.
-ep0	Deactivates *ECC* controller for *TORNADO-542L*, i.e. remove *ECC* from ISA-bus I/O address space and disconnect it from scan-path interface of TMS320C542 DSP. Once *T54CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB' MIRAGE-510D emulator is allowed to *TORNADO-542L*.
-ex	For *TORNADO-542L* this option is identical to '*-ep0*' command line option, i.e. it removes *ECC* from ISA-bus I/O address space and disconnects it from scan-path interface of on-board TMS320C542 DSP. For *TORNADO-548/549* with *UECM* installed this option configures *UECM* to connect to external TMS320 DSP via optional MPSD or JTAG pod. Once *T54CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB' MIRAGE-510D emulator is allowed to *TORNADO-54x*.
-er	Perform software reset of *ECC* or *UECM*. Recommended on invocation and exit from TI TMS320C54x HLL Debugger or GoDSP TMS320C54x Code Composer IDE.

Utility Options

-p	Set page-by-page display mode. The "ESC" keypress terminates display output whereas any other keypress results in the next page display.
-?	Display list of available options for *T54CC.EXE* utility program. Help list is also displayed when *T54CC.EXE* utility program is invoked without command line options.

T54CC.EXE utility processes command line options in accordance with the following priority list:
1. *CONTROL REGISTER* control options
2. *FLAG STATUS REGISTER* and *FLAG CONTROL REGISTER* control options
3. HPI control options
4. *ECC* control options

5. SB access control options.

T54CC.EXE utility returns DOS *exit code* in case it is invoked with *-im*, *-c*, *-cg*, *-cl*, *-cie*, *-cim*, *-fsr*, *-fr*, *-frs*, *-fe*, *-fb*, *-fh*, *-fhh, -fhe, -fhi, -fhie* and *-fhih* command line options, which correspond to display of contents of registers, bits and flags of *TORNADO-54x* host ISA-bus interface. The exit code returned corresponds to current value or contents of last displayed bit, bit field, flag or register. Exit code is useful when *T54CC.EXE* utility is integrated into DOS batch (.BAT) file that provides conditional processing. Exit code of *T54CC.EXE* utility program can be analyzed using succeeding '*IF ERRORLEVEL*' DOS batch file commands. The following example of DOS batch file performs conditional processing of *SB_ERROR* flag of *TORNADO-54x*:

```
              ...
              T54CC -fed
              IF ERRORLEVEL 1  T54CC -fe0

              ...
```

When multiple data display options for the *T54CC.EXE* utility are specified, then the returned exit code will correspond to the last processed data display command line option.

In case error is detected by *T54CC.EXE* utility, then the exit code '255' is returned. If *T54CC.EXE* utility is invoked without any data display command line options and no errors is detected, than the exit code '0' is returned.

4.2   Uploading TMS320C54x COFF-files via Host ISA-bus Memory Interface

Uploading of TI TMS320C54x COFF-files (output .OUT files from TI TMS320C54x C/Assembler compilers) into *TORNADO-54x* on-board SRAM/PIOX-16 areas and TMS320C54x DSP on-chip environment can be performed by means of *T54COFF.EXE* software utility, that is included with utility software for *TORNADO-54x*. *T54COFF.EXE* utility loads TI TMS320C54x COFF-file into *TORNADO-54x* environment via host ISA-bus memory interface without utilization of emulation controller *ECC* or *UECM* emulation control daughter card module.

COFF-file can be uploaded into the *TORNADO-54x* environment using different modes:
- *standard mode*, i.e. when data is uploaded to on-board SRAM/PIOX-16 areas via host ISA-bus memory interface without affecting TMS320C54x DSP chip reset line and SB locking
- *reset mode*, i.e. when data is uploaded to on-board SRAM/PIOX-16 areas and TMS320C54x DSP on-chip environment via host ISA-bus memory interface while holding TMS320C54x DSP in 'RESET' state
- *global SB locking mode*, i.e. when data is uploaded to on-board SRAM/PIOX-16 areas via host ISA-bus memory interface using global SB locking
- *SB locking mode*, i.e. when data is uploaded to on-board SRAM/PIOX-16 areas via host ISA-bus memory interface using the SB locking.

All modes except for *reset mode* provide uploading of COFF-file into SRAM/PIOX-16 areas only. However, these modes do not effect reset signal for TMS320C54x DSP, and data can be uploaded in parallel with TMS320C54x DSP running.

Reset mode provides uploading of COFF‑file into both on-board SRAM/PIOX-16 areas and TMS320C54x DSP on-chip environment (including DSP on-chip memory and peripherals). This is performed by means of using run-time TMS320C54x loader that is loaded into on-board SRAM and then removed automatically by *T54COFF.EXE* utility each time loader recognizes that COFF‑file data section should be loaded into the DSP on-chip resources.

Uploading of COFF‑file into *TORNADO-54x* is performed by invoking *T54COFF.EXE* utility from DOS command line:

<p style="text-align:center">*T54COFF   FILENAME[.OUT]* [-*option1*] [-*option2*] [-*option3*] ...</p>

If file extension is missed for source *FILENAME* COFF‑file, then .OUT extension is assumed. The following is list of command line options for *T54COFF.EXE* utility, which are grouped into several functional groups.

Upload Mode Control

-lr	Set *RESET* mode for uploading of COFF‑file. COFF‑file is uploaded while holding TMS320C54x DSP in 'RESET' state by means of clearing *M_GO* bit of *CONTROL REGISTER*. This mode is used for uploading of source program/data modules and supports uploading into both on-board SRAM/PIOX-16 areas and TMS320C54x DSP on-chip memory and peripherals. TMS320C54x DSP can be placed into the 'RUN' state on exit from *T54COFF.EXE* utility using *-cr0* command line option. The *-lr* option is assumed as default if none of *-lg*, *-ll* and *-ln* options is specified.
-lg	Set *GLOBAL SB LOCKING* mode for uploading of COFF‑file. COFF‑file is uploaded into on-board SRAM/PIOX-16 areas while holding SB locking by means of setting *SB_GLOCK* bit of *CONTROL REGISTER*. TMS320C54x DSP will not be able to access SRAM/PIOX-16 areas until uploading will be finished. TMS320C54x DSP on-chip resources cannot be loaded in this mode. This mode is normally used for uploading of shared data into on-board SRAM/PIOX-16 areas while TMS320C54x DSP is executing a program.
-ll	Set *SB LOCKING* mode for uploading of COFF‑file. COFF‑file is uploaded into on-board SRAM/PIOX-16 areas while holding SB locking by means of setting *SB_LOCK* bit of *CONTROL REGISTER*. TMS320C54x DSP will not be able to access SRAM/PIOX-16 areas until uploading will be finished. TMS320C54x DSP on-chip resources cannot be loaded in this mode. This mode is normally used for uploading of shared data into on-board SRAM/PIOX-16 areas while TMS320C54x DSP is executing a program.
-ln	Set *STANDARD* mode for uploading of COFF‑file. COFF‑file is uploaded without affecting 'RESET' state of TMS320C54x DSP and without SB locking. TMS320C54x DSP will be able to access on-board SRAM/PIOX-16 areas during uploading of COFF‑file. The on-board TMS320C54x DSP on-chip resources cannot be loaded during this mode. This mode is normally used for uploading of run-time program or data into on-board

SRAM/PIOX-16 areas while on-board TMS320C54x DSP chip is executing a program.

-xi   Exclude uploading of TMS320C54x DSP on-chip memory and peripherals when using *RESET* mode for uploading. This option should be used together with *-lr* option only.

-ovly   Assume that TMS320C54x DSP on-chip DARAM is mapped to program memory space. This option should be used together with *-lr* option only.

Restarting TMS320C542 DSP on Exit

-cr0   Restart TMS320C54x DSP on exit from *T54COFF.EXE* utility. This option corresponds to toggling *M_GO* bit from *CONTROL REGISTER*.

Viewing Directory of COFF-file

-d   List directory (sections loading information) for COFF-file. COFF-file will be not loaded into *TORNADO-54x* environment an all other command line options specified will be ignored.

Setting Base Addresses of ISA-bus Memory and I/O Interfaces

-imXXXXX   Set *XXXXX* hex ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-54x* in accordance with table 2-3 (load *ISA_MI_BADDR_FRG* flag register). If *T54CC.EXE* utility is invoked with *-bd* or *-bw* command line options and option *-im* is not specified (or *ISA_MI_BADDR_FRG* flag register was not loaded previously), then the default *D8000H* ISA-bus memory base address will be used for host ISA-bus memory interface during host-to-SB access, and option *-im0* will be automatically executed on exit from *T54CC.EXE* utility in order to deactivate host ISA-bus memory interface afterthat.

-im0   Deactivates host ISA-bus memory interface of *TORNADO-54x*, i.e. removes it from ISA-bus memory address on exit from *T54CC.EXE* utility.

-ipXXX   Specifies *XXX* hex I/O base address for host ISA-bus I/O interface. If this option is omitted, then default factory setting in accordance with table 2-4 will is used.

Utility Options

-?   Display list of available options for *T54COFF.EXE* utility. Help list is also displayed when *T54COFF.EXE* utility is invoked without command line options and parameters.

In case no errors are detected by *T54COFF.EXE* utility, then exit code '0' will be returned, otherwise exit code '1' will be generated.

CAUTION

If *T54COFF.EXE* utility is used with *-lr* command line option (or when *-lg*, *-ll* and *-ln* options are not specified) and if either emulation controller (*ECC*) or *UECM* emulation control daughter card module is installed or any of TI XDS510 or MicroLAB' *MIRAGE-510D* emulator is attached, then the following error message may appear:

error: missing DSP handshaking

This error message states that the TMS320C54x DSP cannot be initialized correctly during uploading of TMS320C54x DSP on-chip memory or peripherals. This problem is caused by DSP on-chip execution controller that is locked by attached emulator or *ECC/UECM*.

In order to avoid this problem you have to reset the *ECC/UECM* or attached emulator. The emulator can be reset using the supplied software reset utility, whereas *ECC/UECM* can be reset by invoking *T54CC.EXE* utility program with the *-er* command line option.

Appendix A.   On-board Jumpers and Connectors.

This Appendix includes a summarized description for the *TORNADO-54x* on-board configuration jumpers, connectors and switches.

The layout for the *TORNADO-54x* on-board configuration jumpers, connectors and switches is presented at fig.A-1. Fig.A-1a contains information for the *TORNADO-542L* layout, whereas fig.A-1b contains information for the *TORNADO-548/549* layout.
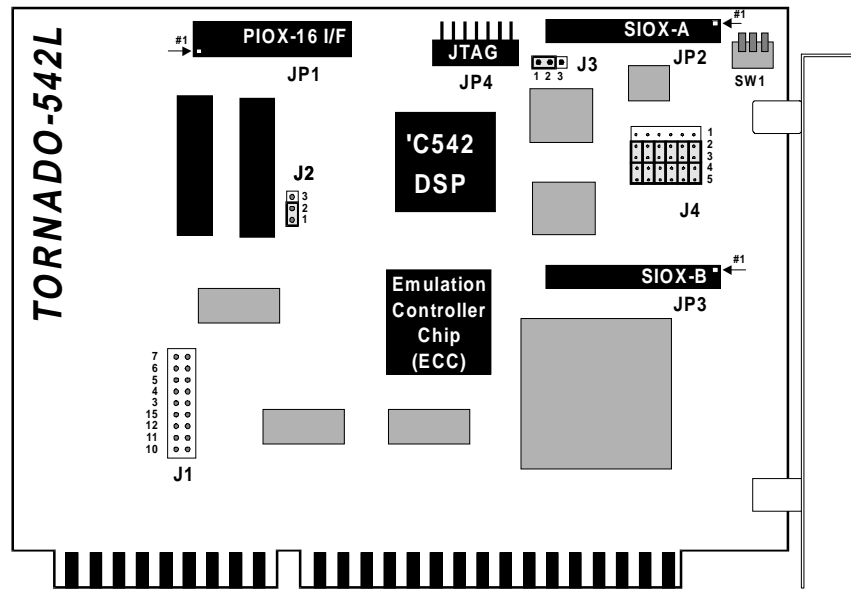

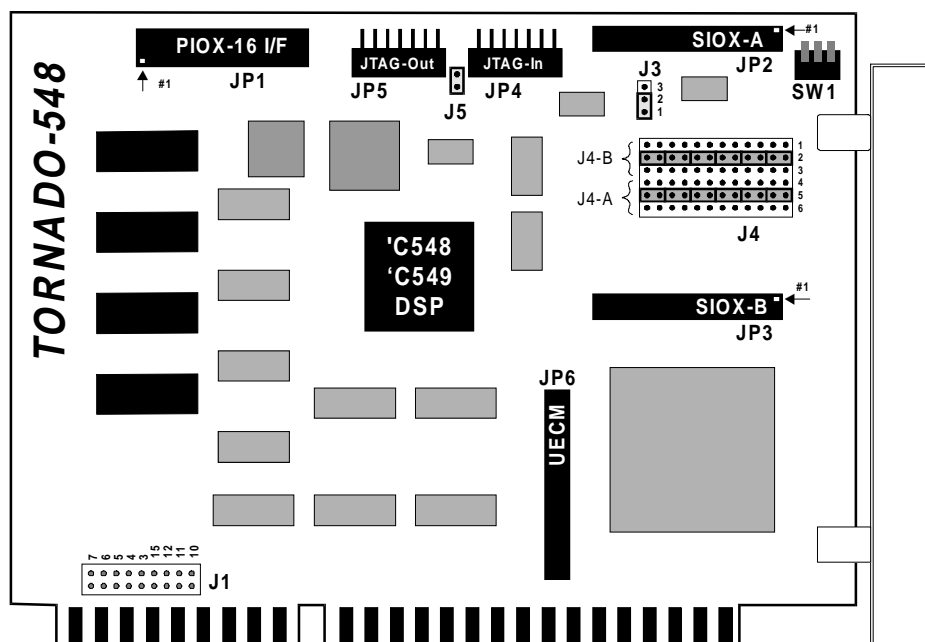*Fig.A-1a.* On-board layout for *TORNADO-542L*.

Fig.A-1b. On-board layout for *TORNADO-548/549*.

On-board Configuration Switches

All on-board configuration switches for *TORNADO-54x* DSP systems are summarized in table A-1.

Table A-1. On-board configuration switches for *TORNADO-54x*.

switch ID	switch function description	reference information
SW1	ISA -bus I/O base address for host ISA-bus I/O interface.	Section 2.5 and table 2-4.

On-board Configuration Jumpers

All on-board configuration jumpers for *TORNADO-54x* DSP systems are summarized in table A-2.

Table A-2.   On-board configuration jumpers for *TORNADO-54x*.

jumper ID	jumper function description	reference information
J1	Host ISA-bus interrupt request line selector.	Sections 2.6 and 3.2.
J2	SRAM DIP-chips type selector (*TORNADO-542L* only).	Section 2.2
J3	*XIOF-0*/TM selector for SIOX and PIOX-16 interface sites.	Sections 2.6 and 2.7 , tables 2-11 and 2-12
J4	SIO-0/1 ports configurator for SIOX-B site (note: this jupmer settings are different for *TORNADO-542L* and *TORNADO-548/549*).	Section 2.7 and fig.2-13.
J5	JTAG path terminator (*TORNADO-548/549* only).	Section 2.8 and fig.2-15.

On-board Connectors

All on-board connectors for *TORNADO-54x* DSP systems are summarized in table A-3.

Table A-3.   On-board connectors and headers for *TORNADO-54x*.

connector ID	connector function description	reference information
JP1	PIOX-16 expansion interface site header.	Section 2.6 and fig.2-7.
JP2 JP3	SIOX-A/B expansion interface sites headers.	Section 2.7 and fig.2-12.
JP4 JP5	JTAG-IN and JTAG-OUT (*TORNADO-548/549* only) connectors	Section 2.8 and fig.2-15.
JP6	UECM site header (*TORNADO-548/549* only).	Sections 2.8 and 3.6.