

TORNADO-54x

High Performance 16-bit Fixed-Point TMS320C54x DSP Systems
and Emulators for host ISA-bus PC

User's Guide

covers:
TORNADO-542L rev.1B
TORNADO-548/549/5402/5410/5416 rev.2C

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About this Document

This user's guide contains description for *TORNADO-54x* 16-bit fixed-point digital signal processing (DSP) systems and emulators for host ISA-bus PC, which utilize the Texas Instruments (TI) TMS320C54x DSP:

- *TORNADO-542L* rev.1A/1B
- *TORNADO-548/549/5402/5410/5416* rev.2C (note: earlier revisions are not covered by this document).

This document does not include detail description neither for TI TMS320C54x DSP nor for the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C54x DSP. CPU and Peripherals.*** Texas Instruments Inc, SPRU131F, USA, 1999.
2. ***TMS320C54x DSP. Enhanced Peripherals.*** Texas Instruments Inc, SPRU302, USA, 1999.
3. ***TMS320C54x DSP. Mnemonic Instruction Set.*** Texas Instruments Inc, SPRU172, USA, 1996.
4. ***TMS320C54x DSP. Algebraic Instruction Set.*** Texas Instruments Inc, SPRU179A, USA, 1997.
5. ***TMS320C54x Optimizing C Compiler User's Guide.*** Texas Instruments Inc, SPRU103D, USA, 1999.
6. ***TMS320C54x Assembly Language Tools User's Guide.*** Texas Instruments Inc, SPRU102D, USA, 1999.

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Chapter 1. Introduction

This chapter contains general description for *TORNADO-54x* DSP systems product line, which comprises of *TORNADO-542L* and *TORNADO-548/549/5402/5410/5416/5416* DSP systems.

CAUTION

Here and further in this document the '*TORNADO-54x*' notation denotes that the supplied information is applicable to all *TORNADO-54x* DSP systems (*TORNADO-542L* and *TORNADO-548/549/5402/5410/5416* products).

Should information be a product specific, then the name of the corresponding product (*TORNADO-542L* or *TORNADO-548/549/5402/5410/5416*) will be highlighted.

1.1 General Information

TORNADO-54x are high performance fixed point DSP system boards and emulators for host ISA-bus PC computers. *TORNADO-54x* are designed to plug into 16-bit ISA-bus slot of host PC and feature flexible modular system architecture with DCM (DCM) in order to meet requirements for multiple applications while keeping a cost of project to a minimum.

TORNADO-54x DSP systems comprise of *TORNADO-542L* and *TORNADO-548/549/5402/5410/5416* and feature compatible host ISA-bus interface and TMS320C54x DSP environment. *TORNADO-548/549/5402/5410/5416* features extended memory capacity and enhanced emulation facility.



Fig.1-1.a. *TORNADO-542L* DSP system board with SIOX DCM and ECC emulation controller.



Fig.1-1b. TORNADO-548/549/5402/5410/5416 DSP system board with SIOX and UECMX DCM, and external JTAG pod.

The following are some applications for TORNADO-54x DSP systems:

- *real-time DSP and signal acquisition*
- *speech signal processing*
- *fax and modem*
- *audio signal processing*
- *multimedia*
- *instrumentation and industrial*
- *acoustics*
- *medical*
- *universal emulator for TI C2xx/C3x/C4x/C5x/C54x/C6x DSP (TORNADO-548/549/5402/5410/5416 only with universal emulation control DCM (UECMX) and external MPD/JTAG pod)*
- *evaluation and education*
- *many more ...*

TORNADO-54x utilize TMS320C54x 16-bit fixed point DSP (40 MIPS TMS320C542 in TORNADO-542L, 66/80 MIPS TMS320LC548 in TORNADO-548, 100 MIPS TMS320VC549 in TORNADO-549, 100 MIPS TMS320VC5402 in TORNADO-5402 , 100 MIPS TMS320VC5410 in TORNADO-5410 and 160 MIPS TMS320VC5416 in TORNADO-5416). The on-board static RAM (SRAM) for program and data includes 128Kx16 (TORNADO-542L) and 256Kx16 (TORNADO-548/549/5402/5410/5416). On-board SRAM is splitted into program and data memory banks each having 64Kx16 (TORNADO-542L) and 128Kx16 (TORNADO-548/549/5402/5410/5416) capacity.

TORNADO-54x have on-board shared bus (SB) architecture that shares access to SRAM and PIOX-16 shared resources between the on-board TMS320C54x DSP and host ISA-bus memory interface. Host ISA-bus memory

interface can provide access to SRAM/PIOX-16 both in random and block data transfer modes in parallel with DSP operation and almost without consuming the DSP time.

TORNADO-54x feature optional facility for installation of serial I/O expansion (SIOX) DCM from a variety of AD/DA and digital I/O SIOX modules for real-time instrumentation, industrial and speech, telecommunication and audio signal processing applications.

TORNADO-54x feature optional facility for installation of parallel I/O expansion (PIOX-16) DCM from a variety of AD/DA and digital I/O PIOX-16 daughter cards modules for high-speed real-time instrumentation, industrial and speech, telecommunication and audio signal processing applications.

TORNADO-54x offer access to HPI (host port interface) of on-board TMS320C54x DSP from host ISA-bus I/O interface. Along with host ISA-bus memory interface this provides a second data path for communication between host and DSP.

TORNADO-54x use scan-path emulation control for the on-board TMS320C54x DSP in order to debug resident TMS320C54x DSP software. Scan-path emulation control of the on-board TMS320C54x DSP is available either via external TI XDS510 or MicroLAB' *MIRAGE-510D* scan-path emulators, or by means of optional *emulation controller chip (ECC)* for *TORNADO-542L* that plugs into dedicated on-board socket, or by means of optional *emulation control DCM (UECMX)* for *TORNADO-548/549/5402/5410/5416* that plugs into dedicated on-board daughter card site. Both *ECC* and *UECMX* are low cost replacements for TI XDS510 and MicroLAB's *MIRAGE-510D* scan-path emulators and run under identical industry standard TI TMS320C54x HLL Debugger and TMS320C5000 Code Composer IDE. Furthermore, *UECMX* allows optional connection to external MPSD and JTAG pods (which are the pods used with MicroLAB's *MIRAGE-510D* scan-path emulator) in order to emulate any external TI C2xx/C3x/C4x/C5x/C54x/C6x DSP. This converts *TORNADO-548/549/5402/5410/5416* into universal emulator for TI DSP.

TORNADO-54x software development tools include TI TMS320C54x DSP C compiler and Assembly language tools.

TORNADO-54x are supported by a variety of industry standard 3rd party DSP software tools, that include real-time operating systems (RTOS), digital filter design tools, DSP/vector/math function libraries, vocoder/fax/modem function libraries, and many more...

TORNADO-54x provide unique burn-in device serial codes, that can be read by host software and used for hardware copyright protection of software tools for software vendors and DSP system integrators.

1.2 Host PC Specifications

TORNADO-54x require that host ISA-bus IBM PC configuration should be at least 80386SX CPU and provides at least one 16-bit ISA-bus slot.

In order to learn configuration requirements for host PC running TMS320C54x DSP software development and debugging tools, refer to the corresponding documentation from TI and Go DSP Corp as well as to MicroLAB' "*UECMX/ECC User's Guide*".

1.3 Technical Specification

The following are the technical specifications for *TORNADO-54x* system specified for the temperature +25°C of the environment.

<i><u>Parameter description</u></i>	<i><u>parameter value</u></i>
power supply voltage	+5V for <i>TORNADO-54x</i> board, optional $\pm 5V/\pm 12V$ for SIOX/PIOX DCM
power consumption (no <i>ECC</i> or <i>UECMX</i> installed)	+5V@1.5A
DSP performance	40 MIPS (<i>TORNADO-542L</i>) 66/80 MIPS (<i>TORNADO-548</i>) 100 MIPS (<i>TORNADO-549</i>) 100 MIPS (<i>TORNADO-5402</i>) 100 MIPS (<i>TORNADO-5410</i>) 160 MIPS (<i>TORNADO-5416</i>)
dimensions	160x110 mm
operating temperature	0..+50°C
I/O expansion interfaces	two sites (SIOX-A and SIOX-B) for <i>TORNADO/SIOX</i> DCM. One site for <i>TORNADO/PIOX-16</i> DCM.
<i>host ISA-bus interface:</i>	
number of 8-bit I/O ports in host ISA-bus I/O interface	16
size of ISA-bus memory page in the UMB memory address area for SB access via host ISA-bus memory interface	32Kx8
host timeout control time for SB grant, SB ready and HPI ready	6 μ s for <i>TORNADO-542L</i> 3 μ s for <i>TORNADO-548/5416</i> 2.5 μ s for <i>TORNADO-549/5402/5410</i>
host IRQ lines	IRQ 3, 4, 5, 6, 7, 10, 11, 12, 15
<i>on-board SRAM:</i>	
SRAM capacity	128Kx16 0ws (<i>TORNADO-542L</i>) 256Kx16 1ws (<i>TORNADO-548/549/5402/5410</i>) 256Kx16 2ws (<i>TORNADO-5416</i>)
Program memory area	64Kx16 (<i>TORNADO-542L</i>) 2x64Kx16 (<i>TORNADO-548/549/5402/5410/5416</i>)

Data memory area

64Kx16 (*TORNADO-542L*)
4x32Kx16 (*TORNADO-548/5495410*)
2x64Kx16 (*TORNADO-5402*)

*external clock generators for McBSP-0/1/2 serial ports of
TMS320VC5410 DSP for TORNADO-5410 only:*

maximum external frequency for CLKS inputs of McBSP-
0/1/2 TMS320VC5410 DSP serial ports

50 MHz (*TORNADO-5410* with on-board DSP
in the BGA package)

Chapter 2. System Architecture and Construction

This chapter contains description for *TORNADO-54x* system architecture, construction, host ISA-bus interface, and SIOX/PIOX-16 I/O expansion sites.

2.1 *TORNADO-54x* System Architecture

TORNADO-54x DSP system mainboards install into 16-bit ISA-bus slot of host PC (fig.1-1). *TORNADO-542L* and *TORNADO-548/549/5402/5410/5416* system architectures are presented at fig.2-1.

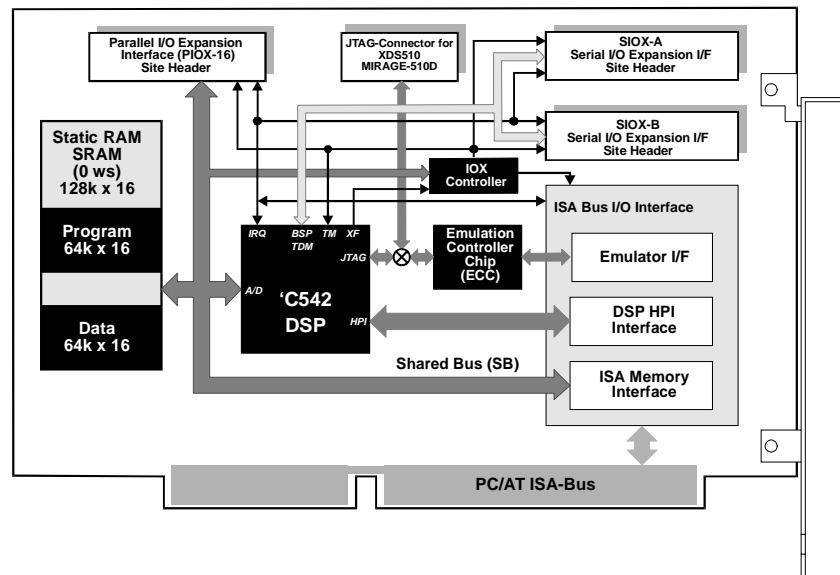


Fig.2-1a. Architecture of *TORNADO-542L* mainboard.

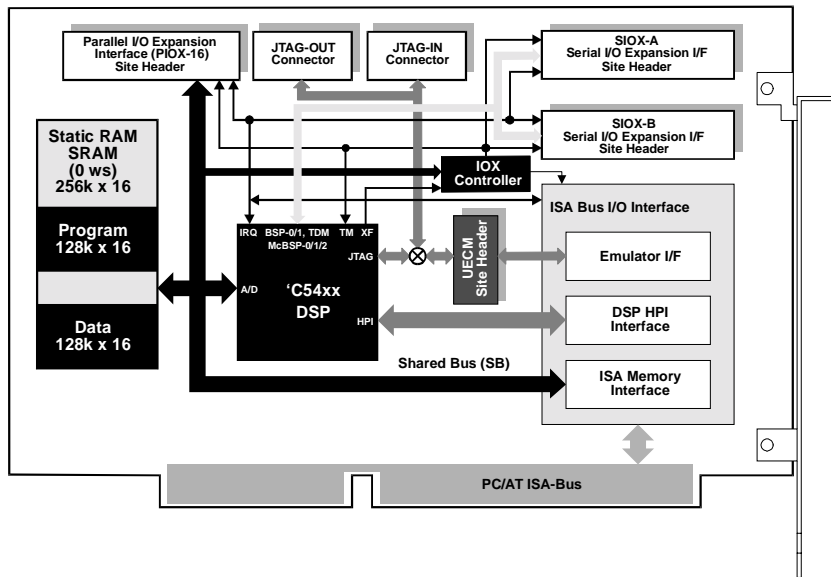


Fig.2-1b. Architecture of TORNADO-548/549/5402/5410/5416 mainboard.

Main components of TORNADO-54x mainboard are:

- TMS320C54x 16-bit fixed point DSP
- on-board SRAM comprising of PROGRAM and DATA memory areas
- host ISA-bus memory and I/O interfaces
- I/O expansion flag controller (IOX)
- serial I/O expansion interface (SIOX) site
- 16-bit parallel I/O expansion interface (PIOX-16) site
- emulation controller chip (ECC) for TORNADO-542L or site for universal emulation control DCM (UECMX) for TORNADO-548/549/5402/5410/5416.

The on-board TMS320C54x DSP, SRAM, PIOX-16 and host ISA-bus memory interface are linked together by means of the on-board *Shared Bus (SB)*. SB shares SRAM/PIOX-16 resources between two 'bus masters', that can execute SB access cycles: the on-board TMS320C54x DSP and host ISA-bus memory interface. On-board SB arbitration assumes that TMS320C54x DSP bus master has highest SB access priority whereas ISA-bus memory interface is designed to access SB in-parallel with DSP internal operation, without any DSP and host software overhead and almost without consuming the DSP time.

Constructions for TORNADO-542L and TORNADO-548/549/5402/5410/5416 DSP systems mainboards are presented at fig.2-2.

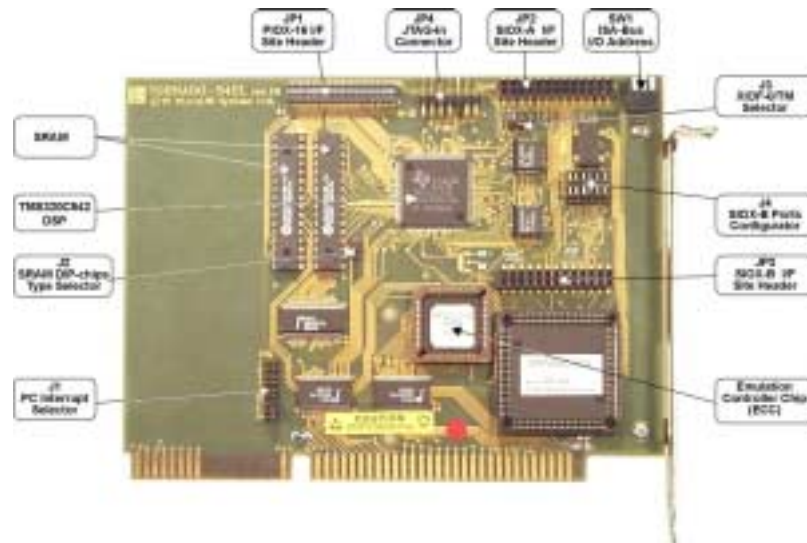


Fig.2-2a. Construction of TORNADO-542L mainboard.

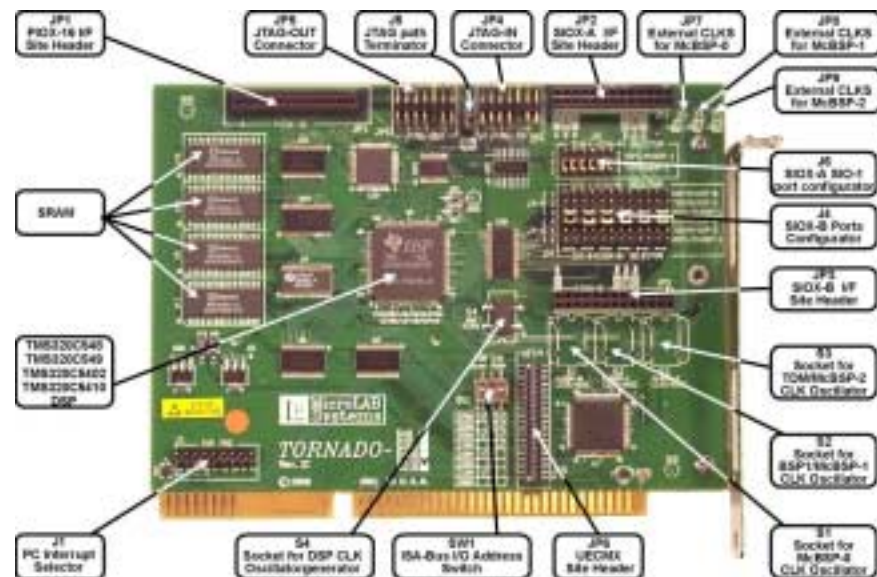


Fig.2-2b. Construction of TORNADO-548/549/5402/5410/5416 mainboard.

TMS320C54x DSP

All *TORNADO-54x* DSP systems feature compatible 16-bit fixed point DSP chip with on-chip Harvard architecture as the following:

- 40MIPS TMS320C542 DSP in *TORNADO-542L*
- 66MIPS/80MIPS TMS320LC548 DSP in *TORNADO-548*
- 100MIPS TMS320VC549 DSP in *TORNADO-549*
- 100MIPS TMS320VC5402 DSP in *TORNADO-5402*
- 100MIPS TMS320VC5410 DSP in *TORNADO-5410*
- 160MIPS TMS320VC5416 DSP in *TORNADO-5416*.

Static RAM (SRAM) for Program and Data

TORNADO-54x provides on-board static RAM (SRAM) for TMS320C54x DSP program and data memory areas.

TORNADO-542L features 128Kx16 0ws of on-board SRAM that comprises of PROGRAM and DATA memory areas each having equal 64Kx16 SRAM capacity.

TORNADO-548/549/5402/5410 features 256Kx16 of on-board SRAM, which comprises of 128Kx16 PROGRAM and 128Kx16 DATA memory areas. The on-board SRAM meets 1ws for *TORNADO-548/549/5402/5410* boards and 2ws for *TORNADO-5416* board. The 128Kx16 PROGRAM memory area is organized as two 64Kx16 memory pages (PMEM-pages #0 and #1), so build-in extended program memory addressing capabilities of TMS320LC548/VC549/VC5402/VC5410/VC5416 DSP should be used to address this program memory.

The on-board 128Kx16 DATA memory for *TORNADO-548/549/5410/5416* DSP systems is organized as the multi-page memory with on-board extended data memory addressing hardware (extended data memory page register (*XDMPR*)), which is used to switch between these data memory pages from the DSP software. The data memory organization differs for different *TORNADO-548/549/5402/5410/5416* DSP systems as the following:

- on-board 128Kx16 DATA memory for *TORNADO-548/549/5410/5416* is organized as four pages of 32Kx16 each with each page being mapped into the upper (off-chip) half of data memory address space of TMS320LC548/VC549/5410/5416 DSP
- on-board 128Kx16 DATA memory for *TORNADO-5402* is organized as two pages of 64Kx16 each with each page mapped into the upper 48Kx16 (off-chip) data memory address space of TMS320LC5402 DSP.

Shared Bus (SB)

TORNADO-54x on-board SB delivers access to the on-board SRAM and PIOX-16 shared resources for both on-board TMS320C54x DSP and host ISA-bus memory interface. The SB address space comprises of SRAM/PROGRAM memory area, SRAM/DATA memory area and I/O area, which is mapped into PIOX-16 expansion interface. SB supports 16-bit data cycles. It is important to note, that all host accesses to the on-board SRAM and PIOX-16 resources are performed concurrently with the DSP running and without any DSP and host software overhead.

Host ISA-bus Interface

TORNADO-54x host ISA-bus interface was designed for DSP/system control and high-speed data transfer between host ISA-bus and on-board SRAM/PIOX-16 and HPI port of on-board TMS320C54x DSP. *TORNADO-54x* host ISA-bus interface includes:

- *ISA-bus memory interface* that performs access to SRAM and PIOX-16
- *ISA-bus I/O interface* that provides *TORNADO-54x* system control and access to TMS320C54x on-chip HPI (host port interface).

Host ISA-bus memory interface can access SB SRAM/PIOX-16 resources via 32Kx8 *shared memory page (SMP)* that is mapped into ISA-bus UMB memory address space. Once ISA-bus executes memory cycle within address range of *SMP*, then the on-board *TORNADO-54x* ISA-bus memory interface generates request to SB. Particular allocation of *SMP* onto SB address space is defined by *SB PAGE MAPPER* register from ISA-bus I/O interface. Host can access the SB data using 16-bit data cycles. Host ISA-bus memory interface has lowest SB access priority.

Base ISA-bus memory address for host ISA-bus memory might be set by host software and might be switched off in case *TORNADO-54x* board is not used.

ISA-bus base I/O address for ISA-bus I/O interface is configured by the on-board SW1 DIP-switch into one of eight predefined I/O address areas.

TMS320C54x HPI (host port interface)

TORNADO-54x host ISA-bus I/O interface also delivers access to TMS320C54x on-chip HPI, which comes as a second data path for communication between host PC and on-board DSP along with on-board SRAM. HPI offers access from host PC to TMS320C54x shared memory area and allows generation of mutual interrupts. However, unlike access to on-board SRAM, HPI does not support random access to HPI memory from host PC using standard ISA-bus memory cycle, and assumes that HPI memory address should be pre-latched into HPI address register prior HPI data access will be performed. However, the HPI address auto post-incrementing feature is available and simplifies data array upload/download.

I/O Expansion Flag Controller (IOX)

TORNADO-54x has on-board I/O expansion flag controller (IOX) that provides some extra I/O ports used by the on-board TMS320C54x DSP environment. IOX controller can be accessed by the on-board TMS320C54x DSP only.

Serial I/O Expansion Interface (SIOX) sites

TORNADO-54x on-board SIOX interface sites are used for installation of AD/DA/DIO DCM and comprises of signals for TMS320C54x DSP on-chip serial ports (BSP, TDM or McBSP), timer and interrupt control, and *XIOF-0/1* I/O flags.

SIOX compatible DCM include a variety of speech/fax/modem AD/DA, telecom interfaces, audio AD/DA, DAT interface, multichannel instrumentation AD/DA/DIO, and many more.

Parallel I/O Expansion Interface (PIOX-16) site

TORNADO-54x PIOX-16 interface site is used for installation of AD/DA/DIO DCM and comprises of SB signals, *XIOF-0/1* I/O flags and TMS320C54x DSP on-chip timer and interrupt control. *TORNADO-54x* PIOX-16 interface is allocated into TMS320C54x I/O address area and can be accessed both by on-board DSP and host ISA-bus memory interface.

PIOX-16 compatible DCM include a variety of multichannel instrumentation AD/DA/DIO modules and many more.

Debugging of resident TMS320C54x DSP Software

Resident TMS320C54x DSP software for *TORNADO-54x* can be debugged using TI XDS510 and MicroLAB' *MIRAGE-510D* scan-path emulators. However, in order to minimize cost of debugging tools, the emulation controller chip (*ECC*) can be plugged into the dedicated on-board socket of *TORNADO-542L* or universal emulation control DCM (*UECMX*) can be plugged into the dedicated site on *TORNADO-548/549/5402/5410/5416*. Both *ECC* and *UECMX* are low cost replacement for XDS510 and *MIRAGE-510D* emulators and run under identical industry standard TI TMS320C54x HLL Debugger and TMS320C5000 Code Composer IDE.

Debugging of external TI TMS320 DSP Software with TORNADO-548/549/5402/5410/5416 and UECMX

TORNADO-548/549/5402/5410/5416 DSP systems easily convert into universal scan-path emulator for any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP. This requires the *UECMX* DCM installed onto *TORNADO-548/549/5402/5410/5416* mainboard and optional external MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x) pod attached to *UECMX*. The MPSD and JTAG pods are the pods used with MicroLAB' *MIRAGE-510D* emulator. The *UECMX* runs under the industry standard TI HLL Debuggers and GoDSP Code Composer IDE.

2.2 Shared Bus

The *TORNADO-54x* on-board shared bus (SB) architecture provides SRAM/PROGRAM, SRAM/DATA and I/O areas and supports 16-bit data cycles. SB comprises SRAM and PIOX-16 shared resources and is shared between the on-board TMS320C54x DSP and host ISA-bus memory interface.

SB Address Space

The SB address space is actually the address space for *TORNADO-54x* on-board TMS320C54x DSP. Table 2-1 specifies valid SB address areas.

Table 2-1. SB address areas and data ready wait times.

SB address areas	address range (in 16-bit word units)	wait time for <i>SB_READY</i> signal (SB data ready) after SB is granted to...	
		<i>on-board TMS320C54x DSP</i>	<i>host ISA-bus memory interface</i>
SRAM/PROGRAM memory area	0000H...FFFFH @PROG (<i>TORNADO-542L</i>)	0ws (should be programmed via PROGRAM field of SWWSR for <i>TORNADO-542L</i>)	0ws (<i>TORNADO-542L</i>)
	00000H...1FFFFH @PROG (<i>TORNADO-548/549/5402/5410/5416</i>)	1ws (should be programmed via PROGRAM field of SWWSR for <i>TORNADO-548/549/5402/5410/5416</i>)	1ws (<i>TORNADO-548/549/5402/5410/5416</i>)
SRAM/DATA memory area	2800H...FFFFH @DATA (<i>TORNADO-542L</i>)	0ws (should be programmed via DATA field of SWWSR for <i>TORNADO-542L</i>)	0ws (<i>TORNADO-542L</i>)
	8000H...FFFFH @DATA (4 overlapped memory pages for <i>TORNADO-548/549/5410/5416</i> on-board DSP; memory page is selected by <i>XDMPR</i>)	1ws (should be programmed via DATA field of SWWSR for <i>TORNADO-548/549/5402/5410</i>)	1ws (<i>TORNADO-548/549/5402/5410/5416</i>)
	4000H...FFFFH @DATA (2 overlapped memory pages for <i>TORNADO-5402</i> on-board DSP; memory page is selected by <i>XDMPR</i>)	2ws (should be programmed via DATA field of SWWSR for <i>TORNADO-5416</i>)	
	08000H...0FFFFH 18000H...1FFFFH 28000H...2FFFFH 38000H...3FFFFH @DATA (for host ISA-bus memory I/F of <i>TORNADO-548/549/5410/5416</i>)		
	04000H...0FFFFH 14000H...1FFFFH @DATA (for host ISA-bus memory I/F of <i>TORNADO-5402</i>)		

PIOX I/O area	0000H...FFFFH @I/O	(4ws + <i>PIOX_RDY</i>) (should be programmed via I/O field of SWWSR)	(1ws + <i>PIOX_READY</i>), but not longer than 4μS timeout
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The SB address space in host ISA-bus memory interface appears as a series of dual-access 32KB *shared memory pages* (*SMP*) that are mapped onto the predefined ISA-bus UMB (upper memory blocks) memory window by means of *SB PAGE MAPPER* register in host ISA-bus I/O interface. The SB can be accessed by host ISA-bus memory interface by means of random accesses to software variables or data arrays that are allocated within *SMP*, or by means of block data transfers between PC main memory and *SMP* using either host i80x286 CPU MOVSB/MOVSX/etc instructions or host DMA controller.

SRAM area for TORNADO-542L

TORNADO-542L allows user to install up to 128Kx16 0ws of on-board SRAM using two 8K/32K/64K/128Kx8 SRAM DIP chips in DIP-28 and DIP-32 packages with 15ns access time. The on-board J2 jumper (refer to fig.2-2 and fig A-1) should be set in accordance with particular type of SRAM chips installed.

CAUTION

On-board J2 jumper for *TORNADO-542L* should be set to 1-2 position in case the 32K/64K/128Kx8 SRAM DIP-32 chips are installed.

On-board J2 jumper for *TORNADO-542L* should be set to 2-3 position in case the 8Kx8 SRAM DIP-28 chips are installed.

TORNADO-542L on-board hardware automatically splits the on-board installed SRAM capacity into two PROGRAM and DATA memory areas each having equal SRAM capacity. For example, for 128Kx16 SRAM installed, the PROGRAM and DATA memory areas will equal to 64Kx16 SRAM capacity each, whereas for 32Kx16 SRAM installed this results to 16Kx16 PROGRAM and DATA memory areas.

CAUTION

Table 2-1 shows the SRAM/PROGRAM and SRAM/DATA memory area address ranges for *TORNADO-542L* with 128Kx16 SRAM installed. This covers full address range for PROGRAM and DATA memory areas of TMS320C542 DSP.

In case the installed SRAM has smaller capacity (i.e. 8K/32K/64Kx16), then the SRAM/PROGRAM and SRAM/DATA memory areas will appear as overlapped memory pages in the PROGRAM and DATA memory areas of TMS320C54x DSP. In this case the recommended allocation for SRAM/PROGRAM and SRAM/DATA memory pages will be allocation at the most high memory page addresses, i.e. the highest memory page address must fit to 0FFFFH PROGRAM and 0FFFFH DATA memory address of TMS320C54x DSP.

SRAM area for TORNADO-548/549/5402/5410/5416

TORNADO-548/549/5402/5410/5416 features 256Kx16 of on-board SRAM that comprises of 128Kx16 PROGRAM and 128Kx16 DATA memory areas. The on-board SRAM meets 1ws for *TORNADO-548/549/5402/5410* boards and 2ws for *TORNADO-5416* board. The 128Kx16 PROGRAM memory area is organized as two 64Kx16 memory pages (PMEM-pages #0 and #1), so build-in extended program memory addressing capabilities of TMS320LC548/VC549/VC5402/VC5410/VC5416 DSP should be used to address this program memory.

The on-board 128Kx16 DATA memory for *TORNADO-548/549/5402/5410/5416* DSP systems is organized as the multi-page memory with on-board extended data memory addressing hardware (extended data memory page register (*XDMPR*)), which is used to switch between these data memory pages from the DSP software. The data memory organization differs for different *TORNADO-548/549/5402/5410/5416* DSP systems as the following:

- on-board 128Kx16 DATA memory for *TORNADO-548/549/5410/5416* is organized as four pages of 32Kx16 each with each page being mapped into the upper (off-chip) half of data memory address space of TMS320LC548/VC549/5410/5416 DSP
- on-board 128Kx16 DATA memory for *TORNADO-5402* is organized as two pages of 64Kx16 each with each page mapped into the upper 48Kx16 (off-chip) data memory address space of TMS320LC5402 DSP.

SB Data Ready Signal

SB has internal *SB_READY* signal that is generated by passive addressed device (SRAM or PIOX-16) in order to acknowledge that SB data are valid after SB is granted to requesting SB master. When SB is accessed by the on-board TMS320C54x DSP master, the *SB_READY* signal is logically connected to the *READY* pin of TMS320C54x DSP, whereas for accesses from host ISA-bus memory interface the *SB_READY* signal is automatically processed by the SB access controller of ISA-bus memory interface.

SB Data Cycle Formats

SB supports 16-bit data cycles only. The on-board TMS320C54x DSP master provides only 16-bit SB data cycles whereas host ISA-bus memory interface can perform 8-bit or 16-bit ISA-bus memory cycles. In case host

ISA-bus memory interface executes 8-bit ISA-bus cycle while accessing the SB areas, then LSB or MSB are temporary stored in on-board register transceivers depending upon the memory read or memory write cycle is being performed correspondingly (refer to section 2.4).

SB Arbitration

When SB is requested by any of the SB masters (TMS320C54x DSP or host ISA-bus memory interface), then some time is required to resolve the arbitration. This normally takes about 1-2 TMS320C54x DSP clock cycles.

In case TMS320C54x DSP is requesting SB while SB is occupied by host ISA-bus memory interface, then the DSP should wait until host ISA-bus memory interface will release SB. After SB is granted to DSP, it is holded by DSP in order to provide 0ws (*TORNADO-542L*) or 1ws (*TORNADO-548/549/5402/5410/5416*) for all further SB accesses.

In case host ISA-bus memory interface is requesting SB while SB is occupied by TMS320C54x DSP, then host ISA-bus memory interface has to wait until DSP will complete current SB access cycle and release SB.

When SB is requested by both DSP and host ISA-bus memory interface, then DSP has the highest SB access priority.

SB Locking

The SB arbiter supports program *SB locking* in order to lock the SB access for processing of program semaphores or shared PIOX-16 resources.

The SB locking by the on-board TMS320C54x DSP bus master is performed when DSP set *MLock* flag in I/O expansion flag area (IOX).

CAUTION

Time interval between setting and resetting *MLock* flag by the on-board TMS320C54x DSP should not exceed 2.5 μ S in order to avoid timeout condition for host-to-SB access.

The SB locking by host ISA-bus memory interface master is performed by means of setting the *SB_GLOCK* or the *SB_LOCK* bits of *CONTROL REGISTER* by host ISA-bus I/O interface.

CAUTION

Continuous SB locking by host ISA-bus memory interface by means of setting the *SB_GLOCK* and *SB_LOCK* bits can result in continuous halting of the on-board TMS320C54x DSP bus master and may lead to time distortions of real-time data processing.

2.3 TMS320C54x DSP Environment

The *TORNADO-54x* DSP systems utilize TMS320C54x high-performance 16-bit fixed point DSP from TI:

- 40MIPS TMS320C542 DSP in *TORNADO-542L*
- 66MIPS/80MIPS TMS320LC548 DSP in *TORNADO-548*
- 100MIPS TMS320VC549 DSP in *TORNADO-549*
- 100MIPS TMS320VC5402 DSP in *TORNADO-5402*
- 100MIPS TMS320VC5410 DSP in *TORNADO-5410*
- 160MIPS TMS320VC5416 DSP in *TORNADO-5416*.

TMS320C54x DSP Address Space

TMS320C54x DSP supports three external address spaces (areas): program area, data area and I/O area. Each area can be accessed by a specific set of instructions. Address areas for on-board TMS320C54x DSP are presented in table 2-2.

Table 2-2. Address areas for TMS320C54x DSP in TORNADO-54x DSP systems.

Address area of TMS320C54x DSP	value on DSP RESET	access mode	address range (in 16-bit words)	wait states
SRAM/PROGRAM area, which is the shared resource of the on-board SB and can be accessed by both TMS320C54x DSP and host ISA-bus memory interface	-	r/w	0000H...FFFFH @PROG (TORNADO-542L) 00000H...1FFFFH @PROG (TORNADO-548/549/5402/5410/5416)	0ws/SWS-M (TORNADO-542L) 1ws/SWS-M (TORNADO-548/549/5402/5410) 2ws/SWS-M (TORNADO-5416)
SRAM/DATA area, which is the shared resource of the on-board SB and can be accessed by both TMS320C54x DSP and host ISA-bus memory interface	-	r/w	2800H...FFFFH @DATA (TORNADO-542L) (TORNADO-548/549/5410/5416): <u>page #0</u> : 8000H..FFFFH @XDMPR=0 @DATA <u>page #1</u> : 8000H..FFFFH @XDMPR=1 @DATA <u>page #2</u> : 8000H..FFFFH @XDMPR=2 @DATA <u>page #3</u> : 8000H..FFFFH @XDMPR=3 @DATA (TORNADO-5402): <u>page #0</u> : 4000H..FFFFH @XDMPR=0 @DATA <u>page #1</u> : 4000H..FFFFH @XDMPR=1 @DATA	0ws/SWS-M (TORNADO-542L) 1ws/SWS-M (TORNADO-548/549/5402/5410) 2ws/SWS-M (TORNADO-5416)
IOX area: XDMPR register (extended data memory page register), TORNADO-548/549/5402/5410/5416 only	0 (data memory page#0 is selected)	r/w	2000H @I/O while XF=1 (bits D0..D1 only)	2ws/SWS-IO (TORNADO-542L/548/549/5402/5410) 4ws/SWS-IO (TORNADO-5416)
IOX area: XIOF-DATA register (I/O expansion flags data)	0	r/w	4000H @I/O while XF=1 (bits D0..D1 only)	
IOX area: XIOF-DIR register (I/O expansion flags direction)	0 (XIOF-0/1 are inputs)	r/w	4001H @I/O while XF=1 (bits D0..D1 only)	

IOX area: <i>XIO_CNF</i> register (configuration register for <i>XIO-0/1</i> pins of SIOX/PIOX-16 expansion interface sites), <i>TORNADO-548/549/5402/5410/5416</i> only	0 (<i>XIO-0/1</i> pins are configured as I/O pins)	r/w	4002H @I/O while XF=1 (<i>TORNADO-5402</i> : bits D0..D1 only <i>TORNADO-548/549/5410/5416</i> : bit D0 only)	
IOX area: <i>MH_RQ</i> register (DSP_master-to-Host request flag)	-	w	8000H @I/O while XF=1 (data written is ignored)	
IOX area: <i>Mlock</i> register (SB lock by DSP_master flag)	0 (no SB Lock)	r/w	8001H @I/O while XF=1 (bit D0 only)	
IOX area: <i>PXSX_RUN</i> register (software reset signal for SIOX and PIOX-16 expansion interface sites), <i>TORNADO-548/549/5402/5410/5416</i> only	0 (software reset is ON)	r/w	8002H @I/O while XF=1 (bits D0..D2 only)	
PIOX-16 area	-	r/w	0000H...FFFFH @I/O while XF=0	2ws/SWS-IO + <i>PIOX_READY</i> (<i>TORNADO-542L/548/549/5402/5410</i>) 4ws/SWS-IO + <i>PIOX_READY</i> (<i>TORNADO-5416</i>)

Notes:

1. 'XF' denotes XF output of TMS320C54x DSP.
2. IOX area denotes I/O Expansion Flag controller, that is accessible with I/O cycles while XF=1.
3. 'SWS-M' denotes recommended number of software wait states programmed in the PROGRAM and DATA fields of TMS320C54x on-chip SWWSR register. The XPA bit of SWWSR register for TMS320LC548/VC549/VC5402/VC5410/VC5416 DSP of *TORNADO-548/549/5402/5410/5416* DSP systems should be set to logical '0'.
4. 'SWS-IO' denotes recommended number of software wait states programmed in the I/O field of TMS320C54x on-chip SWWSR register.
5. The DROM bit of PMST register of TMS320VC5410/VC5416 DSP should be set to DROM=0 value (default value on DSP reset) in order to enable external data memory addressing for TMS320VC5410/VC5416 DSP and in order to access the on-board DATA memory of *TORNADO-5410/5416*.
6. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

PROGRAM and DATA SRAM Areas

TORNADO-54x on-board PROGRAM and DATA memory areas reside in the on-board SRAM, which has the following capacity:

- 128Kx16 0ws SRAM in *TORNADO-542L*
- 256Kx16 SRAM in *TORNADO-548/549/5402/5410/5416*. (1ws for *TORNADO-548/549/5402/5410* boards and 2ws for *TORNADO-5416* board).

Each PROGRAM and DATA memory area occupies one half of total SRAM capacity as the following:

- 64Kx16 program memory area and 64Kx16 data memory area (only 2800H..FFFFH data address space for TMS320C542 DSP is accessible) for *TORNADO-542L*
- 2x64Kx16 program memory area (pages #0 and #1 of extended program memory address space of TMS320LC548/VC549/VC5402/VC5410/VC5416 DSP) and either 4x32Kx16 (*TORNADO-548/549/5410/5416*) or 2x64Kx16 (*TORNADO-5402*) data memory area (overlapped pages of data memory in external data memory address area of TMS320LC548/VC549/VC5402/VC5410/VC5416 DSP, which are selected by the on-board *XDMPR* register). Refer to the section below for details about extended data memory addressing for *TORNADO-548/549/5402/5410/5416*.

IOX Area

TMS320C54x DSP environment of *TORNADO-54x* features special I/O expansion (IOX) area, which is allocated into I/O area. IOX area is used for DSP environment control and includes the following IOX registers:

- *MH_RQ* generation register (DSP master-to-Host request)
- *MLock* flag register (SB lock by DSP)
- *XIOF-0/1* control registers (I/O expansion flags #0 and #1)
- *PXSX_RUN* flag register (software reset signal for SIOX/PIOX-16 expansion interface sites)
- *XDMPR* (extended data memory page) register in *TORNADO-548/549/5402/5410/5416* DSP systems.

CAUTION

IOX area is available during TMS320C54x DSP I/O accesses with the DSP' XF output flag set to logical '1'. IOX area can be accessed only by TMS320C54x DSP and is not visible from host ISA-bus memory interface.

All IOX area registers are accessible with two software wait states (four wait states for *TORNADO-5416* board) programmed via *SWWSR* register of TMS320C54x DSP. Details about IOX area are described below in this section.

PIOX-16 Area and PIOX-16 expansion interface site

TORNADO-54x provides 16-bit parallel I/O expansion interface (PIOX-16) site for compatible AD/DA/DIO DCM. PIOX-16 occupies 64Kx16 of DSP I/O address space and is available during TMS320C54x DSP I/O accesses with the DSP' XF output flag set to '0'. PIOX-16 area can be accessed both by the on-board TMS320C54x DSP and host ISA-bus memory interface.

Setting *SWWSR* and *BSCR* Control Registers of TMS320C54x DSP

In order to benefit of full performance of TMS320C54x DSP and to provide correct operation of on-board hardware, be sure to setup TMS320C54x on-chip *SWWSR/BSCR* peripheral access control registers in your TMS320C54x DSP software as the following:

- the *SWWSR* register (software programmable wait state generator) of TMS320C54x DSP should be programmed to 0200H hex value for *TORNADO-542L* DSP system, to 2209H hex value for

TORNADO-548/549/5402/5410 DSP systems and to 4412H hex value for *TORNADO-5416* DSP system. This corresponds to the following settings:

- on-board SRAM/PROGRAM memory area is accessed with 0ws in *TORNADO-542L*, with 1ws in *TORNADO-548/549/5402/5410*, and with 2ws in *TORNADO-5416*
- on-board SRAM/DATA memory area is accessed with 0ws in *TORNADO-542L*, with 1ws in *TORNADO-548/549/5402/5410*, and with 2ws in *TORNADO-5416*
- IOX area is accessed with 2ws (accessible from TMS320C54x DSP environment only) in *TORNADO-542L/548/549/5402/5410* and with 4ws in *TORNADO-5416*
- PIOX-16 I/O area is accessed with (2ws + *PIOX_READY*) signal in *TORNADO-542L/548/549/5402/5410* and with (4ws+ *PIOX_READY*) in *TORNADO-5416*
- the *BSCR* register (programmable memory bank switching) should be programmed to 0000H hex value

TMS320C54x HPI (host port interface)

TORNADO-54x offers access from host ISA-bus I/O interface to TMS320C54x on-chip HPI (host port interface). All HPI features are supported, including mutual interrupt generation between host ISA-bus I/O interface and TMS320C54x DSP. For details about TMS320C54x HPI refer to original TI documentation and refer to the corresponding section later in this chapter.

CAUTION

TORNADO-542L/548/549 DSP systems allow Host-to-DSP communication using DSP on-chip HPI port via dedicated 2Kx16 DSP on-chip shared memory area only (DSP data memory address range 0x1000...0x17ff, which corresponds to Host HPI address range 0x0000...0x07ff).

TORNADO-5402 DSP system allows Host-to-DSP communication using DSP on-chip HPI port via entire 16Kx16 DSP on-chip memory (DSP data memory address range 0x0060...0x3fff, which corresponds to Host HPI address range 0x0060...0x3fff).

TORNADO-5410/5416 DSP system allows Host-to-DSP communication using DSP on-chip HPI port via entire 32Kx16 DSP on-chip memory (DSP data memory address range 0x0060...0x7fff, which corresponds to Host HPI address range 0x0060...0x7fff), as well as via extended 32Kx16 SARAM1 DSP on-chip memory area (DSP data memory address range 0x8000...0xffff, which corresponds to Host HPI address range 0x18000...0x1ffff).

The DSP on-chip HPI feature might be disabled in *TORNADO-5402* DSP system via host ISA-bus I/O interface in order to allow output from the second DSP on-chip timer (*TM1*) to be available via on-board SIOX and PIOX-16 expansion interface sites. Refer to the '*Host ISA-bus I/O Interface*' section later in this chapter for details how to enable/disable the HPI port for *TORNADO-5402* DSP systems.

Extended Data Memory Addressing with XDMPR register in TORNADO-548/549/5402/5410/5416

TORNADO-548/549/5402/5410/5416 allows the on-board TMS320LC548/VC549/VC5402/VC5410/VC5416 DSP to address data memory beyond conventional 64Kx16 data memory address range for TMS320LC548/VC549/VC5402/VC5410/5416 DSP.

The extended data memory addressing for TMS320C54x DSP in **TORNADO-548/549/5402/5410/5416** DSP system is performed by means of either two-bit (**TORNADO-548/549/5410/5416**) or one-bit (**TORNADO-5402**) external extended data memory page register (**XDMPR**), which selects between four (**TORNADO-548/549/5410/5416**) or two (**TORNADO-5402**) available overlapped external data memory pages while TMS320LC548/VC549/VC5402/VC5410/VC5416 DSP accesses external data memory area. **XDMPR** might be accessed by TMS320LC548/VC549/VC5402/VC5410/VC5416 DSP via IOX area in accordance with table 2-2.

The on-board 128Kx16 DATA memory for **TORNADO-548/549/5402/5410/5416** DSP systems is organized as the multi-page memory with on-board extended data memory addressing hardware (extended data memory page register (**XDMPR**)), which is used to switch between these data memory pages from the DSP software. The data memory organization differs for different **TORNADO-548/549/5402/5410/5416** DSP systems as the following:

- on-board 128Kx16 DATA memory for **TORNADO-548/549/5410/5416** is organized as four pages of 32Kx16 each with each page being mapped into the 8000H..FFFFH@DATA off-chip data memory address space of TMS320LC548/VC549/VC5410/VC5416 DSP
- on-board 128Kx16 DATA memory for **TORNADO-5402** is organized as two pages of 64Kx16 each with each page mapped into the 4000H..FFFFH@DATA off-chip data memory address space of TMS320LC5402 DSP.

The extended data memory addressing for TMS320LC548/VC549/VC5410/VC5416 DSP in **TORNADO-548/549/5410/5416** DSP systems operates as the following:

- while data memory within 0000H..7FFFH@DATA data memory address range is addressed by TMS320LC548/VC549/VC5410/VC5416 DSP, then the DSP on-chip RAM is selected
- once data memory within 8000H..FFFFH@DATA data memory address range is addressed by TMS320LC548/VC549/VC5410/VC5416 DSP, then external SRAM/DATA area is selected. Page #0 of external SRAM/DATA area is selected while **XDMPR**=0. Correspondingly, page #1 of external SRAM/DATA area is selected while **XDMPR**=1, page #2 - while **XDMPR**=2, and page #3 - while **XDMPR**=3. The reset value of **XDMPR** is '0' in order to provide compatibility with **TORNADO-542L** DSP system.

CAUTION

The TMS320VC5410/VC5416 DSP provides 64Kx16 of on-chip data memory, which is allocated as two blocks within 0000H..7FFFFH@DATA (DARAM and SARAM1) and 8000H..FFFFH@DATA (SARAM2) data address areas.

Once the SARAM2 DSP on-chip memory is allocated into the DSP on-chip memory by setting bit DROM=1 from the PMST register of TMS320VC5410/VC5416 DSP, then the external DATA memory of *TORNADO-5410/5416* is not available for TMS320VC5410/VC5416 DSP, and there is no communication between DSP and host ISA-bus memory interface via DATA memory area.

Your DSP software should set bit DROM=0 (default value on DSP reset) of PMST register of TMS320VC5410/VC5416 DSP in order to disable SARAM2 DSP on-chip memory and to enable external DATA memory feature for TMS320VC5410/VC5416 DSP via 128Kx16 on-board DATA memory of *TORNADO-5410/5416*.

The extended data memory addressing for TMS320VC5402 DSP in *TORNADO-5402* DSP system operates as the following:

- while data memory within 0000H..3FFFFH@DATA data memory address range is addressed by TMS320VC5402 DSP, then the DSP on-chip RAM is selected
- once data memory within 4000H..FFFFH@DATA data memory address range is addressed by TMS320VC5402 DSP, then external SRAM/DATA area is selected. Page #0 of external SRAM/DATA area is selected while *XDMPR*=0 and page #1 of external SRAM/DATA area is selected while *XDMPR*=1. The reset value of *XDMPR* is '0' in order to provide compatibility with *TORNADO-542L* DSP system.

XDMPR register can be accessed by TMS320LC548/VC549/VC5402/VC5410/VC5416 DSP via IOX area in accordance with table 2-2. *XDMPR* register is available during both read/write I/O cycles and has the following data format (note, that bit *XDMP-1* is ignored for *TORNADO-5402* DSP system):

***XDMPR* IOX Register (r/w)**

X	X	X	X	X	X	X	<i>XDMP-1</i> (r/w, 0+)	<i>XDMP-0</i> (r/w, 0+)
(TORNADO-548/549/5410/5416 only)								
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XIO-0/1 Pins of SIOX/PIOX-16 Interface Sites and XIOF-0/1 I/O Flags

XIO-0/1 pins of *TORNADO-54x* on-board SIOX/PIOX-16 interface sites might be configured either as I/O pins or as on-board TMS320C54x DSP timer outputs.

After the *XIO-0/1* pins are configured as I/O pins, then the corresponding *XIOF-0/1* I/O flag appears on the *XIO-0/1* pin. Each of *XIOF-0/1* I/O flags is controlled by the *XIOF-DATA* and *XIOF-DIR* IOX registers and can be individually configured by DSP as either input or output flag.

XIO-0/1 pins of SIOX/PIOX-16 interface sites of *TORNADO-54x* DSP systems and *XIOF-0/1* I/O flags are controlled by DSP software via IOX area in accordance with table 2-2 and occupies several registers in the IOX area:

- *XIOF-DIR* IOX register (*XIOF* flags direction register)
- *XIOF-DATA* IOX register (*XIOF* flags data register)
- *XIO-CNF* IOX register (configuration register for *XIO* pins of SIOX/PIOX-16 expansion interface sites), *TORNADO-548/549/5402/5410/5416* DSP systems only.

CAUTION

Different *TORNADO-54x* DSP systems provide different options for configuring *XIO-0/1* pins of on-board SIOX/PIOX-16 interface sites.

Configuring *XIO-0/1* Pins of SIOX/PIOX-16 Interface Sites for *TORNADO-542L* DSP System

TORNADO-542L DSP system provides hardware configuration for *XIO-0* pin of SIOX/PIOX-16 interface sites via the on-board J3 jumper, whereas the *XIO-1* pin of SIOX/PIOX-16 interface sites is always configured as I/O pin.

CAUTION

TORNADO-542L DSP system assumes *XIO-0* pin of SIOX/PIOX-16 interface sites to be configured by the on-board J3 jumper (refer to fig.A-1) as either I/O pin (*XIOF-0* IOX flag) or as TMS320C542 DSP on-chip timer output (*TM*).

XIO-1 pin of SIOX/PIOX-16 interface sites of *TORNADO-542L* DSP system is always configured as I/O pin (*XIOF-1* IOX flag).

Configuring *XIO-0/1* Pins of SIOX/PIOX-16 Interface Sites for *TORNADO-548/549/5402/5410/5416* DSP Systems

TORNADO-548/549/5402/5410/5416 DSP systems rev.2x provides extremely flexible software control for configuration of *XIO-0/1* pins of the on-board SIOX and PIOX-16 expansion interface sites via *XIO-CNF* IOX register, which can be accessed by the on-board DSP.

CAUTION

TORNADO-548/549 DSP systems rev.1x did not provide software configuration for *XIO-0* pin of SIOX/PIOX-16 interface sites as either I/O pin or TMS320C54x DSP timer output. Instead, the on-board jumper was used for setting configuration of *XIO-0* pin as either I/O pin or TMS320C54x DSP timer output (*TM*).

CAUTION

TORNADO-548/549/5410/5416 DSP systems assume *XIO-0* pin of SIOX/PIOX-16 interface sites to be software configured as either I/O pin (*XIOF-0* IOX flag) or as TMS320C54x DSP on-chip timer output (*TM*).

XIO-1 pin of SIOX/PIOX-16 interface sites of *TORNADO-548/549/5410/5416* DSP systems is always configured as I/O pin (*XIOF-1* IOX flag).

CAUTION

TORNADO-5402 DSP system assumes *XIO-0* pin of SIOX/PIOX-16 interface sites to be software configured as either I/O pin (*XIOF-0* IOX flag) or as TMS320VC5402 DSP on-chip timer output (*TM*).

XIO-1 pin of SIOX/PIOX-16 interface sites of *TORNADO-5402* DSP system is always configured as I/O pin (*XIOF-1* IOX flag) in case the HPI port of on-board TMS320VC5402 DSP is enabled. In case the HPI port of on-board TMS320VC5402 DSP is disabled, then the *XIO-1* pin of SIOX/PIOX-16 interface sites might be configured as either I/O pin (*XIOF-1* IOX flag) or as output of the second TMS320VC5402 DSP on-chip timer (*TM1*).

XIO-CNF IOX register configures the *XIO-0* pin and *XIO-1* pin (*TORNADO-5402* only) of SIOX/PIOX-16 expansion interface sites of *TORNADO-548/549/5402/5410/5416* DSP systems. *XIO-CNF* IOX register might be accessed by DSP via IOX area in accordance with table 2-2, and has the following data format:

XIO-CNF IOX Register (r/w)

X	X	X	X	X	X	X	<i>XIO-1_CNF</i> (r/w, 0+) (TORNADO-5402)	<i>XIO-0_CNF</i> (r/w, 0+) (TORNADO-548/549/5410/5416)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Logical '0' for *XIO-0_CNF* bit (this value is set as default on the DSP reset) denotes that the *XIO-0* pin of SIOX/PIOX-16 expansion interface sites of *TORNADO-548/549/5402/5410/5416* DSP systems is configured as the *XIOF-0* I/O flag. Logical '1' for *XIO-0_CNF* bit denotes that the *XIO-0* pin of SIOX/PIOX-16 expansion interface sites of *TORNADO-548/549/5402/5410/5416* DSP systems is configured as the DSP on-chip timer output (*TM*).

For *TORNADO-548/549/5410/5416* DSP systems the *XIOF-1* I/O flag is directly wired to SIOX and PIOX-16 expansion interface sites as it is available in *TORNADO-542L* DSP system.

CAUTION

The *XIO-1_CNF* bit of *XIO-CNF* IOX register is available for *TORNADO-5402* DSP systems only.

The *XIO-1_CNF* bit might be set by on-board TMS320VC5402 DSP software only when the DSP HPI port is disabled by host PC software (refer to the '*Host ISA-bus I/O Interface*' section later in this chapter for details how to enable/disable the HPI port for *TORNADO-5402* DSP systems).

It is recommended that the on-board TMS320VC5402 DSP software verifies the post-write value of *XIO-1_CNF* bit of *XIO-CNF* IOX register in case the *XIO-1_CNF*=1 state should be programmed. Once the *XIO-1_CNF* bit does not set to the *XIO-1_CNF*=1 state, then the HPI port is enabled.

In case the TMS320VC5402 DSP on-chip HPI port for *TORNADO-5402* is disabled (refer to '*Host ISA-bus I/O Interface*' section later in this chapter for details how to enable/disable the HPI port for *TORNADO-5402* DSP system), then the output of second TMS320VC5402 DSP on-chip timer (*TM1*) might be programmed to appear on the *XIO-1* pin of SIOX/PIOX-16 expansion interface sites in case the *XIO-1_CNF* bit of *XIO-CNF* IOX register is set to logical '1'. In case the *XIO-1_CNF* bit of *XIO-CNF* IOX register is set to logical '0', then the *XIO-1* pin of SIOX/PIOX-16 expansion interface sites is configured as *XIOF-1* I/O flag.

Once the TMS320VC5402 DSP on-chip HPI port for *TORNADO-5402* DSP system is enabled, then the *XIO-1_CNF* bit of *XIO-CNF* IOX register is ignored and the *XIO-1* pin of SIOX/PIOX-16 expansion interface sites of *TORNADO-5402* DSP system is configured as *XIOF-1* I/O flag.

CAUTION

Enable/disable control for TMS320VC5402 DSP on-chip HPI port for *TORNADO-5402* DSP system might be changed only while DSP is in the reset state (refer to ‘*Host ISA-bus I/O Interface*’ section later in this chapter for details how to enable/disable the HPI port for *TORNADO-5402* DSP system).

XIOF-0/1 I/O Flags

XIOF-0/1 I/O flags are used as expansion of DSP I/O facilities and might be configured to be available at the *XIO-0/1* I/O pins of *TORNADO-54x* on-board SIOX/PIOX-16 interface sites for control of compatible DCM. Each of *XIOF-0/1* I/O flags might be independently programmed as input or output flag.

XIOF-0/1 flag control registers are available within the IOX area of TMS320C54x DSP environment in accordance with table 2-2 and comprise of the following registers:

- *XIOF-DIR* IOX register (*XIOF* flags direction register)
- *XIOF-DATA* IOX register (*XIOF* flags data register)

XIOF-DIR register configures direction for *XIOF-0/1* I/O flags and might be accessed by TMS320C54x DSP via IOX area in accordance with table 2-2, and has the following data format:

***XIOF-DIR* IOX Register (r/w)**

x	x	x	x	x	x	x	<i>XIOF-1_DIR</i> (r/w, 0+)	<i>XIOF-0_DIR</i> (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Logical ‘0’ for *XIOF-0_DIR* and *XIOF-1_DIR* bits corresponds to configuring the corresponding *XIOF-0/1* I/O flag as input, whereas logical ‘1’ corresponds to configuring the corresponding *XIOF-0/1* I/O flag as output. *XIOF-0_DIR* and *XIOF-1_DIR* bits of *XIOF-DIR* register defaults to ‘0’ during DSP reset.

XIOF-DATA register specifies current state of *XIOF-0/1* I/O flags and might be accessed by TMS320C54x DSP via IOX area in accordance with table 2-2, and has the following data format:

***XIOF-DATA* IOX Register (r/w)**

x	x	x	x	x	x	x	<i>XIOF-1</i> (r/w, 0+)	<i>XIOF-0</i> (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Note, that in case any of *XIOF-0/1* I/O flags is configured as input, then writing to the corresponding bit of *XIOF-DATA* register is ignored, however data written will be hold in *XIOF-DATA* register and will appear on *XIOF-0/1* output as soon as it will be configured as the output.

SB Locking by the on-board TMS320C54x DSP Master

SB locking technique is used for processing of software shared semaphores that can be allocated in on-board SRAM or PIOX shared resources.

SB locking/unlocking by the on-board TMS320C54x DSP master is performed by means of *MLock* IOX flag (refer to table 2-2). *MLock* flag can be set/reset by TMS320C54x DSP via IOX area in accordance with table 2-2. Note, that when writing or reading to/from *MLock* IOX register, only bit D0 is valid:

Mlock IOX Register (r/w)

X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	<i>Mlock</i> (r/w, 0+)
bit-15	bit-14	bit-13	bit-12	bit-12	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

When *MLock* flag is set to logical '0' (this value is set as default on TMS320C54x DSP reset), then there is no active SB locking from on-board TMS320C54x DSP, and both TMS320C54x DSP and host ISA-bus memory interface can access shared SB resources.

When *MLock* flag is set to logical '1', then there active SB locking from on-board TMS320C542 DSP and SB access from host ISA-bus memory interface will be pending until SB will be unlocked by TMS320C54x DSP (*MLock* flag will be set to logical '0').

The SB lock-to-unlock time interval is not limited by *TORNADO-54x* hardware, however long duration of SB locking by DSP may cause timeout access faults for SB accesses by host ISA-bus memory interface.

The following is an example of C-code for TMS320C54x DSP that demonstrates processing of software shared semaphore using SB locking technique:

```

...
ioport unsigned port8001;          /* declare MLock I/O port */
#define SET_XF1      asm(" ssbx xf") /* declare MACROS to set XF=1 */
int Sem;                          /* declare software shared semaphore Sem */

...
SET_XF1;
while (1)
{
    port8001=1;          /* lock SB */
    if (Sem==0) break;    /* verify for semaphore is free (Sem=0)*/
    port8001=0;          /* unlock SB and repeat */
}

Sem=1;                   /* semaphore is free, set it to Sem=1 */
port8001=0;              /* and unlock SB */

...
...                       /* perform some critical data processing */
...
port8001=1;              /* reset semaphore using SB locking */
Sem=0;
port8001=0;              /* unlock SB */
...

```

Note that *TORNADO-54x* provide hardware timeout control for SB granting wait time. This hardware timeout interval is setup to 6 μ sec. In case timeout will occur due to SB locking by DSP, the *SB_ERROR* flag in *FLAG STATUS REGISTER* of host ISA-bus I/O interface will be set to the *SB_ERROR=1* state. This will result in

cancellation of all further SB requests from host ISA-bus memory interface until the **SB_ERROR** flag will be reset to the **SB_ERROR=0** state by host PC software.

CAUTION

Time interval between SB locking and unlocking by the on-board TMS320C54x DSP should not exceed 2.5 μ S in order to avoid timeout condition on host-to-SB access.

Generating DSP-to-host requests

TORNADO-54x supports attention request (interrupt request) from the on-board TMS320C54x DSP to host IBM PC CPU in order to synchronize between program execution in host and on-board DSP environments. Two methods for generation of DSP-to-host requests are supported in **TORNADO-54x**:

- **MH_RQ** (master to host request), that results in setting flag **MH_RQ** in **SYS_STATUS_FRG** flag register in host ISA-bus I/O interface. **MH_RQ** is generated when the on-board TMS320C54x DSP executes I/O write cycle to **MH_RQ** IOX register (refer to table 2-2). Data written to this I/O port is ignored. Generation of **MH_RQ** DSP-to-host request results in setting flag **MH_RQ** in **FLAG STATUS REGISTER** of host ISA-bus I/O interface into the **MH_RQ=1** state and may generate active host PC interrupt request in case **MH_RQ_IE** bit in the **CONTROL REGISTER** from host ISA-bus I/O interface is set to the **MH_RQ_IE=1** state.. The following is an example of C-code for TMS320C54x DSP that generates request to the host PC:

```

...
ioport unsigned port8000;                /* declare MH-RQ I/O port */
#define SET_XF1      asm(" ssbx xf")      /* declare MACROS to set XF=1 */
...
SET_XF1;
port8000=0;                             /* DSP-to-host request is generated */
...

```

- **HPI_HINT** (host interrupt request via HPI), that results in setting bit **HINT** of HPIC register of TMS320C54x HPI and flag **HPI_HINT** in **SYS_STATUS_FRG** flag register of host ISA-bus I/O interface. **HPI_HINT** can generate active host PC interrupt request in case **HPI_HINT_IE** bit in **HPI_IE_FRG** flag register from host ISA-bus I/O interface is set to **HPI_HINT_IE=1** state.

Processing request from host PC

TORNADO-54x supports attention request (interrupt request) from host PC to TMS320C54x DSP in order to synchronize between the program execution in host and on-board DSP environments. Two methods for generation of host-to-DSP requests is supported in **TORNADO-54x**:

- **HM_RQ** (host to master request), that results in generation of active **INT3** external interrupt request for the on-board TMS320C54x DSP. In order to generate output **HM_RQ** flag, host PC software has to write any data into **SET_HM_RQ_FRG** flag register from host ISA-bus I/O interface. User software for the TMS320C54x DSP should provide processing of **INT3** hardware interrupt request in accordance with software requirements. This is the recommended method for generation of host-to-DSP request since it delivers compatibility with all other **TORNADO** DSP systems for PC.

- *HPI_DSPINT* (host-to-DSP interrupt via HPI), that results in setting bit *DSPINT* in HPIC register of TMS320C54x HPI and generation *HPIINT* on-chip interrupt request for TMS320C54x DSP. In order to generate *HPI_DSPINT* interrupt request to DSP, host PC software has to write 0505H hex value to HPIC register of TMS320C54x DSP via host ISA-bus I/O interface. User software for the TMS320C54x DSP should provide processing of *HPIINT* interrupt request in accordance with software requirements. This is the **TORNADO-54x** specific method for generation of host-to-DSP request, and it is recommended for simulation of host-to-DSP communication via TMS320C54x DSP on-chip HPI.

External hardware interrupts for TMS320C54x DSP

TORNADO-54x on-board TMS320C54x DSP supports four external hardware interrupt requests *INT0...INT3* with the *INT0* request having the highest priority. These requests correspond to the following events:

- *INT0...INT2* interrupt requests can be generated by SIOX/PIOX-16 daughter modules
- *INT3* is on-board wired for software request *HM_RQ* from host PC to TMS320C54x DSP.

TORNADO-54x hardware provides direct wiring of external interrupt request source signals to the corresponding *INT0...INT3* pins of TMS320C54x DSP chip. All *INT0...INT3* external interrupt request pins of TMS320C54x DSP are edge-triggered (active interrupt is generated on falling edge) and allow pulse ($\tau_p > 40\text{ns}$) or static external interrupt request signals to applied to these input pins.

SIOX interface sites

TORNADO-54x provides two serial I/O expansion interface (SIOX) sites (SIOX-A and SIOX-B) for compatible AD/DA/DIO DCM.

SIOX comprises of the TMS320C54x DSP-on-chip BSP/TDM serial ports control lines (BSP/TDM/BSP1 for **TORNADO-548/549/5402/5410/5416**), DSP-on-chip timer output, *XIOF-0/1* I/O flags, *INT0..2* external interrupt requests and $\pm 5\text{v}/\pm 12\text{v}$ ISA-bus power supply lines. For details about SIOX sites refer to the corresponding section later in this chapter.

Generating Reset Signal for SIOX/PIOX-16 Expansion Interface Sites for TORNADO-548/549/5402/5410/5416

TORNADO-548/549/5402/5410/5416 rev.2C allows generation of individual reset signals for for SIOX and PIOX-16 expansion interface sites (refer to the corresponding sections later in this chapter) using the following logical conditions:

- all SIOX/PIOX reset signals are active in case on-board DSP is in the 'RESET' state
- the corresponding SIOX/PIOX reset signal(s) might be released only in case DSP is in the 'RUN' state and the corresponding bit(s) of *PXSX_RUN* IOX register is(are) set to logical '1' value by DSP software.

This allows correct initialization of the SIOX/PIOX daughter-card hardware and correct synchronization with the DSP software.

CAUTION

TORNADO-548/549/5402/5410/5416 rev.2C hardware provides different on-board logic for generation of SIOX/PIOX reset signals if compared to the earlier revisions of *TORNADO-548/549/5402/5410/5416* hardware.

TORNADO-548/549/5402/5410/5416 rev.2B and earlier generate common SIOX/PIOX reset signal using *XRESET* IOX register, and this reset signal was generated as the logical OR between the DSP reset signal and bit D0 of *XRESET* IOX register.

PXSX_RUN IOX register comprises of bits for individual ‘RESET’ control for PIOX-16, SIOX-A and SIOX-B interface sites.

PXSX_RUN IOX register might be set by the DSP software only (refer to table 2-2). Note, that when writing or reading to/from *PXSX_RUN* IOX register, only bits D0..D2 are valid.

***PXSX_RUN* IOX Register (r/w)**

x	x	x	x	x	x	<i>SIOX-B_RUN</i> (r/w, 0+)	<i>SIOX-A_RUN</i> (r/w, 0+)	<i>PIOX_RUN</i> (r/w, 0+)
bit-31...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

In case DSP is in the ‘RUN’ state (refer to section 2.5 for more details), then the corresponding reset signals for SIOX/PIOX-16 expansion interface sites can be released by means of writing ‘1’ value to the corresponding bit of *PXSX_RUN* IOX register, thus allowing operation of the corresponding SIOX/PIOX-16 DCM hardware. Writing logical ‘0’ to the corresponding bit of *PXSX_RUN* IOX register, which is also the default value on the DSP reset condition, will set the corresponding reset signal for SIOX/PIOX-16 expansion interface sites.

2.4 Host ISA-bus Memory Interface

Host ISA-bus memory interface of *TORNADO-54x* is designed to transfer data between host PC environment and *TORNADO-54x* on-board SRAM/PIOX-16 SB resources without any software overhead for both host PC and on-board TMS320C54x DSP sides.

The SB address space appears in host ISA-bus memory interface as a series of dual-access 32KB *shared memory pages (SMP)*, which are mapped onto the ISA-bus UMB (upper memory blocks) memory window by means of *SB PAGE MAPPER* register in host ISA-bus I/O interface. The SB can be accessed by host ISA-bus memory interface by means of random accesses to software variables or data arrays that are allocated within *SMP*, or by means of block data transfers between PC main memory and *SMP* using either host i80x86 CPU MOVSB/MOVSX/etc instructions or host DMA controller.

Host ISA-bus memory interface issues SB request and provides SB access using 16-bit data cycles each time host PC performs ISA-bus memory read/write cycle within the ISA-bus *SMP* address range. Particular selection of the UMB area is performed by host software by programming the *ISA_MI_BADDR_FRG* flag register of host ISA-bus I/O interface.

SMP ISA-bus Memory Base Address

SMP ISA-bus memory base address can be set within the ISA-bus UMB (upper memory blocks) memory address range by means of programming the *ISA_MI_BADDR_FRG* flag register from *TORNADO-54x* host ISA-bus I/O interface (refer to section 2.5) in accordance with predefined configuration settings in table 2-3. Only three least significant bits of *ISA_MI_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes.

***ISA_MI_BADDR_FRG* Flag Register** (r/w)

0	0	0	0	0	<i>MI_BA2</i> (r/w, 0+)	<i>MI_BA1</i> (r/w, 0+)	<i>MI_BA0</i> (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-3. ISA-bus memory base address for *SMP*.

ISA-bus memory base address for <i>SMP</i>	ISA-bus memory address range for <i>SMP</i>	bit settings for <i>ISA_MI_BADDR_FRG</i> flag register		
		<i>bit#2</i> <i>MI_BA2</i>	<i>bit#1</i> <i>MI_BA1</i>	<i>bit#0</i> <i>MI_BA0</i>
<i>SMP is switched OFF</i>	-	0	0	0
<i>B8000H</i>	<i>B8000H ... BFFFFH</i>	0	0	1
<i>C0000H</i>	<i>C0000H ... C7FFFH</i>	0	1	0
<i>C8000H</i>	<i>C8000H ... CFFFFH</i>	0	1	1
<i>D0000H</i>	<i>D0000H ... D7FFFH</i>	1	0	0
<i>D8000H</i>	<i>D8000H ... DFFFFH</i>	1	0	1
<i>E0000H</i>	<i>E0000H ... E7FFFH</i>	1	1	0
<i>E8000H</i>	<i>E8000H ... EFFFFH</i>	1	1	1

Notes:

1. The highlighted configuration corresponds to power on default value.

TORNADO-54x, as well as all other *TORNADO* DSP systems for PC ISA-bus host computer, offers software control for the **SMP** activity, i.e. switching **SMP** to either 'ON' or 'OFF' state in ISA-bus memory address space.

CAUTION

SMP is activated and appears in ISA-bus memory address space after loading any non-zero value to *ISA_MI_BADDR_FRG* flag register in accordance with table 2-3.

SMP is de-activated and disappears from ISA-bus memory address space after loading the zero value to *ISA_MI_BADDR_FRG* flag register.

Software control over *SMP* activity in *TORNADO-54x* delivers rational usage of deficit UMB area in host PC and allows multiple *TORNADO* DSP systems to operate within one PC environment.

Software Applications for ISA-bus Memory Interface

Once *TORNADO-54x* host ISA-bus memory interface provides direct mapping of 32KB *SMP* onto ISA-bus UMB window, the following host-to-SB data transfer techniques are applicable:

- random access to variables or data arrays allocated within the *SMP* by host PC software
- block data transfers using *MOVS/MOVSb/MOVSsw* instructions of host PC i80x86 CPU
- block data transfers under control of host PC DMA controller using memory-to-memory or memory-to-port transfer cycles.

Operation Description for ISA-bus Memory Interface

The SB access from host ISA-bus memory interface is performed under hardware control of the on-board programmable *SB Access Controller* from ISA-bus interface of *TORNADO-54x*. Timing diagram for SB read cycle invoked by ISA-bus memory interface is presented at fig.2-3.

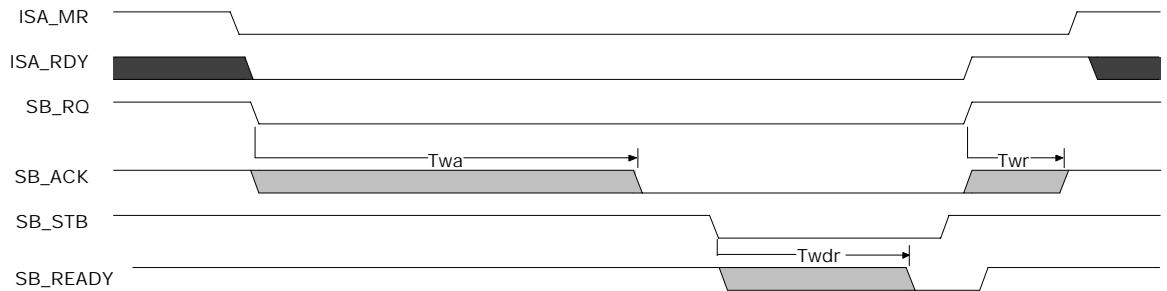


Fig.2-3. Timing diagram of SB read cycle invoked by ISA-bus memory interface.

Any request to the *SMP* memory address space on the host ISA-bus (*ISA_MR*=0 or *ISA_MW*=0) will result in activation of host ISA-bus memory interface that will immediately generate request to SB arbiter (*SB_RQ*=0) and set ISA-bus data ready signal to 'NOT READY' state (*ISA_RDY*=0). Host ISA-bus interface will stay in this state until SB will be granted (*SB_ACK*=0) by SB arbiter. SB will be granted at least after T_{wa} =50ns delay.

After that, the SB access cycle will be generated by host ISA-bus memory interface with *SB_STB* signal set to the *SB_STB*=0 state. Host ISA-bus memory interface will now wait for *SB_READY* signal comes true (*SB_READY*=0) in order to finish current SB access cycle. SB data ready signal *SB_READY* will come true

($SB_READY=0$) after T_{wdr} delay after SB_STB will come active ($SB_STB=0$). Wait time for SB_READY signal depends upon the SB address subspace selected (refer to table 2-1). Minimum wait time for SB_READY data ready signal is $T_{wdr}=0ns$ and corresponds to accessing on-board SRAM area, whereas accesses PIOX-16 interface require at least 1ws with further awaiting for $PIOX_READY$ signal sets true. After SB_READY signal sets true, the SB_RQ signal is removed ($SB_RQ=1$) and ISA_RDY signal is set to $ISA_RDY=1$ state in order to finish current ISA-bus memory access cycle. SB_ACK signal will return to its inactive state ($SB_ACK=1$) within $T_{wr}=25ns$ after SB_RQ will be removed ($SB_RQ=1$).

SB Access Timeout Control

TORNADO-54x provides hardware timeout control for the SB grant and for SB data ready conditions during host-to-SB access. This avoids idling and crashing of host PC environment.

The hardware timeout for both SB grant and SB data ready conditions vary for different **TORNADO-54x** DSP systems and are equal to:

- 6.2 μ sec for 40 MIPS **TORNADO-542L**
- 3.1 μ sec for 80 MIPS **TORNADO-548** and for 80 MIPS **TORNADO-5416**
- 2.5 μ sec for 100 MIPS **TORNADO-549/5402/5410**.

Once SB grant of SB ready timeout condition occurs, then the SB_ERROR bit of SYS_STATUS_FRG flag register of host ISA-bus I/O interface will be set to the $SB_ERROR=1$ state. This will cancel current host-to-SB access and returned data will be undefined. The $SB_ERROR=1$ condition can generate interrupt request to host PC in case SB_ERROR_IE bit of **CONTROL REGISTER** of host ISA-bus I/O interface is set to the '1' state.

The SB_ERROR bit can be reset by host software by writing to the $CLEAR_SB_ERROR_FRG$ write-only flag register of host ISA-bus I/O interface.

Data Formats for Host SB Data Access Cycles

TORNADO-54x DSO systems support only 16-bit SB data access cycles for both DSP and host ISA-bus memory interface.

However, PC can access **SMP** using both 8-bit and 16-bit ISA-bus memory cycles. In case 16-bit ISA-bus memory cycle is generated within **SMP** address space, then this will result in immediate generation of SB request and SB access cycle on SB grant. However, in case 8-bit ISA-bus memory cycle is generated within **SMP** address space, then SB request will be generated only if MSB (most significant byte) is accessed during ISA-bus memory write cycle or if LSB (least significant byte) is accessed during ISA-bus memory read cycle. The corresponding LSB for memory write cycle is acquired from the on-board register transceiver, which stores LSB data since previous access to LSB during ISA-bus memory write cycle. Similar, the corresponding MSB will be latched in on-board register transceiver during memory read from LSB, and will be read later when ISA-bus memory read cycle to MSB will be generated.

SB Locking by Host ISA-bus Memory Interface

SB locking is used in order to lock SB access when processing software shared semaphores allocated in SRAM/PIOX-16 SB resources.

SB locking by ISA-bus memory interface may be set by means of setting either the SB_GLOCK bit or SB_LOCK bit of **CONTROL REGISTER** from ISA-bus I/O interface.

Timing diagrams of SB locking using *SB_GLOCK* and *SB_LOCK* bits are presented at fig. 2-4 and fig. 2-5.

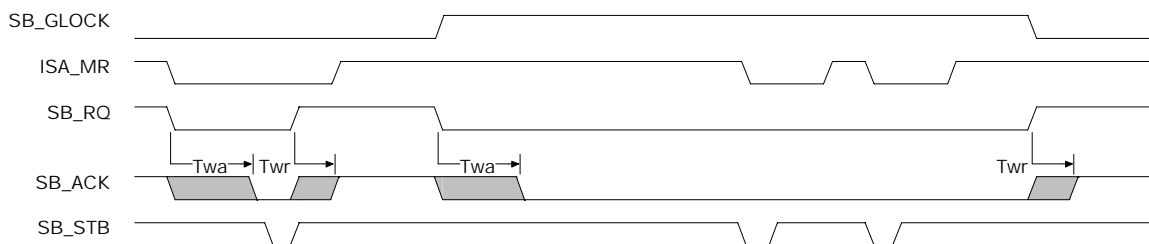


Fig.2-4. Timing diagram for SB access cycle invoked by ISA-bus memory interface with SB locking using *SB_GLOCK* bit.

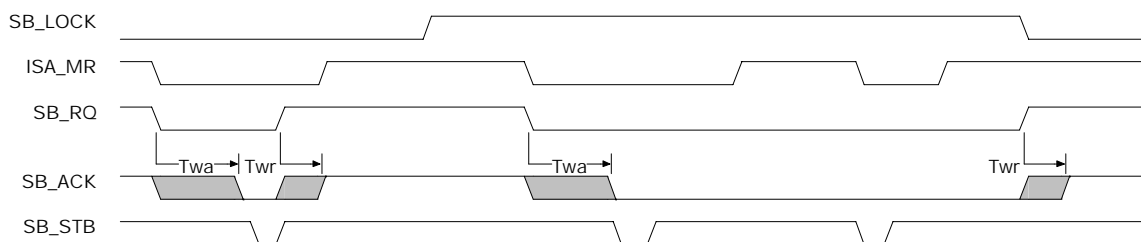


Fig.2-5. Timing diagram for SB access cycle invoked by ISA-bus memory interface with SB locking using *SB_LOCK* bit.

CAUTION

SB locking by ISA-bus memory interface using *SB_GLOCK* and *SB_LOCK* bits of *CONTROL REGISTER* from ISA-bus I/O interface should be used for short-time SB locking.

Continuous SB locking by ISA-bus memory interface using *SB_GLOCK* and *SB_LOCK* bits may result in continuous holding of TMS320C54x DSP (in case it requests access to SB data) and may lead to significant time distortions of real-time data processing.

2.5 Host ISA-bus I/O Interface

TORNADO-54x host ISA-bus I/O interface should be used for *TORNADO-54x* system control, accessing TMS320C54x DSP on-chip HPI, and interrupt handshaking between host PC CPU and TMS320C54x DSP.

I/O Base Address of Host ISA-bus I/O Interface

Host ISA-bus I/O interface occupies sixteen 8-bit registers inside ISA-bus I/O address space. Base address of host ISA-bus I/O interface is defined by means of 3-button on-board DIP-switch SW1 (refer to fig.2-2) in accordance with predefined settings listed in table 2-4.

Table 2-4. ISA-bus I/O base address for host ISA-bus I/O interface.

ISA-bus I/O base address for Host ISA-bus I/O interface	ISA-bus I/O address range	button SW1-3	button SW1-2	button SW1-1
300H	300H..30FH	OFF	OFF	OFF
310H	310H..31FH	OFF	OFF	ON
320H	320H..32FH	OFF	ON	OFF
330H	330H..33FH	OFF	ON	ON
340H	340H..34FH	ON	OFF	OFF
350H	350H..35FH	ON	OFF	ON
360H	360H..36FH	ON	ON	OFF
370H	370H..37FH	ON	ON	ON

Note:

1. Highlighted configuration corresponds to the factory setting.

ISA-bus I/O Interface Registers

List of *TORNADO-54x* ISA-bus I/O interface registers is presented in table 2-5.

Table 2-5. Register set of Host ISA-bus I/O interface.

register #	register address	access mode	reset value	description
#0	BA+0	r/w	00H	SB PAGE MAPPER (LSB)
#1	BA+1	r/w	00H	SB PAGE MAPPER (MSB)
#2	BA+2	r/w	10H	CONTROL REGISTER
#3	BA+3	r/w	-	FLAG DATA REGISTER
		or	-	FLAG STATUS REGISTER
		r/w	-	FLAG CONTROL REGISTER
#403	BA+403H	r/w	00H	FLAG SELECTOR REGISTER
#4	BA+4			reserved (do not use)
#5	BA+5			reserved (do not use)
#6	BA+6			reserved (do not use)
#7	BA+7			reserved (do not use)
#8	BA+8	r/w	refer to TI documentation	HPIC (LSB) register (TMS320C54x HPI)
#9	BA+9	r/w	refer to TI documentation	HPIC (MSB) register (TMS320C54x HPI)
#10	BA+10	r/w	-	HPI Data Latch (LSB) register (HPIDAI) with HPI address autoincrement facility (TMS320C54x HPI)
#11	BA+11	r/w	-	HPI Data Latch (MSB) register (HPIDAI) with HPI address autoincrement facility (TMS320C54x HPI)
#12	BA+12	r/w	-	HPI Address Latch (LSB) register (HPIA), (TMS320C54x HPI)
#13	BA+13	r/w	-	HPI Address Latch (MSB) register (HPIA), (TMS320C54x HPI)
#14	BA+14	r/w	-	HPI Data Latch (LSB) register (HPID) without HPI address autoincrement facility (TMS320C54x HPI)
#15	BA+15	r/w	-	HPI Data Latch (MSB) register (HPID) without HPI address autoincrement facility (TMS320C54x HPI)

Notes:

1. 'BA' denotes ISA-bus I/O base address of host ISA-bus I/O interface in accordance with table 2-5.

2. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.
3. All HPI registers access should be performed with bit *BOB* of HPI HPIC register being set to *BOB*=1 value. This correspond to LSB first data transmission protocol for ISA-bus host.

SB PAGE MAPPER Register

Registers #0 and #1 of **TORNADO-54x** ISA-bus I/O interface are least significant byte (LSB) and most significant byte (MSB) of 16-bit **SB PAGE MAPPER** register, which is used to setup the **SMP** SB base address in PROGRAM/DATA/IO SB areas in 16Kx16 (32Kx8) increments. Default reset value for **SB PAGE MAPPER** register is 0000H.

SB PAGE MAPPER LSB register comprises of bits **A14..A15** for **TORNADO-542L**, of bits **A14..A16** for **TORNADO-5402**, and of bits **A14..A17** for **TORNADO-548/549/5402/5410/5416** of SB address and **I/O** and **D/P** SB area selector bits. All other bits of **SB PAGE MAPPER LSB** and **SB PAGE MAPPER MSB** registers are ignored on writing and are read as zeros. The **A0..A13** bits of SB address for 16-bit SB words within **SMP** are derived from ISA-bus memory address bits **ISA_A1..ISA_A14**, whereas address bit **ISA_A0** is used to select particular byte within addressed 16-bit **SMP** SB word.

SB PAGE MAPPER (LSB) (r/w)

0	0	0	0	0 (TORNADO-542L/5402)	0 (TORNADO-542L)	A15 (r/w, 0+)	A14 (r/w, 0+)
				A17 (r/w, 0+) (TORNADO-548/549/5410/5416)	A16 (r/w, 0+) (TORNADO-548/549/5402/5410/5416)		
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

SB PAGE MAPPER (MSB) (r/w)

I/O (r/w, 0+)	D/P (r/w, 0+)	0	0	0	0	0	0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Particular SB area accessed is defined by bits **I/O** and **D/P** of **SB PAGE MAPPER MSB** register in accordance with table 2-6.

Table 2-6. SB Area Selector for Host-to-SB Accesses.

SB Area	I/O bit of SB PAGE MAPPER MSB register	D/P bit of SB PAGE MAPPER MSB register
SRAM/PROGRAM area 64Kx16 for <i>TORNADO-542L</i> 128Kx16 for <i>TORNADO-548/549/5402/5410/5416</i>	0	0
SRAM/DATA area 64Kx16 for <i>TORNADO-542L</i> 128Kx16 for <i>TORNADO-548/549/5402/5410/5416</i>	0	1
PIOX-16 area (64Kx16)	1	x

Note: 1. Highlighted configuration corresponds to default power-on setting.

It is important to note some specifics of extended memory addressing for *TORNADO-548/549/5402/5410/5416* DSP systems.

CAUTION

If SRAM/PROGRAM area (128Kx16) of *TORNADO-548/549/5402/5410/5416* is selected, then bits *A14..A16* of *SB PAGE MAPPER LSB* are used, and bit *A17* is ignored.

If SRAM/DATA area (4x32Kx16) of *TORNADO-548/549/5410/5416* is selected, then all *A14..A17* bits of *SB PAGE MAPPER LSB* are used, however actual SB access is performed only if bit *A14*=1, i.e. the addressed DATA memory area corresponds to the TMS320LC548/VC549/VC5410/VC5416 DSP off-chip data memory area.

If SRAM/DATA area (2x64Kx16) of *TORNADO-5402* is selected, then bits *A14..A16* of *SB PAGE MAPPER LSB* are used, however actual SB access is performed only if bits {*A15*, *A16*} are any of the {1,0}, {0,1} and {1,1} combinations, i.e. the addressed DATA memory area corresponds to the TMS320LC5402 DSP off-chip data memory area.

CONTROL Register

Register #2 of *TORNADO-54x* ISA-bus I/O interface is called **CONTROL REGISTER**. It used for reset control of on-board TMS320C54x DSP, for configuration of ISA-bus memory interface and for DSP-to-host interrupt communication.

CONTROL REGISTER (r/w)

SB_ERROR_IE (r/w, 0+)	MH_RQ_IE (r/w, 0+)	0 (reserved)	1 (reserved)	SB_LOCK (r/w, 0+)	SB_GLOCK (r/w, 0+)	0 (reserved)	M_GO (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-7 contains detail description for bits and bit fields of **CONTROL REGISTER**. Note, that some bits of **CONTROL REGISTER** are reserved for compatibility with other **TORNADO** DSP systems, and are ignored on writing and read as shown above.

Table 2-7. Bit description of **CONTROL REGISTER**.

bit of CONTROL REGISTER	power on default state	description
M_GO	0	On-board TMS320C54x DSP reset line control: <ul style="list-style-type: none"> '0' corresponds to the 'RESET' state for the on-board TMS320C54x DSP '1' corresponds to the 'RUN' state for the on-board TMS320C54x DSP (i.e. the on-board DSP is in the program execution mode)
SB_GLOCK	0	Shared Bus Global Lock. With the SB_GLOCK =1 the SB access controller of ISA-bus memory interface generates active SB locking.
SB_LOCK	0	Shared Bus Lock. With the SB_LOCK =1 the SB access controller of ISA-bus memory interface generates active SB locking starting from first next SB request cycle after the SB_LOCK bit is set to the SB_LOCK =1.
MH_RQ_IE	0	Master TMS320C54x DSP to Host Request Interrupt Enable. If MH_RQ_IE =1 and MH_RQ =1, active interrupt request to host PC is generated. Host PC interrupt request is logical OR between (MH_RQ_IE & MH_RQ), (SB_ERROR_IE & SB_ERROR), (HPI_ERROR_IE & HPI_ERROR) and (HPI_HINT_IE & HPI_HINT) logic terms.
SB_ERROR_IE	0	SB Error Interrupt Enable. If SB_ERROR_IE =1 and SB_ERROR =1, active interrupt request to host PC is generated. Host PC interrupt request is logical OR between (MH_RQ_IE & MH_RQ), (SB_ERROR_IE & SB_ERROR), (HPI_ERROR_IE & HPI_ERROR) and (HPI_HINT_IE & HPI_HINT) logic terms.

Accessing TMS320C54x DSP on-chip HPI port

TORNADO-54x host ISA-bus I/O interface supports optional DSP-to-host communication via TMS320C54x DSP on-chip HPI port (refer to original TI documentation about details on TMS320C54x HPI port).

CAUTION

The TMS320C54x DSP on-chip HPI port feature is always enabled for *TORNADO-542L/548/549/5410/5416* DSP systems.

In *TORNADO-5402* DSP systems, the TMS320VC5402 DSP on-chip HPI port might be enabled/disabled by host PC software via the *HPI_DISABLE* bit of *HPI_IE_FRG* flag register (refer to subsection below in this section). This feature also allows alternative disable/enable for output of the second TMS320VC5402 DSP on-chip timer for SIOX and PIOX-16 expansion interface sites of *TORNADO-5402* in accordance with the *XIOF-TM_CNF IOX* register from the TMS320VC5402 DSP environment (refer to '*DSP Environment*' section earlier in this chapter).

CAUTION

The TMS320C54x DSP on-chip HPI port of *TORNADO-542L/548/549/5410/5416* DSP systems can operate when DSP is either in the 'RESET' or 'RUN' state.

The TMS320C5402 DSP on-chip HPI port of *TORNADO-5402* DSP system can operate only when DSP is in the 'RUN' state.

Along with the on-board SB SRAM, the TMS320C54x DSP on-chip HPI port is a second data path for communication between DSP and host via DSP shared memory areas.. Along with data communication, mutual DSP-to-host (*HPI_HINT*) and host-to-DSP (*HPI_DSPINT*) interrupts are supported. On the host PC side, the *HPI_HINT* DSP-to-host interrupt can be individually masked and generate PC ISA-bus interrupt.

CAUTION

TORNADO-542L/548/549 DSP system allows Host-to-DSP communication using DSP on-chip HPI port via dedicated 2Kx16 DSP on-chip shared memory area only (DSP data memory address range 0x1000...0x17ff, which corresponds to Host HPI address range 0x0000...0x07ff).

TORNADO-5402 DSP system allows Host-to-DSP communication using DSP on-chip HPI port via entire 16Kx16 DSP on-chip memory (DSP data memory address range 0x0060...0x3fff, which corresponds to Host HPI address range 0x0060...0x3fff).

TORNADO-5410/5416 DSP system allows Host-to-DSP communication using DSP on-chip HPI port via entire 32Kx16 DSP on-chip memory (DSP data memory address range 0x0060...0x7fff, which corresponds to Host HPI address range 0x0060...0x7fff), as well as via extended 32Kx16 SARAM1 DSP on-chip memory area (DSP data memory address range 0x8000...0xffff, which corresponds to Host HPI address range 0x18000...0x1ffff).

CAUTION

All host-to-HPI accesses to HPIC, HPIDAI, HPIA, XHPIA and HPID registers of TMS320C54x DSP HPI should be performed as to 16-bit I/O registers only. Any violation of this may result in invalid data passed.

Bit *BOB* of HPIC register should be set to logical '1' prior any further data transfer will be performed via HPI and HPI address will be loaded. This corresponds to LSB first communication via ISA-bus.

Timeout Control for Host-to-HPI Accesses

Normally, if TMS320C54x DSP is executing the program while the *SMODE* bit of HPIC register is set to the '1' state (this corresponds to shared mode for accessing HPI shared RAM area), or if the *SMODE* bit of HPIC register is set to the '0' state (this corresponds to host-only mode for accessing HPI shared RAM area), then the TMS320C54x DSP on-chip HPI will set the *HPI_READY* hardware signal to the 'true' state almost without any wait states.

However, in case *SMODE* bit of HPIC register is set to the '1' state and HPI is accessed by host ISA-bus I/O interface after TMS320C54x DSP has executed *IDLE 3* instruction (which results in DSP on-chip clock stopped), then this host-to-HPI access will be pending with the *HPI_READY* hardware signal set to the 'false' state until DSP clock will recover. This infinite wait of host for the HPI ready condition can result in idling and crashing of host PC environment.

In order to avoid idling and crashing of host PC environment during host-to-HPI access, *TORNADO-54x* host ISA-bus I/O interface features hardware timeout control for host-to-HPI access. The timeout interval for host-to-HPI accesses varies for different *TORNADO-54x* DSP systems and is equal to:

- 6.2 μ sec for 40 MIPS *TORNADO-542L*
- 3.1 μ sec for 80 MIPS *TORNADO-548* and for 80 MIPS *TORNADO-5416*
- 2.5 μ sec for 100 MIPS *TORNADO-549/5402/5410*.

Once HPI timeout will occur (in case DSP clock is stopped while host executes host-to-HPI access), this will result in cancel of current host-to-HPI access and setting active *HPI_ERROR* flag (*HPI_ERROR*=1) in *SYS_STATUS_FRG* flag register. The HPI read data will be undefined during HPI timeout condition.

Once *HPI_ERROR* bit is set to the '1' state, then this can generate host interrupt in case *HPI_ERROR_IE* bit in *HPI_IE_FRG* flag register is set to the *HPI_ERROR_IE*=1 state.

Host software can clear *HPI_ERROR* flag by writing to the *CLEAR_HPI_ERROR_FRG* flag register of host ISA-bus I/O interface.

CAUTION

If *SMODE* bit of HPIC register is set to logical '1' and HPI is accessed by host ISA-bus I/O interface after TMS320C54x DSP has executes *IDLE 3* instruction, then this will result in pending host-to-HPI access and can cause host-to-HPI access timeout.

HPI timeout condition will result in setting *HPI_ERROR* bit in *SYS_STATUS_FRG* flag register and cancel of current host-to-HPI access. HPI timeout condition can generate host PC interrupt.

FLAG Registers

Registers #3 and #403 of *TORNADO-54x* ISA-bus I/O interface are used for auxiliary control (*flags*) of *TORNADO-54x*.

Flags are comprised into a set of multiplexed 8-bit *flag registers*. Particular *flag register* is addressed by *FLAG SELECTOR REGISTER* (register #403H). Flags within a currently addressed (selected) *flag register* can be read/written using I/O read/write operation into *FLAG DATA REGISTER* (register #3).

FLAG SELECTOR REGISTER is available for I/O r/w operations has the following data format:

FLAG SELECTOR REGISTER (r/w)							
<i>FSEL-7</i> (r/w, 0+)	<i>FSEL-6</i> (r/w, 0+)	<i>FSEL-5</i> (r/w, 0+)	<i>FSEL-4</i> (r/w, 0+)	<i>FSEL-3</i> (r/w, 0+)	<i>FSEL-2</i> (r/w, 0+)	<i>FSEL-1</i> (r/w, 0+)	<i>FSEL-0</i> (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

List of available flag registers for *TORNADO-54x*, which can be addressed by *FLAG SELECTOR REGISTER*, is presented in table 2-8.

Table 2-8. Flag registers for TORNADO-54x.

contents of FLAG SELECTOR REGISTER	corresponding flag register	access mode	reset value	description
10H	SYS_STATUS_FRG SET_HM_RQ_FRG	r w	-	<p>In read mode indicates current status of major run-time systems flags of TORNADO-54x (refer to subsection "SYS_STATUS_FRG Flag Register" later in this section).</p> <p>In write mode sets active <i>Host_to_Master_Request (HM_RQ)</i> via INT3 external interrupt request input for TMS320C54x DSP. Data written to SET_HM_RQ_FRG register has no meaning and is ignored.</p>
20H	SYS_STATUS_FRG CLEAR_MH_RQ_FRG	r w	-	<p>In read mode indicates current status of major run-time systems flags of TORNADO-54x (refer to subsection "SYS_STATUS_FRG Flag Register" later in this section).</p> <p>In write mode clears active <i>Master_to_Host_Request (MH_RQ)</i> flag in SYS_STATUS_FRG flag register. <i>Master_to_Host_Request</i> flag can be set by resident TMS320C54x DSP software in order to set attention or interrupt request to host PC. Data written to CLEAR_MH_RQ_FRG register has no meaning and is ignored. Host PC should perform this operation in the end of corresponding procedure or interrupt handler (in case MH_RQ_IE=1) after MH_RQ interrupt source has been identified.</p>
30H	SYS_STATUS_FRG CLEAR_SB_ERROR_FRG	r w	-	<p>In read mode indicates current status of major run-time systems flags of TORNADO-54x (refer to subsection "SYS_STATUS_FRG Flag Register" later in this section).</p> <p>In write mode clears active <i>SB_ERROR</i> flag in SYS_STATUS_FRG flag register. Active <i>SB_ERROR</i> flag is set by timeout during host-to-SB access. Data written to CLEAR_SB_ERROR_FRG register has no meaning and is ignored. Host PC should perform this operation in the end of corresponding interrupt handler (in case SB_ERROR_IE=1) after SB_ERROR interrupt source has been identified. Also, host PC should perform this operation in the end of data transmission between host ISA-bus and SB in case active <i>SB_ERROR</i> flag is detected.</p>

40H	<i>CLEAR_HPI_ERROR_FRG</i>	w	-	In write mode clears active <i>HPI_ERROR</i> flag in <i>SYS_STATUS_FRG</i> flag register. Active <i>HPI_ERROR</i> flag is set by timeout during host-to-HPI access. Data written to <i>CLEAR_HPI_ERROR_FRG</i> register has no meaning and is ignored. Host PC should perform this operation in the end of corresponding interrupt handler (in case <i>HPI_ERROR_IE</i> =1) after <i>HPI_ERROR</i> interrupt source has been identified. Also, host PC should perform this operation in the end of data transmission between host ISA-bus and HPI in case active <i>HPI_ERROR</i> flag is detected. This flag register is write-only
50H	<i>HPI_IE_FRG</i>	r/w	00H	<i>HPI Enable and Interrupt Enable Register</i> . This flag register sets interrupt enable masks for interrupting host PC on <i>HPI_ERROR</i> and <i>HPI_HINT</i> events. For <i>TORNADO-5402</i> DSP systems this register also sets enable status for TMS320VC5402 DSP on-chip HPI port facility and alternatively enables output of the second DSP on-chip timer for SIOX and PIOX-16 expansion interface sites. Host PC interrupt request is logical OR between (<i>MH_RQ_IE</i> & <i>MH_RQ</i>), (<i>SB_ERROR_IE</i> & <i>SB_ERROR</i>), (<i>HPI_ERROR_IE</i> & <i>HPI_ERROR</i>) and (<i>HPI_HINT_IE</i> & <i>HPI_HINT</i>) logic terms.
60H	<i>DSP_STATUS_FRG</i>	r	-	<i>DSP Status Register</i> . This flag register returns current state of <i>DSP_Mlock</i> and <i>DSP_M_GO</i> control signals from the TMS320C54x DSP environment, and of the <i>DSP_HPI_DISABLE</i> control signal (<i>TORNADO-5402</i> only). This register is provided for compatibility with <i>TORNADO</i> multiprocessor DSP systems
E0H	<i>ISA_MI_BADDR_FRG</i>	r/w	00H	<i>ISA-bus Memory Interface Base Address Register</i> . Sets ISA-bus memory base address for host ISA-bus memory interface of <i>TORNADO-54x</i> in accordance with table 2-3. Sets/resets activity of host ISA-bus memory interface of <i>TORNADO-54x</i> within UMB area of ISA-bus memory address space. Only three least significant bits of this register are valid; all other bits are ignored and reads as zeros.
E2H	<i>ISA_ECC_BADDR_FRG</i> (<i>TORNADO-542L</i> only)	r/w	00H	<i>ECC ISA-bus I/O Base Address Register</i> . Sets ISA-bus I/O base address for <i>TORNADO-542L</i> optional on-board emulation controller (<i>ECC</i>) in accordance with table 2-10. Sets/resets activity of <i>ECC</i> within ISA-bus I/O address space. Only three least significant bits of this register are valid; all other bits are ignored and reads as zeros.

<i>F0H</i> <i>F1H</i>	<i>DEV_ID0_FRG</i> <i>DEV_ID1_FRG</i>	<i>r</i>	<i>-</i>	<i>Device Identifier and S/N Registers #0/#1. These registers are read only and contain LSB and MSB of unique device and s/n identifier for TORNADO-54x</i>
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- Notes:
1. Unused codes for flag registers are reserved for future expansion.
 2. Access modes: *r* - read only; *w* - write only; *r/w* - read and write.

Once a desired flag register is selected by loading the corresponding code into *FLAG SELECTOR REGISTER* in accordance with table 2-8, current flags status can be obtained by reading *FLAG DATA REGISTER (FLAG STATUS REGISTER)*, whereas flag settings can be performed by writing to *FLAG DATA REGISTER (FLAG CONTROL REGISTER)*. Note, that *FLAG STATUS REGISTER* and *FLAG CONTROL REGISTER* are actually read and write synonym of *FLAG DATA REGISTER* that is available for both read and write operations. However, this makes useful sense since some of *TORNADO-54x* flag registers have different format for read and write operations.

Table 2-9. Bits of SYS_STATUS_FRG flag register for TORNADO-54x.

<i>bit name</i>	<i>reset value</i>	<i>description</i>
<i>SB_ACK</i>	0	<i>SB Request Acknowledge</i> . <i>SB_ACK</i> =1 denotes that SB arbiter has granted SB access to host ISA-bus memory interface. <i>SB_ACK</i> flag can be read during active SB locking from host ISA-bus memory interface. This bit is used for diagnostic purposes.
<i>HPI_ERROR</i>	0	<i>HPI Error (HPI_ERROR)</i> . <i>HPI_ERROR</i> =1 denotes that host-to-HPI timeout has been detected during host-to-HPI access. <i>HPI_ERROR</i> flag will keep staying in active <i>HPI_ERROR</i> =1 state until it will be reset by host PC software by means of writing to <i>CLEAR_HPI_ERROR_FRG</i> flag register. If <i>HPI_ERROR</i> flag has been set to active (<i>HPI_ERROR</i> =1) state, all succeeding host-to-HPI accesses from host ISA-bus memory interface of <i>TORNADO-54x</i> will be ignored and data returned will be undefined. If <i>HPI_ERROR_IE</i> =1 and <i>HPI_ERROR</i> =1, an active host PC CPU interrupt request is generated.
<i>HPI_HINT</i>	0	<i>DSP_to_Host Request via HPI (HPI_HINT)</i> . <i>HPI_HINT</i> =1 denotes that TMS320C54x DSP has generated active request to host PC CPU via HPI. <i>HPI_HINT</i> flag will keep staying in active <i>HPI_HINT</i> =1 state until it will be reset by host PC software by means of writing 0909H hex value to HPIC register of TMS320C54x DSP HPI. If <i>HPI_HINT_IE</i> =1 and <i>HPI_HINT</i> =1, then active host PC CPU interrupt request is generated.
<i>MH_RQ</i>	0	<i>Master_to_Host Request (MH_RQ)</i> . <i>MH_RQ</i> =1 denotes that TMS320C54x DSP has generated active request to host PC CPU. <i>MH_RQ</i> flag will keep staying in active <i>MH_RQ</i> =1 state until it will be reset by host PC software by means of writing to <i>CLEAR_MH_RQ_FRG</i> flag register. If <i>MH_RQ_IE</i> =1 and <i>MH_RQ</i> =1, then active host PC CPU interrupt request is generated.
<i>SB_ERROR</i>	0	<i>SB Error (SB_ERROR)</i> . <i>SB_ERROR</i> =1 denotes that SB access timeout has been detected during previous SB access from host ISA-bus memory interface. <i>SB_ERROR</i> flag will keep staying in active <i>SB_ERROR</i> =1 state until it will be reset by host PC software by means of writing to <i>CLEAR_SB_ERROR_FRG</i> flag register. If <i>SB_ERROR</i> flag is set active (<i>SB_ERROR</i> =1), all succeeding host-to-SB requests from host ISA-bus memory interface of <i>TORNADO-54x</i> will be ignored and data returned will be undefined. If <i>SB_ERROR_IE</i> =1 and <i>SB_ERROR</i> =1, an active host PC CPU interrupt request is generated.

SYS_STATUS_FRG Flag Register

SYS_STATUS_FRG flag register comprises of major *TORNADO-54x* run-time system flags settings. It is available as read only register and has the following data format:

SYS_STATUS_FRG Flag Register (read only)

<i>SB_ERROR</i>	<i>MH_RQ</i>	<i>HPI_HINT</i>	0	0	0	<i>HPI_ERROR</i>	<i>SB_ACK</i>
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Detail description for bits of *SYS_STATUS_FRG* flag register is presented in table 2-9.

HPI Interrupt Enable Flag Register (HPI_IE_FRG)

HPI_IE_FRG flag register comprises of the interrupt enable bit masks for generation of host PC interrupt on HPI events and of the HPI enable/disable control (*TORNADO-5402* DSP system only). *HPI_IE_FRG* flag register defaults to the 00H value on the host PC power on and has the following data format:

HPI_IE_FRG Flag Register (r/w)							
0	0	<i>HPI_HINT_IE</i> (r/w, 0+)	<i>HPI_DISABLE</i> (r/w, 0+) (<i>TORNADO-5402</i>)	0	0	<i>HPI_ERROR_IE</i> (r/w, 0+)	0
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

In case the *HPI_HINT_IE* bit is set to logical '1' and *HPI_HINT* flag is active (*HPI_HINT*=1) in *SYS_STATUS_FRG* flag register or HINT register of HPI, then this will result in generation of active host PC interrupt request. In case the *HPI_HINT_IE* bit is set to logical '0' (PC power on default value), then no host PC interrupt will be generated when *HPI_HINT* flag will come active.

In case the *HPI_ERROR_IE* bit is set to logical '1' and *HPI_ERROR* flag is active (*HPI_ERROR*=1) in *SYS_STATUS_FRG* flag register, then this will result in generation active host PC interrupt request. In case the *HPI_ERROR_IE* bit is set to logical '0' (PC power on default value), then no host PC interrupt will be generated when *HPI_ERROR* flag will come active.

The *HPI_DISABLE* bit is valid for *TORNADO-5402* DSP system only and is used to enable/disable the TMS320VC5402 DSP on-chip HPI port feature of *TORNADO-5402*. This alternatively disables/enables output of the second TMS320VC5402 DSP on-chip timer (*TM1*) to be available at the *XIO-1* I/O pin of SIOX and PIOX-16 interface sites in case the *XIO-1_CNF* bit of the *XIO-CNF* IOX register is set (refer to table 2-2 and '*DSP Environment*' section earlier in this chapter).

CAUTION

Host PC software can write to the *HPI_DISABLE* bit only while the TMS320VC5402 DSP of *TORNADO-5402* DSP system is in the ‘RESET’ state (*M_GO* bit of *CONTROL REGISTER* of *TORNADO-5402* host ISA-bus I/O interface is set to the *M_GO*=0 state). As soon as the DSP reset signal will be released, the last state of *HPI_DISABLE* bit will be latched by TMS320VC5402 DSP and the DSP HPI feature will be correspondingly enabled/disabled with the corresponding alternative disable/enable of second TMS320VC5402 DSP on-chip timer output (*TM1*).

All writes to the *HPI_DISABLE* bit while DSP is in the ‘RUN’ state (*M_GO* bit of *CONTROL REGISTER* of *TORNADO-5402* host ISA-bus I/O interface is set to the *M_GO*=1 state) will be ignored and the value of *HPI_DISABLE* bit will be not altered.

Writing to the *HPI_DISABLE* bit during DSP is in the ‘RESET’ state (*M_GO* bit of *CONTROL REGISTER* of *TORNADO-5402* host ISA-bus I/O interface is set to the *M_GO*=0 condition) will not effect operation of TMS320VC5402 DSP HPI port unless the DSP reset signal will be released.

The *DSP_HPI_DISABLE* bit of *DSP_STATUS_FLAG_REGISTER* of *TORNADO-5402* host ISA-bus I/O interface should be used to verify the current TMS320VC5402 DSP HPI port enable/disable status.

The *HPI_DISABLE*=0 condition (PC power on default value) will enable TMS320VC5402 DSP on-chip HPI port and disable output from the second DSP on-chip timer (*TM1*) as soon as the DSP reset signal will be released (i.e. when the *M_GO* bit of *CONTROL REGISTER* of *TORNADO-5402* host ISA-bus I/O interface will change from the *M_GO*=0 state to *M_GO*=1 state). In this case the *XIO-1_CNF* bit of the *XIO-CNF* IOX register is ignored and the *XIOF-1* I/O flag is wired to the *XIO-1* pin of the SIOX and PIOX-16 interface sites of *TORNADO-5402* DSP system.

The *HPI_DISABLE*=1 condition will disable the TMS320VC5402 DSP on-chip HPI port and enable output from the second DSP on-chip timer (*TM1*) as soon as the DSP reset signal will be released (i.e. when the *M_GO* bit of *CONTROL REGISTER* of *TORNADO-5402* host ISA-bus I/O interface will change from the *M_GO*=0 state to *M_GO*=1 state). In this case the particular functional assignment of the *XIO-1* pin of the SIOX and PIOX-16 interface sites of *TORNADO-5402* DSP system is defined by the *XIO-1_CNF* bit of the *XIO-CNF* IOX register (refer to ‘*DSP Environment*’ section earlier in this chapter).

DSP_STATUS_FRG Flag Register

DSP_STATUS_FRG read-only flag register comprises of the most important TMS320C54x DSP control signals settings and has the following data format:

DSP_STATUS_FRG Flag Register (read only)

0	0	0	<i>DSP_HPI_DISABLE</i> (<i>TORNADO-5402</i>)	0	0	<i>DSP_M_GO</i>	<i>DSP_MLock</i>
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

The *DSP_M_GO* bit is actually the returned value of *M_GO* bit from the *CONTROL REGISTER*, whereas the *DSP_MLock* bit indicates the SB locking condition by the on-board TMS320C54x DSP master (refer to section 2.3 “TMS320C54x DSP Environment” earlier in this chapter). The *DSP_MLock*=1 denotes that TMS320C54x DSP has set the SB lock request. The SB will be locked by DSP immediately in case there is no current host-to-SB request or immediately upon the current host-to-SB request will terminate.

The *DSP_HPI_DISABLE* bit is valid for *TORNADO-5402* DSP system only and reflects the current state of enable status for TMS320VC5402 DSP HPI port. The *DSP_HPI_DISABLE* bit is actually the returned latched value of *HPI_DISABLE* bit of *HPI_IE_FRG* flag register, and is latched on transition from the *M_GO*=0 state to the *M_GO*=1 state, i.e. when the DSP reset signal is released and DSP is put into the ‘RUN’ state.

CAUTION

The *DSP_HPI_DISABLE* bit should be used by host PC software to determine current enable (*DSP_HPI_DISABLE*=0) or disable (*DSP_HPI_DISABLE*=1) status of TMS320VC5402 DSP on-chip HPI port of *TORNADO-5402* DSP system and the corresponding alternative state of the output of the second DSP on-chip timer (*TM1*).

Once the DSP HPI port is enabled (*DSP_HPI_DISABLE*=0), then the output of the second DSP on-chip timer (*TM1*) is disabled, and the *XIO-1_CNF* bit of *XIOF-CNF* IOX register from the TMS320VC5402 DSP environment (refer to table 2-2) is ignored. In case the DSP HPI port is disabled (*DSP_HPI_DISABLE*=1), then the output of the second DSP on-chip timer (*TM1*) is enabled, and the *XIO-1_CNF* bit of *XIOF-CNF* IOX register will define whether the *XIOF-1* I/O flag or *TM1* timer output will appear on the *XIO-1* pin of SIOX and PIOX-16 interface sites of *TORNADO-5402* DSP system.

Flag Registers for Identification of TORNADO-54x DSP Systems

TORNADO-54x includes *DEV_ID0_FRG* and *DEV_ID1_FRG* read-only flag registers (refer to table 2-8), which contain unique code for identification of *TORNADO-54x* DSP systems (*DEV_ID1_FRG*) and its serial number (*DEV_ID0_FRG*).

Usage of *DEV_ID0_FRG/DEV_ID1_FRG* flag registers in host PC software is recommended for those applications that require to be protected from unauthorized duplication of software.

Generating Request to TMS320C54x DSP

TORNADO-54x can generate requests from host PC to TMS320C54x DSP in order to synchronize between programs execution in host and on-board DSP environments. Two methods for generation of host-to-DSP requests is supported in *TORNADO-54x*:

- *HM_RQ* (host to master request), that results in generation of active *INT3* external interrupt request for the on-board TMS320C54x DSP. In order to generate output *HM_RQ* flag, host PC software has to write to *SET_HM_RQ_FRG* flag register. This is the recommended method for generation of host-to-DSP request since it delivers compatibility with all other *TORNADO* DSP systems for PC.
- *HPI_DSPINT* (DSP interrupt via HPI), that results in setting bit *DSPINT* of HPIC register of TMS320C54x HPI. In order to generate *HPI_DSPINT* interrupt request to DSP, host PC software has to write 0505H hex value to HPIC register of TMS320C54x DSP. This is the *TORNADO-54x*

specific method for generation of host-to-DSP request, and it is recommended for simulation of host-to-DSP communication via TMS320C54x DSP on-chip HPI.

Processing Requests from TMS320C54x DSP

TORNADO-54x can generate requests from TMS320C54x DSP to host CPU in order to synchronize between program execution in host and on-board DSP environments. Two methods for generation of DSP-to-host requests is supported in **TORNADO-54x**:

- **MH_RQ** (master to host request), that results in setting flag **MH_RQ** in **SYS_STATUS_FRG** flag register. **MH_RQ** can generate active host PC interrupt request in case **MH_RQ_IE** bit in the **CONTROL REGISTER** is set to the **MH_RQ_IE=1** state. **MH_RQ** will remain in active state **MH_RQ=1** until it will be recognized and reset by host software. In order to reset the **MH_RQ** flag, host PC software has to write to **Clear_Master_to_Host_Request** flag register. This is the recommended method for generation of DSP-to-host request since it delivers compatibility with all other **TORNADO** DSP systems for PC.
- **HPI_HINT** (host interrupt request via HPI), that results in setting bit **HINT** of HPIC register of TMS320C54x HPI and flag **HPI_HINT** in **SYS_STATUS_FRG** flag register. **HPI_HINT** can generate active host PC interrupt request in case **HPI_HINT_IE** bit in **HPI_IE_FRG** flag register is set to **HPI_HINT_IE=1** state. **HPI_HINT** will remain in active state **HPI_HINT=1** until it will be recognized and reset by host software. In order to reset the **HPI_HINT** flag, host PC software has to write 0909H hex value to HPIC register of TMS320C54x DSP. This is the **TORNADO-54x** specific method for generation of DSP-to-host request, and it is recommended for simulation of DSP-to-host communication via TMS320C54x DSP on-chip HPI.

Host PC Interrupt Conditions

Host ISA-bus I/O interface can generate active interrupts to host PC CPU in the following cases:

- when **SB_ERROR** flag is active (**SB_ERROR=1**) in **SYS_STATUS_FRG** flag register and **SB_ERROR_IE** bit in **CONTROL REGISTER** is set to **SB_ERROR_IE=1** state
- when **MH_RQ** is active (**MH_RQ=1**) in **SYS_STATUS_FRG** flag register and **MH_RQ_IE** bit in **CONTROL REGISTER** is set to **MH_RQ_IE=1** state
- when **HPI_ERROR** flag is active (**HPI_ERROR=1**) in **SYS_STATUS_FRG** flag register and **HPI_ERROR_IE** bit in **HPI_IE_FRG** flag register is set to **HPI_ERROR_IE=1** state
- when **HPI_HINT** is active (**HPI_HINT=1**) in **SYS_STATUS_FRG** flag register or **HINT** register of HPI and **HPI_HINT_IE** bit in **HPI_IE_FRG** flag register is set to **HPI_HINT_IE=1** state

Host ISA-bus interrupt request is generated as logical 'OR' of the above events. Decoding of interrupt source should be performed by host PC software by means of analyzing the contents of **SYS_STATUS_FRG** flag register.

Host PC interrupt request may be generated using one of nine available ISA-bus interrupt request lines. Particular PC interrupt line is selected by the on-board interrupt configuration jumper J3 (refer to fig.2-2). The following ISA-bus interrupt request lines are available: IRQ-3, IRQ-4, IRQ-5, IRQ-6, IRQ-7, IRQ-10, IRQ-11, IRQ-12 and IRQ-15.

Setting ISA-bus memory base address for Host ISA-bus Memory Interface

TORNADO-54x provides software setting of ISA-bus memory base address for host ISA-bus memory interface by means of writing to *ISA_MI_BADDR_FRG* flag register. Only three least significant bits of *ISA_MI_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes. Available settings for *ISA_MI_BADDR_FRG* flag register are presented in table 2-3.

<i>ISA_MI_BADDR_FRG</i> Flag Register (r/w)							
0	0	0	0	0	<i>MI_BA2</i> (r/w, 0+)	<i>MI_BA1</i> (r/w, 0+)	<i>MI_BA0</i> (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Setting ISA-bus I/O base address for ECC in TORNADO-542L

TORNADO-542L provides software setting of ISA-bus I/O base address for optional on-board emulation controller chip (*ECC*) by means of writing to *ISA_ECC_BADDR_FRG* flag register. Only three least significant bits of *ISA_ECC_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes. Available settings for *ISA_ECC_BADDR_FRG* flag register are presented in table 2-10.

<i>ISA_ECC_BADDR_FRG</i> Flag Register (r/w)							
0	0	0	0	0	<i>ECC_BA2</i> (r/w, 0+)	<i>ECC_BA1</i> (r/w, 0+)	<i>ECC_BA0</i> (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-10. ISA-bus I/O base address for *TORNADO-542L* optional on-board emulation controller chip (*ECC*).

ISA-bus I/O base address for <i>ECC</i>	ISA-bus I/O address range for <i>ECC</i>	bit setting for <i>ISA_ECC_BADDR_FRG</i> flag register		
		bit#2 <i>ECC_BA2</i>	bit#1 <i>ECC_BA2</i>	bit#0 <i>ECC_BA2</i>
<i>ECC is disconnected from host ISA-bus; attachment of external TI XDS510 or MicroLAB' MIRAGE-510D emulator is allowed</i>	-	0	x	x
²⁾ 240H	240H ... 25FH	1	0	0
280H	280H ... 29FH	1	0	1
320H	320H ... 33FH	1	1	0
340H	340H ... 35FH	1	1	1

Note:

1. Highlighted configuration corresponds to host PC power on default setting.
2. This configuration is used as default by *T54CC.EXE* software utility.

CAUTION

Attachment of external TI XDS510 or MicroLAB' *MIRAGE-510D* emulator to *TORNADO-542L* is allowed only in case on-board emulation controller (*ECC*) is either not installed or is software 'disconnected' from ISA-bus (refer to table 2-10).

Attachment of external TI XDS510 or MicroLAB' *MIRAGE-510D* emulator to *TORNADO-542L* while the on-board emulation controller (*ECC*) is active is strongly prohibited and may result in damaging emulator and/or *ECC*.

2.6 Parallel I/O Expansion Interface (PIOX-16)

TORNADO-54x architecture provides expansion of the on-board I/O resources using 16-bit parallel I/O expansion interface (PIOX-16) and compatible PIOX-16 daughter modules. PIOX-16 is designed to carry compatible DCM over *TORNADO-54x* mainboard (refer to fig.1-1, fig.2-2 and fig.A-1) and is compatible with all *TORNADO* DSP systems for PC and all *TORNADO-E/EL* embedded DSP controllers.

Description

PIOX-16 appears as 64Kx16 I/O address space of *TORNADO-54x* on-board SB and can be accessed by both the on-board TMS320C54x DSP and host ISA-bus memory interface. It includes SB control signals, TMS320C54x DSP on-chip timer and external interrupt inputs, DSP reset signal, and *XIOF-0/1* I/O flags from DSP IOX area..

PIOX-16 provides data transfer timing using data strobe and write enable signals, and generates data ready signal *PIOX_READY*. PIOX-16 supports 16-bit SB access cycles only.

Installation of PIOX-16 DCM onto TORNADO-54x mainboard

Figure 2-6 shows installation of PIOX-16 DCM onto *TORNADO-54x* mainboard.

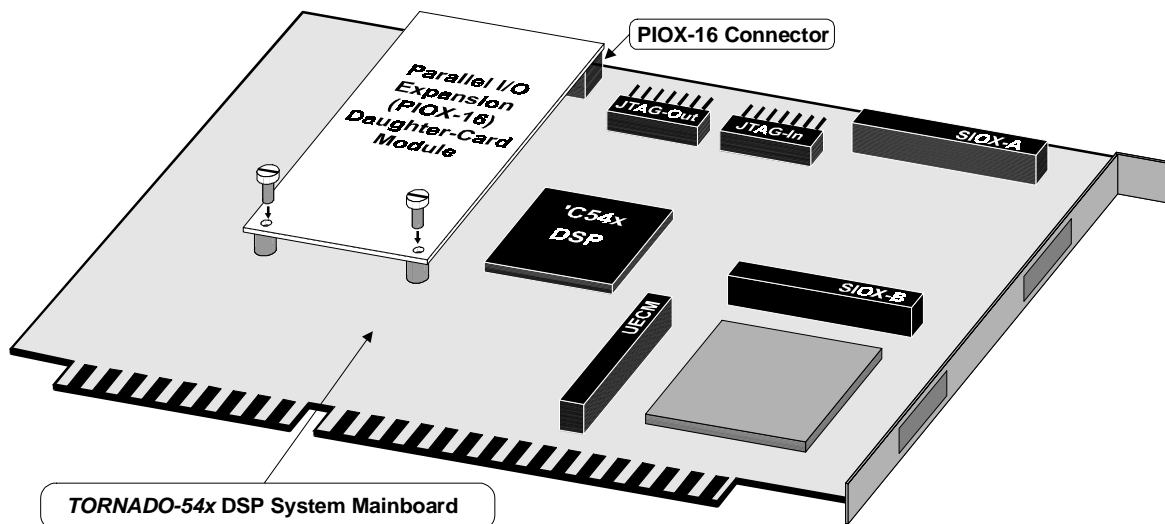


Fig.2-6. Installation of PIOX-16 DCM onto *TORNADO-54x* mainboard.

Accessing PIOX-16 from TMS320C54x DSP Environment

PIOX-16 can be accessed by the on-board TMS320C54x DSP during I/O instructions while DSP XF flag is set to the '0' state (refer to the '*TMS320C54x DSP Environment*' section earlier in this chapter).

CAUTION

The I/O field of DSP on-chip SWWSR register should be set to the 02H value (04H value for *TORNADO-5416*) in order to set two software wait states with further processing of *PIOX_READY* signal when accessing PIOX-16.

Accessing PIOX-16 from Host ISA-bus Memory Interface

PIOX-16 can be accessed by host ISA-bus memory interface when I/O bit of *SB PAGE MAPPER MSB* register from host ISA-bus I/O interface is set to logical '1' (refer to the '*Host ISA-bus I/O Interface*' section earlier in this chapter).

CAUTION

PIOX-16 area is accessed by host ISA-bus memory interface with one hardware wait state and with further processing of *PIOX_READY* signal.

PIOX-16 Connector Pinout

TORNADO-54x on-board PIOX-16 connector is a high-density DDK 50-pin DHB-series dual-row female connector with 0.05" pin pitch. Compatible PIOX-16 plugs for customer designed DCM are available from MicroLAB Systems upon request.

PIOX-16 pinout specification is presented at fig 2-7 whereas signal specification is listed in table 2-11.

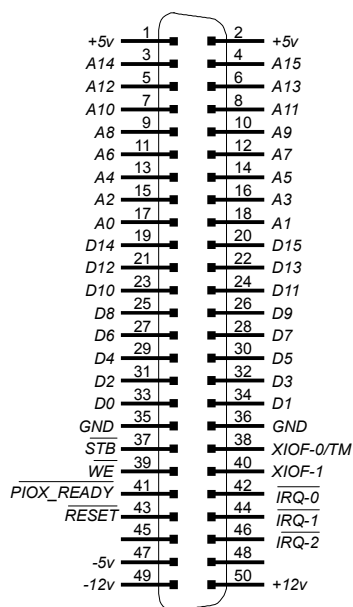


Fig.2-7. PIOX-16 connector pinout (top view).

Table 2-11. PIOX-16 signal specification.

Signal name	signal type	description
A0..A15	O	SB address bus.
D0..D15	I/O	SB data bus.
\overline{STB}	O	Active low PIOX-16 data transfer strobe.
\overline{WE}	O	Active low PIOX-16 write enable.
$\overline{PIOX_READY}$	I	Active low PIOX-16 data ready signal. This signal must be generated by PIOX-16 DCM.

<i>XIO-0</i>	I/O/Z	<p>For <i>TORNADO-542L</i> this pin might be configured by the on-board J3 jumper as either <i>XIOF-0</i> I/O flag from the DSP IOX area or as DSP on-chip timer output (<i>TM</i>). If J3 jumper of <i>TORNADO-542L</i> is set to the 2-3 state (refer to fig.A-1), then this pin is configured as <i>XIOF-0</i> I/O flag and can be configured by DSP as input or output general purpose pin. If J3 jumper is set to the 1-2 state, then this pin is configured as DSP on-chip timer output, i.e. it wires non-buffered DSP on-chip timer pin signal to this connector pin.</p> <p>For <i>TORNADO-548/549/5402/5410/5416</i> this pin might be configured by the DSP software via <i>XIO-0_CNF</i> bit of <i>XIO-CNF</i> IOX register (refer to table 2-2) as either <i>XIOF-0</i> I/O flag from DSP IOX area or as DSP on-chip timer output (<i>TM</i>).</p>
<i>XIO-1</i>	I/O/Z	<p>For <i>TORNADO-542L/548/549/5410/5416</i> this pin is the <i>XIOF-1</i> I/O flag from the DSP IOX area. It can be configured by DSP as input or output general purpose pin.</p> <p>For <i>TORNADO-5402</i> this pin might be configured by on-board TMS320VC5402 DSP software via <i>XIO-1_CNF</i> bit of <i>XIO-CNF</i> IOX register (refer to table 2-2) as either <i>XIOF-1</i> I/O flag from the DSP IOX area or as the output from the second DSP on-chip timer output (<i>TM1</i>) in case the TMS320VC5402 DSP on-chip HPI port is disabled.</p>
\overline{RESET}	O	<p>Active low reset signal for the on-board PIOX-16 expansion interface site:</p> <ul style="list-style-type: none"> for <i>TORNADO-542L</i> DSP system this is the active low DSP reset signal for <i>TORNADO-548/549/5402/5410/5416</i> DSP systems this is the output state of the <i>PIOX_RUN</i> bit from <i>PXSX_RUN</i> IOX register from the DSP environment (refer to table 2-2)
$\overline{IRQ-0}$, $\overline{IRQ-1}$, $\overline{IRQ-2}$	I	<p>Hardware interrupt request lines ($\overline{IRQ-0}$ has the highest priority) for the on-board TMS320C54x DSP chip, which correspond to <i>INT0...INT2</i> external user interrupts for TMS320C54x DSP. Both static and one-shot signals are supported. Actual hardware interrupt requests (<i>INT0...INT2</i>) will be generated on the falling edge (1→0) of the corresponding $\overline{IRQ-0}$.. $\overline{IRQ-2}$ signals.</p>
<i>GND</i>		Ground.
<i>+5v</i>		+5v power (from ISA-bus).
<i>+12v</i>		+12v power (from ISA-bus).
<i>-5v</i>		-5v power (from ISA-bus).
<i>-12v</i>		-12v power (from ISA-bus).

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
2. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

PIOX-16 Data Transfer Cycles

PIOX-16 interface site of *TORNADO-54x* supports 16-bit data transfer cycles only, and, therefore PIOX-16 connector does not contain the cycle definition signals.

Data Transfer Timing for PIOX-16

PIOX-16 data transfer timing is presented at fig.2-8. This data transfer timing is known as the industry standard MOTO mode and assumes usage of data strobe signal and write enable signal.

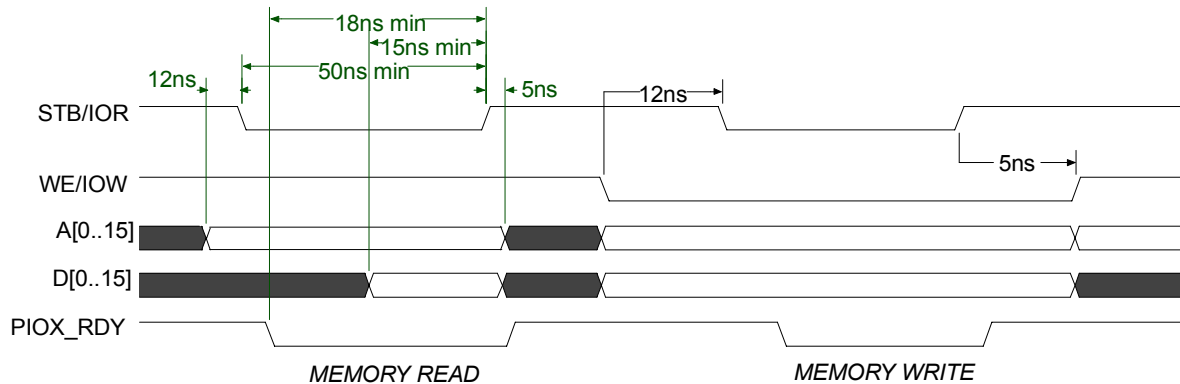


Fig.2-8. PIOX-16 data transfer timing diagram.

Generating Reset Signal for SIOX and PIOX/PIOX-16 Expansion Interface Sites of TORNADO-542L

TORNADO-542L DSP system provides generation of the reset signal (*RESET*) for SIOX and PIOX-16 expansion interface sites as the reset signal for the on-board TMS320C542 DSP.

Generating Reset Signal for SIOX/PIOX-16 Expansion Interface Sites of TORNADO-548/549/5402/5410/5416

TORNADO-548/549/5402/5410/5416 generates individual reset signal for PIOX-16 expansion interface site (refer to the corresponding sections earlier in this chapter) using the following logical conditions:

- PIOX-16 reset signal is active in case the on-board DSP is in the 'RESET' state
- reset signal for PIOX-16 expansion site can be released only in case DSP is in the 'RUN' state and bit *PIOX_RUN* of *PXSX_RUN* IOX register is set to logical '1' value by DSP software.

This allows correct initialization of the PIOX-16 DCM hardware and correct synchronization with the DSP software.

CAUTION

TORNADO-548/549/5402/5410/5416 rev.2C hardware provides different on-board logic for generation of SIOX/PIOX-16 reset signals if compared to the previous revisions of *TORNADO-548/549/5402/5410/5416* hardware.

TORNADO-548/549/5402/5410/5416 rev.2B and earlier generate common SIOX/PIOX-16 reset signal using *XRESET* IOX register, and this reset signal was generated as the logical OR between the DSP reset signal and bit D0 of *XRESET* IOX register.

PIOX-16 reset signal can be released by the TMS320C54x DSP software by means of writing logical '1' value to the *PIOX_RUN* bit of *PXSX_RUN* IOX register (refer to table 2-2 and to the corresponding subsection in section "TMS320C54x DSP Environment" earlier in this chapter), and this will allow operation of the PIOX-16 daughter-card hardware. Writing logical '0' to the *PIOX_RUN* bit of *PXSX_RUN* IOX register, which is the default value on the DSP reset, will set the PIOX-16 reset signal active.

XIO-0/1 Pins of SIOX/PIOX-16 Interface Sites

XIO-0/1 pins of *TORNADO-54x* on-board SIOX/PIOX-16 interface sites might be configured to appear either as I/O pins or as on-board TMS320C54x DSP timer outputs.

When *XIO-0/1* pins are configured as I/O pins, then the corresponding *XIOF-0/1* I/O flag appears on the *XIO-0/1* pin. Each of *XIOF-0/1* I/O flags is controlled by the *XIOF-DATA* and *XIOF-DIR* IOX registers and might be independently programmed by TMS320C54x DSP as input or output flag.

XIO-0/1 pins of SIOX/PIOX-16 interface sites of *TORNADO-54x* DSP systems, and *XIOF-0/1* I/O flags are controlled by TMS320C54x DSP software via IOX area in accordance with table 2-2 and occupies several registers in the IOX area:

- *XIOF-DIR* IOX register (*XIOF-0/1* flags direction register)
- *XIOF-DATA* IOX register (*XIOF-0/1* flags data register)
- *XIOF-CNF* IOX register (configuration register for *XIO-0/1* pins of SIOX/PIOX-16 expansion interface sites), *TORNADO-548/549/5402/5410/5416* DSP systems only.

CAUTION

TORNADO-542L DSP system assumes *XIO-0* pin of SIOX/PIOX-16 interface sites to be configured by the on-board J3 jumper as either I/O pin (*XIOF-0* IOX flag) or as TMS320C542 DSP on-chip timer output (*TM*). *XIO-1* pin of SIOX/PIOX-16 interface sites is always configured as I/O pin (*XIOF-1* IOX flag).

TORNADO-548/549/5410/5416 DSP systems assume *XIO-0* pin of SIOX/PIOX-16 interface sites to be software configured via *XIO-CNF* IOX register as either I/O pin (*XIOF-0* IOX flag) or as TMS320C54x DSP on-chip timer output (*TM*). *XIO-1* pin of SIOX/PIOX-16 interface sites is always configured as I/O pin (*XIOF-1* IOX flag).

TORNADO-5402 DSP system assumes *XIO-0* pin of SIOX/PIOX-16 interface sites to be software configured via *XIO-CNF* IOX register as either I/O pin (*XIOF-0* IOX flag) or as TMS320VC5402 DSP on-chip timer output (*TM*). *XIO-1* pin of SIOX/PIOX-16 interface sites is always configured as I/O pin (*XIOF-1* IOX flag) in case the HPI port of on-board TMS320VC5402 DSP is enabled via clearing the *HPI_DISABLE* bit of *HPI_IE_FRG* flag register of host ISA-bus I/O interface. In case the HPI port of on-board TMS320VC5402 DSP is disabled via setting the *HPI_DISABLE* bit of *HPI_IE_FRG* flag register of host ISA-bus I/O interface, then the *XIO-1* pin of SIOX/PIOX-16 interface sites might be configured via *XIO-CNF* IOX register as either I/O pin (*XIOF-1* IOX flag) or as output of the second TMS320VC5402 DSP on-chip timer (*TM1*).

Physical Dimensions for PIOX-16 DCM

Physical dimensions for PIOX-16 DCM are presented at fig. 2-9. This information is intended for those **TORNADO** customers, who need to design customized PIOX-16 DCM.

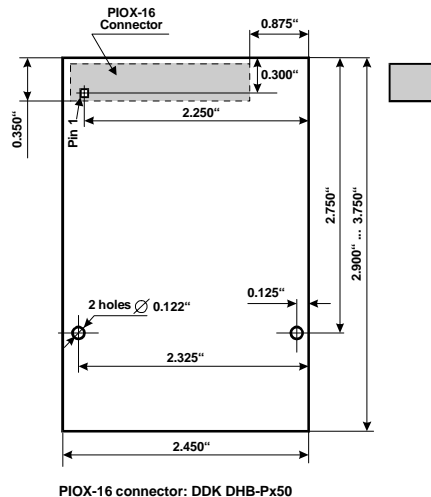


Fig.2-9. Physical dimensions for PIOX-16 DCM.

2.7 Serial I/O Expansion Interfaces (SIOX-A/B)

TORNADO-54x architecture provides expansion of the on-board TMS320C54x I/O resources via two serial I/O expansion interface sites (SIOX-A and SIOX-B), which are designed to carry compatible DCM (refer to fig.1-1, fig.2-2 and fig.A-1). SIOX interface sites of *TORNADO-54x* is compatible with SIOX interface sites for all *TORNADO* DSP systems for PC and stand-alone *TORNADO-E/EL/SX* DSP controllers.

Available SIOX daughter cards for *TORNADO-3x/54x* DSP systems include a variety of AD/DA/DIO daughter cards for telecommunication, speech and audio signal processing, industrial and instrumentation applications, and many more.

CAUTION

The *TORNADO-548/549/5402/5410/5416* on-board area for SIOX-B site is shared with the on-board area for *UECMX* emulation control DCM. Only one of SIOX-B or *UECMX* daughter cards can be installed simultaneously onto *TORNADO-548/549/5402/5410/5416* mainboard.

Description

Each of SIOX-A/B interface sites comprises of signals for SIO-0 and SIO-1 serial ports, TMS320C54x DSP on-chip timer and interrupts control, as well as optional *XIOF-0/1* I/O flags, DSP reset signal and ISA-bus power supply lines.

The connection diagrams for SIO-0 and SIO-1 ports of SIOX-A and SIOX-B expansion interface sites for all *TORNADO-54x* DSP systems is presented at fig.2-10.

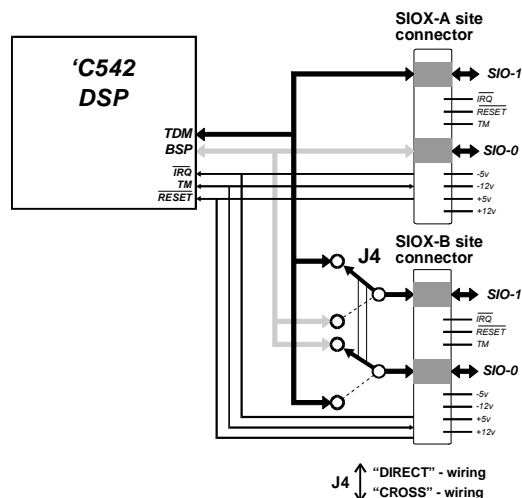


Fig.2-10a. SIOX sites connection diagram for *TORNADO-542L*.

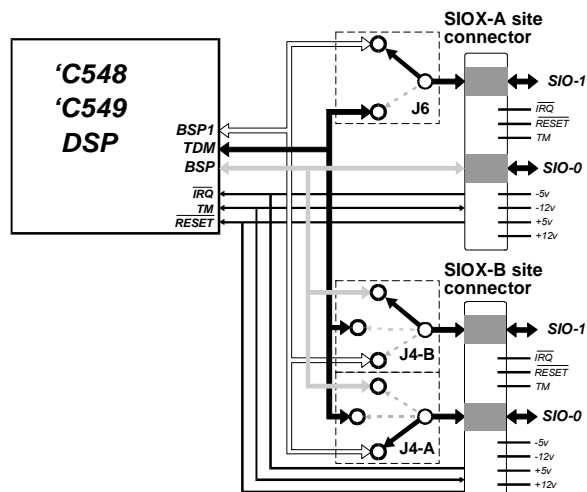


Fig.2-10b. SIOX sites connection diagram for *TORNADO-548/549*.

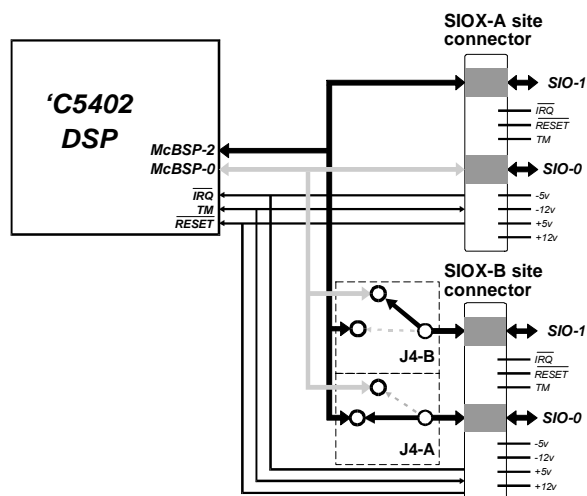


Fig.2-10c. SIOX sites connection diagram for *TORNADO-5402*.

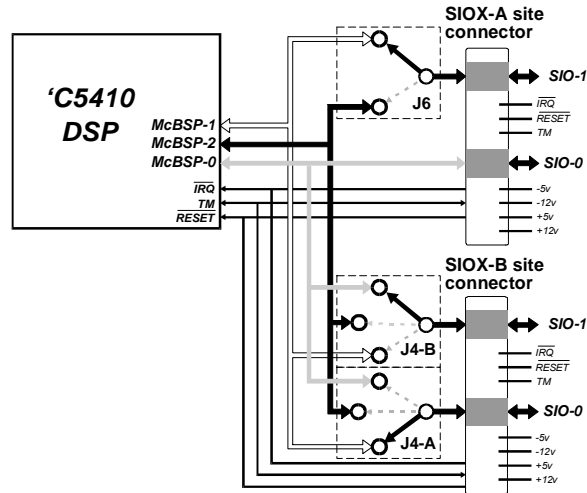


Fig.2-10d. SIOX sites connection diagram for *TORNADO-5410*.

Such a connection flexibility for SIOX-A and SIOX-B sites of *TORNADO-54x* DSP systems delivers an outstanding flexibility for selection the DSP serial ports for particular application, simplifies software design and allows simultaneous installation of two SIOX DCM onto *TORNADO-54x* board, most of which utilize only SIO-0 serial port of SIOX interface.

External analog and digital I/O signals for installed SIOX daughter cards should be attached by means of the SIOX daughter card on-board I/O connector via rear panel of host PC.

Correspondence between SIO-0/SIO-1 ports of SIOX-A/SIOX-B sites and the TMS320C542 DSP on-chip BSP/TDM serial ports for *TORNADO-542L*

For *TORNADO-542L* DSP system the SIO-0 and SIO-1 ports of SIOX-A site are on-board wired to the TMS320C542 DSP on-chip buffered serial port (BSP) and time division multiplexed serial port (TDM) correspondingly.

The SIO-0 and SIO-1 ports of SIOX-B site can connect to any of the TMS320C542 DSP on-chip BSP or TDM port via the on-board J4 jumper set. Maximum throughput of serial ports for *TORNADO-542L* is 20 Mbit/sec. See subsection below for more details.

Correspondence between SIO-0/SIO-1 ports of SIOX-A/SIOX-B sites and the TMS320LC548/VC549 DSP on-chip BSP/TDM/BSP1 serial ports for *TORNADO-548/549*

For *TORNADO-548/549* DSP systems the SIO-0 port of SIOX-A site is on-board wired to the TMS320LC548/VC549 DSP on-chip BSP port, whereas SIO-1 port of SIOX-A site may connect to any of the DSP on-chip BSP1 or TDM port via the on-board J6 jumper.

The SIO-0 and SIO-1 ports of SIOX-B site of *TORNADO-548/549* can connect to any of the DSP on-chip BSP, BSP1 or TDM port via the on-board J4 jumper set. Maximum throughput of serial ports is 40 Mbit/sec for *TORNADO-548* and 50 Mbit/sec for *TORNADO-549*. See subsection below for more details.

Correspondence between SIO-0/SIO-1 ports of SIOX-A/SIOX-B sites and the TMS320VC5402 DSP on-chip McBSP-0/McBSP-2 serial ports for TORNADO-5402

For *TORNADO-5402* DSP system the SIO-0 and SIO-1 ports of SIOX-A site are on-board wired to the TMS320VC5402 DSP on-chip multichannel BSP ports McBSP-0 and McBSP-2 correspondingly.

The SIO-0 and SIO-1 ports of SIOX-B site can connect to any of the TMS320VC5402 DSP on-chip McBSP-0 or McBSP-2 port via the on-board J4 jumper set. Maximum throughput of serial ports for *TORNADO-5402* is 50 Mbit/sec. See subsection below for more details.

Correspondence between SIO-0/SIO-1 ports of SIOX-A/SIOX-B sites and the TMS320VC5410 DSP on-chip McBSP-0/McBSP-1/McBSP-2 serial ports for TORNADO-5410

For *TORNADO-5410* DSP system the SIO-0 port of SIOX-A site is on-board wired to the TMS320VC5410 DSP on-chip McBSP-0 port, whereas SIO-1 port of SIOX-A site may connect to any of the DSP on-chip McBSP-1 or McBSP-2 port via the on-board J6 jumper.

The SIO-0 and SIO-1 ports of SIOX-B site of *TORNADO-5410* can connect to any of the DSP on-chip McBSP-0, McBSP-1 or McBSP-2 port via the on-board J4 jumper set. Maximum throughput of serial ports is 50 Mbit/sec for *TORNADO-5410*. See subsection below for more details.

Installation of SIOX DCM onto TORNADO-54x Mainboard

Figure 2-11 shows installation of SIOX DCM onto *TORNADO-54x* and *TORNADO-62MX/67MX* mainboard.



Fig.2-11a. *TORNADO-542L* mainboard with SIOX-A and SIOX-B DCM.

CAUTION

The on-board area for SIOX-B site of *TORNADO-548/549/5402/5410/5416* is shared with the on-board area for *UECMX* emulation control DCM. Either SIOX-B or *UECMX* DCM can be installed onto *TORNADO-548/549/5402/5410/5416* mainboard.



Fig.2-11b. *TORNADO-548/549/5402/5410/5416* mainboard with SIOX-A and SIOX-B DCM.



Fig.2-11c. *TORNADO-548/549/5402/5410/5416* mainboard with SIOX-A and UECMX DCM.

SIOX site connector

SIOX sites connector is and industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. SIOX connector pinout is presented at fig.2-12 and signal specifications are listed in table 2-12.

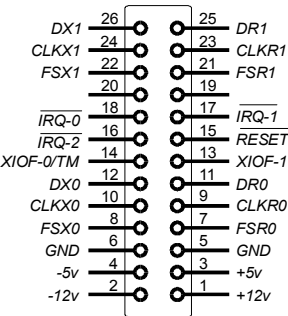


Fig.2-12. SIOX connector pinout (top view).

Table 2-12. SIOX signal specification.

SIOX signal name	signal type	description
SIO-0 port control		
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	<p>Data, frame synchronization and serial clock signals for transmitter of SIO-0 port.</p> <p>For SIOX-A site these signals correspond to the transmitter of DSP on-chip BSP (TORNADO-542L/548/549) or McBSP-0 (TORNADO-5402/5410/5416) serial port.</p> <p>For SIOX-B site these signals might be configured by on-board J4 jumper set to connect to the transmitter of any of the DSP on-chip BSP/TDM/BSP1 (TORNADO-542L/548/549), McBSP-0/McBSP-2 (TORNADO-5402), or McBSP-0/McBSP-1/McBSP-2 (TORNADO-5410) serial ports.</p>
DR0 FSR0 CLKR0	I I I	<p>Data, frame synchronization and serial clock signals for receiver of SIO-0 port.</p> <p>For SIOX-A site these signals correspond to the receiver of DSP on-chip BSP (TORNADO-542L/548/549) or McBSP-0 (TORNADO-5402/5410/5416) serial port.</p> <p>For SIOX-B site these signals might be configured by the on-board J4 jumper set to connect to the receiver of any of the DSP on-chip BSP/TDM/BSP1 (TORNADO-542L/548/549), McBSP-0/McBSP-2 (TORNADO-5402), or McBSP-0/McBSP-1/McBSP-2 (TORNADO-5410) serial ports.</p>

SIO-1 port control		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	<p>Data, frame synchronization and serial clock signals for transmitter of SIO-1 port.</p> <p>For SIOX-A site of <i>TORNADO-542L/TORNADO-5402</i> these signals correspond to the transmitter of DSP on-chip TDM (<i>TORNADO-542L</i>) or McBSP-2 (<i>TORNADO-5402</i>) serial port.</p> <p>For SIOX-A site of <i>TORNADO-548/549/5410/5416</i> these signals might be configured by the on-board J6 jumper to connect to the transmitter of any of the DSP on-chip TDM/BSP1 (<i>TORNADO-548/549</i>) or McBSP-1/McBSP-2 (<i>TORNADO-5410</i>) serial ports.</p> <p>For SIOX-B site these signals might be configured by the on-board J4 jumper set to connect to the transmitter of any of the DSP on-chip BSP/TDM/BSP1 (<i>TORNADO-542L/548/549</i>), McBSP-0/McBSP-2 (<i>TORNADO-5402</i>), or McBSP-0/McBSP-1/McBSP-2 (<i>TORNADO-5410</i>) serial ports.</p>
DR1 FSR1 CLKR1	I I/O I	<p>Data, frame synchronization and serial clock signals for receiver of SIO-1 port.</p> <p>For SIOX-A site of <i>TORNADO-542L/TORNADO-5402</i> these signals correspond to the receiver of DSP on-chip TDM (<i>TORNADO-542L</i>) or McBSP-2 (<i>TORNADO-5402</i>) serial port.</p> <p>For SIOX-A site of <i>TORNADO-548/549/5410/5416</i> these signals might be configured by the on-board J6 jumper to connect to the receiver of any of the DSP on-chip TDM/BSP1 (<i>TORNADO-548/549</i>) or McBSP-1/McBSP-2 (<i>TORNADO-5410</i>) serial ports.</p> <p>For SIOX-B site these signals might be configured by the on-board J4 jumper set to connect to the receiver of any of the DSP on-chip BSP/TDM/BSP1 (<i>TORNADO-542L/548/549</i>), McBSP-0/McBSP-2 (<i>TORNADO-5402</i>), or McBSP-0/McBSP-1/McBSP-2 (<i>TORNADO-5410</i>) serial ports.</p>
Timers/IO, DSP Reset and Interrupt Requests		
XIO-0	I/O/Z	<p>For <i>TORNADO-542L</i> this pin might be configured by the on-board J3 jumper as either <i>XIOF-0</i> I/O flag from the DSP IOX area or as DSP on-chip timer output (<i>TM</i>). If J3 jumper of <i>TORNADO-542L</i> is set to the 2-3 state (refer to fig.A-1), then this pin is configured as <i>XIOF-0</i> I/O flag and can be configured by DSP as input or output general purpose pin. If J3 jumper is set to the 1-2 state, then this pin is configured as DSP on-chip timer output, i.e. it wires non-buffered DSP on-chip timer pin signal to this connector pin.</p> <p>For <i>TORNADO-548/549/5402/5410/5416</i> this pin might be configured by the DSP software via <i>XIO-0_CNF</i> bit of <i>XIO-CNF</i> IOX register (refer to table 2-2) as either <i>XIOF-0</i> I/O flag from DSP IOX area or as DSP on-chip timer output (<i>TM</i>).</p>

<i>XIO-1</i>	I/O/Z	<p>For <i>TORNADO-542L/548/549/5410/5416</i> this pin is the <i>XIOF-1</i> I/O flag from the DSP IOX area. It can be configured by DSP as input or output general purpose pin.</p> <p>For <i>TORNADO-5402</i> this pin might be configured by on-board TMS320VC5402 DSP software via <i>XIO-1_CNF</i> bit of <i>XIO-CNF</i> IOX register (refer to table 2-2) as either <i>XIOF-1</i> I/O flag from the DSP IOX area or as the output from the second DSP on-chip timer output (<i>TM1</i>) in case the TMS320VC5402 DSP on-chip HPI port is disabled.</p>
\overline{RESET}	O	<p>Active low reset signal for the on-board SIOX-A/SIOX-B expansion interface site:</p> <ul style="list-style-type: none"> • for <i>TORNADO-542L</i> DSP system this is the active low DSP reset signal • for <i>TORNADO-548/549/5402/5410/5416</i> DSP systems this is the output state of either <i>SIOX-A_RUN</i> bit (for SIOX-A site) or <i>SIOX-B_RUN</i> bit (for SIOX-B site) of <i>PXSX_RUN</i> IOX register from the DSP environment (refer to table 2-2)
$\overline{IRQ-0}$, $\overline{IRQ-1}$, $\overline{IRQ-2}$	I	<p>Hardware interrupt request lines ($\overline{IRQ-0}$ has the highest priority) for the on-board TMS320C54x DSP chip, which correspond to <i>INT0...INT2</i> external user interrupts for TMS320C54x DSP. Both static and one-shot signals are supported. Actual hardware interrupt requests (<i>INT0...INT2</i>) will be generated on the falling edge (1→0) of the corresponding $\overline{IRQ-0} \dots \overline{IRQ-2}$ signals.</p>
Power Supplies		
<i>GND</i>		Ground.
+5v		+5v power (from ISA-bus).
+12v		+12v power (from ISA-bus).
-5v		-5v power (from ISA-bus).
-12v		-12v power (from ISA-bus).

Note:

1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
1. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

Configuring SIO-0/SIO-1 ports of SIOX-B site for TORNADO-542L

Selection between SIO-0/1 ports of SIOX-B site and TMS320C542 DSP on-chip BSP/TDM serial ports for *TORNADO-542L* DSP system is performed by means of the on-board jumper array J4 (refer to fig.2-13a). Only two combinations are available: “direct”-wiring (BSP→SIO-0@SIOX-B, TDM→SIO-1@SIOX-B) and “cross”-wiring (TDM→SIO-0@SIOX-B, BSP→SIO-1@SIOX-B).

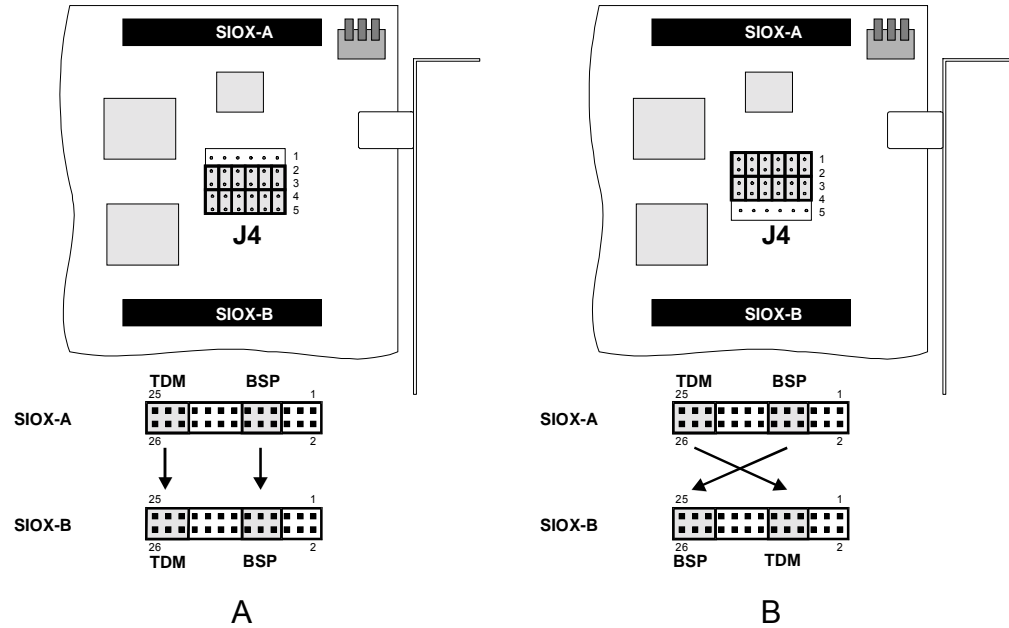


Fig. 2-13a. “Direct” (A) and “cross” (B) wiring configurations for SIO-0/1 ports of SIOX-B site for TORNADO-542L.

Configuring SIO-1 port of SIOX-A site for TORNADO-548/549

In TORNADO-548/549 DSP systems selection between SIO-1 port of SIOX-A site and TMS320LC548/VC549 DSP on-chip TDM/BSP1 serial ports is performed by means of on-board jumper J6 (refer to fig.2-13b).

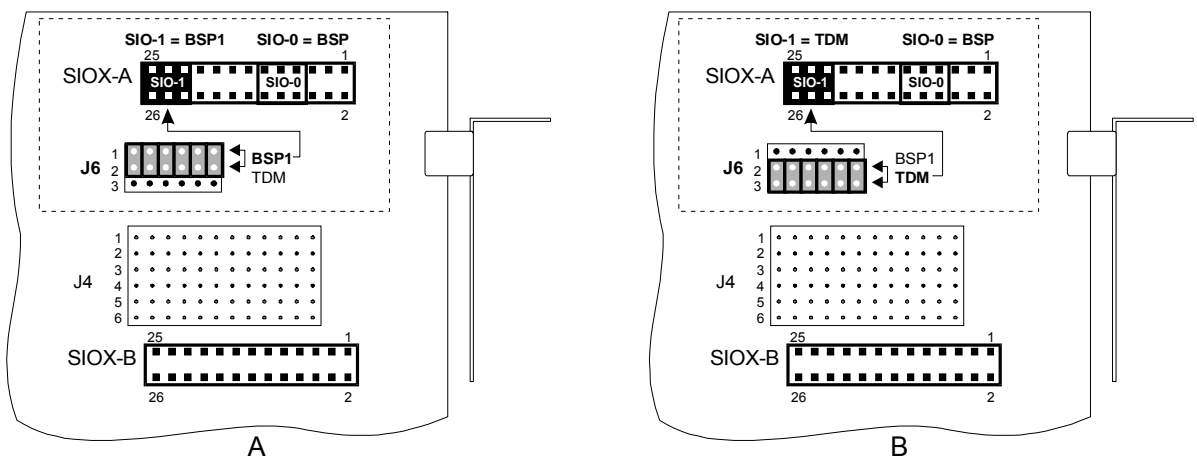


Fig. 2-13b. Configurations for SIO-1 port of SIOX-A site for TORNADO-548/549.

Configuring SIO-0/SIO-1 ports of SIOX-B site for TORNADO-548/549

In *TORNADO-548/549* DSP systems selection between SIO-0/1 ports of SIOX-B site and TMS320LC548/VC549 DSP on-chip BSP/TDM/BSP1 serial ports is performed by means of on-board jumper arrays J4-A and J4-B (refer to fig.2-13c). Independent configurations for SIO-0 (using J4-A jumper array) and SIO-1 (using J4-B jumper array) ports are supported, i.e. each of SIO-0/1 ports can connect to any of the TMS320LC548/VC549 DSP on-chip BSP/TDM/BSP1 serial ports. This delivers more flexibility than that with *TORNADO-542L* DSP system.

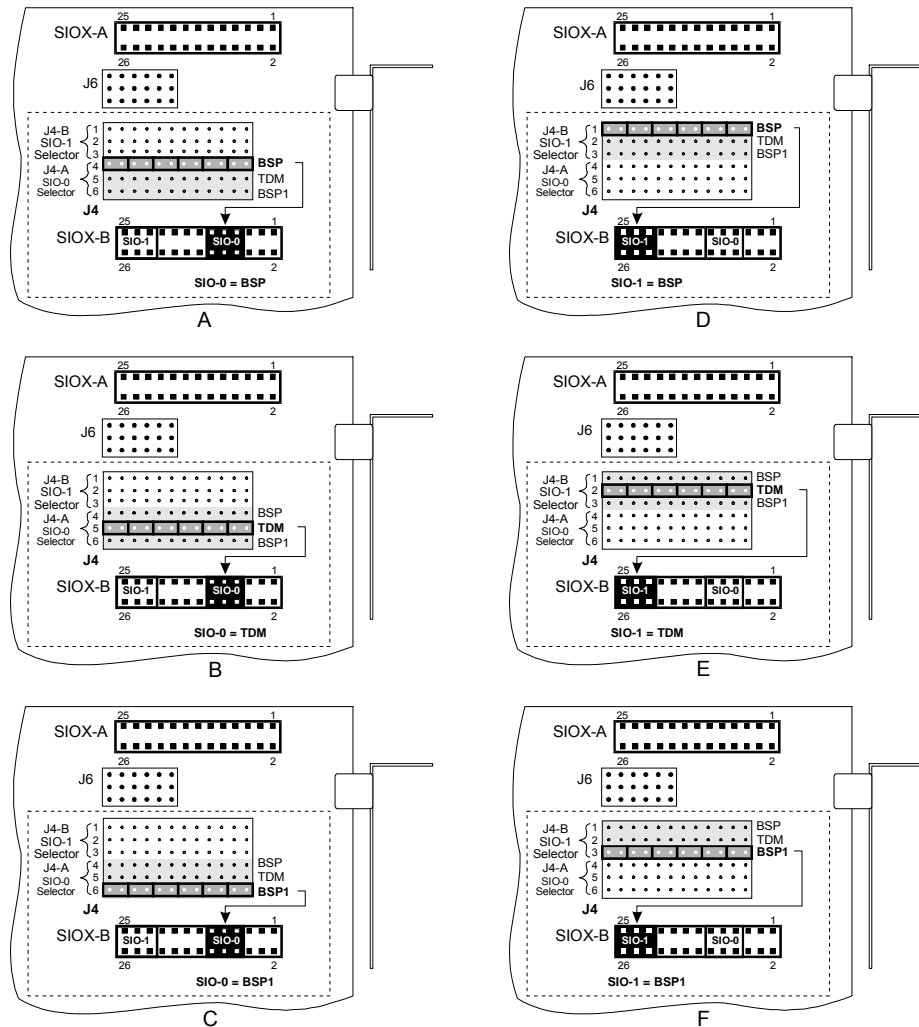


Fig. 2-13c. Configurations of SIO-0/1 ports for SIOX-B site for *TORNADO-548/549*.

Configuring SIO-0/SIO-1 ports of SIOX-B site for TORNADO-5402

Selection between SIO-0/1 ports of SIOX-B site and TMS320VC5402 DSP on-chip McBSP-0/McBSP-2 serial ports for *TORNADO-5402* DSP system is performed by means of the on-board jumper array J4 (refer to fig.2-13d). Only two combinations are available: “direct”-wiring (McBSP-0→SIO-0@SIOX-B, McBSP-2→SIO-1@SIOX-B) and “cross”-wiring (McBSP-2→SIO-0@SIOX-B, McBSP-0→SIO-1@SIOX-B).

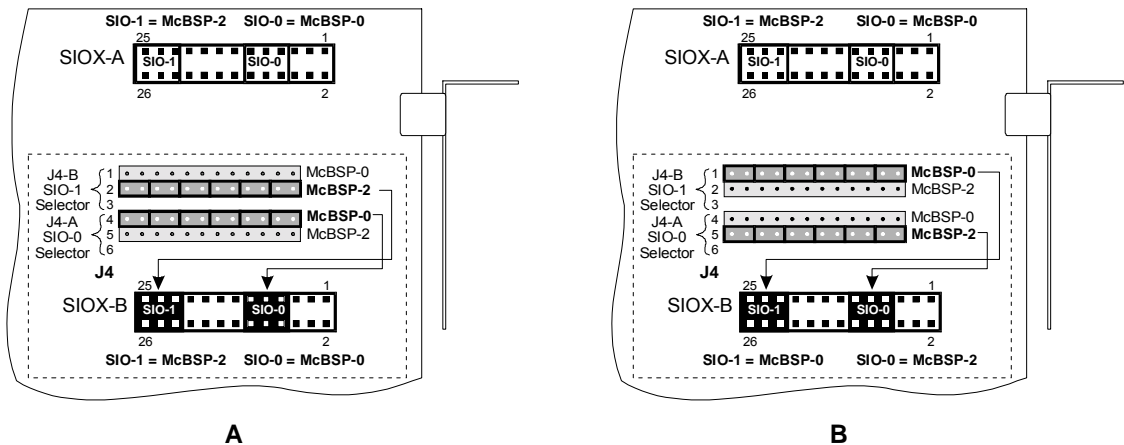


Fig. 2-13d. “Direct” (A) and “cross” (B) wiring configurations for SIO-0/1 ports of SIOX-B site for *TORNADO-5402*.

Configuring SIO-1 port of SIOX-A site for TORNADO-5410

In *TORNADO-5410* DSP system selection between SIO-1 port of SIOX-A site and TMS320VC5410 DSP on-chip McBSP-1/McBSP-2 serial ports is performed by means of on-board jumper J6 (refer to fig.2-13e).

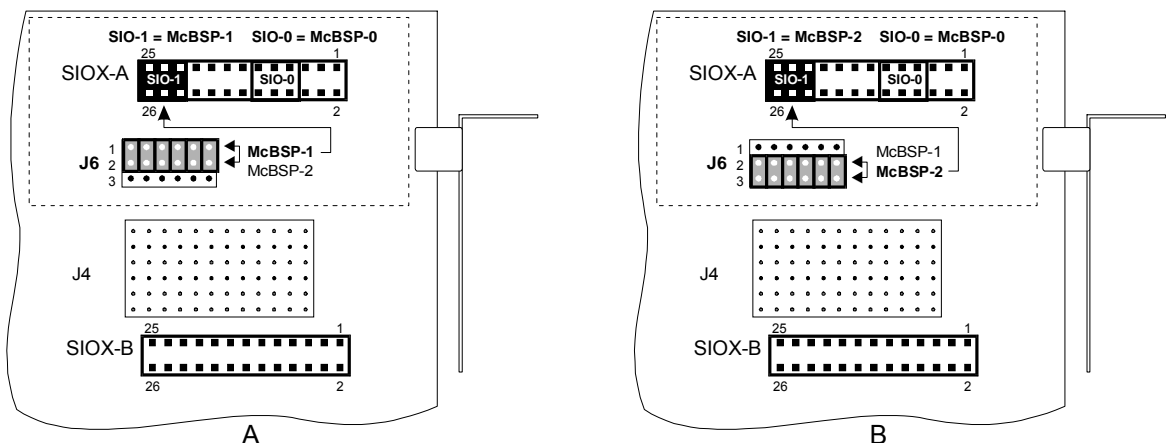


Fig. 2-13e. Configurations for SIO-1 port of SIOX-A site for *TORNADO-5410*.

Configuring SIO-0/SIO-1 ports of SIOX-B site for TORNADO-5410

In *TORNADO-5410* DSP system selection between SIO-0/1 ports of SIOX-B site and TMS320VC5410 DSP on-chip McBSP-0/McBSP-1/McBSP-2 serial ports is performed by means of on-board jumper arrays J4-A and J4-B (refer to fig.2-13f). Independent configurations for SIO-0 (using J4-A jumper array) and SIO-1 (using J4-B jumper array) ports are supported, i.e. each of SIO-0/1 ports can connect to any of the TMS320VC5410 DSP on-chip McBSP-0/McBSP-1/McBSP-2 serial ports.

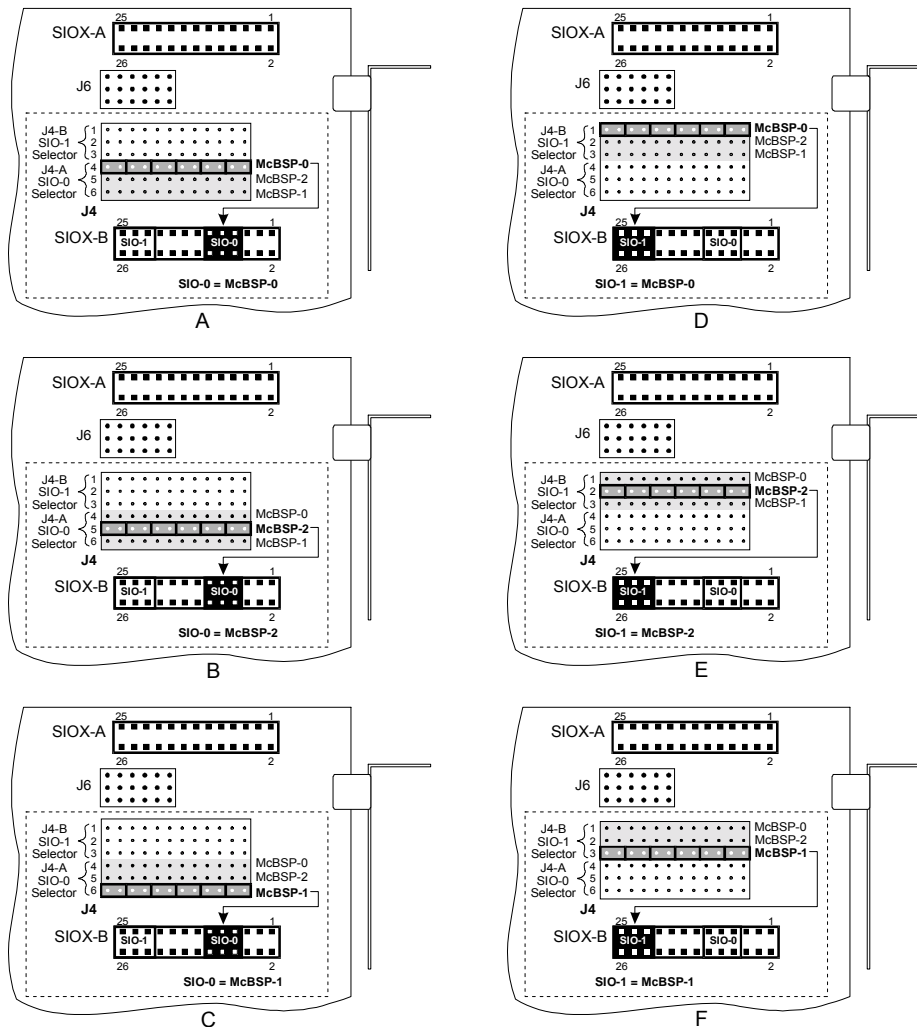


Fig. 2-13f. Configurations of SIO-0/1 ports for SIOX-B site for *TORNADO-5410*.

Generating Reset Signal for SIOX and PIOX/PIOX-16 Expansion Interface Sites for TORNADO-542L

TORNADO-542L DSP system provides generation of the reset signal (*RESET*) for SIOX and PIOX-16 expansion interface sites as the reset signal for the on-board TMS320C542 DSP.

Generating Reset Signal for SIOX/PIOX-16 Expansion Interface Sites in TORNADO-548/549/5402/5410/5416

TORNADO-548/549/5402/5410/5416 generate individual reset signals for SIOX-A and SIOX-B expansion interface sites (refer to the corresponding sections earlier in this chapter) using the following logical conditions:

- SIOX-A/B reset signals are active in case the on-board DSP is in the ‘RESET’ state
- reset signal(s) for SIOX-A/B expansion site can be released only in case DSP is in the ‘RUN’ state and the corresponding bit(s) *SIOX-A_RUN* and *SIOX-B_RUN* of *PXSX_RUN* IOX register is(are) set to the logical ‘1’ value by DSP software.

This allows correct initialization of the SIOX-A/B daughter-card hardware and correct synchronization with the DSP software.

CAUTION

TORNADO-548/549/5402/5410/5416 rev.2C hardware provides different on-board logic for generation of SIOX/PIOX reset signals if compared to the earlier revisions of **TORNADO-548/549/5402/5410/5416** hardware.

TORNADO-548/549/5402/5410/5416 rev.2B and earlier generate common SIOX/PIOX reset signal using *XRESET* IOX register, and this reset signal was generated as the logical OR between the DSP reset signal and bit D0 of *XRESET* IOX register.

SIOX-A reset signal can be released by the TMS320C54x DSP software by means of writing logical ‘1’ value to the *SIOX-A_RUN* bit of *PXSX_RUN* IOX register (refer to table 2-2 and to the corresponding subsection in section “TMS320C54x DSP Environment” earlier in this chapter), and this will allow operation of the SIOX-A daughter-card hardware. Writing logical ‘0’ to *SIOX-A_RUN* bit of *PXSX_RUN* IOX register, which is the default value on the DSP reset, will set the SIOX-A reset signal active.

SIOX-B reset signal can be released by the TMS320C54x DSP software by means of writing logical ‘1’ value to the *SIOX-B_RUN* bit of *PXSX_RUN* IOX register (refer to table 2-2 and to the corresponding subsection in section “TMS320C54x DSP Environment” earlier in this chapter), and this will allow operation of the SIOX-B daughter-card hardware. Writing logical ‘0’ to *SIOX-B_RUN* bit of *PXSX_RUN* IOX register, which is the default value on the DSP reset, will set the SIOX-B reset signal active.

Connecting External Clocks to McBSP-0/McBSP-1/McBSP-2 Serial Ports

TORNADO-5410 DSP systems with the on-board TMS320VC5410GGW100 DSP in the BGA package allow optional facilities for connection of external clock source to the DSP on-chip McBSP-0/McBSP-1/McBSP-2 serial ports. These external clocks are known as BCLKS0/BCLKS1/BCLKS2 signals in accordance with TI TMS320VC5410 specifications.

Usage of BCLKS0/BCLKS1/BCLKS2 external clocks for the DSP on-chip McBSP-0/McBSP-1/McBSP-2 serial ports delivers outstanding flexibility in generation of virtually any serial data clock frequency for the McBSP-0/McBSP-1/McBSP-2 serial ports in order to meet the requirements of any application.

External clock source signals BCLKS0/BCLKS1/BCLKS2 for each of the McBSP-0/McBSP-1/McBSP-2 serial ports independently are available via either of the following signal sources:

- via JP7 (for McBSP-0 port), JP8 (for McBSP-1 port) and JP9 (for McBSP-2 port) on-board edge connectors (refer to fig.2-1 and fig.A-1)
- via 5v TTL/CMOS crystal oscillators in the DIP-4 package (0.3"x0.3" footprint, example: EPSON SG-531 crystal oscillators), which can be installed into the S1 (for McBSP-0 port), S2 (for McBSP-1 port) and S3 (for McBSP-2 port) on-board sockets (refer to fig.2-1 and fig.A-1).

Details of JP7/JP8/JP9 connector specifications and location of the S1/S2/S3 crystal oscillators sites for connection of clock source signals BCLKS0/BCLKS1/BCLKS2 for McBSP-0/McBSP-1/McBSP-2 serial ports are shown at figure 2-14.

Selection of the BCLKS0/BCLKS1/BCLKS2 source clock as the timing source clock for McBSP-0/McBSP-1/McBSP-2 instead of DSP clock is performed by means of programming the DSP on-chip McBSP-0/McBSP-1/McBSP-2 control registers. Refer to original TI TMS320VC5410GGW100 documentation for getting more information on programming the McBSP serial ports.

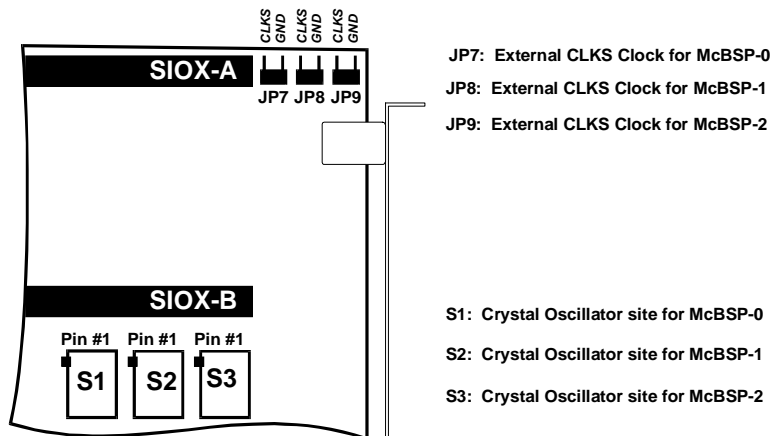


Fig. 2-14. On-board connectors and sockets for crystal oscillators for external serial port clock (BCLKS) for McBSP-0/1/2 serial ports of *TORNADO-5410*.

XIO-0/1 Pins of SIOX/PIOX-16 Interface Sites

XIO-0/1 pins of *TORNADO-54x* on-board SIOX/PIOX-16 interface sites might be configured to appear either as I/O pins or as on-board TMS320C54x DSP timer outputs.

When XIO-0/1 pins are configured as I/O pins, then the corresponding XIOF-0/1 I/O flag appears on the XIO-0/1 pin. Each of XIOF-0/1 I/O flags is controlled by the XIOF-DATA and XIOF-DIR IOX registers and might be independently programmed by TMS320C54x DSP as input or output flag.

XIO-0/1 pins of SIOX/PIOX-16 interface sites of *TORNADO-54x* DSP systems, and *XIOF-0/1* I/O flags are controlled by TMS320C54x DSP software via IOX area in accordance with table 2-2 and occupies several registers in the IOX area:

- *XIOF-DIR* IOX register (*XIOF-0/1* flags direction register)
- *XIOF-DATA* IOX register (*XIOF-0/1* flags data register)
- *XIOF-CNF* IOX register (configuration register for *XIO-0/1* pins of SIOX/PIOX-16 expansion interface sites), *TORNADO-548/549/5402/5410/5416* DSP systems only.

CAUTION

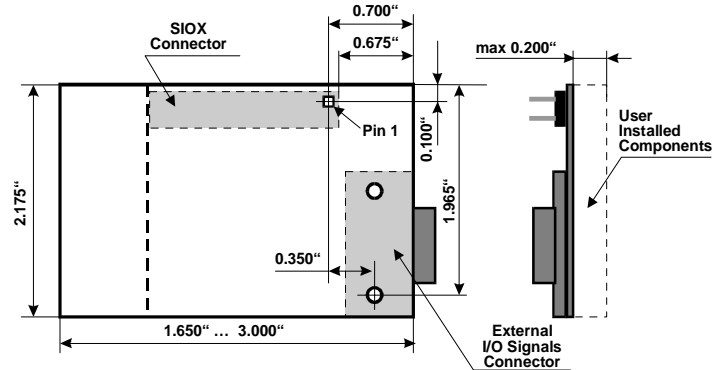
TORNADO-542L DSP system assumes *XIO-0* pin of SIOX/PIOX-16 interface sites to be configured by the on-board J3 jumper as either I/O pin (*XIOF-0* IOX flag) or as TMS320C542 DSP on-chip timer output (*TM*). *XIO-1* pin of SIOX/PIOX-16 interface sites is always configured as I/O pin (*XIOF-1* IOX flag).

TORNADO-548/549/5410/5416 DSP systems assume *XIO-0* pin of SIOX/PIOX-16 interface sites to be software configured via *XIO-CNF* IOX register as either I/O pin (*XIOF-0* IOX flag) or as TMS320C54x DSP on-chip timer output (*TM*). *XIO-1* pin of SIOX/PIOX-16 interface sites is always configured as I/O pin (*XIOF-1* IOX flag).

TORNADO-5402 DSP system assumes *XIO-0* pin of SIOX/PIOX-16 interface sites to be software configured via *XIO-CNF* IOX register as either I/O pin (*XIOF-0* IOX flag) or as TMS320VC5402 DSP on-chip timer output (*TM*). *XIO-1* pin of SIOX/PIOX-16 interface sites is always configured as I/O pin (*XIOF-1* IOX flag) in case the HPI port of on-board TMS320VC5402 DSP is enabled via clearing the *HPI_DISABLE* bit of *HPI_IE_FRG* flag register of host ISA-bus I/O interface. In case the HPI port of on-board TMS320VC5402 DSP is disabled via setting the *HPI_DISABLE* bit of *HPI_IE_FRG* flag register of host ISA-bus I/O interface, then the *XIO-1* pin of SIOX/PIOX-16 interface sites might be configured via *XIO-CNF* IOX register as either I/O pin (*XIOF-1* IOX flag) or as output of the second TMS320VC5402 DSP on-chip timer (*TM1*).

Physical Dimensions for SIOX DCM

Physical dimensions for SIOX DCM are presented at fig.2-15. This information is intended for those *TORNADO* customers, who need to design customized SIOX DCM.



SIOX connector: 20-pin or 26-pin straight dual-row mail header
(0.025" Sq., 0.1"x0.1" pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.2-15. Physical dimensions for SIOX DCM.

2.8 Scan-path Emulation Tools for **TORNADO-54x**

TORNADO-54x uses scan-path emulation technique for the on-board TMS320C54x DSP in order to debug resident TMS320C54x DSP environment and software. Compatible scan-path emulation tools, which can be used with **TORNADO-54x** are as the following:

- TI XDS510 and MicroLAB' **MIRAGE-510D** universal scan-path emulators
- low cost emulation controller chip (**ECC**) for **TORNADO-542L**, which plugs into the dedicated on-board S5 socket on **TORNADO-542L** mainboard
- low cost emulation control DCM (**UECMX**) for **TORNADO** DSP systems, which plugs into the dedicated JP6 site on **TORNADO-548/549/5402/5410/5416**. The **UECMX** converts **TORNADO-548/549/5402/5410/5416** DSP system into universal emulator for all TI TMS320 DSP if used with optional external buffer pod
- TI HLL Debuggers C5000 Code Composer Studio IDE as the debugging environments for TMS320 DSPs, which run with all of the above emulator tools (**ECC**, **UECMX**, TI XDS510 and MicroLAB' **MIRAGE-510D** universal scan-path emulators).

CAUTION

The DSP must be released from the 'RESET' state and placed into the 'RUN' state prior running TI C54x HLL Debugger C5000 Code Composer Studio IDE for debugging the on-board TMS320C54x DSP chip of *TORNADO-542L/548/549/5402/5410/5416* DSP system via JTAG path (use *-cr0* command line option of *T54CC.EXE* software utility).

It is recommended that the *T54CC.EXE* software utility will be invoked with the *-r* command line option just after the host power on or after any DSP software trouble situation. This will guarantee that the TMS320C54x DSP will be in the known state after the DSP will be released prior running the TI C54x HLL Debugger or C5000 Code Composer Studio IDE.

TORNADO-548/549/5402/5410/5416 on-board JTAG path for connection to external JTAG emulator

TORNADO-548/549/5402/5410/5416 on-board JTAG path for connection to external TI XDS510 or MicroLAB' *MIRAGE-510D* JTAG emulator is presented at figure 2-16 (refer to also fig. 2-1 and fig. A-1) and comprises of JTAG-IN connector (JP4), TMS320C54x JTAG port, JTAG-OUT connector (JP5) and JTAG path terminating jumper (J5).

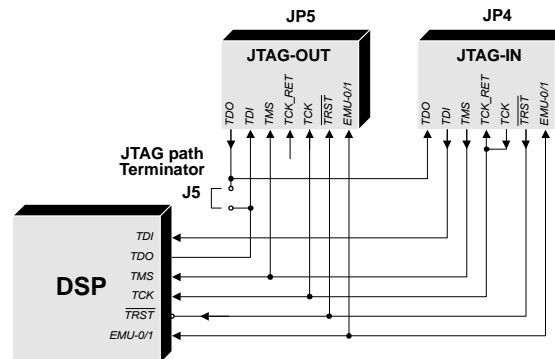


Fig. 2-16. On-board JTAG path for connection external JTAG emulator to *TORNADO-548/549/5402/5410/5416*.

The on-board JTAG-IN connector should be used for connection of either external JTAG emulator or for connection to the JTAG-OUT connector of 'previous' JTAG device in the JTAG path.

The on-board JTAG-OUT connector should be used in case another JTAG device(s) is(are) included in the same JTAG path 'after' *TORNADO-548/549/5402/5410/5416* board. In this case, the succeeding JTAG device should connect to JTAG-OUT connector of *TORNADO-548/549/5402/5410/5416* using JTAG EXTENSION CABLE in the daisy-chain manner. Last JTAG device should terminate JTAG path and return JTAG *TDO* signal back to the emulator, which is connected to the first JTAG device in JTAG path. JTAG devices, included into the JTAG path together with *TORNADO-548/549/5402/5410/5416* board, might include any JTAG supporting devices without any restrictions (logic, FPGA, other DSPs, etc). However the debugger JTAG path configuration file for JTAG emulator must accurately specify all JTAG devices in JTAG path.

CAUTION

The *TORNADO-548/549/5402/5410/5416* on-board J5 jumper is used for termination of JTAG path on *TORNADO-548/549/5402/5410/5416*.

J5 jumper should set to ON (installed) once *TORNADO-548/549/5402/5410/5416* is either the only or the last JTAG device in JTAG path.

J5 jumper should set to OFF (removed) once two or more JTAG devices are included into JTAG path, and *TORNADO-548/549/5402/5410/5416* is not the last JTAG device in JTAG path.

CAUTION

In case *TORNADO-548/549/5402/5410/5416* is used with other JTAG devices connected to the JTAG-OUT connector, then the succeeding JTAG devices should use the JTAG default *TCK* clock source, which outcomes from the JTAG-OUT connector of *TORNADO-548/549/5402/5410/5416*.

Using external JTAG emulator with single *TORNADO-548/549/5402/5410/5416* board

If external TI XDS510 or MicroLAB' *MIRAGE-510D* JTAG emulator is used for debugging single *TORNADO-548/549/5402/5410/5416* board, then this emulator must connect to the dedicated on-board JTAG-IN connector on *TORNADO-548/549/5402/5410/5416* mainboard with JTAG terminator jumper (J5) installed and the JTAG-OUT connector left unconnected (fig. 2-17). In this case the debugger JTAG path configuration file for JTAG emulator should be normally omitted (refer to your debugger user's guide for details how to handle the JTAG path configuration file).

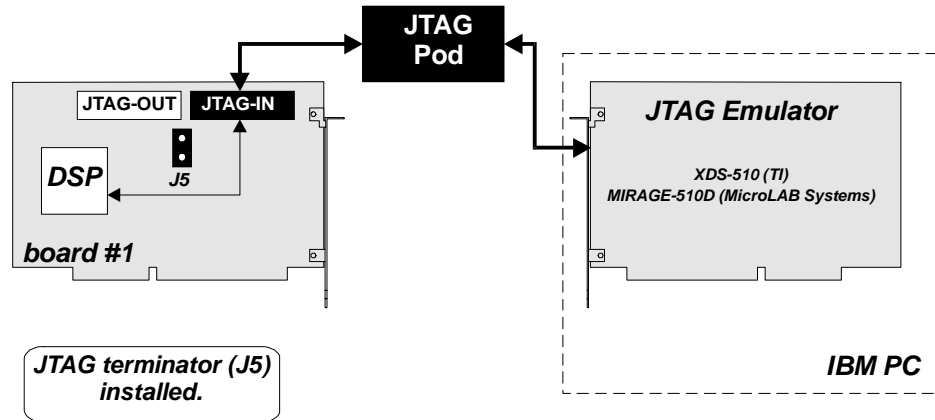


Fig. 2-17. Connection of external JTAG emulator to single *TORNADO-548/549/5402/5410/5416* board.

Using external JTAG emulator with multiple *TORNADO-548/549/5402/5410/5416* boards

If either TI XDS510 or MicroLAB' *MIRAGE-510D* universal JTAG emulator is used for debugging either multiple *TORNADO-548/549/5402/5410/5416* boards or *TORNADO-548/549/5402/5410/5416* board with other JTAG devices (other *TORNADO* boards, FPGA, other DSPs) in the same JTAG path, then this emulator should connect to the on-board JTAG-IN connector (JP4) of the 'first' *TORNADO-548/549/5402/5410/5416* board in JTAG-path (refer to fig. 2-18).

The on-board JTAG-OUT connector (JP5) of the 'first' and 'intermediate' boards should connect to the 'next' JTAG device in the JTAG path using JTAG EXTENSION CABLE in the daisy-chain manner.

The 'last' JTAG device in JTAG path should terminate JTAG path via JTAG terminator jumper (J5) and return the JTAG *TDO* signal back to JTAG emulator, which is connected to the first JTAG device in JTAG path.

The debugger JTAG path configuration file for JTAG emulator must accurately specify all JTAG devices in the JTAG path (refer to your debugger user's guide for details how to handle the JTAG path configuration file).

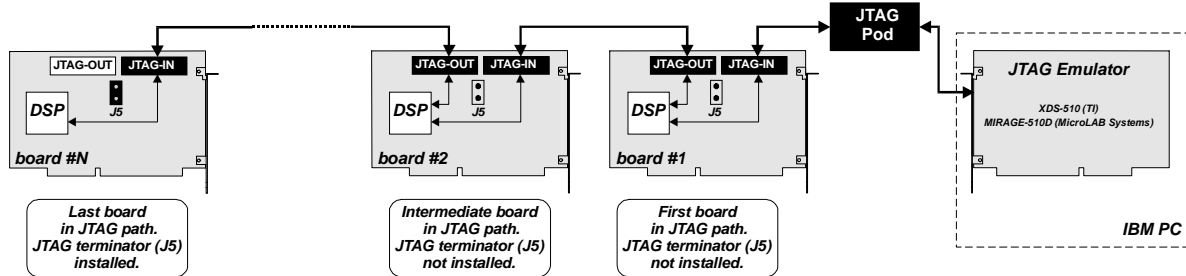


Fig. 2-18. Connection of external JTAG emulator to multiple *TORNADO-548/549/5402/5410/5416* boards.

TORNADO-548/549/5402/5410/5416 on-board JTAG path for UECMX emulator DCM

UECMX is actually the low-cost replacement for external TI XDS510 and MicroLAB' *MIRAGE-510D* universal JTAG emulators, however it does not require external JTAG pod for connection to *TORNADO-548/549/5402/5410/5416* board via JTAG-IN connector. Instead, the on-board *TORNADO-548/549/5402/5410/5416* hardware provides direct connection of the *UECMX* JTAG port to the on-board TMS320C54x DSP in case *UECMX* is installed and configured for operation with on-board DSP. Therefore, all available JTAG-path configurations for *UECMX* is similar to that with external JTAG emulator.

TORNADO-548/549/5402/5410/5416 on-board JTAG path for connection to low-cost MicroLAB' *UECMX* universal JTAG emulator DCM for *TORNADO* DSP systems is presented at figure 2-19 (refer to also fig. 2-1 and fig. A-1) and comprises of *UECMX* site header connector (JP6), TMS320C54x JTAG port, JTAG-OUT connector (JP5) and JTAG path terminating jumper (J5).

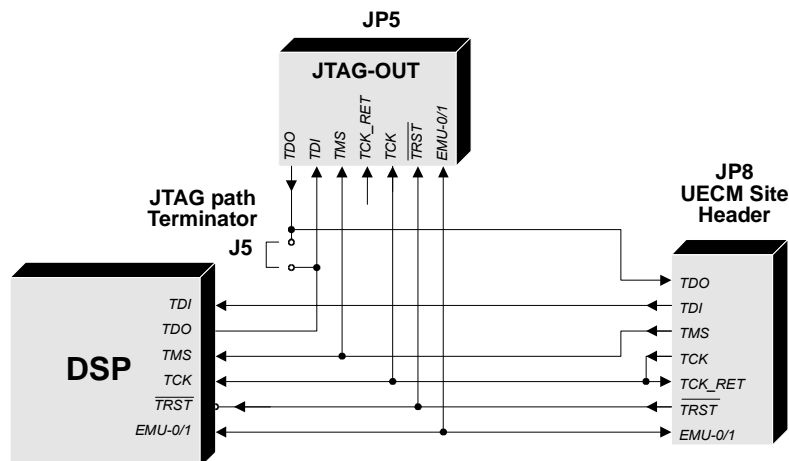


Fig. 2-19. On-board JTAG path for connection *UECMX* to *TORNADO-548/549/5402/5410/5416*.

UECMX might be configured to connect either to *TORNADO-548/549/5402/5410/5416* on-board TMS320C54x DSP or to any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP via optional MPD or JTAG pod. This configuration is performed by the *T54CC.EXE* software utility, which is included with the *TORNADO-548/549/5402/5410/5416* board (refer to chapter 4).

UECMX runs under the industry standard TI C54x HLL Debugger and C5000 Code Composer Studio IDE, when it is configured for debugging the *TORNADO-548/549/5402/5410/5416* on-board TMS320C54x DSP environment, and runs under any of TI C2xx, C3x, C4x, C5x, C54x, C6x HLL Debuggers or any of C2xx/C5x, C3x/C4x, C5000 and C6000 Code Composer IDE in case it is used for emulation of external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP via optional MPD or JTAG pod.

CAUTION

Once *UECMX* is installed onto *TORNADO-548/549/5402/5410/5416* mainboard and configured for connection to the on-board DSP, then the on-board hardware disconnects the JTAG-IN (JP4) connector from on-board JTAG-path.

In this case the external TI XDS510 or MicroLAB' *MIRAGE-510D* emulator, which is connected to JTAG-IN connector *TORNADO-548/549/5402/5410/5416* is ignored and its operation does not effect the functionality of *TORNADO-548/549/5402/5410/5416* board.

Using *UECMX* with single *TORNADO-548/549/5402/5410/5416* board

If *UECMX* is used for debugging single *TORNADO-548/549/5402/5410/5416* board, then *UECMX* should install onto this board to the dedicated *UECMX* site header (JP6) on *TORNADO-548/549/5402/5410/5416* mainboard with the JTAG terminator jumper (J5) installed and the JTAG-OUT connector left unconnected (fig. 2-20). In this case the debugger JTAG path configuration file for *UECMX* should be normally omitted (refer to your debugger user's guide for details how to handle the JTAG path configuration file).

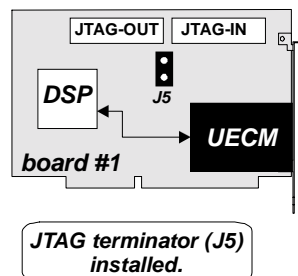


Fig. 2-20. Connection of *UECMX* to single *TORNADO-548/549/5402/5410/5416* board.

Using *UECMX* with multiple *TORNADO-548/549/5402/5410/5416* boards

If *UECMX* is used for debugging either multiple *TORNADO-548/549/5402/5410/5416* boards or *TORNADO-548/549/5402/5410/5416* board with other JTAG devices (other *TORNADO* boards, FPGA,

other DSPs) in the same JTAG path, then *UECMX* should install onto the 'first' *TORNADO-548/549/5402/5410/5416* board in JTAG-path (refer to fig. 2-21).

The on-board JTAG-OUT connector (JP5) of the 'first' and 'intermediate' boards should connect to the 'next' JTAG device in the JTAG path using JTAG EXTENSION CABLE in the daisy-chain manner.

The 'last' JTAG device in JTAG path should terminate JTAG path via JTAG terminator jumper (J5) and return the JTAG *TDO* signal back to JTAG emulator, which is connected to the first JTAG device in JTAG path.

The debugger JTAG path configuration file for JTAG emulator must accurately specify all JTAG devices in the JTAG path (refer to your debugger user's guide for details how to handle the JTAG path configuration file).

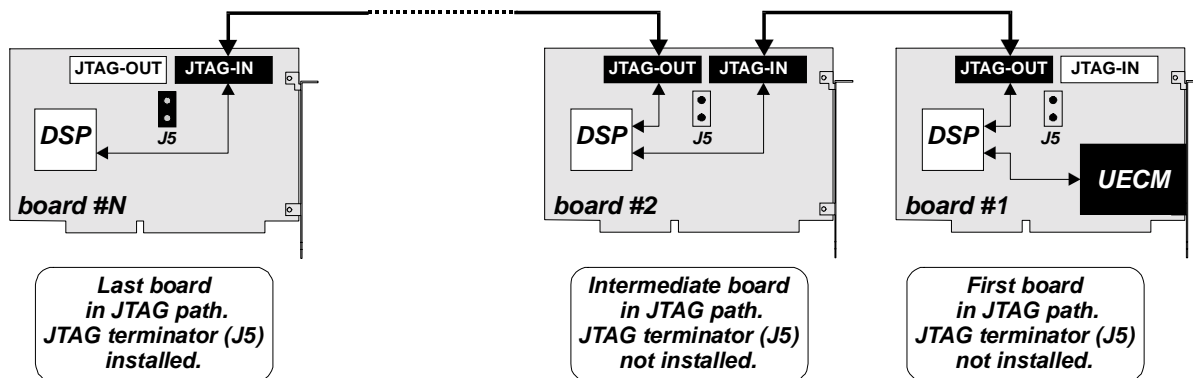


Fig. 2-21. Connection of *UECMX* to multiple *TORNADO-548/549/5402/5410/5416* boards.

Using *UECMX* for emulation external TI TMS320 DSPs

UECMX also converts *TORNADO-548/549/5402/5410/5416* into universal scan-path emulator for any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP. This feature requires optional external MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x) pod connected to *UECMX* (fig.2-22). This optional external pod also connects to target TMS320 DSP. The MPSD and JTAG pods for *UECMX* are the pods used with MicroLAB' *MIRAGE-510D* emulator.

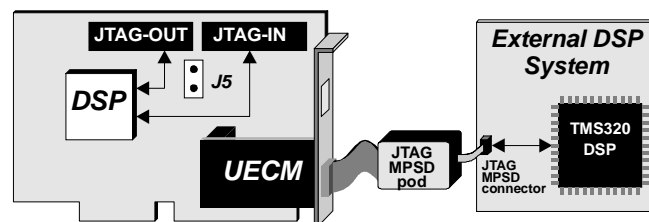


Fig. 2-22. Connection of *UECMX* to external TMS320 DSP via optional MPSD or JTAG path.

When *UECMX* is configured for emulation of any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP via optional MPSPD or JTAG pod, then it may run under any of TI C2xx, C3x, C4x, C5x, C54x, C6x HLL Debuggers or any of C2xx/C5x, C3x/C4x, C5000 and C6000 Code Composer IDE.

CAUTION

Once *UECMX* is installed onto *TORNADO-548/549/5402/5410/5416* mainboard and configured for connection to external TMS320 DSP via optional MPSPD or JTAG pod, then the on-board hardware disconnects *UECMX* from on-board JTAG-path and configures the on-board JTAG-path for connection to external TI XDS510 or MicroLAB' *MIRAGE-510D* emulator via JTAG-IN (JP4) connector.

This allows any of single- or multi- board JTAG-path device configurations in accordance with the described above for external TI XDS510 or MicroLAB' *MIRAGE-510D* emulator.

TORNADO-542L on-board JTAG-path

The on-board JTAG path for *TORNADO-542L* (fig.2-23) comprises of JTAG-IN connector (JP4), TMS320C542 DSP and the *ECC* (emulation control chip, also known as TBC) socket site (S5).

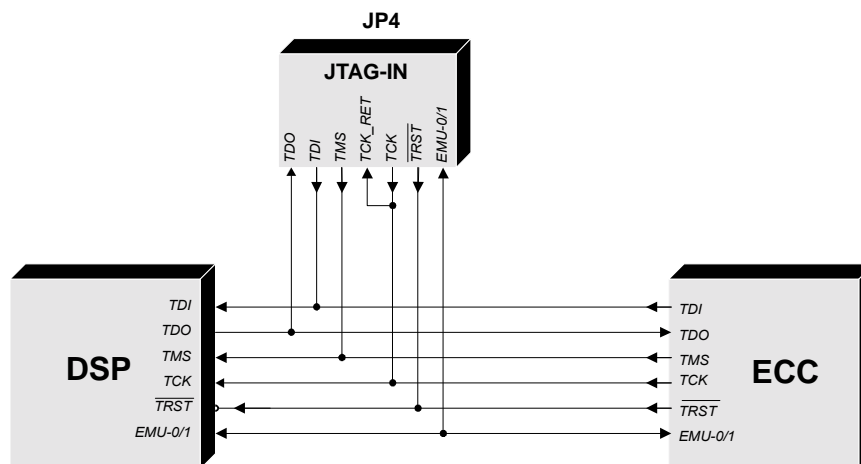


Fig. 2-23. On-board JTAG path of *TORNADO-542L*.

JTAG-IN connector is designed for connection of external TI XDS510 or MicroLAB' *MIRAGE-510D* JTAG emulator, and is actually paralleled with optional on-board *ECC*.

CAUTION

If TI XDS510 or MicroLAB' *MIRAGE-510D* universal scan-path emulator is being used with *TORNADO-542L*, then the emulation controller chip (*ECC*) should be switched off, and vice-versa.

Connection of external XDS510 and *MIRAGE-510D* emulators to the *TORNADO-542L* on-board JTAG-IN connector while *ECC* is installed and is configured to connect to the on-board TMS320C542 DSP is strongly prohibited and may result in damage of either *ECC* or external XDS510 and *MIRAGE-510D* emulators.

CAUTION

JTAG path of *TORNADO-542L* does not provide the dedicated JTAG 'multiprocessor-chaining' hardware (JTAG-OUT connector and JTAG path terminator).

When either of external JTAG emulator or *ECC* is used for emulation the *TORNADO-542L* on-board TMS320C542 DSP, then JTAG 'multiprocessor-chain' mode is not allowed as standard with this JTAG connection.

Should the user consider to use *TORNADO-542L* in JTAG 'multiprocessor-chain' while emulating the on-board TMS320C542 DSP, then optional external JTAG-path IN/OUT splitter is required. Call MicroLAB Systems for details.

Using external JTAG emulator with TORNADO-542L

If external TI XDS510 or MicroLAB' *MIRAGE-510D* JTAG emulator is considered for debugging the *TORNADO-542L* on-board TMS320C542 DSP environment, then this emulator should connect to the dedicated on-board JTAG-IN connector on *TORNADO-542L* mainboard (refer to fig.2-1, fig.2-24 and fig. A-1).

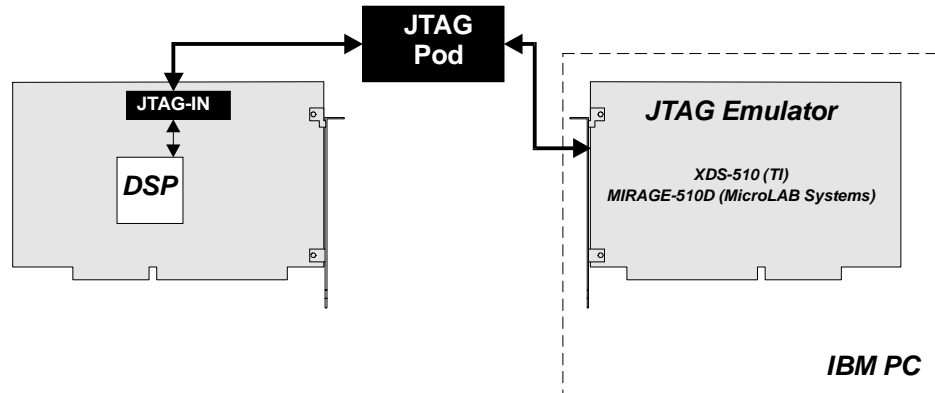


Fig. 2-24. Connection of external JTAG emulator to TORNADO-542L.

CAUTION

If TI XDS510 or MicroLAB' *MIRAGE-510D* universal scan-path emulator is being used with *TORNADO-542L*, then the emulation controller chip (*ECC*) should be switched off.

Connection of external XDS510 and *MIRAGE-510D* emulators to the *TORNADO-542L* on-board JTAG-IN connector while *ECC* is installed and is configured to connect to the on-board TMS320C542 DSP is strongly prohibited and may result in damage of either *ECC* or external XDS510 and *MIRAGE-510D* emulators.

Using *ECC* for emulation the TORNADO-542L on-board TMS320C542 DSP

In case *TORNADO-542L* is used inside the closed computer package, or external TI XDS510 or MicroLAB' *MIRAGE-510D* universal JTAG emulator is not available, then optional *ECC* (emulation controller chip, also known as TBC) is recommended for emulation of *TORNADO-542L* on-board TMS320C542 DSP.

ECC is a low-cost replacement for external TI XDS510 and MicroLAB' *MIRAGE-510D* universal JTAG emulators and installs into the dedicated S5 socket on *TORNADO-542L* mainboard (fig.2-25). *ECC* does not require external JTAG pod for connection to *TORNADO-542L* board via JTAG-IN connector. Instead, the on-board *TORNADO-542L* hardware provides direct connection of *ECC* JTAG port to the on-board TMS320C542 DSP in case *ECC* is installed.

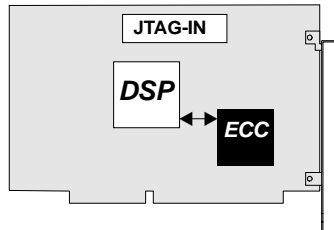


Fig. 2-25. Connection of *ECC* to *TORNADO-542L* on-board TMS320C542 DSP.

ECC runs under the industry standard TI TMS320C54x HLL Debugger and GoDSP TMS320C54x Code Composer IDE.

Note, that *ECC* might be activated and allocated into the host PC-bus I/O area by means of the *T54CC.EXE* software utility, which is included with the *TORNADO-542L* board (refer to chapter 4).

CAUTION

Once *ECC* is installed, then the external XDS510 or *MIRAGE-510D* emulator should be disconnected from the JTAG-IN connector of *TORNADO-542L*.

Connection of external XDS510 and *MIRAGE-510D* emulators to the *TORNADO-542L* on-board JTAG-IN connector while *ECC* is installed and is configured to connect to the on-board TMS320C542 DSP is strongly prohibited and may result in damage of either *ECC* or external XDS510 and *MIRAGE-510D* emulators.

2.9 Software Development Tools

TMS320C54x DSPs are now the industry standard DSPs and are supported by a variety of software development tools from multiple 3rd party vendors.

Compilers and Debuggers

Software development for *TORNADO-54x* is supported by TI TMS320C54x DSP Optimizing C Compiler and Assembly Language Tools.

Debugging of TMS320C54x DSP resident software for *TORNADO-54x* is supported by TI HLL Debugger and C5000 Code Composer Studio IDE (www.ti.com). Both debuggers require either on-board optional emulation controller chip (*ECC*) installed for *TORNADO-542L* or *UECMX* emulation control DCM installed for *TORNADO-548/549/5402/5410/5416*, which may ship together with *TORNADO-54x* DSP system.

Real-time Multitasking Operating Systems (RTOS)

TORNADO-54x is supported by multiple RTOS that provide multitasking capabilities:

- ***VIRTUOSO*** from Eonic Systems Inc (www.eonic.com) is an industry standard high-performance RTOS and provides full feature multitasking support. It comes standard with capabilities for host file, keyboard and screen text/graphics I/O from DSP environment via *TORNADO-54x* host ISA-bus interface, and is available with a wide selection of function libraries for DSP, math, matrix, 2D, etc. computations.
- ***NUCLEUS PLUS*** from Accelerated Technology Inc (www.atinucleus.com) is an industry standard single-processor high-performance RTOS and provides full feature multitasking support. It features low cost and comes standard with source codes. Available options include ***NUCLEUS FILE***, ***NUCLEUS NET***, and ***NUCLEUS DBUG+*** that also come in source codes.

Application Software Tools for TORNADO-54x

Application specific software tools for *TORNADO-54x* DSP system include a variety of function libraries for DSP, math, vector, image, etc computation, as well as function libraries for vocoder/fax/modem applications and audio multimedia.

Chapter 3. Installation and Configuration

This chapter includes instructions for configuring and installation of *TORNADO-54x* DSP system into host ISA-bus PC.

3.1 Setting I/O Base Address for Host ISA-bus I/O Interface

You have to setup ISA-bus I/O base address for host ISA-bus I/O interface of *TORNADO-542L* prior installation of *TORNADO-54x* board into ISA-bus slot of host PC. This procedure should be done while host PC power is switched off.

I/O base address for host ISA-bus I/O interface of *TORNADO-54x* is configured by means of on-board DIP-switch SW1 (refer to fig.2-2 and fig.A-1) in accordance with configuration setting in table 2-4.

CAUTION

When setting I/O base address for host ISA-bus I/O interface be sure to check I/O base address for other hardware installed in your host PC in order to avoid I/O address conflicts on ISA-bus.

TORNADO-54x is shipped from factory with I/O base address for host ISA-bus I/O interface in accordance with default settings from table 2-4.

3.2 Setting Interrupt Request Line for Host PC

Setting of host PC interrupt request line is optional procedure for *TORNADO-54x* and should be performed in accordance with requirements of application software that you use together with *TORNADO-54x*. This procedure should be done while host PC power is switched off.

Setting of host PC interrupt request line is provided via on-board host PC interrupt request jumper J1 (refer to fig.2-2 and fig.A-1). See section 2.5 for details about *TORNADO-54x* host PC interrupt support. *TORNADO-54x* is shipped from factory without PC interrupt request jumper installed.

CAUTION

When setting host CPU interrupt request line be sure to check interrupt requests for other hardware installed in your host PC in order to avoid interrupt request conflicts on ISA-bus.

3.3 Installation of *TORNADO-54x* Mainboard into Host PC

After I/O base address for host ISA-bus I/O interface of *TORNADO-54x* has been configured and host PC interrupt request line has been setup, you can now install *TORNADO-54x* board into 16-bit ISA-bus slot of host PC and screw on-board *TORNADO-54x* mounting bracket to rear panel of host PC. Afterthat, you can safely switch on power of host PC and load operating system of your PC.

3.4 Setting Memory Base Address for Host ISA-bus Memory Interface

After *TORNADO-54x* has been installed into host PC, the PC power has been switched on, and DOS has been loaded, you can proceed with configuring ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-54x*.

It is recommended to use *T54CC.EXE* software utility for configuring ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-54x* at DOS prompt.

Setting host PC software environment for accessing host ISA-bus memory interface of TORNADO-54x

Prior you will start working with *TORNADO-54x* host ISA-bus memory interface, you have to configure host PC software environment in order it can properly communicate with host ISA-bus memory interface of *TORNADO-54x*.

If memory base address of *TORNADO-54x* host ISA-bus memory interface should be set to *D8000H* hex value, then this requires including the following line into CONFIG.SYS file of host DOS or WINDOWS 3x/95/98 operating system:

Device=C:\DOS\EMM386.EXE noems x=D800-DFFF

or

Device=C:\WINDOWS\EMM386.EXE noems x=D800-DFFF

The "x=D800-DFFF" option for the *EMM386.EXE* memory driver informs *EMM386.EXE* memory driver to reserve the *D8000H..DFFFFH* UMB area, so it will might be used for communication with *TORNADO-54x* host ISA-bus memory interface.

Should you need to setup different memory base address of *TORNADO-54x* host ISA-bus memory interface in accordance with table 2-3, then you should setup appropriate "x=" option for *EMM386.EXE* memory driver in CONFIG.SYS file. Please refer to documentation for DOS and WINDOWS operating system for details.

Setting memory base address for host ISA-bus memory interface in *TORNADO-54x*

You have to invoke *T54CC.EXE* software utility with *-imXXXXX* command line option in order to setup ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-542L* at DOS prompt in accordance with table 2-3.

The following example sets *D8000H* memory base address for host ISA-bus memory interface of *TORNADO-54x*:

T54CC -imD8000

In case I/O base address of host ISA-bus I/O interface of *TORNADO-54x* differs from default value specified in table 2-4, then you have also specify *-ipXXX* command line option (where *XXX* denotes I/O base address of host ISA-bus I/O interface for *TORNADO-54x*) in DOS command line when invoking *T54CC.EXE* software utility. The following example demonstrates how to invoke *T54CC.EXE* software utility for *TORNADO-54x* DSP system with I/O base address for host ISA-bus I/O interface being configured to 300H value:

T54CC -imD8000 -ip300

Switching Off host ISA-bus memory interface of *TORNADO-54x*

The following example demonstrates how to switch off host ISA-bus memory interface of *TORNADO-54x* DSP system:

T54CC -im0

CAUTION

When setting memory base address for host ISA-bus memory interfaces be sure to check memory base address for other hardware installed in your host PC in order to avoid memory address conflicts on ISA-bus.

3.5 Installation of Emulation Controller (ECC) onto *TORNADO-542L* Mainboard

Installation of emulation controller chip (ECC) onto *TORNADO-542L* board should be performed while host PC power off.

Installation of ECC

In order to install emulation controller chip (ECC) onto *TORNADO-542L* board follow recommendations below (refer to fig. 3-1):

- switch off power of host PC
- remove *TORNADO-542L* board from host PC ISA-bus slot
- take *ECC* by your fingers in such way that its front (labeling) surface is turned at you
- adjust *ECC* to be parallel to surface of the corresponding PLCC-44 socket on *TORNADO-542L* board
- orient *ECC* in such way, that the key corner of its PLCC-44 package would match the corresponding corner of on-board PLCC-44 socket
- safely insert *ECC* into on-board PLCC-44 socket
- safely plug and fix *ECC* in the on-board PLCC-44 socket
- install *TORNADO-542L* into 16-bit ISA-bus slot of host PC
- switch on power of host PC

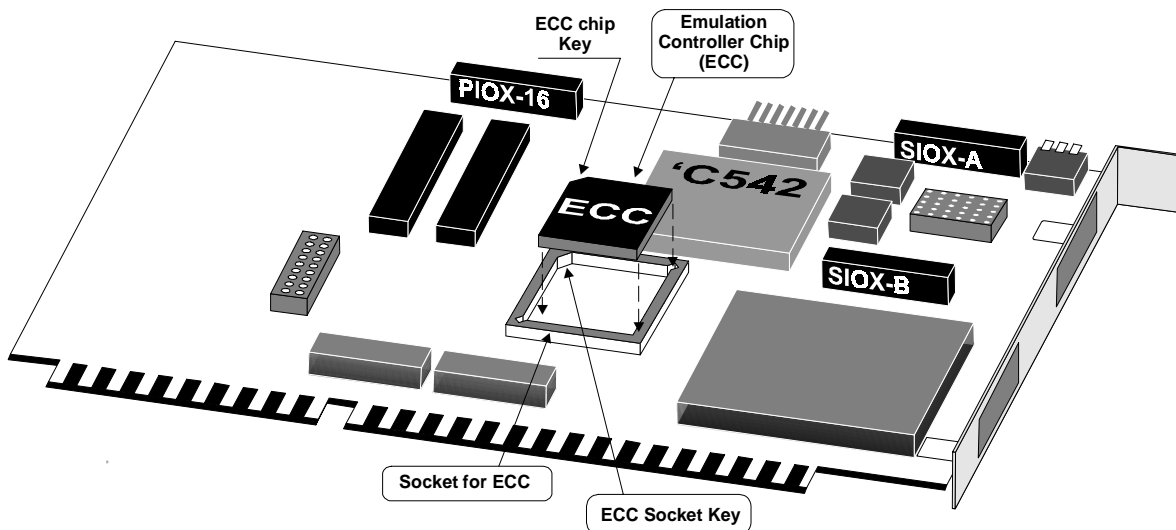


Fig.3-1. Installation of emulation controller chip (ECC) onto *TORNADO-542L* board.

Setting I/O Base Address for ECC

You have to invoke *T54CC.EXE* software utility with *-epXXX* command line option in order to setup ISA-bus I/O base address for *ECC* at DOS prompt in accordance with table 2-10.

The following example sets *240H* I/O base address for *ECC*:

T54CC -ep240

In case I/O base address of host ISA-bus I/O interface of *TORNADO-542L* differs from default value specified in table 2-4, then you have also specify *-ipXXX* command line option (where *XXX* denotes I/O base address of

host ISA-bus I/O interface for *TORNADO-542L*) in DOS command line when invoking *T54CC.EXE* software utility. The following example demonstrates how to invoke *T54CC.EXE* software utility for *TORNADO-542L* DSP system with I/O base address for host ISA-bus I/O interface being configured to 300H value:

```
T54CC -ep240 -ip300
```

Switching ECC Out from ISA-bus I/O Address Space

The following example demonstrates how to switch *ECC* out from ISA-bus I/O address space:

```
T54CC -ep0
```

CAUTION

When setting I/O base address for *ECC* be sure to check I/O base address for other hardware installed in your host PC in order to avoid I/O address conflicts on ISA-bus.

3.6 Installation of *UECMX* DCM onto *TORNADO-548/549/5402/5410/5416* Mainboard

You have to install *UECMX* module as a DCM (refer to fig.1-1) into the dedicated on-board connector of *TORNADO-548/549/5402/5410/5416* mainboard (refer to fig.2-2 and fig.A-1).

CAUTION

Once you install the *UECMX* DCM onto the *TORNADO-548/549/5402/5410/5416* mainboard, you cannot use SIOX-B site for installation of SIOX AD/DA/DIO DCM.

In order to install *UECMX* module onto *TORNADO-548/549/5402/5410/5416* mainboard you have to follow the instructions below (refer to fig.3-2):

- slant *UECMX* module
- insert the on-module connector for active buffer pod into the corresponding hole in the *TORNADO-548/549/5402/5410/5416* mounting bracket
- plug in the *UECMX* male header into the dedicated female connector on *TORNADO-548/549/5402/5410/5416* mainboard
- setup the ISA-bus I/O base address for the *UECMX* module using the on-module DIP-switch in accordance with the “*UECMX/ECC* User’s Guide”.

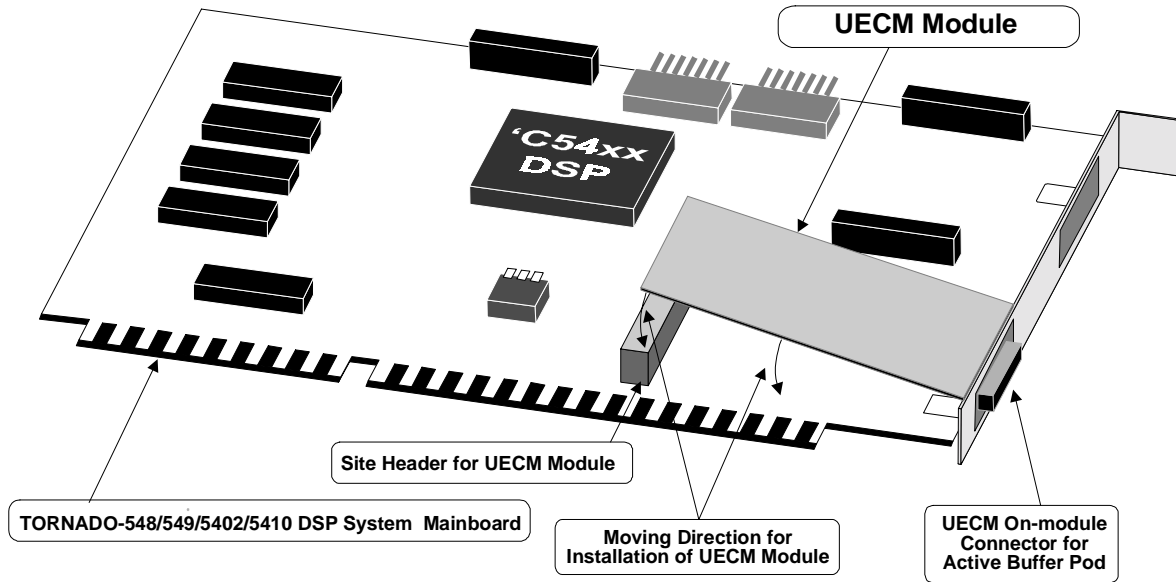


Fig.3-2. Installation of *UECMX* DCM onto *TORNADO-548/549/5402/5410/5416* mainboard.

The *UECMX* can connect either to the on-board DSP of *TORNADO-548/549/5402/5410/5416* or to any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP via optional external buffer pod.

Configuring *UECMX* to connect to the on-board DSP JTAG path of *TORNADO-548/549/5402/5410/5416*

After power-on, the *UECMX* is connect to the on-board DSP JTAG path of *TORNADO-548/549/5402/5410/5416*. You do not need to use any external JTAG pod for this configuration.

CAUTION

When using the *UECMX* DCM to emulate the on-board DSP of *TORNADO-548/549/5402/5410/5416*, be sure to set properly the on-board JTAG path terminator jumper (J5) in accordance with figure 2-15.

If you want to setup this connection again, you should use the *T54CC.EXE* software utility with '*-ei*' command line option. If *UECMX* is allocated at the I/O base address that differs from the 240H I/O base address, then use '*-epXXX*' command line option for specifying the I/O base address for *UECMX* (default is the '*-ep240*' configuration).

The following command line configures the *UECMX*, which is allocated at the 280H I/O base address, to connect to the on-board DSP JTAG path of *TORNADO-548/549/5402/5410/5416*:

T54CC -ei -ep280

Using UECMX for emulation of external TMS320 DSP

If you want to use *UECMX* to emulate any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x DSP, you have to use optional MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x) external buffer pod for connection between the *UECMX* and external TMS320 DSP.

In order to configure the *UECMX* to connect to external TMS320 DSP, you can use the *T54CC.EXE* software utility with ‘*-EX*’ command line option and the ‘*-epXXX*’ command line option for specifying the I/O base address for *UECMX* (default is the ‘*-epXXX*’ configuration).

The following command line configures the *UECMX* (allocated at the 280H I/O base address) to connect to external TMS320 DSP via optional external buffer MPSD or JTAG pod:

T54CC -ex -ep280

Chapter 4. Utility Software

This chapter contains description of utility software for *TORNADO-54x* DSP system.

4.1 *T54CC.EXE* Control Center Utility

T54CC.EXE (“*TORNADO-54x* Control Center”) utility is a DOS command line control tool for *TORNADO-54x* that delivers simple and powerful user control for *TORNADO-54x* hardware. *T54CC.EXE* utility runs under DOS and Windows 3.x/95/98, and features the following functionality:

- display and set all registers of *TORNADO-54x* host ISA-bus I/O interface
- read/write from/to on-board SRAM (Program/Data memory areas) and PIOX-16 I/O area via *TORNADO-54x* host ISA-bus memory interface
- access to the HPI port of TMS320C54x DSP
- configure the *ECC* emulation controller for *TORNADO-542L* and *UECMX* emulation control DCM for *TORNADO-548/549/5402/5410/5416*.

T54CC.EXE utility should be invoked from DOS with up to ten command line options specified:

T54CC [-option1] [-option2] [-option3] ...

Each command line option corresponds to specific *TORNADO-54x* hardware control operation. The following is a list of available command line options for *T54CC.EXE* utility.

System Control via *CONTROL REGISTER*

-c	Display and interpret contents of <i>CONTROL REGISTER</i> .
-cg	Display current state of <i>SB_GLOCK</i> bit (global SB locking by host ISA-bus memory interface) of <i>CONTROL REGISTER</i> .
-cg0	Clear <i>SB_GLOCK</i> bit of <i>CONTROL REGISTER</i> and unlock SB.
-cg1	Set <i>SB_GLOCK</i> bit of <i>CONTROL REGISTER</i> for immediate active SB locking.
-cl	Display current state of <i>SB_LOCK</i> bit (SB locking by host ISA-bus memory interface) of <i>CONTROL REGISTER</i> .
-cl0	Clear <i>SB_LOCK</i> bit of <i>CONTROL REGISTER</i> and unlock SB.
-cl1	Set <i>SB_LOCK</i> bit of <i>CONTROL REGISTER</i> and issue active SB locking during nearest SB access from host ISA-bus memory interface.
-cie	Display current state of <i>SB_ERROR_IE</i> bit (host interrupt enable on SB error) of <i>CONTROL REGISTER</i> .
-cie0	Clear <i>SB_ERROR_IE</i> bit of <i>CONTROL REGISTER</i> and disable host interrupts on SB error.
-cie1	Set <i>SB_ERROR_IE</i> bit of <i>CONTROL REGISTER</i> and enable host interrupts on SB error.

<i>-cim</i>	Display current state of <i>MH_RQ_IE</i> bit (host interrupt enable on requests from TMS320C54x DSP) of <i>CONTROL REGISTER</i> .
<i>-cim0</i>	Clear <i>MH_RQ_IE</i> bit of <i>CONTROL REGISTER</i> and disable host interrupts on requests from TMS320C54x DSP.
<i>-cim1</i>	Set <i>MH_RQ_IE</i> bit of <i>CONTROL REGISTER</i> and enable host interrupts on requests from TMS320C54x DSP.
<i>-cr</i>	Display current state of reset signal for TMS320C54x DSP, which is specified by <i>M_GO</i> bit of <i>CONTROL REGISTER</i> .
<i>-cr0</i>	Remove reset signal for TMS320C54x DSP, i.e. put DSP into “RUN” state. This option sets <i>M_GO</i> bit of <i>CONTROL REGISTER</i> .
<i>-cr1</i>	Apply reset signal for TMS320C54x DSP, i.e. put DSP into “RESET” state. This option clears <i>M_GO</i> bit of <i>CONTROL REGISTER</i> .

Flag Registers Control

<i>-fsr</i>	Display contents of <i>FLAG SELECTOR REGISTER</i> .
<i>-fsrXX</i>	Select flag register #XX (hex), i.e. load XX 8-bit hex data into <i>FLAG SELECTOR REGISTER</i> .
<i>-fr</i>	Display contents of currently selected flag register (display <i>FLAG STATUS REGISTER</i>). The number of currently selected flag register is defined by the contents of <i>FLAG SELECTOR REGISTER</i> .
<i>-frXX</i>	Loads XX 8-bit hex data into the currently selected flag register (load <i>FLAG CONTROL REGISTER</i>). The number of currently selected flag register is defined by the contents of <i>FLAG SELECTOR REGISTER</i> .
<i>-frs</i>	Display and interpret contents of <i>SYS_STATUS_FRG</i> flag register.
<i>-fe</i>	Display current state of <i>SB_ERROR</i> flag from <i>SYS_STATUS_FRG</i> flag register.
<i>-fe0</i>	Clear <i>SB_ERROR</i> flag, i.e. write to <i>CLEAR_SB_ERROR_FRG</i> flag register.
<i>-fb</i>	Display current state of <i>SB_ACK</i> flag from <i>SYS_STATUS_FRG</i> flag register.
<i>-fh</i>	Display current state of <i>MH_RQ</i> flag from <i>SYS_STATUS_FRG</i> flag register.
<i>-fh0</i>	Clear <i>MH_RQ</i> flag, i.e. write to <i>CLEAR_MH_RQ_FRG</i> flag register.
<i>-fhh</i>	Display current state of <i>HPI_HINT</i> DSP-to-host interrupt request via HPI from <i>SYS_STATUS_FRG</i> flag register.
<i>-fhe</i>	Display current state of <i>HPI_ERROR</i> flag from <i>SYS_STATUS_FRG</i> flag register.

<i>-fhe0</i>	Clear <i>HPI_ERROR</i> flag, i.e. write to <i>CLEAR_HPI_ERROR_FRG</i> flag register.
<i>-fm1</i>	Generate interrupt request to TMS320C54x DSP, i.e. write to <i>SET_HM_RQ_FRG</i> flag register.
<i>-fhi</i>	Display and interpret contents of <i>HPI_IE_FRG</i> flag register.
<i>-fhie</i>	Display current state of <i>HPI_ERROR_IE</i> bit (host interrupt enable on <i>HPI_ERROR</i>) of <i>HPI_IE_FRG</i> flag register.
<i>-fhie0</i>	Clear <i>HPI_ERROR_IE</i> bit of <i>HPI_IE_FRG</i> flag register and disable host interrupts on <i>HPI_ERROR</i> .
<i>-fhie1</i>	Set <i>HPI_ERROR_IE</i> bit of <i>HPI_IE_FRG</i> flag register and enable host interrupts on <i>HPI_ERROR</i> .
<i>-fhih</i>	Display current state of <i>HPI_HINT_IE</i> bit (host interrupt enable on <i>HPI_HINT</i>) of <i>HPI_IE_FRG</i> flag register.
<i>-fhih0</i>	Clear <i>HPI_HINT_IE</i> bit of <i>HPI_IE_FRG</i> flag register and disable host interrupts on <i>HPI_HINT</i> .
<i>-fhih1</i>	Set <i>HPI_HINT_IE</i> bit of <i>HPI_IE_FRG</i> flag register and enable host interrupts on <i>HPI_HINT</i> .
<i>-fhid</i>	Display current state of <i>HPI_DISABLE</i> bit of <i>HPI_IE_FRG</i> flag register of <i>TORNADO-5402</i> DSP system.
<i>-fhid0</i>	Clear <i>HPI_DISABLE</i> bit of <i>HPI_IE_FRG</i> flag register of <i>TORNADO-5402</i> DSP system, i.e. enable HPI feature of on-board TMS320VC5402 DSP and disable output of second DSP on-chip timer (<i>TM1</i>) as soon as the DSP reset signal will be released (i.e. when the <i>M_GO</i> bit of <i>CONTROL REGISTER</i> will change from the <i>M_GO</i> =0 state to <i>M_GO</i> =1 state). This options is allowed only during TMS320VC5402 DSP is in the 'RESET' state (<i>M_GO</i> =0).
<i>-fhid1</i>	Set <i>HPI_DISABLE</i> bit of <i>HPI_IE_FRG</i> flag register for <i>TORNADO-5402</i> DSP system, i.e. disable HPI feature of on-board TMS320VC5402 DSP and enable output of second DSP on-chip timer (<i>TM1</i>) as soon as the DSP reset signal will be released (i.e. when the <i>M_GO</i> bit of <i>CONTROL REGISTER</i> will change from the <i>M_GO</i> =0 state to <i>M_GO</i> =1 state). This options is allowed only during TMS320VC5402 DSP is in the 'RESET' state (<i>M_GO</i> =0).
<i>-fds</i>	Display and interpret contents of <i>DSP_STATUS_FRG</i> flag register.
<i>-fdsm</i>	Display current state of <i>DSP_MLock</i> bit of <i>DSP_STATUS_FRG</i> flag register.
<i>-fdsr</i>	Display current state of <i>DSP_M_GO</i> bit (read-back value of <i>M_GO</i> bit of <i>CONTROL REGISTER</i>) of <i>DSP_STATUS_FRG</i> flag register.

- fdsh** Display current state of *DSP_HPI_DISABLE* bit (current state of HPI TMS320VC5402 DSP HPI enable feature for *TORNADO-5402* DSP system) of *DSP_STATUS_FRG* flag register.
- frdi** Display *TORNADO-54x* device ID and s/n, which are contained in *DEV_ID0_FRG* and *DEV_ID1_FRG* flag registers.

SB Access Control

- ba** Display contents of *SB PAGE MAPPER* register that defines *SMP* SB base address for host-to-SB access.
- baIA@Z** Load *SB PAGE MAPPER* register with *SMP* SB base address that corresponds to *A* five digit hex SB address of 16-bit SB data word in *Z* SB area ('P' - for program area, 'D' - for data area, and 'I' - for I/O area).
- bdSA,EA@Z** Display 16-bit SB data. *SA* and *EA* parameters specify five digit hex SB starting and ending addresses for 16-bit SB data words correspondingly in *Z* SB area ('P' - for program area, 'D' - for data area, and 'I' - for I/O area). Final contents of *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *EA* address.
- bwA,XXXX@Z** Write 16-bit *XXXX* hex data word at *A* five digit hex SB address. *A* parameter defines SB address of 16-bit SB word in *Z* SB area ('P' - for program area, 'D' - for data area, and 'I' - for I/O area). *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *A* address. (refer to section 2.4)

HPI Access Control

- hc** Display and interpret contents of HPIC register of TMS320C54x DSP.
- hch0** Clear *HINT* bit of HPIC register (DSP-to-host interrupt request via HPI) of TMS320C54x DSP.
- hcd1** Set *DSPINT* bit of HPIC register (host-to-DSP interrupt request via HPI) of TMS320C54x DSP.
- hdSA,EA** Display HPI shared memory data of TMS320C54x DSP within the *SA...EA* hex HPI address range.
- hwA,XXXX** Write 16-bit *XXXX* hex data word at *A* hex HPI shared memory address of TMS320C54x DSP.

Setting I/O and Memory Base Addresses for Host ISA-bus Interface

- im** Display ISA-bus memory base for host ISA-bus memory interface of *TORNADO-54x* in accordance with table 2-3 (display and interpret contents of *ISA_MI_BADDR_FRG* flag register).
- imXXXXX** Set *XXXXX* hex ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-54x* in accordance with table 2-3 (load

ISA_MI_BADDR_FRG flag register). If *T54CC.EXE* utility is invoked with *-bd* or *-bw* command line options and option *-im* is not specified (or *ISA_MI_BADDR_FRG* flag register was not loaded previously), then the default *D8000H* ISA-bus memory base address will be used for host ISA-bus memory interface during host-to-SB access, and option *-im0* will be automatically executed on exit from *T54CC.EXE* utility in order to deactivate host ISA-bus memory interface afterthat.

- im0* Deactivates host ISA-bus memory interface of *TORNADO-54x*, i.e. removes it from ISA-bus memory address on exit from *T54CC.EXE* utility.
- ipXXX* Specifies *XXX* hex I/O base address for host ISA-bus I/O interface. If this option is omitted, then default factory setting in accordance with table 2-4 will be used.

Control for Emulation Controller (ECC) and Emulation DCM (UECMX)

- ep* Display current ISA-bus I/O base for *ECC* for *TORNADO-542L* in accordance with table 2-10 (display and interpret contents of *ISA_ECC_IO_BADDR_FRG* flag register).
- epXXX* Set *XXX* hex I/O base address for *ECC* for *TORNADO-542L* in accordance with table 2-10 and activate it, i.e. include *ECC* into ISA-bus I/O address space and connect it to scan-path interface of TMS320C542 DSP. For *TORNADO-548/549/5402/5410/5416* with *UECMX* installed, this option specified the I/O base address for *UECMX*. Once *T54CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB' MIRAGE-510D emulator is not allowed for *TORNADO-542L* unless *T54CC.EXE* utility will be invoked with *-ex* command line option.
- ei* Set default I/O base address for *ECC* for *TORNADO-542L* in accordance with table 2-10 and activate *ECC*, i.e. include *ECC* into ISA-bus I/O address space and connect it to scan-path interface of TMS320C542 DSP. In case *D_OPTIONS* DOS system variable for TI TMS320C54x C Source Debugger is set and its list includes *-pXXX* option, then *XXX* hex I/O address will be used as default I/O base address for *ECC* instead of that in accordance with table 2-10. For *TORNADO-548/549/5402/5410/5416* with *UECMX* installed, this option configures *UECMX* to connect to the on-board TMS320LC548/VC549 JTAG path. Once *T54CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB' MIRAGE-510D emulator is not allowed to *TORNADO-542L* and is ignored for *TORNADO-548/549/5402/5410/5416* unless *T54CC.EXE* utility will be invoked with *-ex* command line option.
- ep0* Deactivates *ECC* controller for *TORNADO-542L*, i.e. remove *ECC* from ISA-bus I/O address space and disconnect it from scan-path interface of TMS320C542 DSP. Once *T54CC.EXE* utility has been invoked with this

command line option, attachment of external TI XDS510 or MicroLAB[®] MIRAGE-510D emulator is allowed to *TORNADO-542L*.

-ex For *TORNADO-542L* this option is identical to '**-ep0**' command line option, i.e. it removes *ECC* from ISA-bus I/O address space and disconnects it from scan-path interface of on-board TMS320C542 DSP. For *TORNADO-548/549/5402/5410/5416* with *UECMX* installed this option configures *UECMX* to connect to external TMS320 DSP via optional MPSD or JTAG pod. Once *T54CC.EXE* utility has been invoked with this command line option, attachment of external TI XDS510 or MicroLAB[®] MIRAGE-510D emulator is allowed to *TORNADO-54x*.

-er Perform software reset of *ECC* or *UECMX*. Recommended on invocation and exit from TI TMS320C54x HLL Debugger or GoDSP TMS320C54x Code Composer IDE.

General System Control Options

-r Perform software reset of *TORNADO-54x* host ISA-bus interface. All registers of host ISA-bus interface are put into default states, the *ECC* chip of *TORNADO-542L* is reset, DSP is put into 'RESET' state, all error flags are reset, and all host interrupt enable masks are reset. Also, the <B 0xff80> program code is written into the reset vector location of DSP interrupt table (default address 0xff80@P-MEM after DSP reset), which guarantees that DSP will be put into known state after the DSP reset line will be released prior running the TI C54x HLL Debugger or GoDSP C54x Code Composer IDE via DSP JTAG interface.

Utility Options

-p Set page-by-page display mode. The "ESC" keypress terminates display output whereas any other keypress results in the next page display.

-? Display list of available options for *T54CC.EXE* utility program. Help list is also displayed when *T54CC.EXE* utility program is invoked without command line options.

T54CC.EXE utility processes command line options in accordance with the following priority list:

1. *CONTROL REGISTER* control options
2. *FLAG STATUS REGISTER* and *FLAG CONTROL REGISTER* control options
3. HPI control options
4. *ECC* control options
5. SB access control options.

T54CC.EXE utility returns DOS *exit code* in case it is invoked with *-im*, *-c*, *-cg*, *-cl*, *-cie*, *-cim*, *-fsr*, *-fr*, *-frs*, *-fe*, *-fb*, *-fh*, *-fhf*, *-fhe*, *-fhi*, *-fhie* and *-fhfh* command line options, which correspond to display of contents of registers, bits and flags of *TORNADO-54x* host ISA-bus interface. The exit code returned corresponds to current value or contents of last displayed bit, bit field, flag or register. Exit code is useful when *T54CC.EXE* utility is integrated into DOS batch (.BAT) file that provides conditional processing. Exit code of *T54CC.EXE*

utility program can be analyzed using succeeding '*IF ERRORLEVEL*' DOS batch file commands. The following example of DOS batch file performs conditional processing of *SB_ERROR* flag of *TORNADO-54x*:

```
...
T54CC -fed
IF ERRORLEVEL 1 T54CC -fe0
...
```

When multiple data display options for the *T54CC.EXE* utility are specified, then the returned exit code will correspond to the last processed data display command line option.

In case error is detected by *T54CC.EXE* utility, then the exit code '255' is returned. If *T54CC.EXE* utility is invoked without any data display command line options and no errors is detected, then the exit code '0' is returned.

4.2 Uploading TMS320C54x COFF-files via Host ISA-bus Memory Interface

Uploading of TI TMS320C54x COFF-files (output .OUT files from TI TMS320C54x C/Assembler compilers) into *TORNADO-54x* on-board SRAM/PIOX-16 areas and TMS320C54x DSP on-chip environment can be performed by means of *T54COFF.EXE* software utility, which is included with utility software for *TORNADO-54x*.

T54COFF.EXE software utility runs under DOS and Windows 3.x/95/98 and performs upload of TI TMS320C54x COFF-file into *TORNADO-54x* on-board DSP environment via host ISA-bus memory interface without utilization of emulation controller *ECC* or *UECMX* emulation control DCM. The following uploaded modes are supported:

- *standard mode*, i.e. when data is uploaded to on-board SRAM/PIOX-16 areas via host ISA-bus memory interface without affecting TMS320C54x DSP chip reset line and SB locking
- *reset mode*, i.e. when data is uploaded to on-board SRAM/PIOX-16 areas and TMS320C54x DSP on-chip environment via host ISA-bus memory interface while holding TMS320C54x DSP in 'RESET' state
- *global SB locking mode*, i.e. when data is uploaded to on-board SRAM/PIOX-16 areas via host ISA-bus memory interface using global SB locking
- *SB locking mode*, i.e. when data is uploaded to on-board SRAM/PIOX-16 areas via host ISA-bus memory interface using the SB locking.

All modes except for *reset mode* allow uploading of COFF-file into SRAM/PIOX-16 areas only. However, these modes do not effect reset signal for TMS320C54x DSP, and data can be uploaded in parallel with the TMS320C54x DSP running.

Reset mode allows uploading of COFF-file into both on-board SRAM/PIOX-16 areas and TMS320C54x DSP on-chip environment (including DSP on-chip memory and peripherals). This is performed by means of special run-time TMS320C54x loader, which is loaded into on-board SRAM and then removed automatically by *T54COFF.EXE* utility each time loader recognizes that COFF-file data section, which must be uploaded into the DSP on-chip resources.

Uploading of COFF-file into *TORNADO-54x* is performed by invoking *T54COFF.EXE* utility from DOS command line:

T54COFF *FILENAME[.OUT]* [-option1] [-option2] [-option3] ...

If file extension is missed for source *FILENAME* COFF-file, then .OUT extension is assumed. The following is list of command line options for *T54COFF.EXE* utility, which are grouped into several functional groups.

Upload Mode Control

- lr*

Set *RESET* mode for uploading of COFF-file. COFF-file is uploaded while holding TMS320C54x DSP in 'RESET' state by means of clearing *M_GO* bit of *CONTROL REGISTER*. This mode is used for uploading of source program/data modules and supports uploading into both on-board SRAM/PIOX-16 areas and TMS320C54x DSP on-chip memory and peripherals. TMS320C54x DSP can be placed into the 'RUN' state on exit from *T54COFF.EXE* utility using *-cr0* command line option. The *-lr* option is assumed as default if none of *-lg*, *-ll* and *-ln* options is specified.
- lg*

Set *GLOBAL SB LOCKING* mode for uploading of COFF-file. COFF-file is uploaded into on-board SRAM/PIOX-16 areas while holding SB locking by means of setting *SB_GLOCK* bit of *CONTROL REGISTER*. TMS320C54x DSP will not be able to access SRAM/PIOX-16 areas until uploading will be finished. TMS320C54x DSP on-chip resources cannot be loaded in this mode. This mode is normally used for uploading of shared data into on-board SRAM/PIOX-16 areas while TMS320C54x DSP is executing a program.
- ll*

Set *SB LOCKING* mode for uploading of COFF-file. COFF-file is uploaded into on-board SRAM/PIOX-16 areas while holding SB locking by means of setting *SB_LOCK* bit of *CONTROL REGISTER*. TMS320C54x DSP will not be able to access SRAM/PIOX-16 areas until uploading will be finished. TMS320C54x DSP on-chip resources cannot be loaded in this mode. This mode is normally used for uploading of shared data into on-board SRAM/PIOX-16 areas while TMS320C54x DSP is executing a program.
- ln*

Set *STANDARD* mode for uploading of COFF-file. COFF-file is uploaded without affecting 'RESET' state of TMS320C54x DSP and without SB locking. TMS320C54x DSP will be able to access on-board SRAM/PIOX-16 areas during uploading of COFF-file. The on-board TMS320C54x DSP on-chip resources cannot be loaded during this mode. This mode is normally used for uploading of run-time program or data into on-board SRAM/PIOX-16 areas while on-board TMS320C54x DSP chip is executing a program.
- xi*

Exclude uploading of TMS320C54x DSP on-chip memory and peripherals when using *RESET* mode for uploading. This option should be used together with *-lr* option only.
- ovly*

Assume that TMS320C54x DSP on-chip DARAM is mapped to program memory space. This option should be used together with *-lr* option only.

Restarting TMS320C542 DSP on Exit

-cr0 Restart TMS320C54x DSP on exit from *T54COFF.EXE* utility. This option corresponds to toggling *M_GO* bit from *CONTROL REGISTER*.

Viewing Directory of COFF-file

-d List directory (sections loading information) for COFF-file. COFF-file will be not loaded into *TORNADO-54x* environment and all other command line options specified will be ignored.

Setting Base Addresses of ISA-bus Memory and I/O Interfaces

-imXXXXX Set *XXXXX* hex ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-54x* in accordance with table 2-3 (load *ISA_MI_BADDR_FRG* flag register). If *T54CC.EXE* utility is invoked with *-bd* or *-bw* command line options and option *-im* is not specified (or *ISA_MI_BADDR_FRG* flag register was not loaded previously), then the default *D8000H* ISA-bus memory base address will be used for host ISA-bus memory interface during host-to-SB access, and option *-im0* will be automatically executed on exit from *T54CC.EXE* utility in order to deactivate host ISA-bus memory interface after that.

-im0 Deactivates host ISA-bus memory interface of *TORNADO-54x*, i.e. removes it from ISA-bus memory address on exit from *T54CC.EXE* utility.

-ipXXX Specifies *XXX* hex I/O base address for host ISA-bus I/O interface. If this option is omitted, then default factory setting in accordance with table 2-4 will be used.

Utility Options

-? Display list of available options for *T54COFF.EXE* utility. Help list is also displayed when *T54COFF.EXE* utility is invoked without command line options and parameters.

In case no errors are detected by *T54COFF.EXE* utility, then exit code '0' will be returned, otherwise exit code '1' will be generated.

CAUTION

If *T54COFF.EXE* utility is used with *-lr* command line option (or when *-lg*, *-ll* and *-ln* options are not specified) and if either emulation controller (*ECC*) or *UECMX* emulation control DCM is installed or any of TI XDS510 or MicroLAB' *MIRAGE-510D* emulator is attached, then the following error message may appear:

error: missing DSP handshaking

This error message states that the TMS320C54x DSP cannot be initialized correctly during uploading of TMS320C54x DSP on-chip memory or peripherals. This problem is caused by DSP on-chip execution controller that is locked by attached emulator or *ECC/UECMX*.

In order to avoid this problem you have to reset the *ECC/UECMX* or attached emulator. The emulator can be reset using the supplied software reset utility, whereas *ECC/UECMX* can be reset by invoking *T54CC.EXE* utility program with the *-er* command line option.

Appendix A. On-board Jumpers and Connectors.

This Appendix includes a summarized description for the *TORNADO-54x* on-board configuration jumpers, connectors, switches and sockets.

The layout for the *TORNADO-54x* on-board configuration jumpers, connectors, switches and sockets is presented at fig.A-1. Fig.A-1a contains information for the *TORNADO-542L* layout, whereas fig.A-1b contains information for the *TORNADO-548/549/5402/5410/5416* layout.

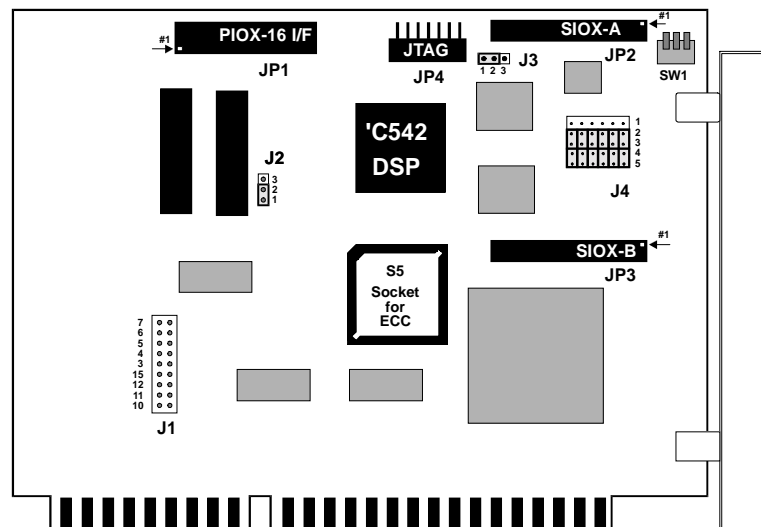


Fig.A-1a. On-board layout for *TORNADO-542L*.

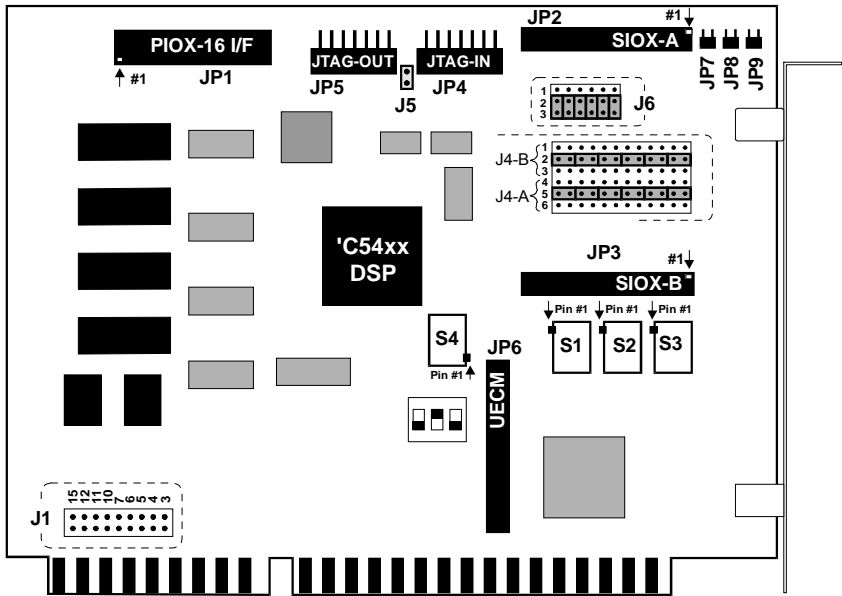


Fig.A-1b. On-board layout for *TORNADO-548/549/5402/5410/5416*.

On-board Configuration Switches

All on-board configuration switches for *TORNADO-54x* DSP systems are summarized in table A-1.

Table A-1. On-board configuration switches for *TORNADO-54x*.

switch ID	switch function description	reference information
SW1	ISA -bus I/O base address for host ISA-bus I/O interface.	Section 2.5, table 2-4.

On-board Configuration Jumpers

All on-board configuration jumpers for *TORNADO-54x* DSP systems are summarized in table A-2.

Table A-2. On-board configuration jumpers for *TORNADO-54x*.

jumper ID	jumper function description	reference information
<i>J1</i>	Host ISA-bus interrupt request line selector.	Sections 2.6 and 3.2.
<i>J2</i>	SRAM DIP-chips type selector (<i>TORNADO-542L</i> only).	Section 2.2
<i>J3</i>	<i>XIOF-0/TM</i> selector for SIOX and PIOX-16 interface sites (<i>TORNADO-542L</i> only).	Sections 2.6 and 2.7 , tables 2-11 and 2-12
<i>J4</i>	SIO-0/1 ports configurator for SIOX-B site (note: this jumper settings are different for <i>TORNADO-542L</i> and <i>TORNADO-548/549/5402/5410/5416</i>).	Section 2.7, fig.2-13.
<i>J5</i>	JTAG path terminator (<i>TORNADO-548/549/5402/5410/5416</i> only).	Section 2.8, fig.2-16..2-21.
<i>J6</i>	SIO-1 ports configurator for SIOX-A site (<i>TORNADO-548/549/5410/5416</i> only).	Section 2.7, fig.2-13.

On-board Connectors

All on-board connectors for *TORNADO-54x* DSP systems are summarized in table A-3.

Table A-3. On-board connectors and headers for *TORNADO-54x*.

connector ID	connector function description	reference information
<i>JP1</i>	PIOX-16 expansion interface site header.	Section 2.6, fig.2-7.
<i>JP2</i> <i>JP3</i>	SIOX-A/B expansion interface sites headers.	Section 2.7, fig.2-12.
<i>JP4</i> <i>JP5</i>	JTAG-IN and JTAG-OUT (<i>TORNADO-548/549/5402/5410/5416</i> only) connectors	Section 2.8, fig.2-16..2-21.
<i>JP6</i>	UECMX site header (<i>TORNADO-548/549/5402/5410/5416</i> only)	Sections 2.8 and 3.6.
<i>JP7</i>	Connector for external TTL clock for McBSP-0 serial port of TMS320VC5410 DSP (<i>TORNADO-5410L</i> only with TMS320VC5410 DSP in the BGA package).	Section 2.7, fig.2-14.

<i>JP8</i>	Connector for external TTL clock for McBSP-1 serial port of TMS320VC5410 DSP (<i>TORNADO-5410L</i> only with TMS320VC5410 DSP in the BGA package).	Section 2.7, fig.2-14.
<i>JP9</i>	Connector for external TTL clock for McBSP-2 serial port of TMS320VC5410 DSP (<i>TORNADO-5410L</i> only with TMS320VC5410 DSP in the BGA package).	Section 2.7, fig.2-14.

On-board Sockets

All on-board sockets for *TORNADO-54x* DSP systems are summarized in table A-4.

Table A-4. On-board sockets for *TORNADO-54x*.

socket ID	switch function description	reference information
<i>S1</i>	DIP-4 socket (0.3"x0.3" footprint) for TTL/CMOS 5v crystal oscillator (example: EPSON SG-531 clock oscillators) for external clock source of McBSP-0 serial port of TMS320VC5410 DSP (<i>TORNADO-5410L</i> only with TMS320VC5410GGW100 DSP in the BGA package).	Section 2.7, fig.2-14.
<i>S2</i>	DIP-4 socket (0.3"x0.3" footprint) for TTL/CMOS 5v crystal oscillator (example: EPSON SG-531 clock oscillators) for external clock source of BSP1/McBSP-1 serial port of TMS320C54x DSP (<i>TORNADO-5410L</i> only with TMS320VC5410GGW100 DSP in the BGA package).	Section 2.7, fig.2-14.
<i>S3</i>	DIP-4 socket (0.3"x0.3" footprint) for TTL/CMOS 5v crystal oscillator (example: EPSON SG-531 clock oscillators) for external clock source of TDM/McBSP-0 serial port of TMS320C54x DSP (<i>TORNADO-5410L</i> only with TMS320VC5410GGW100 DSP in the BGA package).	Section 2.7, fig.2-14.
<i>S4</i>	PLCC-44 socket for <i>ECC</i> (emulation controller chip) for local emulation of <i>TORNADO-542L</i> on-board TMS320C54x DSP (<i>TORNADO-542L</i> only).	Section 2.8; fig.2-23.

Appendix B. Glossary of Terms.

This Glossary contains definition for terms and other synchronism used along in this databook.

A

B

C

CLEAR_HPI_ERROR_FRG

Write-only flag register of host ISA-bus I/O interface, which clears the *HPI_ERROR* flag bit (HPI access timeout) in *SYS_STASTUS_FRG* flag register of host ISA-bus I/O interface. Refer to section 2.5 for more details.

CLEAR_MH_RQ_FRG

Write-only flag register of host ISA-bus I/O interface, which clears the *MH_RQ* flag bit (DSP-to-host interrupt request) in *SYS_STATUS_FRG* flag register of host ISA-bus I/O interface. Refer to sections 2.4 and 2.5 for more details.

CLEAR_SB_ERROR_FRG

Write-only flag register of host ISA-bus I/O interface, which clears the *SB_ERROR* flag bit in *SYS_STASTUS_FRG* flag register of host ISA-bus I/O interface. Refer to sections 2.4 and 2.5 for more details.

COFF

Common object file format files, which are output from the TI TMS320 DSP compiler tools. These files are loaded to the DSP environment either via JTAG emulator or via host ISA-bus interface using *T54COFF.EXE* software utility. Refer to section 4.2 for more details.

CONTROL REGISTER

Register of host ISA-bus I/O interface, which controls the DSP reset signal, SB access cycles format, SB locking mechanism and some interrupt enable masks. Refer to section 2.5 for more details.

D

DCM

Daughter-card module (SIOX, PIOX-16, UECMX), which can be installed onto *TORNADO-54x* DSP systems into the dedicated on-board sites.

DEV_ID0_FRG and DEV_ID1_FRG

Read-only flag registers of host ISA-bus I/O interface, which contains device ID for *TORNADO-54x* DSP system. Refer to section 2.5 for more details.

DSP_STATUS_FRG

Read-only flag register of host ISA-bus I/O interface, which comprises of flag bits of current DSP status. Refer to section 2.5 for more details.

E

ECC

Emulation Controller Chip (also known as TBC), which is used for emulation control of TMS320C542 DSP on *TORNADO-542L* DSP system via DSP on-chip JTAG port. Refer to section 2.8 and to TI documentation for more details.

F

FLAG DATA REGISTER

Register of host ISA-bus I/O interface, which contains read/write data for particular flag register, which is selected by the *FLAG SELECTOR REGISTER*. Refer to section 2.5 for more details.

FLAG SELECTOR REGISTER

Register of host ISA-bus I/O interface, which selects particular flag register for further read/write via *FLAG DATA REGISTER*. Refer to section 2.5 for more details.

G

H

HM_RQ

Host-to-DSP interrupt request, which is generated when host writes to the *SET_HM_RQ_FRG* flag register of host ISA-bus I/O interface. Refer to sections 2.3 and 2.5 for more details.

Host ISA-bus interface

TORNADO-6x on-board host ISA-bus interface, which comprises of host ISA-bus memory interface and host ISA-bus I/O interface. Refer to sections 2.4 and 2.5 for more details.

HPI

TMS320C54x DSP on-chip Host Port Interface, which is used for access to entire DSP environment from host PC. Refer to section 2.5 and to TI TMS320C54x documentation for more details.

HPI Access Timeout

Timeout condition when host ISA-bus I/O interface accesses TMS320C54x DSP on-chip Host Port Interface, which sets *HPI_ERROR* flag bit in *SYS_STATUS_FRG* flag registers. Refer to section 2.5 and to TI TMS320C54x documentation for more details.

HPI_IE_FRG

HPI-to-host interrupt enable register of host ISA-bus I/O interface. Refer to section 2.5 for more details.

HPI_HINT

DSP-to-Host interrupt request source via DSP on-chip HPI port. Refer to sections 2.3 and 2.5 for more details.

HPI Address Latch (HPIA)

16-bit DSP on-chip HPI Address Register, which is mapped to host ISA-bus I/O interface. Refer to section 2.5 and TI TMS320C54x DSP documentation for more details.

HPIC

16-bit DSP on-chip HPI Control Register, , which is mapped to host ISA-bus I/O interface. Refer to section 2.5 and TI TMS320C54x DSP documentation for more details.

HPID_AI

16-bit DSP on-chip HPI Data Register with address post-increment feature, , which is mapped to host ISA-bus I/O interface. Refer to section 2.5 and TI TMS320C54x DSP documentation for more details.

HPID

16-bit DSP on-chip HPI Data Register, , which is mapped to host ISA-bus I/O interface. Refer to section 2.5 and TI TMS320C54x DSP documentation for more details.

HPI_ERROR

Flag bit in *SYS_STASTUS_FRG* flag register of host ISA-bus I/O interface, which indicates that the timeout condition has been occurred for host-to-HPI access via host ISA-bus I/O interface. Refer to sections 2.4 and 2.5 for more details.

I

INT-0, INT-1, INT-2,

External hardware DSP interrupt request from SIOX and PIOX-16 daughter-card sites, which can generate active DSP interrupt request. Refer to sections 2.3, 2.6 and 2.7 for more details.

IOX Area

DSP mapped I/O registers. Refer to section 2.3 for more details.

IOX Controller

On-board hardware, which is mapped to the DSP environment and is used for generation of optional signal and control of the DSP environment. Refer to section 2.3 for more details.

ISA_ECC_BADDR_FRG

Flag register from host ISA-bus I/O interface, which defines I/O base address of the ECC for host ISA-bus I/O interface. Refer to sections 2.5 and 2.8 for more details.

ISA_MI_BADDR_FRG

Flag register from host ISA-bus I/O interface, which defines SMP ISA-bus memory base address within the UMB area of host PC environment. Refer to sections 2.4 and 2.5 for more details.

J

JTAG

Joint Test Action Group interface, which is a part of the TMS320C2xx/C4x/C5x/C54x/C6x/C8x DSP on-chip hardware and is used for debugging the DSP hardware/software using external JTAG emulators (TI XDS510 and MicroLAB' *MIRAGE-510DX*).

JTAG-IN, JTAG-OUT

On-board input and output connectors, which are used for connection to external JTAG emulator and to the next device/board in JTAG path correspondingly. Refer to section 2.8 for more details.

K

L

M

MH_RQ

DSP-to-Host interrupt request source, which is generated when DSP writes to the *MH_RQ* DSP IOX register. Refer to sections 2.3 and 2.5 for more details.

MicroPC

Industrial PC form-factor from Octagon Systems Inc.

MLock

DSP IOX register, which is used to lock SB by the DSP. Refer to section 2.3 for more details.

MPSD

Modular Port Scan Device interface, which is a TI propriety and is a part of the TMS320C3x DSP on-chip hardware and is used for debugging the DSP hardware/software using external MPSD emulators (TI XDS510 and MicroLAB' *MIRAGE-510DX*).

N**O****P*****PIOX-16***

16-bit Parallel I/O eXpansion interface site for compatible daughter-card modules (DCM). Refer to section 2.6 for more details.

PIOX_RUN

Bit of the DSP IOX register, which controls the reset signal for PIOX-16 interface site. Refer to section 2.3 for more details.

Pod

Electronic device, which connects PC plug-in JTAG/MPSD emulator board with JTAG/MPSD interface of target external TMS320 DSP.

PXSX_RUN

IOX register, which offers control over reset signals for SIOX and PIOX-16 daughter-card sites. Refer to section 2.3 for more details.

Q**R****S*****Shared Bus (SB)***

TORNADO-54x on-board data bus, which connects on-board SRAM and PIOX-16 resources with DSP and host ISA-bus memory interface bus masters. SB offers shared access to the on-board SRAM/PIOX-16 shared resources for the on-board TMS320C54x DSP and host ISA-bus memory interface. Host ISA-bus memory interface can provide access to SRAM/PIOX-16 both in random and block data transfer modes in parallel with DSP operation and almost without consuming the DSP time. Refer to section 2.2 for more details.

SB Access Timeout

Timeout condition for host-to-SB access via host ISA-bus memory interface, which generates active **SB_ERROR** flag bit in **SYS_STASTUS_FRG** flag register of host ISA-bus I/O interface. Refer to sections 2.2 and 2.4 for more details.

SB_ERROR

Flag bit in **SYS_STASTUS_FRG** flag register of host ISA-bus I/O interface, which indicates that the timeout condition has been occurred for host-to-SB access via host ISA-bus memory interface. Refer to sections 2.4 and 2.5 for more details.

SB_GLOCK

Bit of **CONTROL REGISTER** from host ISA-bus I/O interface, which allows immediate SB locking by host ISA-bus memory interface. Refer to sections 2.4 and 2.5 for more details.

SB Locking

SB acquisition feature, which offers monopoly access to SB for either DSP or host ISA-bus memory interface and prevents another SB master to access SB. Refer to sections 2.2 and 2.4 for more details.

SB_LOCK

Bit of **CONTROL REGISTER** from host ISA-bus I/O interface, which allows the deferred SB locking by host ISA-bus memory interface. Refer to sections 2.4 and 2.5 for more details.

SB PAGE MAPPER

SB base address register from host ISA-bus I/O interface, which defines base address for 32KB SMP page for further host-to-SB access from host ISA-bus memory interface. Refer to sections 2.4 and 2.5 for more details.

SET_HM_RQ_FRG

Write-only flag register of host ISA-bus I/O interface, which generates **HM_RQ** host-to-DSP interrupt request. Refer to sections 2.3 and 2.5 for more details.

SIOX

Serial I/O eXpansion interface sites for compatible daughter-card modules (DCM). Refer to section 2.7 for more details.

SIOX-A_RUN and SIOX-B_RUN

Bits of the DSP IOX register, which control the reset signal for SIOX-A and SIOX-B sites correspondingly. Refer to section 2.3 for more details.

SMP

Shared memory page mechanism, which is used for host-to-SB access from host ISA-bus memory interface. SMP size is set to 32KB for *TORNADO-54x* DSP systems. Refer to sections 2.2 and 2.4 for more details.

SMP ISA-bus Memory Base Address

Host ISA-bus memory base address for SMP of host ISA-bus memory interface, which is mapped to the UMB area of host PC environment using *ISA_MI_BADDR_FRG* flag register from *TORNADO-6x* host ISA-bus I/O interface. Refer to sections 2.4 and 2.5 for more details.

SRAM

Static RAM, which comprises of program and data memory areas. SRAM is a part of on-board DSP environment and can be also accessed from host ISA-bus memory interface. Refer to section 2.3 for more details.

SYS_STATUS_FRG

Read-only flag register of host ISA-bus I/O interface, which comprises of flag bits of most important *TORNADO-54x* control signal. Refer to section 2.5 for more details.

T

T54CC.EXE

TORNADO-54x Control center software utility. Refer to section 4.1 for more details.

T54COFF.EXE

TORNADO-54x COFF loader software utility. Refer to section 4.2 for more details.

U

UECMX

Universal Emulator Control daughter-card Module for *TORNADO* DSP Systems for ISA-bus and *MIRAGE-510DX* emulator.

UMB

Upper memory blocks area (below 1MB and higher than 640KB) of host PC memory.

V

W

X

XDMPR

DSP IOX register, which provides extended data memory addressing. Refer to section 2.3 for more details.

XIO-CNF

DSP IOX register, which configures the *XIO-0* pin and *XIO-1* I/O pins of SIOX/PIOX-16 interface sites. Refer to section 2.3 for more details.

XIOF-DATA

DSP IOX register, which defines current state of the *XIOF-0/1* I/O flags. Refer to section 2.3 for more details.

XIOF-DIR

DSP IOX register, which defines current I/O direction of the *XIOF-0/1* I/O flags. Refer to section 2.3 for more details.

Y

Z