DIGITAL SIGNAL PROCESSING

TORNADO-31x

Floating-Point DSP Systems with TMS320C31 DSP
and Universal TMS320 DSP Emulators
for ISA-bus PC and MicroPC Host Computers

User's Guide

covers:
TORNADO-31x rev.3.A
TORNADO-31Z rev.3.A
TORNADO-31M rev.1.B

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About this Document

This user's guide contains description for *TORNADO-31x* (*TORNADO-31* rev.3.A, *TORNADO-31Z* rev.3.A and *TORNADO-31M* rev.1.B) 32-bit floating-point digital signal processing (DSP) systems with TMS320C31 DSP and universal TMS320 emulators for ISA-bus PC and ISA-bus MicroPC host computers.

This document does not include detail description neither for TI TMS320C31 DSP nor for the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C3x User's Guide.*** Texas Instruments Inc, SPRU031D, USA, 1994.
2. ***TMS320C3x C Source Debugger User`s Guide.*** Texas Instruments Inc, SPRU053D, USA, 1994.
3. ***TMS320 Floating-Point DSP Optimizing C Compiler User`s Guide.*** Texas Instruments Inc, SPRU034B, USA, 1995.
4. ***TMS320 Floating-Point DSP Assembly Language Tools User`s Guide.*** Texas Instruments Inc, SPRU035B, USA, 1995.
5. ***MIRAGE-510DX/UECMX User`s Guide.*** MicroLAB Systems Ltd, 1999.

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Chapter 1. Introduction

This chapter contains general description for *TORNADO-31x* DSP systems product line, which comprises of *TORNADO-31*, *TORNADO-31Z* and *TORNADO-31M* DSP systems.

> **CAUTION**
>
> *TORNADO-31x* DSP systems are designed to accommodate high-performance 32-bit floating-point TMS320C3x DSP from Texas Instruments Inc.

> **CAUTION**
>
> *'TORNADO-31x'* notation denotes that the supplied information is applicable to all *TORNADO-31x* DSP systems (*TORNADO-31*, *TORNADO-31Z* and *TORNADO-31M* products).
>
> Should information be a product specific, then the name of the corresponding product (*TORNADO-31*, *TORNADO-31Z* or *TORNADO-31M*) will be highlighted.

1.1 General Information

TORNADO-31x are high performance floating-point DSP systems and universal TMS320 emulators for host ISA-bus PC and industrial MicroPC (from Octagon Systems Inc) computers.

TORNADO-31x product line comprises of *TORNADO-31*, *TORNADO-31Z* and *TORNADO-31M* DSP systems, which feature compatible modular system design, host ISA-bus interface and TMS320C31 DSP environment. The only differences are the on-board memory capacity, PIOX/SIOX expansion facilities and emulation facilities.

TORNADO-31/31Z are designed to plug into 16-bit ISA-bus slot of standard host PC, whereas *TORNADO-31M* is designed to plug into 8-bit ISA-bus slot of either conventional host PC or industrial MicroPC computer. All *TORNADO-31x* DSP systems feature flexible modular system architecture in order to meet requirements for multiple applications while keeping a cost of hardware to a minimum.

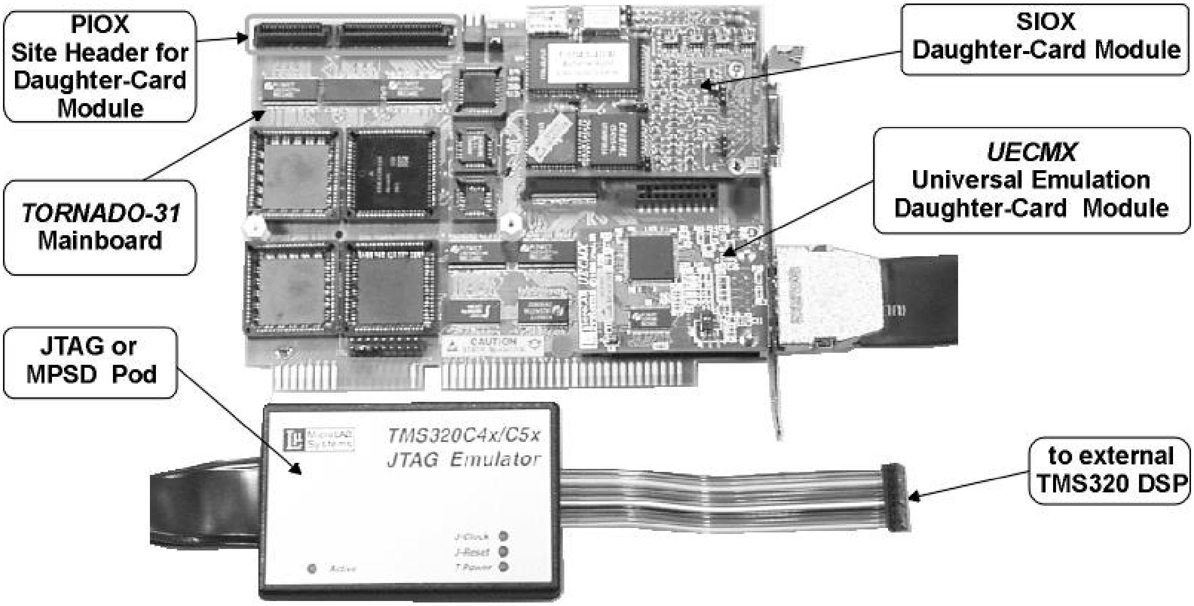


Fig.1-1a. *TORNADO-31* DSP system board with SIOX daughter-card module, *UECMX* universal emulation control daughter-card module and external JTAG pod.

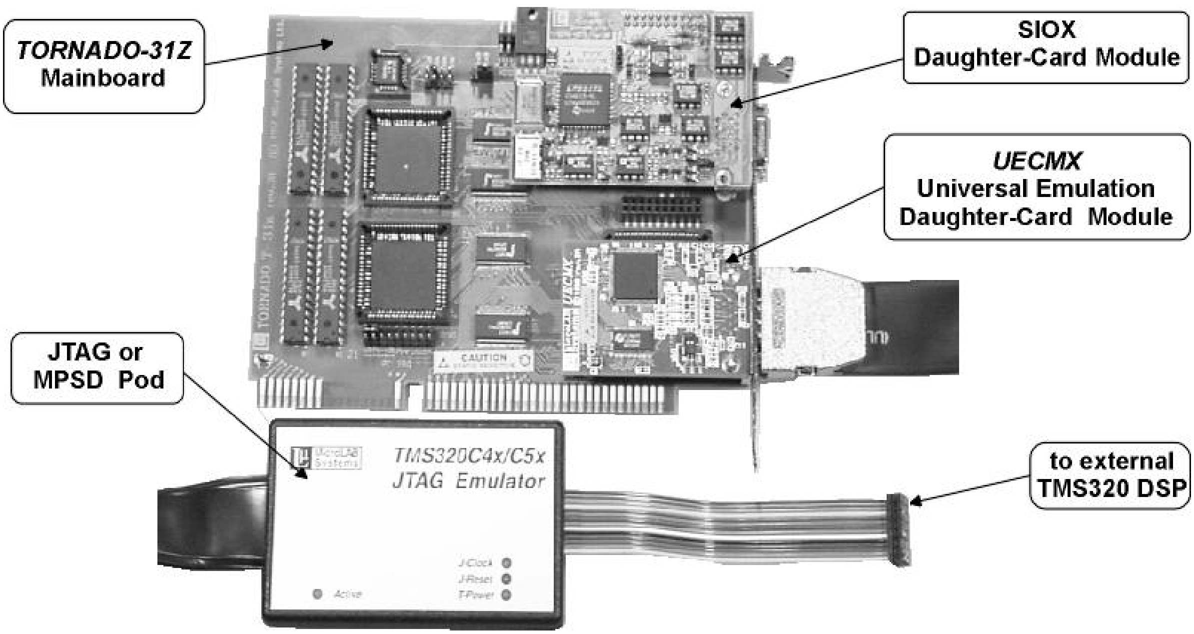


Fig.1-1b. *TORNADO-31Z* DSP system board with SIOX daughter-card module, *UECMX* universal emulation control daughter-card module and external JTAG pod.

Fig.1-1c. *TORNADO-31M* DSP system board with SIOX daughter-card module and *ECC* emulation controller.

The following are some of many application areas for *TORNADO-31x* DSP systems:

- *real-time DSP and signal acquisition*
- *fax/modem communication*
- *vocoders and speech signal processing*
- *audio and acoustics signal processing*
- *multimedia*
- *radars*
- *digital radio*
- *instrumentation and industrial*
- *medical and biomedical*
- *universal emulator for TI C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP (TORNADO-31/31Z only with UECMX daughter-card module and external MPSD/JTAG pod)*
- *TMS320C31 DSP evaluation and education*
- many more ...

TORNADO-31x utilize TMS320C31 32-bit floating- point DSP (60 MFLOPS or 30 MIPS) and feature up to 2Mx32 (*TORNADO-31*) and 1Mx32 (*TORNADO-31Z/31M*) on-board static RAM (SRAM) for program and data.

TORNADO-31x feature on-board shared bus (SB) architecture, which shares access to the on-board SRAM and PIOX resources between the on-board TMS320C31 DSP and host ISA-bus memory interface. Host ISA-bus memory interface provides access to SRAM and PIOX both in random and block data transfer modes in parallel with DSP operation and almost without consuming the DSP time.

TORNADO-31x feature optional facility for installation of serial I/O expansion (SIOX) daughter-card modules from a variety of AD/DA and digital I/O SIOX modules for real-time instrumentation, industrial and speech, telecommunication and audio signal processing applications.

TORNADO-31x feature optional facility for installation of parallel I/O expansion (PIOX/PIOX-16) daughter-card modules from a variety of AD/DA and digital I/O PIOX/PIOX-16 daughter-cards modules for high-speed real-time instrumentation, industrial and speech, telecommunication and audio signal processing applications.

TORNADO-31x use scan-path emulation control for the on-board TMS320C31 DSP in order to debug resident TMS320C31 DSP software. Scan-path emulation control of the on-board TMS320C31 DSP is available either via external TI XDS510 or MicroLAB' *MIRAGE-510DX* scan-path emulators, or by means of optional *emulation controller chip (ECC)* for *TORNADO-31M* or optional *emulation control daughter-card module (UECMX)* for *TORNADO-31/31Z*. *ECC* plugs into dedicated on-board socket of *TORNADO-31M,* whereas *UECMX* plugs into dedicated on-board daughter-card site of *TORNADO-31/31Z*. Both *ECC* and *UECMX* are low cost replacements for TI XDS510 and MicroLAB's *MIRAGE-510DX* scan-path emulators and run under identical industry standard TI C3x HLL Debugger and GoDSP C3x/C4x Code Composer IDE. Furthermore, *UECMX* allows optional connection to external MPSD and JTAG pods (which are the pods used with MicroLAB's *MIRAGE-510DX* scan-path emulator) in order to emulate any external TI C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP using either TI HLL Debuggers or GoDSP Code Composer IDE. This converts *TORNADO-31/31Z* into universal emulator for all TI TMS320 DSPs.

TORNADO-31x software development tools include TI Floating-point TMS320 DSP C compiler and Assembly language tools.

TORNADO-31x are supported by a variety of industry standard 3rd party DSP software tools, that include real-time operating systems (RTOS), DSP algorithm development and simulation tools, digital filter design tools, DSP/vector/math function libraries, vocoder/fax/modem function libraries, and many more...

TORNADO-31x provide unique burn-in device serial codes, that are available for host software and might be used for hardware copyright protection for software vendors and DSP system integrators.

1.2 Host PC Specifications

TORNADO-31x require that host ISA-bus IBM PC configuration should be at least 80386SX CPU and provides at least one 16-bit ISA-bus slot.

In order to learn configuration requirements for host PC running TMS320C31x DSP software development and debugging tools, refer to the corresponding documentation from TI and Go DSP Corp as well as to MicroLAB' "*MIRAGE-510DX/UECMX User's Guide*".

1.4 Technical Specification

The following are the technical specifications for the *TORNADO-31x* system specified for the temperature +25°C of the environment.

Parameter description	*parameter value*
power supply voltage	+5V for *TORNADO-31x* mainboard, ±5V/±12V for PIOX/SIOX daughter-card modules
power consumption (with 128Kx32 SRAM installed)	+5V@1.7A
DSP performance	60 MFLOPS or 30 MIPS
physical dimensions	168x118 mm (*TORNADO-31/31Z*) 125x114 mm (*TORNADO-31M*)
operating temperature	0..+60°C
I/O expansion sites for optional daughter-card modules	*SIOX (serial I/O expansion site)* : *TORNADO-31/31Z* (2), *TORNADO-31M* (1) *PIOX/PIOX-16 (parallel I/O expansion site)* : *TORNADO-31* (1).
host ISA-bus interface:	
number of I/O ports	8
size of ISA-bus memory page in the PC UMB memory address area for SB access via host ISA-bus memory interface	32Kx8
timeout control time for SB granting	4 us
timeout control time for SB data ready	4 us
host IRQ lines	*TORNADO-31/31Z*: IRQ 3, 4, 5, 6, 7, 10, 11, 12, 15 *TORNADO-31M*: IRQ 3, 4, 5, 6, 7
on-board SRAM:	
maximum SRAM capacity (using SRAM/PLCC chips)	*TORNADO-31*: 2Mx32 0ws *TORNADO-31Z/31M*: 1Mx32 0ws
SRAM/PLCC chips type	64K/128K/256K/512Kx32
maximum SRAM capacity (using SRAM/DIP chips)	128Kx32 0ws (*TORNADO-31Z* only)
SRAM/DIP chips type	8K/32K/64K/128Kx8 (*TORNADO-31Z* only)

number of SRAM/DIP chips installed into SRAM bank #0	4 (*TORNADO-31Z* only)
access time for SRAM/DIP chips	≤15 ns (*TORNADO-31Z* only)
SRAM/DIP chips package type	DIP-28/DIP-32 300MIL (*TORNADO-31Z* only)

Chapter 2. System Architecture and Construction

This chapter contains description for system architecture and construction, host ISA-bus interface, SIOX/PIOX I/O expansion sites and emulation facilities for *TORNADO-31x* DSP systems.

2.1 *TORNADO-31x* System Architecture

TORNADO-31x DSP systems are designed to plug into 16-bit ISA-bus slot (*TORNADO-31/31Z*) and into 8-bit ISA-bus slot (*TORNADO-31M*) of host PC. Architectures for all *TORNADO-31x* DSP systems is presented at fig.2-1.

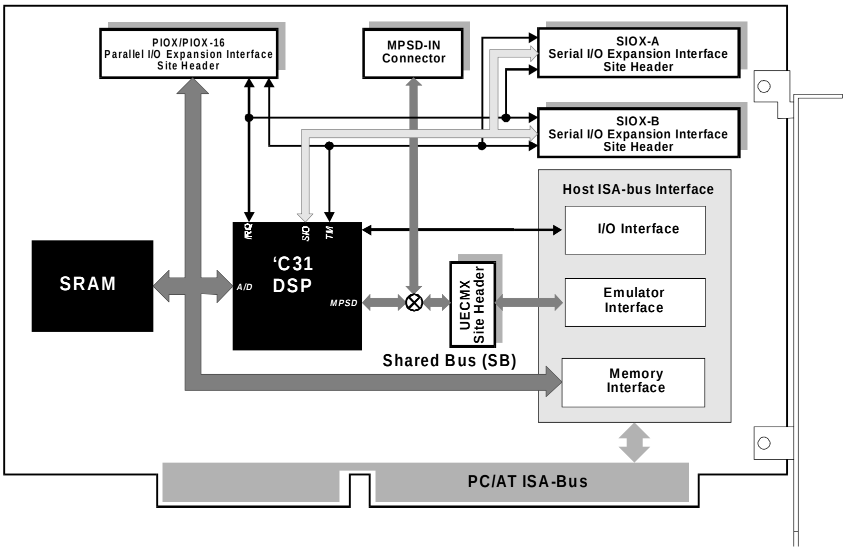


Fig.2-1a. Architecture of *TORNADO-31* mainboard.

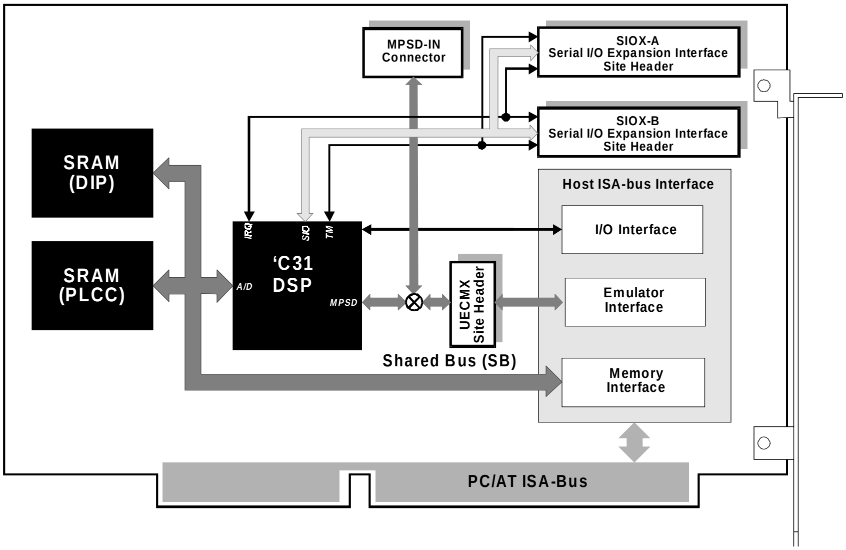


Fig.2-1b. Architecture of *TORNADO-31Z* mainboard.

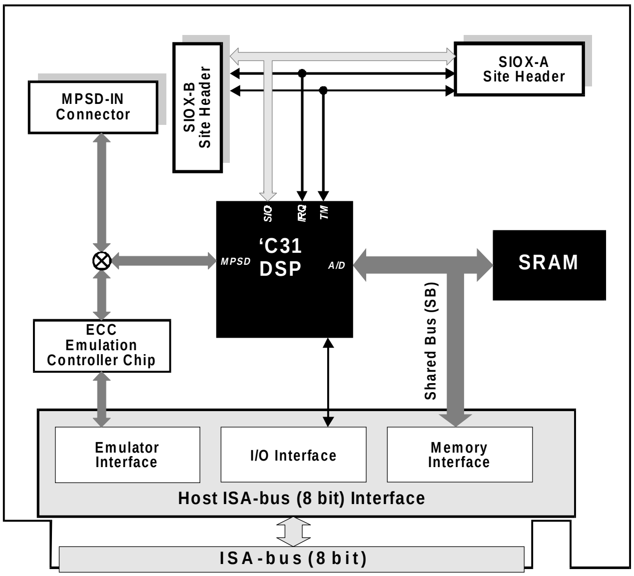


Fig.2-1c. Architecture of *TORNADO-31M* mainboard.

Main components of *TORNADO-31x* mainboards comprise of:

- *32-bit floating-point TMS320C31 DSP*
- *on-board static RAM (SRAM)* for program and data
- *serial I/O expansion interface (SIOX) sites*
- *32/16-bit parallel I/O expansion interface (PIOX) site (TORNADO-31 only)*
- *host ISA-bus memory and I/O interfaces*

- *emulation controller chip (ECC) on TORNADO-31M or site for universal emulation control daughter-card module (UECMX) on TORNADO-31/31Z.*

The on-board TMS320C31 DSP, SRAM, PIOX and host ISA-bus memory interface are linked together by means of on-board *Shared Bus (SB)*. SB shares SRAM/PIOX resources between two ‘bus masters’, which can execute SB access cycles: the on-board TMS320C31 DSP chip and host ISA-bus memory interface. SB arbitration assumes that TMS320C31 DSP bus master has the highest SB priority. Host ISA-bus memory interface can access SB in-parallel with DSP on-chip operation without any software overhead on DSP and host sides and almost without consuming the DSP time.

Construction of the *TORNADO-31x* mainboards is presented at fig.2-2.

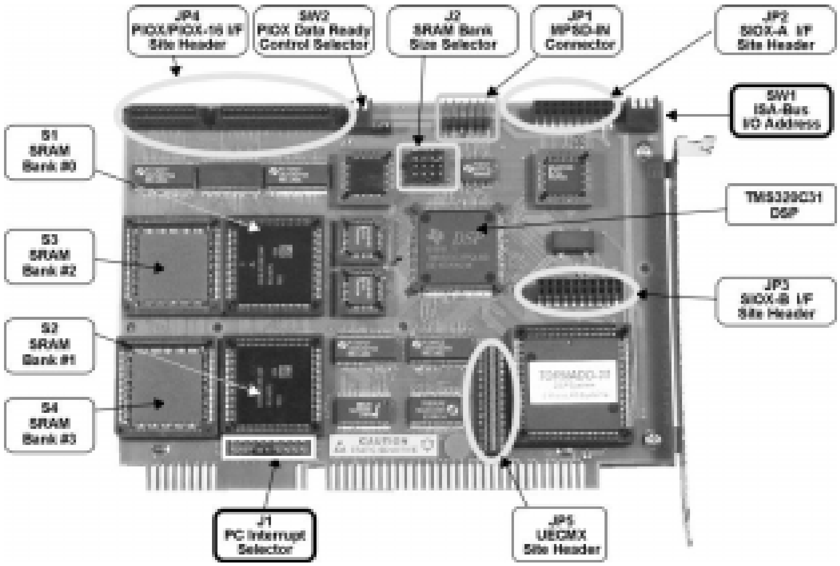


Fig.2-2a. Construction of *TORNADO-31* mainboard.

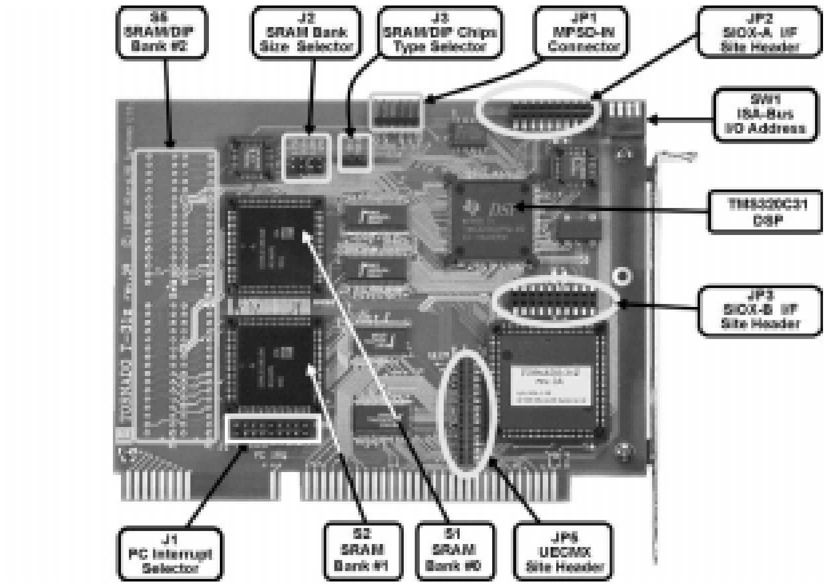


Fig.2-2b. Construction of *TORNADO-31Z* mainboard.

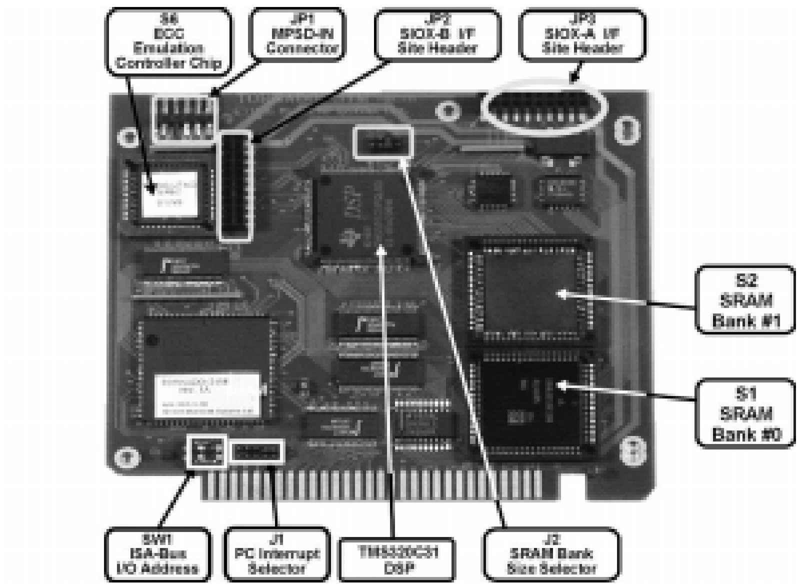


Fig.2-2c. Construction of *TORNADO-31M* mainboard.

On-board TMS320C31 DSP

The on-board TMS320C31 DSP is the 32-bit floating point DSP with on-chip Harvard architecture providing 60 MFLOPS and 30 MIPS of peak performance.

Static RAM (SRAM)

TORNADO-31x DSP systems provides on-board 0ws SRAM for DSP program and data and for communication between host ISA-bus and DSP environments. SRAM is the SB resource.

TORNADO-31 features up to 2Mx32 0ws of the on-board SRAM, which comprises of four SRAM banks (#0..#3). Each SRAM bank is designed to carry one plug-in SRAM/PLCC chip.

TORNADO-31Z features up to 1Mx32 0ws of the on-board SRAM, which comprises of two SRAM banks (#0..#1). Each SRAM bank is designed to carry one plug-in SRAM/PLCC chip, whereas SRAM bank #0 can also carry four SRAM/DIP chips in order to reduce memory cost.

TORNADO-31M features up to 1Mx32 0ws of the on-board SRAM, which comprises of two SRAM banks (#0..#1). Each SRAM bank is designed to carry one plug-in SRAM/PLCC chip.

Shared Bus (SB)

TORNADO-31x on-board SB delivers access to the on-board SRAM and PIOX shared resources for both on-board TMS320C31 DSP and host ISA-bus memory interface. The SB address space is 16Mx32 and comprises of SRAM memory area and PIOX I/O area. SB supports 8/16/32-bit data cycles with maximum throughoutput of 120 MB/sec. It is important to note, that all host accesses to the on-board SRAM and PIOX resources are performed concurrently with the DSP running and without any DSP software overhead.

Host ISA-bus Interface

TORNADO-31x host ISA-bus interface was designed for DSP/system control and high-speed data transfer between host ISA-bus and on-board SB (SRAM and PIOX subspaces). Host ISA-bus interface includes:

- *ISA-bus memory interface* that performs SB access invoked by the ISA-bus memory requests
- *ISA-bus I/O interface* that provides *TORNADO-31x* system control and configuring of the SB access modes for ISA-bus memory interface.

Host ISA-bus memory interface is designed to access SB resources via 32Kx8 *shared memory page* (*SMP*), which is mapped into ISA-bus UMB (Upper Memory Blocks) memory address space (above 640KB and below 1MB), which can be accessed both in PC x86 CPU real and protected operation modes. Once ISA-bus executes memory cycle within the address range of *SMP*, then the on-board *TORNADO-31x* ISA-bus memory interface generates request to SB access. Particular allocation of *SMP* onto SB address space is defines by *SB PAGE MAPPER* register from ISA-bus I/O interface. Host can access the SB data using any of 8/16/32-bit data cycles and features lowest SB access priority.

Base ISA-bus base memory addresses for host ISA-bus memory is setup by host software. ISA-bus memory interface can be switched off in case *TORNADO-31x* board is not used.

ISA-bus base I/O address for ISA-bus I/O interface is configured by the on-board SW1 DIP-switch into one of predefined ISA-bus I/O address areas.

Serial I/O Expansion Interface (SIOX)

TORNADO-31x on-board SIOX interface sites are used for installation of AD/DA/DIO daughter card modules and comprises of signals for TMS320C31 DSP on-chip serial port, timers and interrupt control.

SIOX compatible daughter-card modules include a variety of speech/fax/modem AD/DA, telecom interfaces, audio AD/DA, DAT interface, multichannel instrumentation AD/DA/DIO modules, and many more.

Parallel I/O Expansion Interface (PIOX)

TORNADO-31 feature PIOX/PIOX-16 interface site for installation of high-speed AD/DA/DIO daughter card modules. *TORNADO-31* PIOX/PIOX-16 interface is 4Mx32 shared SB resource and can be accessed both by on-board TMS320C31 DSP and host ISA-bus memory interface.

PIOX/PIOX-16 interface comprise of SB address/data/strobe signals and TMS320C31 DSP on-chip timers and interrupt control. PIOX-16 interface features 16-bit address/data with 16-bit access only, whereas PIOX provides 32-bit data and 22-bit address buses with 8/16/32-bit data access. PIOX/PIOX-16 site is designed to accommodate both 32-bit PIOX daughter-card modules, whereas PIOX-16 can accommodate only 16-bit PIOX-16 daughter-card modules.

PIOX/PIOX-16 compatible daughter-card modules include a variety of multichannel instrumentation AD/DA/DIO modules and many more. Moreover, PIOX daughter-card modules include DSP coprocessors for extending DSP performance of *TORNADO* DSP systems.

Debugging Resident TMS320C31 DSP Software

Resident TMS320C31 DSP software for *TORNADO-31x* DSP systems can be debugged using either TI XDS510 or MicroLAB' *MIRAGE-510DX* scan-path emulators. However, in order to minimize cost of debugging tools, the emulation controller chip (*ECC*) and emulation control daughter card module (*UECMX*) options are available. *ECC* is designed to plug into the dedicated on-board socket on *TORNADO-31M* mainboard, whereas *UECMX* is designed to plug into the dedicated site on *TORNADO-31/31Z* mainboards. Both *ECC* and *UECMX* are low cost replacement for XDS510 and *MIRAGE-510DX* emulators and run under the industry standard GoDSP C3x/C4x Code Composer IDE and TI C3x HLL Debuggers.

Debugging External TI TMS320 DSP Software with TORNADO-31/31Z and UECMX

TORNADO-31/31Z easily convert into universal scan-path emulators for any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP. This requires the *UECMX* daughter-card module installed onto *TORNADO-31/31Z* mainboard and optional external either MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x/C8x) pod attached to *UECMX* via the rear panel of PC chassis. The MPSD and JTAG pods are the same pods as used with MicroLAB' *MIRAGE-510DX* emulator. The *UECMX* runs under the industry standard TI HLL Debuggers and GoDSP Code Composer IDE.

2.2 Shared Bus

The *TORNADO-31x* on-board shared bus (SB) has 16Mx32 of data address space and supports 8/16/32-bit data cycles with the throughout performance of up to 120 MB/sec. SB is shared between the on-board TMS320C31 DSP chip and host ISA-bus memory interface masters and has SRAM and PIOX resources.

On-board SRAM

TORNADO-31x on-board SRAM might be used as external DSP program/data memory area and for DSP-to-PC communication via host ISA-bus memory interface.

TORNADO-31 features up to 2Mx32 0ws of the on-board SRAM, which comprises of four SRAM banks (#0..#3). Each SRAM bank is designed to carry any of the plug-in 64K/128K/256K/512Kx32 SRAM/PLCC chip. All SRAM banks should have identical SRAM/PLCC chips installed in order to exclude ‘memory holes’ in DSP address space. The particular SRAM/PLCC chip type is defined by the on-board jumper J2.

TORNADO-31Z features up to 1Mx32 0ws of the on-board SRAM, which comprises of two SRAM banks (#0..#1). Each SRAM bank is designed to carry any of the plug-in 64K/128K/256K/512Kx32 SRAM/PLCC chip, and SRAM bank #0 can also carry four byte-wide SRAM/DIP chips in order to reduce total memory cost.. Both SRAM banks should have identical SRAM/PLCC chips installed in order to exclude ‘memory holes’ in DSP address space. Compatible SRAM/DIP chips can be 8K/32K/64K/128Kx8 in 300MIL DIP-28 and DIP-32 packages. The particular type of SRAM/PLCC chips installed is defined by on-board jumper J2, whereas the type of .SRAM/DIP chips installed is defined by the on-board jumper J3.

TORNADO-31M features up to 1Mx32 0ws of the on-board SRAM, which comprises of two SRAM banks (#0..#1). Each SRAM bank is designed to carry any of the plug-in 64K/128K/256K/512Kx32 SRAM/PLCC chip. Both SRAM banks should have identical SRAM/PLCC chips installed in order to exclude ‘memory holes’ in DSP address space. The particular SRAM/PLCC chip type is defined by the on-board jumper J2.

SB Address Space

Valid SB address spaces for *TORNADO-31x* DSP systems are listed in table 2-1.

Table 2-1. SB address space and SB data ready wait states.

<table>
<tr><th rowspan="2">SB address subspace name</th><th rowspan="2">size</th><th colspan="2">address range
(wait time for SB_READY signal after SB is granted)</th></tr>
<tr><th>for on-board TMS320C31 DSP
(address in 32-bit words)</th><th>for host ISA-bus memory interface
(address in 8-bit words)</th></tr>
<tr><td>SB SRAM bank #0:
- jumper J2 is set to 64K
- jumper J2 is set to 128K
- jumper J2 is set to 256K
- jumper J2 is set to 512K</td><td>64Kx32
128Kx32
256Kx32
512Kx32</td><td>000000H...00FFFFH
000000H...01FFFFH
000000H...03FFFFH
000000H...07FFFFH
(0 ws)</td><td>00000000H..0003FFFFH
00000000H..0007FFFFH
00000000H..000FFFFFH
00000000H..001FFFFFH
(0 ws)</td></tr>
<tr><td>SB SRAM bank #1:
- jumper J2 is set to 64K
- jumper J2 is set to 128K
- jumper J2 is set to 256K
- jumper J2 is set to 512K</td><td>64Kx32
128Kx32
256Kx32
512Kx32</td><td>010000H...01FFFFH
020000H...03FFFFH
040000H...07FFFFH
080000H...0FFFFFH
(0 ws)</td><td>00040000H..0007FFFFH
00080000H..000FFFFFH
00100000H..001FFFFFH
00200000H..003FFFFFH
(0 ws)</td></tr>
<tr><td>SB SRAM bank #2:
- jumper J2 is set to 64K
- jumper J2 is set to 128K
- jumper J2 is set to 256K
- jumper J2 is set to 512K
(TORNADO-31)</td><td>64Kx32
128Kx32
256Kx32
512Kx32</td><td>020000H...02FFFFH
040000H...05FFFFH
080000H...0BFFFFH
100000H...17FFFFH
(0 ws)</td><td>00080000H..000BFFFFH
00100000H..0017FFFFH
00200000H..002FFFFFH
00400000H..005FFFFFH
(0 ws)</td></tr>
<tr><td>SB SRAM bank #3:
- jumper J2 is set to 64K
- jumper J2 is set to 128K
- jumper J2 is set to 256K
- jumper J2 is set to 512K
(TORNADO-31)</td><td>64Kx32
128Kx32
256Kx32
512Kx32</td><td>030000H...03FFFFH
060000H...07FFFFH
0C0000H...0FFFFFH
180000H...1FFFFFH
(0 ws)</td><td>000C0000H..000FFFFFH
00180000H..001FFFFFH
00300000H..003FFFFFH
00600000H..007FFFFFH
(0 ws)</td></tr>
<tr><td>reserved (do not use)</td><td>-</td><td>TORNADO-31:
200000H...7FFFFFH
80A000H…BFFFFFH
(∞ ws)

TORNADO-31Z/31M:
100000H...7FFFFFH
80A000H…FFFFFFH
(0 ws)</td><td>TORNADO-31:
00800000H...01FFFFFFH
(4 usec timeout)

TORNADO-31Z/31M:
00400000H...03FFFFFFH
(0ws)</td></tr>
<tr><td>SB PIOX-16 area
(TORNADO-31)</td><td>64Kx16
(only 16-bit LSW of 32-bit words is valid)</td><td>C00000H...C00FFFFH
(=f(PIOX_READY))</td><td>00300000H...0303FFFFH
(=f(PIOX_READY)
with 4 usec timeout)</td></tr>
<tr><td>SB PIOX area
(TORNADO-31)</td><td>4Mx32</td><td>C00000H...FFFFFFH
(=f(PIOX_READY))</td><td>00300000H...03FFFFFFH
(=f(PIOX_READY)
with 4 usec timeout)</td></tr>
</table>

The SB address space when accessed via host ISA-bus memory interface appears as a series of dual-access 32KB *shared memory pages* (*SMP*) that are mapped onto the predefined ISA-bus UMB (upper memory blocks) memory window by means of *SB PAGE MAPPER* register in host ISA-bus I/O interface. The SB can be accessed by host ISA-bus memory interface by means of random accesses to software variables or data arrays that are allocated within *SMP*, or by means of block data transfers between PC main memory and *SMP* using either host i80x286 CPU MOVSB/MOVSW/etc instructions or host DMA controller.

SB Data Ready Signal

SB has internal *SB_READY* signal that is generated by passive addressed device (SRAM or PIOX) in order to acknowledge that SB data are valid after SB is granted to the SB requestor. When SB is accessed by the on-board TMS320C31 DSP master, the *SB_READY* signal is logically connected to the *READY* pin of TMS320C31 DSP chip, whereas for accesses from host ISA-bus memory interface the *SB_READY* signal is automatically processed by the SB access controller of ISA-bus memory interface. Table 2-1 lists data wait times for corresponding SB data accesses.

CAUTION

Access to on-board SRAM for *TORNADO-31x* DSP systems
is performed without wait states.

Access to reserved SB areas for *TORNADO-31Z/31M* DSP systems
is performed without wait states.

CAUTION

Access to PIOX area for *TORNADO-31* results in connection of *SB_READY* signal to the *PIOX_READY* signal generated by installed on-board PIOX READY signal generator and installed PIOX daughter-card module.

> **CAUTION**
>
> Access to the reserved SB address space for *TORNADO-31* or to the PIOX/PIOX-16 area while PIOX/PIOX-16 daughter-card module not installed results in missing *SB_READY* signal.
>
> If such SB access is performed by host ISA-bus memory interface of *TORNADO-31*, then 4 usec timeout will be automatically applied by the on-board hardware.
>
> If such SB access is performed by of *TORNADO-31* on-board TMS320C31 DSP, then TMS320C31 DSP may enter into infinite wait state in case DSP on-chip PRIMARY BUS CONTROL REGISTER (@808064H) is set incorrectly.

SB Data Cycle Formats

SB supports 8-bit, 16-bit and 32-bit data access cycles. The on-board TMS320C31 DSP master can access SB data using 32-bit data cycles only, whereas host ISA-bus memory interface can be configured for any of 8/16/32-bit SB data cycles.

Although host ISA-bus is actually the 16-bit data bus (8-bit data bus for *TORNADO-31M*), host ISA-bus memory interface of *TORNADO-31x* is able to support 32-bit SB access cycles. Once host ISA-bus cycle is addressing the SB area, then LSB/LSW or MSB/MSW are temporary stored in on-board register transceivers depending upon the memory read or memory write cycle is being performed correspondingly (see section 2.4).

SB Arbitration

When SB is requested by any of the SB masters (TMS320C31 DSP or host ISA-bus memory interface), then some time is required to resolve the arbitration. This normally takes about 1..4 TMS320C31 DSP clock cycles.

In case TMS320C31 DSP is requesting SB while the latter is occupied by host ISA-bus memory interface, then DSP will wait until host ISA-bus memory interface will release SB. After SB is granted to DSP, it is holded by DSP in order to access the SB resources at maximum speed without arbitration delays between succeeding SB cycles.

In case host ISA-bus memory interface is requesting SB while the latter is being occupied by TMS320C31 DSP, then host ISA-bus memory interface has to wait until DSP will complete current SB access cycle and release SB.

When SB is requested by both DSP and host ISA-bus memory interface, then DSP has the highest SB access priority.

SB Locking

The SB arbiter supports program *SB locking* in order to lock access to SB for processing of shared software semaphores or shared PIOX resources by on-board TMS320C31 DSP and host ISA-bus interface SB masters.

The SB locking by the on-board TMS320C31 DSP bus master is performed automatically when it executes the *LDII/LDFI* instructions. The corresponding SB unlocking is provided by execution of the *STII/STFI/SIGI* instructions. For more details refer to section 2.4 later in this chapter.

> **CAUTION**
>
> Time interval between execution of *LDII/LDFI* and *STII/STFI* instructions by the on-board TMS320C31 DSP should not exceed 4 µsec.

The SB locking by host ISA-bus memory interface master is performed by means of setting *SB_GLOCK* or *SB_LOCK* bits of *CONTROL REGISTER* from host ISA-bus I/O interface. For more details refer to section 2.6 later in this chapter.

> **CAUTION**
>
> Continuous SB locking by host ISA-bus memory interface by means of setting *SB_GLOCK* and *SB_LOCK* bits can result in continuous pending of the on-board TMS320C31 DSP bus master and may lead to time distortions of real-time data processing.

2.3 TMS320C31 DSP Environment

TORNADO-31x on-board TMS320C31 DSP is 60 MFLOPS 32-bit floating point DSP from Texas Instruments Inc (TI). Refer to original TI technical documentation for details about TMS320C31 DSP.

TMS320C31 DSP Address Space

TMS320C31 DSP address space comprises of the address space for SB resources and DSP on-chip memory and peripherals (see table 2-2).

Table 2-2. Address space for TMS320C31 DSP of *TORNADO-31x*.

Address space of TMS320C31 DSP	**address range (in 32-bit words)**	**access wait states**
SB SRAM bank #0: - jumper J2 is set to 64K - jumper J2 is set to 128K - jumper J2 is set to 256K - jumper J2 is set to 512K	 000000H...00FFFFH 000000H...01FFFFH 000000H...03FFFFH 000000H...07FFFFH	0 ws
SB SRAM bank #1: - jumper J2 is set to 64K - jumper J2 is set to 128K - jumper J2 is set to 256K - jumper J2 is set to 512K	 010000H...01FFFFH 020000H...03FFFFH 040000H...07FFFFH 080000H...0FFFFFH	0 ws
SB SRAM bank #2: - jumper J2 is set to 64K - jumper J2 is set to 128K - jumper J2 is set to 256K - jumper J2 is set to 512K (*TORNADO-31*)	 020000H...02FFFFH 040000H...05FFFFH 080000H...0BFFFFH 100000H...17FFFFH	0 ws
SB SRAM bank #3: - jumper J2 is set to 64K - jumper J2 is set to 128K - jumper J2 is set to 256K - jumper J2 is set to 512K (*TORNADO-31*)	 030000H...03FFFFH 060000H...07FFFFH 0C0000H...0FFFFFH 180000H...1FFFFFH	0 ws
reserved (do not use)	*TORNADO-31*: 200000H...7FFFFFH *TORNADO-31Z/31M*: 100000H...7FFFFFH	*TORNADO-31*: *SB_READY* is missed *TORNADO-31Z/31M*: 0 ws
TMS320C31 on-chip memory and registers	800000H...809FFFH	0 ws
reserved (do not use)	*TORNADO-31*: 80A0000H...BFFFFFH *TORNADO-31Z/31M*: 80A0000H...FFFFFFH	*TORNADO-31*: *SB_READY* is missed *TORNADO-31Z/31M*: 0 ws
SB PIOX-16 area (*TORNADO-31*)	C00000H...C00FFFFH (only 16-bit LSW of 32-bit words is valid)	*=f(PIOX_READY)*
SB PIOX area (*TORNADO-31*)	C00000H...FFFFFFH	*=f(PIOX_READY)*

SRAM area

TORNADO-31x on-board SRAM might be used as external DSP program/data memory area and for DSP-to-PC communication via host ISA-bus memory interface. SRAM is the SB resource.

For details about *TORNADO-31x* on-board SRAM and compatible SRAM chips refer to the corresponding subsection of section 'Shared Bus' earlier in this chapter.

PIOX/PIOX-16 Interface Site Area on TORNADO-31

TORNADO-31 provides 16/32-bit parallel I/O expansion (PIOX/PIOX-16) interface site for compatible AD/DA/DIO daughter-card modules. PIOX/PIOX-16 area can be accessed both by the on-board TMS320C31 DSP and host ISA-bus memory interface. PIOX-16 features 16-bit address and data buses, whereas PIOX provides 32-bit data and 22-bit address buses. For details about PIOX/PIOX-16 interface refer to section 2.6 later in this chapter.

Configuring PRIMARY BUS CONTROL REGISTER of TMS320C31 DSP

In order to benefit of full performance of TMS320C31 DSP when it access external SRAM, and to provide correct processing of the on-board *SB_READY* signal, be sure to set the TMS320C31 on-chip *PRIMARY BUS CONTROL REGISTER* (@808064H) as the following:

- 00000800H in case on-board jumper J2 is set to 64K SRAM banks size
- 00000700H in case on-board jumper J2 is set to 128K SRAM banks size
- 00000600H in case on-board jumper J2 is set to 256K SRAM banks size
- 00000500H in case on-board jumper J2 is set to 512K SRAM banks size

CAUTION

When TMS320C31 DSP of *TORNADO-31* accesses either the reserved SB areas or PIOX/PIOX-16 SB area while PIOX/PIOX-16 daughter-card module is not installed (*PIOX_READY* signal is not generated), then *SB_READY* signal is not generated.

In these cases the TMS320C31 DSP of *TORNADO-31* will enter into infinite wait state if TMS320C31 on-chip *PRIMARY BUS CONTROL REGISTER* (@808064H) is set to 00000500H, 00000600H, 00000700H or 00000500H values. To avoid this situation it is recommended to set the SWW and WTCNT fields of TMS320C31 on-chip *PRIMARY BUS CONTROL REGISTER* to SWW=10 and WTCNT=111 values correspondingly.

> **CAUTION**
>
> When TMS320C31 DSP of *TORNADO-31Z/31M* accesses the reserved SB areas, then *SB_READY* signal is generated without wait states as it is done when accessing SRAM area.

SB Locking by the on-board TMS320C31 DSP

SB locking technique is used for processing of shared software semaphores between DSP and host PC software, which can be allocated in on-board SRAM or PIOX shared resources.

SB locking/unlocking by the on-board TMS320C31 DSP master is performed automatically when DSP chips executes *LDII/LDFI/STII/STFI/SIGI* instructions (*Interlocked Operations*). The *LDII/LDFI/STII/STFI/SIGI* instructions assume automatic utilization of TMS320C31 on-chip *XF0/XF1* hardware flags (pins) for handshaking between the SB requester and SB arbiter. The *XF0* flag is used to lock/unlock the SB whereas the *XF1* always reads as '0' and is used to acknowledge the lock/unlock event. For more details refer to original TI documentation.

> **CAUTION**
>
> The *XF0/XF1* flags/pins of *TORNADO-31x* on-board TMS320C31 DSP cannot be used as programmable I/O flags/pins by *TORNADO-31x* resident software.
>
> The *IOF* on-chip register of TMS320C31 DSP should be set to 00000006H value in order to provide correct processing of *XF0/XF1* flags when executing *LDII/LDFI/STII/STFI/SIGI* instructions for SB locking by TMS320C31 DSP master.

When *XF0* flag is set to logical '1' (this value is set as default on TMS320C31 DSP reset and after configuring the *IOF* DSP on-chip register), then there is no active SB locking from on-board TMS320C31 DSP, and both TMS320C31 DSP and host ISA-bus memory interface can access shared SB resources.

The *LDII/LDFI* instructions result in setting flag *XF0* to the *XF0*=0 state that corresponds to active SB locking by TMS320C31 DSP. When *XF0* flag is set to logical '0', then there is active SB locking from on-board TMS320C31 DSP, and SB access from host ISA-bus memory interface will be pending until SB will be unlocked by TMS320C31 DSP (*XF0* flag will be set to logical '1').

The *XF0*=0 state (SB is locked by DSP) is held by TMS320C31 DSP until TMS320C31 DSP will execute *STII/STFI/SIGI* instructions that reset flag *XF0* to the *XF0*=1 state. The SB lock-to-unlock time interval is not limited by *TORNADO-31x* hardware, however long duration of the SB lock event by DSP may cause timeout access faults for SB accesses by host ISA-bus memory interface.

The following is a software example that demonstrates processing of software shared semaphore using SB locking technique:

```
                ...
Wait_Sem_Free:  LDII   @Sem,R1          ; read semaphore using SB locking
```

```
        BZ    L1             ; check for semaphore is free (Sem=0)
        SIGI                 ; semaphore is not free, unlock SB
        B     Wait_Sem_Free  ; repeat semaphore wait cycle
L1:     LDI   1,R1           ; semaphore is free
        STII  R1,@Sem        ; set semaphore (Sem=1) and unlock SB
        ...                  ; perform some processing with the semaphore
        ...                  ; being set (Sem=1)
        LDII  @Sem,R1        ; reset semaphore (Sem=0) using SB locking
        LDI   0,R1
        STII  R1,@Sem        ; save semaphore and unlock SB
        ...
```

TORNADO-31x provides hardware timeout control for SB granting wait time for host ISA-bus memory access. This hardware timeout interval is setup to 4 µsec. In case timeout will occur due to SB locking by DSP, the *SB_ERROR* flag in *FLAG STATUS REGISTER* of host ISA-bus I/O interface will be set to the *SB_ERROR*=1 state. This will result in cancellation of all further SB requests from host ISA-bus memory interface until the *SB_ERROR* flag will be reset to the *SB_ERROR*=0 state by host PC software.

CAUTION

Time interval between execution of *LDII/LDFI* and *STII/STFI* instructions by the on-board TMS320C31 DSP should not exceed 4 µsec in order to avoid timeout on host-to-SB access..

Generating Request to Host PC

TORNADO-31x can generate attention request (interrupt request) from the on-board TMS320C31 DSP to host PC CPU in order to synchronize between program execution in host and on-board DSP environments. This request is called *MH_RQ* (master to host request).

The *MH_RQ* is generated when the on-board TMS320C31 DSP executes *IACK* (*interrupt acknowledge*) instruction. Execution of *IACK* instruction sets *MH_RQ* flag in *FLAG STATUS REGISTER* of host ISA-bus I/O interface into the *MH_RQ*=1 state. The address pointer, which should be specified with the *IACK* instruction is ignored.

The following is the TMS320C31 DSP software example, which generates request to the host PC:

```
...
LDI 0,AR5
IACK *AR5             ; generation of request to host PC
...
```

Setting *MH_RQ*=1 can also generate active interrupt request to host PC in case the *MH_RQ_IE* bit in *CONTROL REGISTER* of host ISA-bus I/O interface is set to the *MH_RQ_IE*=1 state. The *MH_RQ* flag state can be also polled by host PC software when reading *FLAG STATUS REGISTER* of host ISA-bus I/O interface. For more details about how to process *MH_RQ* flag via host ISA-bus I/O interface refer to section 2.5 later in this chapter.

Processing Request from Host PC

TORNADO-31x can generate attention request (interrupt request) from host PC to TMS320C31 DSP in order to synchronize between the program execution in host and on-board DSP environments. This request is called *HM_RQ* (host-to-master request).

The *HM_RQ* is generated when host PC sets *SET_HOST_TO_MASTER_REQUEST* flag in host ISA-bus I/O interface by means of setting *FLAG SELECTOR REGISTER* to the *SET_HOST_TO_MASTER_REQUEST* value and succeeding writing to *FLAG CONTROL REGISTER* of host ISA-bus I/O interface. This results in generation of *INT3* external hardware interrupt for the on-board TMS320C31 DSP. Application software for the TMS320C31 DSP should provide processing of *INT3* hardware interrupt request in accordance with application requirements. For more details about how to generate *HM_RQ* flag via host ISA-bus I/O interface refer to section 2.5 later in this chapter.

External Hardware Interrupts for TMS320C31 DSP

TORNADO-31x on-board TMS320C31 DSP supports four external hardware interrupt requests (*INT0...INT3*) with the *INT0* request having the highest priority. These requests correspond to the following events:

- *INT0...INT2* interrupt requests are generated by SIOX/PIOX daughter-card modules
- *INT3* is known as *HM_RQ* (host-to-master request from host PC to the TMS320C31 DSP) and should be processed as described in subsection "*Processing Request from Host PC*" earlier in this section.

> **CAUTION**
>
> *INT0...INT2* interrupt request inputs on *TORNADO-31x* DSP systems are negative edge triggered inputs and allow both static and single-shot *INT0...INT2* interrupt request signals generated by from SIOX/PIOX daughter-card modules. High-to-low transition on *INT0...INT2* interrupt request inputs will generate one active interrupt request for the on-board TMS320C31 DSP.

SIOX Interface Sites

TORNADO-31x provide two serial I/O expansion interface (SIOX) sites (SIOX-A and SIOX-B) for compatible AD/DA/DIO daughter-card modules.

TORNADO-31/31Z allow installation of either one standard SIOX daughter-cad module or of two SIOX-bus daughter-card modules. *TORNADO-31M* allows installation of only one SIOX or SIOX-bus daughter-card module in either horizontal (recommended for installation into regular PC chassis) or vertical orientation (recommended for installation into MicroPC chassis).

SIOX sites comprise of the TMS320C31 DSP-on-chip serial port control lines, DSP-on-chip timers TM-0/TM-1 input/output, *INT0..2* external interrupt requests and ±5v/±12v ISA-bus power supply lines. For details about SIOX sites refer to section 2.7 later in this chapter.

2.4 Host ISA-bus Memory Interface

Host ISA-bus memory interface is designed for high-speed data transfer between host PC environment and *TORNADO-31x* on-board SB resources (SRAM/PIOX) without any software overhead for both host PC and on-board TMS320C31 DSP.

Operation Description

The SB address space via host ISA-bus memory interface appears as a series of dual-access 32KB *shared memory pages* (*SMP*), which are mapped onto the ISA-bus UMB (upper memory blocks, above 640KB and below 1MB of ISA-bus memory address) memory window by means of *SB PAGE MAPPER* register from host ISA-bus I/O interface.

SB can be accessed by host ISA-bus memory interface by means of random accesses to software variables or data arrays allocated within current *SMP*, or by means of block data transfers between PC memory/HDD and current *SMP* by means of either host i80x86 CPU MOVSB/MOVSW/etc instructions or host DMA controller.

Host ISA-bus memory interface issues SB request and provides SB access using 8-/16/32-bit data cycles each time host PC performs ISA-bus memory read/write cycle within the ISA-bus *SMP* address range. Particular selection of the UMB area should be done by host software by programming the *ISA_MI_BADDR_FRG* flag register from host ISA-bus I/O interface.

SMP ISA-bus Memory Base Address

SMP ISA-bus memory base address can be set within the ISA-bus UMB (upper memory blocks) memory address range by programming *ISA_MI_BADDR_FRG* flag register from *TORNADO-31x* host ISA-bus I/O interface in accordance with predefined configuration settings in table 2-3. Only three least significant bits of *ISA_MI_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes.

ISA_MI_BADDR_FRG Flag Register (r/w)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	*0*	*0*	*0*	*0*	*MI_BA2*	*MI_BA1*	*MI_BA0*

Table 2-3. ISA-bus memory base address for *SMP*.

ISA-bus memory base address for *SMP*	**ISA-bus memory address range for *SMP***	**bit settings for *ISA_MI_BADDR_FRG* flag register**		
		bit#2 MI_BA2	***bit#1 MI_BA1***	***bit#0 MI_BA0***
SMP is switched OFF	-	0	0	0
B8000H	*B8000H ... BFFFFH*	0	0	1
C0000H	*C0000H ... C7FFFH*	0	1	0
C8000H	*C8000H ... CFFFFH*	0	1	1
D0000H	*D0000H ... D7FFFH*	1	0	0
D8000H	*D8000H ... DFFFFH*	1	0	1
E0000H	*E0000H ... E7FFFH*	1	1	0
E8000H	*E8000H ... EFFFFH*	1	1	1

Notes: 1. The highlighted configuration corresponds to PC power on default value.

TORNADO-31x, as well as other *TORNADO* DSP systems, offers control for *SMP* activity from host software, i.e. switching *SMP* to either 'ON' or 'OFF' state in ISA-bus memory address space.

CAUTION

SMP is activated and appears in ISA-bus memory address space after writing any non-zero value into *ISA_MI_BADDR_FRG* flag register in accordance with table 2-3.

SMP is deactivated and disappears from ISA-bus memory address space after writing the zero value o *ISA_MI_BADDR_FRG* flag register.

Software control over *SMP* activity in *TORNADO-31x* delivers optimal utilization of UMB area in host PC and allows multiple *TORNADO* DSP systems to share the same UMB area within one PC environment.

Addressing the SB data via Host ISA-bus Memory Interface

The host ISA-bus memory interface provides access to the following SB areas (see table 2-1):

- *SRAM* area
- *PIOX/PIOX-16* I/O area (for *TORNADO-31* only).

Particular selection of *SMP*, which has the size 32KB and which can be allocated within any SB area in accordance with table 2-1, is performed by 16-bit *SB PAGE MAPPER* register from host ISA-bus I/O interface. For details about the *SB PAGE MAPPER* register programming please refer to subsection "*SMP PAGE MAPPER REGISTER*" in section "Host ISA-bus I/O Interface" later in this chapter. The *SB PAGE MAPPER* register bit format is as the following:

SB PAGE MAPPER (LSB) (r/w)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
A20 (TORNADO-31) *0 (TORNADO-31Z/31M)*	*A19*	*A18*	*A17*	*A16*	*A15*	*A14*	*A13*

SB PAGE MAPPER (MSB) (r/w)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	*0*	*0*	*0*	*0*	*A23 (TORNADO-31)* *0 (TORNADO-31Z/31M)*	*A22 (TORNADO-31)* *0 (TORNADO-31Z/31M)*	*A21 (TORNADO-31)* *0 (TORNADO-31Z/31M)*

CAUTION

TORNADO-31x provides absolute addressing for SB data when SB is accessed by host ISA-bus memory interface (refer to table 2-1).

The following are few examples for setting the SB address and *SB PAGE MAPPER* register when accessing the SB data from host ISA-bus memory interface:

- *Example 1*: TMS320C31 DSP address is 0x000005 for accessing the location within the SRAM bank #0. The corresponding address for host ISA-bus memory interface will be 0x0014 with the *SMP* #0x0000, i.e. the *SB PAGE MAPPER* should be programmed to the 0x0000 hex value.
- *Example 2*: TMS320C31 DSP address is 0x080004 for accessing the location within the SRAM. The corresponding address for host ISA-bus memory interface will be 0x0010 with the *SMP* #0x0040, i.e. the *SB PAGE MAPPER* should be programmed to the 0x0040 hex value.
- *Example 3*: TMS320C31 DSP address is 0xC0400A for accessing the location within the PIOX/PIOX-16 area (*TORNADO-31* only). The corresponding address for host ISA-bus memory interface will be 0x0028 with the *SMP* #0x0602, i.e. the *SB PAGE MAPPER* should be programmed to the 0x0602 hex value.
- *Example 4*: TMS320C31 DSP address is 0x809800 for accessing DSP on-chip memory area. There is no way to access the DSP on-chip memory area from host ISA-bus memory interface.

Accessing SB Data from PC Host Software via ISA-bus Memory Interface

Once *TORNADO-31x* host ISA-bus memory interface provides direct mapping of 32KB *SMP* onto ISA-bus UMB window, then the following host-to-SB data transfer techniques are applicable:

- *random access to variables or data arrays* allocated anywhere within the *SMP* by host PC software
- *block data transfers using MOVS/MOVSB/MOVSW instructions* of host PC i80x86 CPU
- *block data transfers under control of host PC DMA controller* using memory-to-memory or memory-to-port transfer cycles.

Operation Description for ISA-bus Memory Interface

The SB access from host ISA-bus memory interface is performed under hardware control of the on-board programmable *SB Access Controller* from ISA-bus interface of *TORNADO-31x*. Timing diagram for SB read cycle invoked by ISA-bus memory interface is presented at fig.2-3. Understanding of *SB Access Controller* operation is recommended for those applications, which require perfect evaluation of possible time delays when accessing the SB data from ISA-bus memory interface.

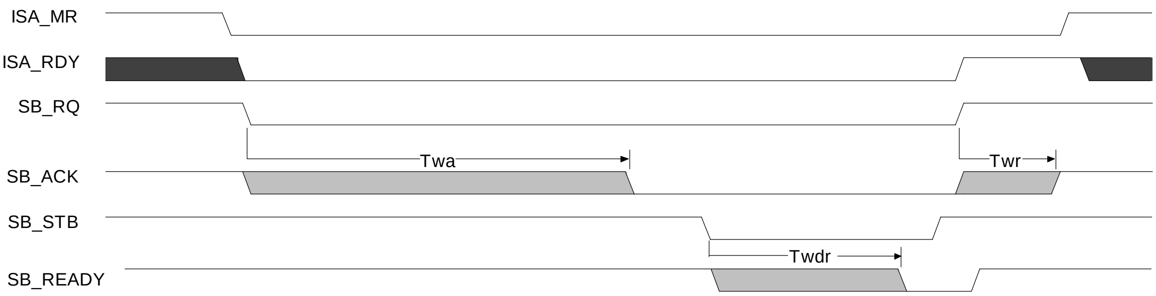


Fig.2-3. Timing diagram of SB read cycle invoked by ISA-bus memory interface.

CAUTION

Any host request from host ISA-bus memory interface to SB will make the upcoming TMS320C31 DSP request to SB (SRAM/PIOX) being pended upon completing of host request, and, therefore will introduce delays into real-time functionality of DSP software.

Host ISA-bus memory interface of *TORNADO-31x* DSP System is designed to minimize these delays to a minimum of available.

Host request to SB data will not introduce any time delays into operation of TMS320C31 DSP in case the latter is executing the program from on-chip cache or on-chip memory while accessing the DSP on-chip data memory.

Any request to the *SMP* memory address space on the host ISA-bus (*ISA_MR*=0 or *ISA_MW*=0) will result in activation of host ISA-bus memory interface, which will immediately generate request to SB arbiter

(*SB_RQ*=0) and set ISA-bus data ready signal to '*NOT READY*' state (*ISA_RDY*=0). Host ISA-bus interface will stay in this state until SB will be granted (*SB_ACK*=0) by SB arbiter to host ISA-bus memory interface. SB will be granted at least after T_{wa}=66ns time delay. After that, the SB access cycle will be generated by host ISA-bus memory interface with *SB_STB* signal set to the *SB_STB*=0 active state. Host ISA-bus memory interface will now wait for *SB_READY* signal comes true (*SB_READY*=0) in order to finish current SB access cycle. SB data ready signal *SB_READY* will come true (*SB_READY*=0) after T_{wdr} delay, which depends upon the SB area being addressed (see table 2-1). Minimum wait time for *SB_READY* data ready signal is T_{wdr}=0ns and corresponds to access to the on-board SRAM area, whereas access to PIOX area requires minimum wait-state condition with further awaiting for *PIOX_READY* signal set to true (refer to section 2.7 later in this chapter). After *SB_READY* signal sets true, the *SB_RQ* signal is removed (*SB_RQ*=1) and *ISA_RDY* signal is set to *ISA_RDY* =1 state in order to finish current ISA-bus memory access cycle. *SB_ACK* signal will return to its inactive state (*SB_ACK*=1) within T_{wr}=33ns after *SB_RQ* will be removed (*SB_RQ*=1).

SB Access Timeout Control

TORNADO-31x provides hardware timeout control for wait times for SB granting and *SB_READY* signal when SB is accessed by host ISA-bus memory interface. This is required in order to avoid infinite pending and crashing of host PC environment.

Hardware timeouts for both the SB granting and SB data ready signals are set to 4 usec. Once SB granting timeout occurs, the *SB_ERROR* bit in *CONTROL REGISTER* from host ISA-bus I/O interface will set to the *SB_ERROR*=1 state. This will cancel all succeeding SB requests from host ISA-bus memory interface until *SB_ERROR* bit will be reset by host software. However, there is no error bit set in case of the SB data ready timeout.

Data Formats for Host SB Data Access Cycles

TORNADO-31x supports 8/16/32-bit SB data cycles for SB access from host ISA-bus memory interface. Host ISA-bus memory interface offers special advanced features in order to minimize induced time delays into functionality of TMS320C31 DSP while the latter accesses the SB data.

Although PC can access *SMP* data using any of 8-bit or 16-bit ISA-bus memory cycles, the on-board hardware allows temporary storage of transferred data in order to reduce number of accesses to SB in case the accessed data format is either 16-bit or 32-bit data words.

The format of SB data cycle, when SB is accessed via host ISA-bus memory interface, can be by host software by means of programming the *SB_CCL* bit field {*SB_CCL-0*,*SB_CCL-1*} of *CONTROL REGISTER* from host ISA-bus I/O interface in accordance with table 2-4.

Table 2-4. Data formats for host SB data cycles..

Format of SB data cycle	***SB_CCL* bit field setting of *CONTROL REGISTER* from ISA-bus I/O interface**		**description**
	SB_CCL-0	***SB_CCL-1***	
8-bit data cycle (set as default on host PC reset)	0	0	Host SB request is generated for *TORNADO-31M* each time host PC CPU executes ISA-bus memory read/write cycle within *SMP* ISA-bus memory address range via 8-bit ISA-bus memory interface. This cycle is also generated when *TORNADO-31/31Z* executes 8-bt memory access within *SMP* via 16-bit ISA-bus memory interface. Actual byte selection within the addressed SB 32-bit word is performed by ISA-bus address bits {*A0, A1*}. *SMP* appears as the 32KB linear byte space.
16-bit data cycle	1	0	Host SB request is generated when host PC CPU performs either ISA-bus memory read cycle for even (*A0*=0) byte or ISA-bus memory write cycle for odd (*A0*=1) byte within the *SMP* ISA-bus memory address range. This cycle is also generated by *TORNADO-31/31Z* DSP systems in case host PC CPU performs ISA-bus memory read/write cycle for 16-bit words allocated at the even (*A0*=0) address boundary within *SMP*. When this data cycle format is set and host PC CPU performs 8-bit memory accesses to other bytes of 16-bit words, then no SB data cycle is generated and data is read/written from/to the on-board bidirectional register transceivers. Actual 16-bit word selection within the addressed SB 32-bit word is performed by ISA-bus address bit *A1*. *SMP* appears as a linear 16Kx16 space of 16-bit words.
32-bit data cycle	0 1	1 1	SB data cycle is generated only when host CPU performs ISA-bus memory read of the least significant byte (*A0*=*A1*=0) or memory write of the most significant byte (*A0*=*A1*=1) of the 32-bit memory words within *SMP* ISA-bus memory address range. When host CPU accesses other bytes of the *SMP* then no SB data cycle is generated and data is read/written from/to the on-board bidirectional register transceivers. SB data are transferred as 32-bit data words. *SMP* appears as a linear 8Kx32 space of 32-bit words.

Notes: 1. The highlighted configuration corresponds to PC power on default setting.

Data format for host SB data access cycle can be changed by host software during *TORNADO-31x* operation and depends upon user requirements for host and resident DSP software.

8-bit data cycles are the recommended selection when host software either assumes *SMP* to appear as a linear set of bytes (8-bit words), which are not grouped into 16-bit or 32-bit words, or when host software may require access to SB data as any of 8/16/32-but memory words. In this case the SB data cycle is generated each time when host PC CPU or DMA controller perform ISA-bus *SMP* memory access cycle. This mode is universal for accessing 8/16/32-bit memory data, however it delivers lower performance for accessing 16-bit or 32-bit memory words than it can be done using 16-bit or 32-bit data cycles.

16-bit data cycles are the recommended selection when host software assumes *SMP* to appear as a linear set of either 16-bit words, which are not grouped into 32-bit words. In this case the SB data cycle is generated when host PC CPU either reads even *SMP* memory bytes or writes to odd *SMP* memory bytes. The 16-bit host data cycle format normally saves about 50% time required for equivalent 8-bit SB access cycles when accessing 16/32-bit memory data words. This mode is universal for accessing 16/32-bit memory data, however it delivers lower performance for accessing 32-bit memory words than it can be done using 32-bit data cycles.

32-bit data cycles are the recommended selection when host software assumes *SMP* to appear as a linear set of 32-bit words. In this case the SB data cycle is generated when host PC CPU either reads least significant byte of 32-bit *SMP* memory words of writes to most significant byte of 32-bit *SMP* memory words. The 32-bit data cycle format normally saves about 75% time required for equivalent 8-bit SB access cycles when accessing 32-bit memory data words.

SB Locking by ISA-bus Memory Interface

SB locking by ISA-bus memory interface is useful for preventing SB access from TMS320C31 DSP while processing shared semaphores allocated in SRAM/PIOX shared SB resources.

SB locking by ISA-bus memory interface can be set by host PC software by means of programming either the *SB_GLOCK* bit or *SB_LOCK* bit of *CONTROL REGISTER* from ISA-bus I/O interface.

Timing diagrams of SB locking using *SB_GLOCK* and *SB_LOCK* bits are presented at fig. 2-4 and fig. 2-5.

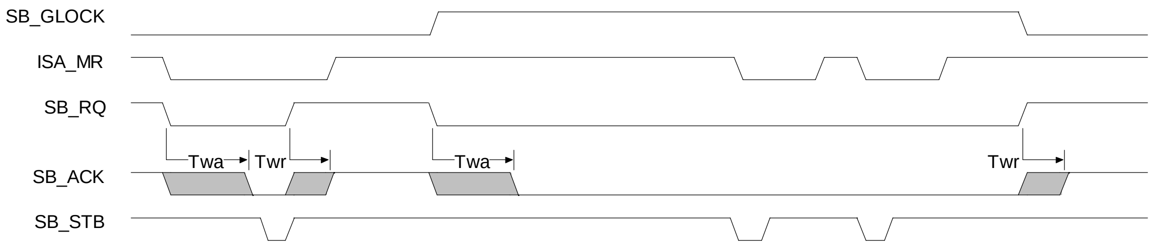


Fig.2-4. Timing diagram for SB access cycle invoked by ISA-bus memory interface with SB locking using *SB_GLOCK* bit.

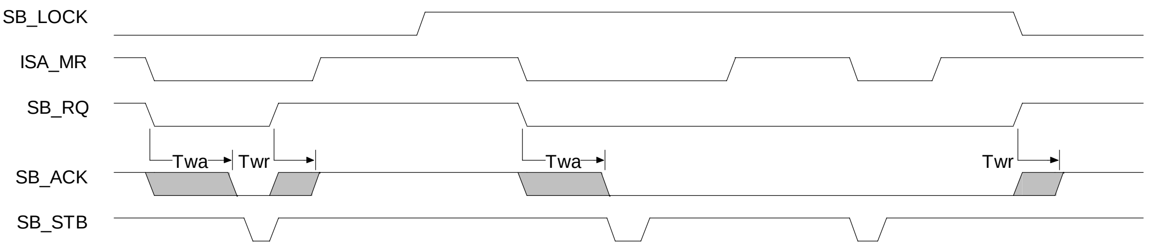


Fig.2-5. Timing diagram for SB access cycle invoked by ISA-bus memory interface with SB locking using *SB_LOCK* bit.

CAUTION

SB locking by ISA-bus memory interface using *SB_GLOCK* and *SB_LOCK* bits of *CONTROL REGISTER* from ISA-bus I/O interface should be used for short-time SB locking.

Continuous SB locking by ISA-bus memory interface using *SB_GLOCK* and *SB_LOCK* bits may result in continuous pending of TMS320C31 DSP (in case it accesses SB data) and may lead to significant time distortions of real-time data processing.

2.5 Host ISA-bus I/O Interface

TORNADO-31x host ISA-bus I/O interface is designed for *TORNADO-31x* system control, configuring of ISA-bus memory interface and interrupt handshaking between host PC and TMS320C31 DSP.

I/O Base Address of the Host ISA-bus I/O Interface

Host ISA-bus I/O interface occupies eight 8-bit registers inside ISA-bus I/O address space. Base address of host ISA-bus I/O interface is defined by means of on-board DIP-switch SW1 (see fig.2-2) in accordance with table 2-5.

Table 2-5a. ISA-bus I/O base address for host ISA-bus I/O interface for *TORNADO-31*.

ISA-bus I/O base address	ISA-bus I/O address range	button SW1-3	button SW1-2	button SW1-1
300H	*300H..307H*	OFF	OFF	OFF
310H	*310H..317H*	OFF	OFF	ON
320H	*320H..327H*	OFF	ON	OFF
330H	*330H..337H*	OFF	ON	ON
340H	*340H..347H*	ON	OFF	OFF
350H	*350H..357H*	ON	OFF	ON
360H	*360H..367H*	ON	ON	OFF
370H	*370H..377H*	ON	ON	ON

Notes: 1. Highlighted configuration corresponds to the factory setting.

Table 2-5b. ISA-bus I/O base address for host ISA-bus I/O interface for *TORNADO-31Z*.

ISA-bus I/O base address	**ISA-bus I/O address range**	**button SW1-3**	**button SW1-2**	**button SW1-1**
300H	*300H..307H*	OFF	OFF	OFF
310H	*310H..317H*	OFF	OFF	ON
320H	*320H..327H*	OFF	ON	OFF
330H	*330H..337H*	OFF	ON	ON
340H	*340H..347H*	ON	OFF	OFF
350H	*350H..357H*	ON	OFF	ON
360H	*360H..367H*	ON	ON	OFF
370H	*370H..377H*	ON	ON	ON
300H	*300H..307H*	OFF	OFF	OFF
310H	*310H..317H*	OFF	OFF	ON
320H	*320H..327H*	OFF	ON	OFF
330H	*330H..337H*	OFF	ON	ON
340H	*340H..347H*	ON	OFF	OFF
350H	*350H..357H*	ON	OFF	ON
360H	*360H..367H*	ON	ON	OFF
370H	*370H..377H*	ON	ON	ON

Notes: 1. Highlighted configuration corresponds to the factory setting.

Table 2-5c. ISA-bus I/O base address for host ISA-bus I/O interface for *TORNADO-31M*.

ISA-bus I/O base address	ISA-bus I/O address range	button SW1-2	button SW1-1
340H	*340H..347H*	OFF	OFF
350H	*350H..357H*	OFF	ON
360H	*360H..367H*	ON	OFF
370H	*370H..377H*	ON	ON

Notes: 1. Highlighted configuration corresponds to the factory setting.

ISA-bus I/O Interface Registers

List of *TORNADO-31x* ISA-bus I/O interface registers is presented in table 2-6.

Table 2-6. Register set of Host ISA-bus I/O interface.

Register #	register address	access mode	reset value	description
#0	*BA*+0	r/w	0	*SB PAGE MAPPER* (*LSB*)
#1	*BA*+1	r/w	0	*SB PAGE MAPPER* (*MSB*)
#2	*BA*+2	r/w	0	*CONTROL REGISTER*
#3	*BA*+3	r/w r w	r/w r w	*FLAG DATA REGISTER* *or* *FLAG STATUS REGISTER* *FLAG CONTROL REGISTER*
#403H	*BA*+0x403H	r/w	0	*FLAG SELECTOR REGISTER*
#4	*BA*+4			reserved (do not use)
#5	*BA*+5			reserved (do not use)
#6	*BA*+6			reserved (do not use)
#7	*BA*+7			reserved (do not use)

Notes: 1. '*BA*' denotes ISA-bus I/O base address of host ISA-bus I/O interface in accordance with table 2-5.
2. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

SB PAGE MAPPER Register

Registers #0 è #1 of *TORNADO-31x* ISA-bus I/O interface are least significant byte (LSB) and most significant byte (MSB) of 16-bit *SB PAGE MAPPER* register, which is used to set *SMP* SB base address within 16Mx32 SB area in the 8Kx32 (32Kx8 or 16Kx16) increments. Reset value for *SB PAGE MAPPER* register is 0x0000.

For *TORNADO-31* DSP system the *SB PAGE MAPPER LSB* register comprises of bits *A13..A20* of SB address whereas *SB PAGE MAPPER MSB* comprises of bits *A21..A23* of SB address. Bits D3..D7 of *SB PAGE MAPPER MSB* register are ignored on writing and read as zeros.

For *TORNADO-31/31Z* DSP systems the *SB PAGE MAPPER LSB* register comprises of bits *A13..A19* of SB address. Bit D7 of *SB PAGE MAPPER LSB* register and all bits of *SB PAGE MAPPER MSB* register are ignored on writing and read as zeros.

For all *TORNADO-31x* DSP systems the *A0..A12* bits of SB address for 32-bit SB words within *SMP* are derived from ISA-bus memory address bits *ISA_A2..ISA_A14*, whereas address bits *ISA_A0..ISA_A1* are used to select particular byte or 16-bit word within addressed 32-bit *SMP* SB word.

SB PAGE MAPPER (LSB) (r/w)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
A20 (TORNADO-31) *0 (TORNADO-31Z/31M)*	*A19*	*A18*	*A17*	*A16*	*A15*	*A14*	*A13*

SB PAGE MAPPER (MSB) (r/w)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	*0*	*0*	*0*	*0*	*A23 (TORNADO-31)* *0 (TORNADO-31Z/31M)*	*A22 (TORNADO-31)* *0 (TORNADO-31Z/31M)*	*A21 (TORNADO-31)* *0 (TORNADO-31Z/31M)*

CONTROL Register

Register #2 of *TORNADO-31x* ISA-bus I/O interface is known as *CONTROL REGISTER*. It is used for reset control of on-board TMS320C31 DSP, for configuration of ISA-bus memory interface and for DSP-to-host interrupt communication.

CONTROL REGISTER (r/w)

SB_ERROR_IE	*MH_RQ_IE*	*SB_CCL-1*	*SB_CCL-0*	*SB_LOCK*	*SB_GLOCK*	*0 (reserved)*	*M_GO*
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-7 contains detail description for bits and bit fields of *CONTROL REGISTER*. Note, that reserved bits of *CONTROL REGISTER* are ignored on writing and read as shown above.

Table 2-7. Bits and bit fields of *CONTROL REGISTER*.

bit or bit field of CONTROL REGISTER	***power on default value***	***description***
M_GO	0	*On-board TMS320C31 DSP reset line* control: • '0' corresponds to the RESET state of on-board TMS320C31 DSP • '1' corresponds to RUN (GO) state of on-board TMS320C31 DSP (i.e. the on-board DSP is in the program execution mode)
SB_GLOCK	0	*Shared Bus Global Lock*. With the *SB_GLOCK*=1 the SB access controller of ISA-bus memory interface generates immediate active SB locking.
SB_LOCK	0	*Shared Bus Lock*. With the *SB_LOCK*=1 the SB access controller of ISA-bus memory interface generates active SB locking starting from first next SB request cycle after the *SB_LOCK* bit is set to the *SB_LOCK*=1.
SB_CCL-0, SB_CCL-1	{0,0}	*Shared Bus Cycle format selector for Host-to-SB accesses* : • {0,0} corresponds to 8-bit host SB data transfer cycle • {0,1} corresponds to 16-bit host SB data transfer cycle • {1,0} correspond to 32-bit host SB data transfer cycle • {1,1} is reserved, do not use
MH_RQ_IE	0	*Master TMS320C31 DSP to Host Request Interrupt Enable*. If *MH_RQ_IE*=1 and *MH_RQ*=1, active interrupt request to host PC is generated. Host PC interrupt request is logical OR between (*MH_RQ_IE & MH_RQ*) and (*SB_ERROR_IE & SB_ERROR*) conditions.
SB_ERROR_IE	0	*SB Error Interrupt Enable*. If *SB_ERROR_IE*=1 and *SB_ERROR*=1, active interrupt request to host PC is generated. Host PC interrupt request is logical OR between (*MH_RQ_IE & MH_RQ*) and (*SB_ERROR_IE & SB_ERROR*) conditions.

FLAG Registers

Registers #3 and #403 of *TORNADO-31x* ISA-bus I/O interface are used for auxiliary control (*flags*) of *TORNADO-31x*.

Optional flags (data bits and control signals) are comprised into a set of multiplexed 8-bit *flag registers*. Particular *flag register* is addressed by *FLAG SELECTOR REGISTER* (register #403H). Flags within a currently addressed (selected) *flag register* can be read/written using I/O read/write operation into *FLAG DATA REGISTER* (register #3).

FLAG SELECTOR REGISTER defaults to the 00H reset value on PC power-on and has the following data format:

FLAG SELECTOR REGISTER (r/w)

FSEL-7	*FSEL-6*	*FSEL-5*	*FSEL-4*	*FSEL-3*	*FSEL-2*	*FSEL-1*	*FSEL-0*
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

List of available flag registers, which can be addressed by *FLAG SELECTOR REGISTER* in *TORNADO-31x*, is presented in table 2-8.

Table 2-8. Flag registers for *TORNADO-31x*.

code written to FLAG SELECTOR REGISTER	***name of addressed flag register (register #3)***	***description***
00H	r: *SYS_STATUS_FRG* w: *T31_1A_FLAG_CONTROL_RG*	Not recommended for usage in *TORNADO-31x*. This flag register Is provided for compatibility with *TORNADO-31* DSP system rev.1A/1B only. Use flag registers #10H/#20H/#30H instead in order to get the same results/ In read mode indicates current status of main run-time system flags of *TORNADO-31* (refer to subsection "*SYS_STATUS_FRG Flag Register*" later in this section). In write mode delivers compatibility with *FLAG CONTROL REGISTER* of *TORNADO-31* rev.1A/1B DSP system. The flag codes listed below in this table (10H/20H/30H) can be loaded directly to *FLAG CONTROL REGISTER* in order to generate output flag signals (refer to subsection "*Emulation of TORNADO-31 rev.1A/1B Flag Control Protocol*" later in this section). This procedure has limited functionality when *TORNADO-31* is installed into i80286 and i80386SX based host PC.
10H	r: *SYS_STATUS_FRG* w: *SET_HM_RQ_FRG*	In read mode indicates current status of main run-time system flags of *TORNADO-31x* (refer to subsection "*SYS_STATUS_FRG Flag Register*" later in this section). In write mode sets active *Host_to_Master_Request (HM_RQ)* via *INT3* external interrupt request input for TMS320C31 DSP. Data written to *SET_HM_RQ_FRG* register is ignored.

20H	r: *SYS_STATUS_FRG* w: *CLEAR_MH_RQ_FRG*	In read mode indicates current status of main run-time systems flags of *TORNADO-31x* (refer to subsection "*SYS_STATUS_FRG Flag Register*" later in this section). In write mode clears active *Master_to_Host_Request (MH_RQ)* flag in *SYS_STATUS_FRG* flag register. *Master_to_Host_Request* flag can be set by TMS320C31 DSP software in order to set attention or interrupt request to host PC. Data written to *CLEAR_MH_RQ_FRG* register is ignored. Host PC should perform this operation in the end of interrupt handler (in case *MH_RQ_IE*=1) after *MH_RQ* interrupt source has been identified.
30H	r: *SYS_STATUS_FRG* w: *CLEAR_SB_ERROR_FRG*	In read mode indicates current status of main run-time systems flags of *TORNADO-31x* (refer to subsection "*SYS_STATUS_FRG Flag Register*" later in this section). In write mode clears *SB_ERROR* flag in *SYS_STATUS_FRG* flag register. Active *SB_ERROR* flag is set by timeout controller during host-to-SB access when the timeout condition occurs for SB granting to host ISA-bus memory interface. Data written to *CLEAR_MH_RQ_FRG* register is ignored. Host PC should perform this operation in the end of interrupt handler (in case *SB_ERROR_IE*=1) after *SB_ERROR* interrupt source has been identified. Also, host PC should perform this operation in the end of data transmission between host ISA-bus and SB in case active *SB_ERROR* flag is detected.
E0H	r/w: *ISA_MI_BADDR_FRG*	*ISA-bus Memory interface Base Address Register*. Sets ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-31x* in accordance with table 2-3. Activates and deactivates host ISA-bus memory interface of *TORNADO-31x* within UMB area of ISA-bus memory address space. Only three least significant bits of this register are valid; all other bits are ignored and reads as zeros.
E2H	r/w: *ISA_ECC_BADDR_FRG* (*TORNADO-31M* only)	*ECC ISA-bus I/O Base Address Register*. Sets ISA-bus I/O base address for *TORNADO-31M* optional on-board emulation controller (*ECC*) in accordance with table 2-11. Activates and deactivates *ECC* within ISA-bus I/O address space. Only three least significant bits of this register are valid; all other bits are ignored and reads as zeros.
F0H *F1H*	r: *DEV_ID0_FRG* r: *DEV_ID1_FRG*	*Device Identifier and S/N Registers #0/#1*. These registers are read only and contain LSB and MSB of device ID and s/n ID for *TORNADO-31x* DSP systems.

Notes:
1. Unused codes for flag registers are reserved for future expansion.
2. Access modes: *r* - read only; *w* - write only; *r/w* - read and write.
3. Highlighted configuration corresponds to PC power on default setting.

Once a desired flag register is selected by loading the corresponding code into *FLAG SELECTOR REGISTER* in accordance with table 2-18, current flags status can be obtained by reading *FLAG DATA REGISTER* (*FLAG STATUS REGISTER*), whereas flag settings can be performed by writing to *FLAG DATA REGISTER* (*FLAG CONTROL REGISTER*). Note, that *FLAG STATUS REGISTER* and *FLAG CONTROL REGISTER* are actually read and write notations of *FLAG DATA REGISTER* that is available for both read and write operations. However, this makes useful sense since some of *TORNADO-31x* flag registers have different format for read and write operations.

SYS_STATUS_FRG Flag Register

SYS_STATUS_FRG flag register comprises of main *TORNADO-31x* run-time system flags settings. It is available as read only register and has the following data format:

FLAG STATUS REGISTER (read only)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
SB_ERROR	*MH_RQ*	*0*	*0*	*0*	*0*	*0*	*SB_ACK*

Detail description for bits of *FLAG STATUS REGISTER* is presented in table 2-9.

Table 2-9. Bits of *FLAG STATUS REGISTER* for *TORNADO-31x*.

bit name	***power on default value***	***description***
SB_ACK	0	*SB Request Acknowledge*. *SB_ACK*=1 denotes that SB arbiter has granted SB access to host ISA-bus memory interface. *SB_ACK* flag can be read during active SB locking from host ISA-bus memory interface.
MH_RQ	0	*Master_to_Host Request (MH_RQ)*. *MH_RQ*=1 denotes that TMS320C31 DSP has generated active request to host PC CPU. *MH_RQ* flag will stay active (*MH_RQ*=1) until it will be reset by host PC software by writing to *CLEAR_MH_RQ_FRG* flag register. If *MH_RQ_IE*=1 and *MH_RQ*=1, then active host PC CPU interrupt request is generated.
SB_ERROR	0	*SB Error (SB_ERROR)*. *SB_ERROR*=1 denotes that the 4 µsec timeout has been detected during SB access from host ISA-bus memory interface. *SB_ERROR* flag will stay active (*SB_ERROR*=1) until it will be reset by host PC software by writing to *CLEAR_SB_ERROR_FRG* flag register. If *SB_ERROR* flag is active (*SB_ERROR*=1), all succeeding host-to-SB requests from host ISA-bus memory interface of *TORNADO-31x* will be ignored and data returned will be undefined. If *SB_ERROR_IE*=1 and *SB_ERROR*=1, an active host PC CPU interrupt request is generated.

Emulation of TORNADO-31 rev.1A/1B Flag Control Facilities

Flag control facilities for *TORNADO-31* rev.1A/1B DSP systems included *FLAG CONTROL REGISTER* and *FLAG STATUS REGISTER* only. Register *FLAG SELECTOR REGISTER* did not exist. In order to generate an output flag signal, one should write a corresponding code directly to *FLAG CONTROL REGISTER*.

In order to gain compatibility with flag control protocol for *TORNADO-31x* rev.1A/1B DSP systems, *TORNADO-31* DSP systems rev.2A and later and all revisions of *TORNADO-31Z/31M* DSP systems include *T31_1A_FLAG_CONTROL_RG* flag pseudo-register, which is available for write only.

T31_1A_FLAG_CONTROL_RG flag pseudo-register is selected as default on host power on and when 00H code is written into *FLAG SELECTOR REGISTER*. After *T31_1A_FLAG_CONTROL_RG* pseudo-register has been selected, then succeeding writing of codes from table 2-10 into *FLAG DATA REGISTER* will generate output flag signals compatible to those for *TORNADO-31* rev.1A/1B DSP systems.

On reading from *T31_1A_FLAG_CONTROL_RG* flag pseudo-register the *SYS_STATUS_FRG* flag register data are read for compatibility with *TORNADO-31x* rev.1A/1B DSP systems.

CAUTION

T31_1A_FLAG_CONTROL_RG flag pseudo-register is not recommended for usage on *TORNADO-31* rev.2 and later and on all revisions of *TORNADO-31Z/31M* DSP systems since it has limited functionality when *TORNADO-31x* DSP system is used with host i80286 or i80386SX based PC.

Use *SET_HM_RQ_FRG*, *CLEAR_MH_RQ_FRG* and *CLEAR_SB_ERROR_FRG* flag registers instead to get the same result.

Table 2-10. Output flags generated on writing to *T31_1A_FLAG_CONTROL_RG* flag pseudo-register.

Code loaded into T31_1A_FLAG_CONTROL_RG	***description***
10H	*Set_Host_to_Master_Request (HM_RQ)*. Set active *Host_to_Master_Request* via *INT3* external interrupt request input for TMS320C31 DSP. (see description for *SET_HM_RQ_FRG* flag register in table 2-8 for details)
20H	*Clear_Master_to_Host_Request (MH_RQ)*. Clear active *Master_to_Host_Request (MH_RQ)* flag in *SYS_STATUS_FRG* flag register. (see description for *CLEAR_MH_RQ_FRG* flag register in table 2-8 for details)
30H	*Clear_Shared_Bus_Error (SB_ERROR)*. Clears active *SB_ERROR* flag in *SYS_STATUS_FRG* flag register. (see description for *CLEAR_SB_ERROR_FRG* flag register in table 2-8 for details)

Flag Registers for Identification of TORNADO-31x DSP Systems

TORNADO-31x DSP systems include *DEV_ID0_FRG/DEV_ID1_FRG* read-only flag registers (see table 2-8), which contain code for identification of *TORNADO-31x* DSP systems and its serial number.

Usage of *DEV_ID0_FRG/DEV_ID1_FRG* flag registers in host PC software is recommended for those applications that require to be protected from unauthorized duplication of software.

Generation of Request to TMS320C31 DSP

TORNADO-31x can generate request from host PC to TMS320C31 DSP in order to synchronize between programs execution in host and DSP environments. This is known as *HM_RQ* (host-to-master request), which results in generation of active *INT3* external interrupt request for the on-board TMS320C31 DSP.

In order to generate output *HM_RQ* flag, host PC software has to write to *SET_HM_RQ_FRG* flag register. Data written *SET_HM_RQ_FRG* flag register is ignored.

Processing of Request from TMS320C31 DSP

TORNADO-31x can generate request from TMS320C31 DSP to host CPU in order to synchronize between program execution in host and on-board DSP environments. This is known as *MH_RQ* (master-to-host request) and results in setting flag *MH_RQ* in *SYS_STATUS_FRG* flag register. Valid *MH_RQ* flag (*MH_RQ*=1) can generate active host PC interrupt request in case *MH_RQ_IE* bit of *CONTROL REGISTER* is set to the *MH_RQ_IE*=1 state.

MH_RQ will remain active (*MH_RQ*=1) until it will be recognized and reset by host software. In order to reset the *MH_RQ* flag, host PC software has to write to *Clear_Master_to_Host_Request_FRG* flag register. Data written *Clear_Master_to_Host_Request_FRG* flag register is ignored.

For details how to generate *MH_RQ* flag from TMS320C31 DSP environment, refer to section 2.3 earlier in this chapter.

Host Interrupts

Host ISA-bus I/O interface can generate active interrupts to host PC in the following cases:

- when *SB_ERROR* flag is active (*SB_ERROR*=1) in *SYS_STATUS_FRG* flag register and *SB_ERROR_IE* bit in *CONTROL REGISTER* is set to *SB_ERROR_IE*=1 state
- when *MH_RQ* is active (*MH_RQ*=1) in *SYS_STATUS_FRG* flag register and *MH_RQ_IE* bit in *CONTROL REGISTER* is set to *MH_RQ_IE*=1 state.

Host ISA-bus interrupt request is generated as logical 'OR' of the above events. Decoding of interrupt source should be performed by host PC software by means of analyzing the contents of *SYS_STATUS_FRG* flag register.

Host PC interrupt request may be generated using one of nine available ISA-bus interrupt request lines. Particular PC interrupt line is selected by the on-board interrupt configuration jumper J1 (see fig.2-2).

For *TORNADO-31/31Z* DSP systems the following ISA-bus interrupt request lines are available: IRQ-3, IRQ-4, IRQ-5, IRQ-6, IRQ-7, IRQ-10, IRQ-11, IRQ-12 and IRQ-15.

For *TORNADO-31M* DSP system the following ISA-bus interrupt request lines are available: IRQ-3, IRQ-4, IRQ-5, IRQ-6, and IRQ-7.

Setting ISA-bus Memory Base Address for Host ISA-bus Memory Interface

TORNADO-31x features software activated/deactivated host ISA-bus memory interface. Setting of ISA-bus memory base address for host ISA-bus memory interface and its activation/deactivation is performed via *ISA_MI_BADDR_FRG* flag register. Only three least significant bits of *ISA_MI_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes. Available settings for *ISA_MI_BADDR_FRG* flag register are presented in table 2-3.

ISA_MI_BADDR_FRG Flag Register (r/w)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	*0*	*0*	*0*	*0*	*MI_BA2*	*MI_BA1*	*MI_BA0*

Setting ISA-bus I/O Base Address for ECC in TORNADO-31M

TORNADO-31M DSP systems features software activated/deactivated on-board emulation facility, which is known as *ECC* emulation controller chip. Setting of ISA-bus I/O base address for on-board *ECC* is performed via *ISA_ECC_BADDR_FRG* flag register. Only three least significant bits of *ISA_ECC_BADDR_FRG* flag register are valid, and all other bits are ignored on writes and reads as zeroes. Available settings for *ISA_ECC_BADDR_FRG* flag register are presented in table 2-11.

ISA_ECC_BADDR_FRG Flag Register (r/w)

bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	*0*	*0*	*0*	*0*	*ECC_BA2*	*ECC_BA1*	*ECC_BA0*

Table 2-11. ISA-bus I/O base address for on-board emulation controller (*ECC*) of *TORNADO-31M*.

ISA-bus I/O base address for *ECC*	**ISA-bus I/O address range for *ECC***	**bit setting for *ISA_ECC_BADDR_FRG* flag register**		
		bit#2 ECC_BA2	***bit#1 ECC_BA1***	***bit#0 ECC_BA0***
ECC is disconnected from host ISA-bus; attachment of external TI XDS510 or MicroLAB' MIRAGE-510DX emulator is allowed	-	0	x	x
[2)]*240H*	*240H ... 25FH*	1	0	0
280H	*280H ... 29FH*	1	0	1
320H	*320H ... 33FH*	1	1	0
340H	*340H ... 35FH*	1	1	1

Note: 1. Highlighted configuration corresponds to host power on default setting.
2. This configuration is used as default by *T3CC.EXE* software utility.

CAUTION

Attachment of external TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator to *TORNADO-31M* is allowed only in case the on-board emulation controller (*ECC*) is either not installed or is programmed as 'disconnected' from ISA-bus (see table 2-11).

Attachment of external TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator to *TORNADO-31M* while the on-board emulation controller (*ECC*) is active is strongly prohibited and may result in damaging emulator and/or *ECC*.

2.6 Parallel I/O Expansion Interface (PIOX and PIOX-16) site of *TORNADO-31*

TORNADO-31 provides expansion of the on-board I/O facilities via parallel I/O expansion interface (PIOX/PIOX-16) site. PIOX/PIOX-16 is designed to carry compatible daughter-card module above *TORNADO-31* mainboard (see fig.1-1).

Typically, PIOX-16 daughter-card modules comprises of AD/DA and telecom daughter-card modules, whereas PIOX daughter-card modules are DSP coprocessor modules.

PIOX-16 daughter-card modules are compatible with all *TORNADO* DSP systems and all *TORNADO-E/EL* embedded DSP controllers, whereas PIOX daughter-card module are compatible with 32-bit *TORNADO* DSP systems only.

Description

PIOX/PIOX-16 interfaces appear as either 4Mx32 (PIOX) or 64Kx16 (PIOX-16) I/O address sub-space of *TORNADO-31* on-board SB, and can be accessed by both the on-board TMS320C31 DSP and host ISA-bus memory interface. PIOX/PIOX-16 include SB data/address buses, SB control signals, TMS320C31 DSP on-chip timers I/O pins and external interrupt inputs, DSP reset signal, and ISA-bus power supply lines.

PIOX-16 features 16-bit data and address buses with 16-bit data transfer cycles only, whereas PIOX is 32-bit extension of PIOX-16 and features 32-bit data and 22-bit address buses and 8/16/32-bit data transfer cycles.

PIOX-16 appears as 64Kx16 address space of *TORNADO-31* on-board SB, whereas PIOX appears as 4Mx32 address space of SB. Both PIOX and PIOX-16 interfaces provides generation of data ready signal using dedicated *PIOX_READY* line and hardware minimum wait state generator.

Installation of PIOX/PIOX-16 Daughter-card Modules onto TORNADO-31 Mainboard

Figure 2-6 shows installation of PIOX and PIOX-16 daughter-card modules onto *TORNADO-31* mainboard.

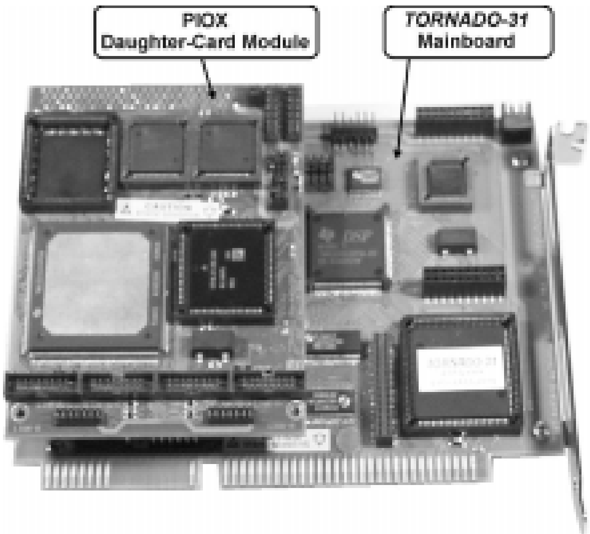


Fig.2-6a. Installation of PIOX daughter-card module onto *TORNADO-31* mainboard.

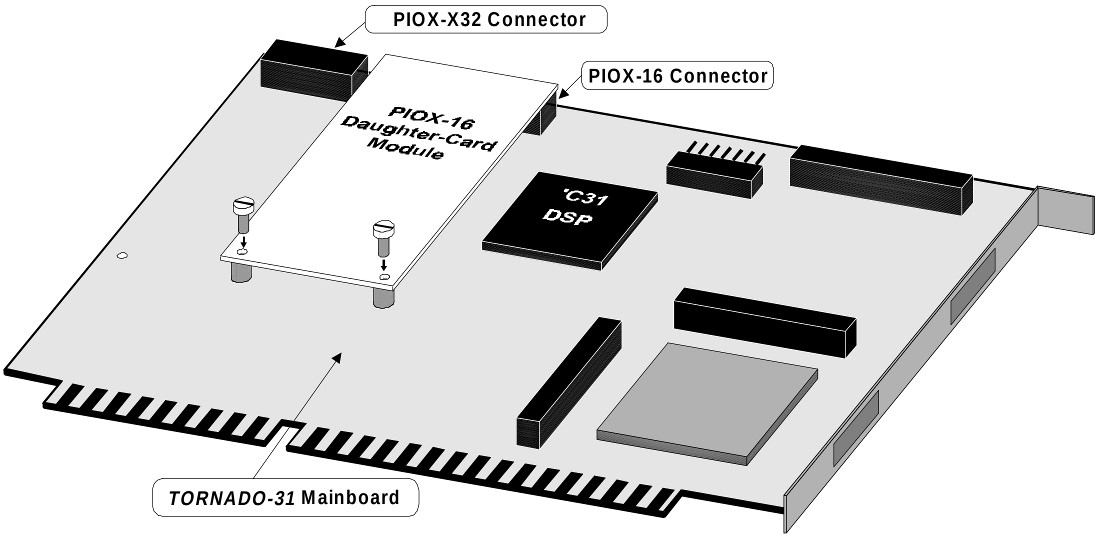


Fig.2-6b. Installation of PIOX-16 daughter-card module onto *TORNADO-31* mainboard.

Accessing PIOX/PIOX-16 from TMS320C31 DSP Environment

PIOX/PIOX-16 can be accessed by on-board TMS320C31 DSP when addressing the corresponding PIOX/PIOX-16 area of TMS320C31 address space (see table 2-2).

Accessing PIOX/PIOX-16 from Host ISA-bus Memory Interface

PIOX/PIOX-16 can be accessed by host ISA-bus memory interface when PIOX/PIOX-16 SB address area is selected by *SB PAGE MAPPER MSB* register from host ISA-bus I/O interface.

PIOX-16 Connector Pinout

TORNADO-31 on-board PIOX-16 connector is a high-density DDK 50-pin DHB-series dual-row female connector with 0.05” pin pitch. Compatible PIOX-16 plugs for customer designed daughter-card modules are available from MicroLAB Systems upon request.

PIOX-16 connector pinout specification is presented at fig 2-7 whereas signal specifications are listed in table 2-12.

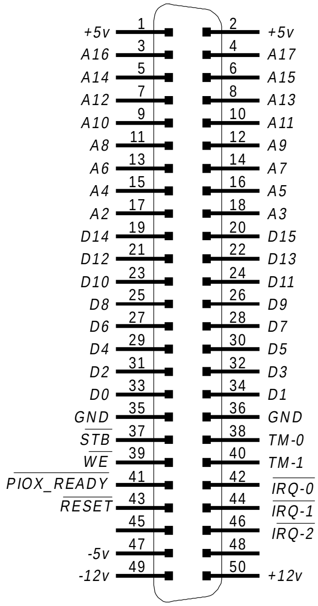


Fig.2-7. PIOX-16 connector pinout (top view).

Table 2-12. PIOX-16 signal description.

Signal name	signal type	description
Address and Data Bus		
A0..A15	O	SB address bus.
D0..D15	I/O	SB data bus.
Data Transfer Control		
$\overline{STB}$	O	Active low PIOX-16 data transfer strobe ($\overline{STB}$ =0).
$\overline{WE}$	O	Active low PIOX-16 write enable signal ($\overline{WE}$ =0).
$\overline{PIOX\_READY}$	I	Active low PIOX-16 data ready acknowledge ($\overline{PIOX\_READY}$ =0) signal. Generated by PIOX-16 module in order to match the PIOX-16 SB cycle timing with timing requirements of memory and I/O devices used in PIOX-16 module. This input has pull-up resistor.

DSP Timers, Reset and Interrupt Requests		
TM-0 *TM-1*	I/O/Z	TMS320C31 DSP on-chip TIMER-0 and TIMER-1 control pins.
$\overline{RESET}$	O	Active low reset signal ($\overline{RESET}$ =0) for on-board TMS320C31 DSP.
$\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, $\overline{IRQ\text{-}2}$	I	Falling edge triggered interrupt request lines for the on-board TMS320C31 DSP with the $\overline{IRQ\text{-}0}$ having the highest priority. These inputs have pulled up resistors. Both static and one-shot (with the pulse length longer than 50 ns) are allowed. Actual TMS320C31 DSP external interrupt requests (*INT0..INT2*) will be generated on the falling edge (1→0) of $\overline{IRQ\text{-}0}$ .. $\overline{IRQ\text{-}2}$ signals.
Power Supplies		
GND		Ground.
+5v		+5v power (from ISA-bus).
+12v		+12v power (from ISA-bus).
-5v		-5v power (from ISA-bus).
-12v		-12v power (from ISA-bus).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

Signal levels for PIOX-16 interface signals correspond to that for the TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

PIOX Connector Pinout

TORNADO-62MX/67MX on-board PIOX connector comprises of the PIOX-16 connector and PIOX 32-bit add-on connector. This allows accommodation of either PIOX-16 daughter-card module for high-speed AD/DA/DIO applications or 32-bit PIOX DSP Coprocessor daughter-card module.

PIOX 32-bit add-on connector is a high-density DDK 30-pin DHB-series dual-row female connector with 0.05” pin pitch. Compatible PIOX-16 plugs for customer designed daughter-card modules are available from MicroLAB Systems upon request.

PIOX connector pinout specification is presented at fig 2-8. As a part of PIOX, the PIOX-16 signal specifications are listed in table 2-12, whereas signal specifications for PIOX add-on connector are listed in table 2-13.

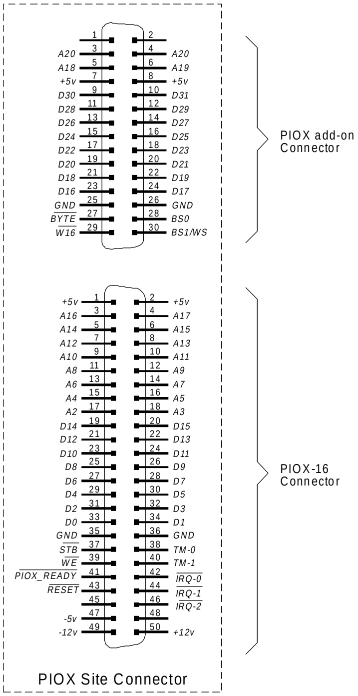


Fig.2-8. PIOX connector pinout (top view).

Table 2-13. PIOX 32-bit add-on connector signal description.

Signal name	signal type	description
		Address and Data Bus
A16..A22	O	Extra SB address lines.
D16..D31	I/O	16-bit MSW of SB data bus.
		Data Transfer Control
$\overline{BYTE}$	O	Defines 8-bit (byte) SB data cycle ($\overline{BYTE}$ =0). The byte selection signals *BS0/BS1* define actual byte #0..#3 (byte #0 is LSB) inside 32-bit SB data word, which will be selected with active $\overline{STB}$ signal. If none of $\overline{BYTE}$ and $\overline{W16}$ signals is active, then current SB access cycle has 32-bit data format.
$\overline{W16}$	O	Defines 16-bit (halfword) SB data cycle ($\overline{W16}$ =0). The halfword selection signal *W0* define actual halfword #0/#1 (halfword #0 is LSW) inside 32-bit SB data word, which will be selected with active $\overline{STB}$ signal. If none of $\overline{BYTE}$ and $\overline{W16}$ signals is active, then current SB access cycle has 32-bit data format.

BS0		Least significant bit of byte selection signals (*BS0*, *BS1*) for 8-bit SB data cycle. Valid during valid $\overline{BYTE}$ =0 signal only.
BS1/WS		Most significant bit of byte selection signals (*BS0*, *BS1*) for 8-bit SB data cycle ($\overline{BYTE}$ =0) or 16-bit halfword selection signal (*WS*) for 16-bit SB data cycle ($\overline{W16}$ =0).
GND		Ground.
+5v		+5v power (from ISA-bus).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

Signal levels for PIOX interface signals correspond to that for the TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

PIOX Data Transfer Cycles

PIOX interface site of *TORNADO-31* supports 8/16/32-bit PIOX data access cycles. Particular type PIOX data access cycle is defined by $\overline{BYTE}$ and $\overline{W16}$ PIOX signals as the following:

- { $\overline{BYTE}$ =0, $\overline{W16}$ =1} state corresponds to *byte (8-bit) PIOX data access cycle*. Selection of particular byte (#0..#3) within addressed 32-bit data word id performed by (*BS0*, *BS1*) byte selection signals.
- { $\overline{BYTE}$ =1, $\overline{W16}$ =0} state corresponds to *16-bit half-word PIOX data access cycle*. Selection of particular 16-bit half-word (#0..#1) within addressed 32-bit data word id performed by *BS1/W0* signals. Signal *BS0* is ignored.
- { $\overline{BYTE}$ =1, $\overline{W16}$ =1} state corresponds to *32-bit word PIOX data access cycle*. (*BS0*, *BS1*) signals are ignored in this mode.
- { $\overline{BYTE}$ =0, $\overline{W16}$ =0} state is reserved.

PIOX-16 Data Transfer Cycles

PIOX-16 interface site of *TORNADO-31* supports 16-bit data transfer cycles only, and, therefore PIOX-16 connector does not contain data cycle definition signals.

Timing Diagram for PIOX/PIOX-16

PIOX/PIOX-16 timing diagram is presented at fig.2-9. This data transfer timing is known as the industry standard MOTOROLA mode and assumes usage of data strobe signal and write enable signal.

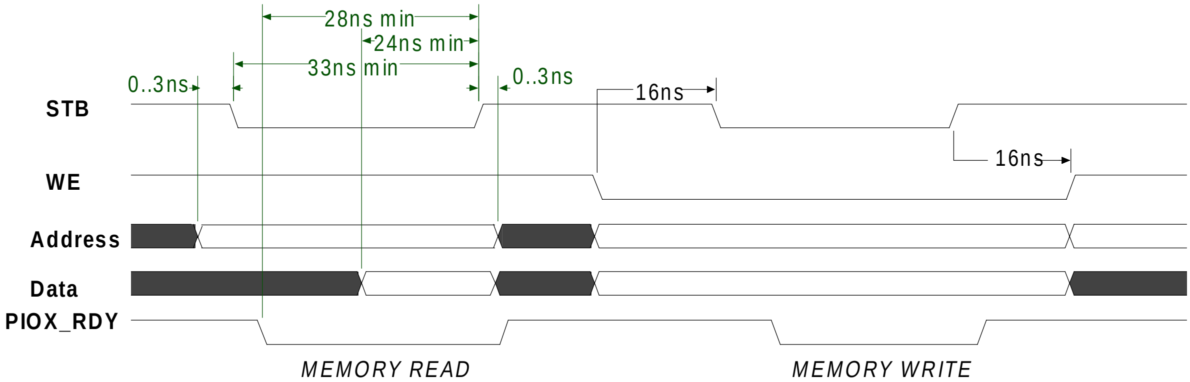


Fig.2-9. Timing diagram of PIOX/PIOX-16 data transfer.

PIOX/PIOX-16 Data Ready Signal

TORNADO-31x on-board PIOX/PIOX-16 data ready controller can generate *SB_READY* data ready signal for active SB bus master using one of four available modes, which is selected by *TORNADO-31* on-board DIP-switch SW2 (see fig.2-2) in accordance with table 2-14.

PX_XWS-0 provides direct translation of *PIOX_READY* signal from installed PIOX/PIOX-16 daughter-card module to *SB_READY* signal without additional wait states added. This mode is standard for AD/DA/DIO daughter-card modules.

Modes *PX_XWS--1/2/3* add one, two or three extra hardware wait states correspondingly prior *PIOX_READY* signal from installed PIOX/PIOX-16 daughter-card module is translated to *SB_READY* signal. These modes should be used with PIOX DSP coprocessor daughter-card modules, which typically utilizes dual-port memory for communication between host PIOX interface and on-module DSP.

Table 2-14. PIOX/PIOX-16 Data Ready Controller Operation Modes.

Mode	**button SW2-1**	**button SW2-2**	**description**
PX_XWS-0	OFF	OFF	Direct translation of *PIOX_READY* signal from installed PIOX/PIOX-16 daughter-card module to *SB_READY* signal without additional wait states added.
PX_XWS-1	ON	OFF	Generated *SB_READY* data ready signal contains one extra hardware wait state (the strobe' signals length is at least 66 ns) and is further defined by the *PIOX_READY* signal.
PX_XWS-2	OFF	ON	Generated *SB_READY* data ready signal contains two extra hardware wait states (the strobe' signals length is at least 99 ns) and is further defined by the *PIOX_READY* signal.
PX_XWS-3	ON	ON	Generated *SB_READY* data ready signal contains three extra hardware wait states (the strobe' signals length is at least 132 ns) and is further defined by the *PIOX_READY* signal.

Notes: 1. Highlighted configuration corresponds to the factory setting.

CAUTION

TMS320C31 DSP on-chip *PRIMARY BUS CONTROL REGISTER* (@808064H) should be set to the SWW field set to '00' value for correct processing of PIOX data ready signal when PIOX daughter-card module is installed. The value of WTCNT field has no meaning.

CAUTION

When TMS320C31 DSP of *TORNADO-31* accesses PIOX/PIOX-16 area while PIOX/PIOX-16 daughter-card module is not installed, then *SB_READY* signal is not generated.

In this case the TMS320C31 DSP of *TORNADO-31* will enter into infinite wait state if TMS320C31 on-chip *PRIMARY BUS CONTROL REGISTER* (@808064H) is set to 00000500H, 00000600H, 00000700H or 00000500H values. In order to avoid this situation it is recommended to set the SWW and WTCNT fields of TMS320C31 on-chip *PRIMARY BUS CONTROL REGISTER* to SWW=10 and WTCNT=111 values correspondingly.

Physical Dimensions for PIOX/PIOX-16 Daughter-card Modules

Physical dimensions for PIOX and PIOX-16 daughter-card modules are presented at fig.2-10. This information is intended for those *TORNADO* customers, who need to design customized PIOX or PIOX-16 daughter-card modules.

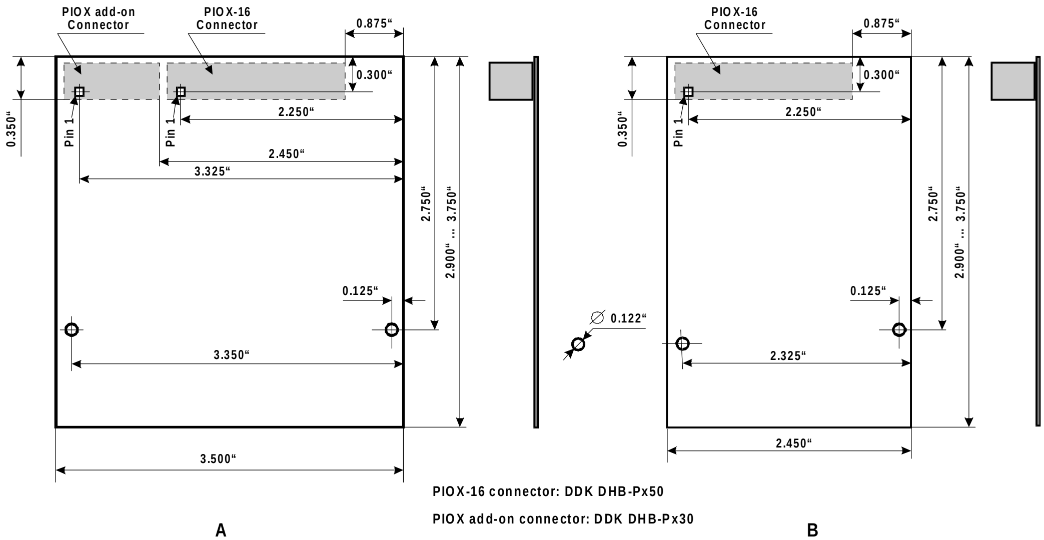


Fig.2-10. Physical dimensions for PIOX (A) and PIOX-16 (B) daughter-card modules.

2.7 Serial I/O Expansion Interface (SIOX) sites

TORNADO-31x provide expansion of the on-board I/O facilities via serial I/O expansion interface (SIOX) sites, which are designed to carry compatible SIOX and SIOX-bus daughter-card modules (see fig.1-1 and fig.2-2). SIOX interface of *TORNADO-31x* is compatible with SIOX interfaces of all *TORNADO* DSP systems and stand-alone *TORNADO-E/EL/SX* DSP controllers.

Available SIOX/SIOX-bus daughter-card modules for *TORNADO* DSP systems include a variety of AD/DA/DIO daughter-cards for telecommunication, speech and audio signal processing, industrial and instrumentation applications, and many more.

Description

Each SIOX site (SIOX-A and SIOX-B) comprises of signals for TMS320C31 DSP on-chip serial port (SIO-0), timers (TM-0/TM-1) and external interrupts control (IRQ-0/IRQ-1/IRQ2), as well as DSP reset signal and ISA-bus power supply lines (fig.2-11).

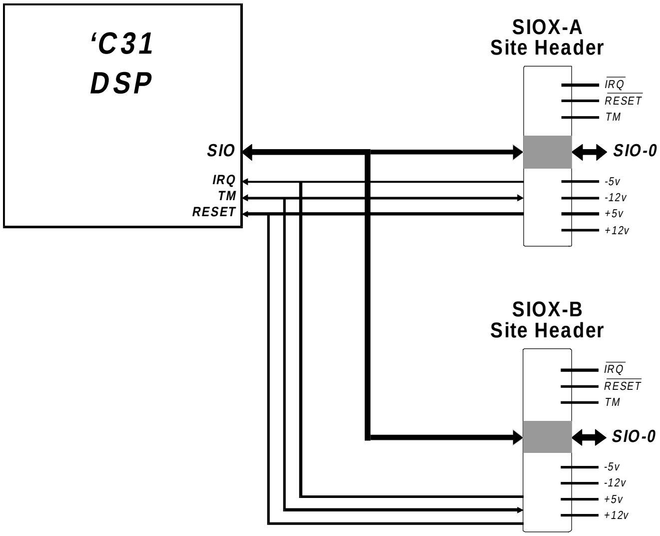


Fig.2-11. SIOX sites connection diagram for *TORNADO-31x*.

Maximum data transfer speed for SIO-0 serial port of SIOX sites for *TORNADO-31* DSP systems is 15 Mbit/s when using DSP generated synchronization and is 11.5 Mbit/s when using external synchronization. Refer to TMS320C3x DSP documentation for more details.

External analog and digital I/O signals for installed SIOX daughter-card modules should be attached via rear panel of host PC.

CAUTION

TORNADO-31x DSP systems feature two on-board SIOX sites (SIOX-A and SIOX-B), which have identical signals and are actually paralleled each other.

One can install either one standard SIOX daughter-card module into either of SIOX-A or SIOX-B sites (so having totally one SIOX module per *TORNADO-31/31Z* mainboard), or can install SIOX-bus compatible daughter-card module into every SIOX-A and SIOX-B sites (so having totally up to two SIOX-bus modules per *TORNADO-31/31Z* mainboard).

TORNADO-31M allows installation of only one SIOX/SIOX-bus module into either of on-board SIOX-A or SIOX-B site depending upon host PC chassis used.

Installation of SIOX Daughter-card Modules onto TORNADO-31x Mainboard

Figure 2-12 shows installation of SIOX daughter-card modules onto *TORNADO-31*, *TORNADO-31Z* and *TORNADO-31M* mainboards.

CAUTION

The on-board area for SIOX-B site of *TORNADO-31/31Z* DSP systems is shared with the on-board area for *UECMX* emulation control daughter-card module. Either SIOX-B or *UECMX* daughter-card module can be installed onto *TORNADO-31/31Z* mainboard.

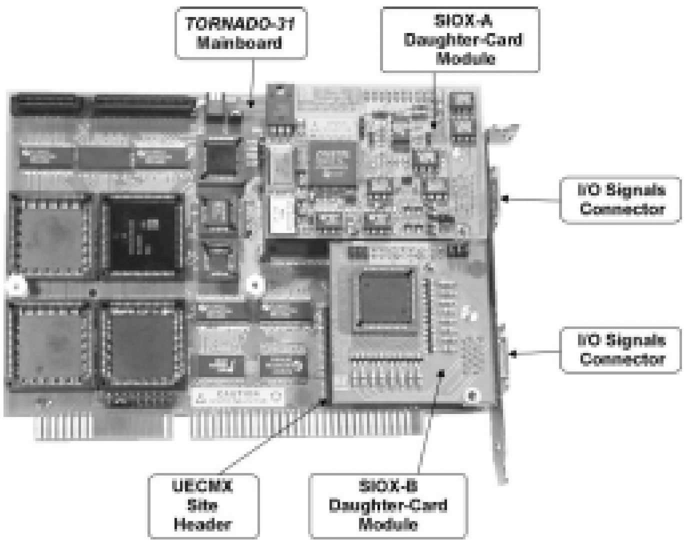


Fig.2-12a. TORNADO-31 mainboard with SIOX-A and SIOX-B daughter-card modules.

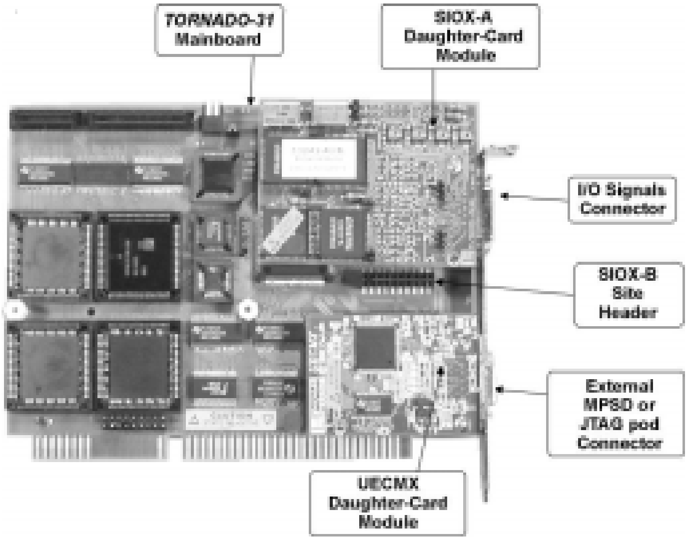


Fig.2-12b. TORNADO-31 mainboard with SIOX-A and UECMX daughter-card modules..

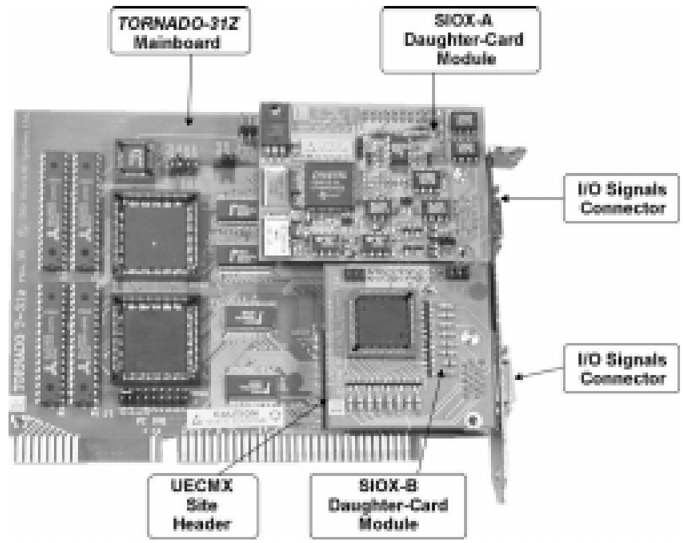


Fig.2-12c. TORNADO-31Z mainboard with SIOX-A and SIOX-B daughter-card modules.

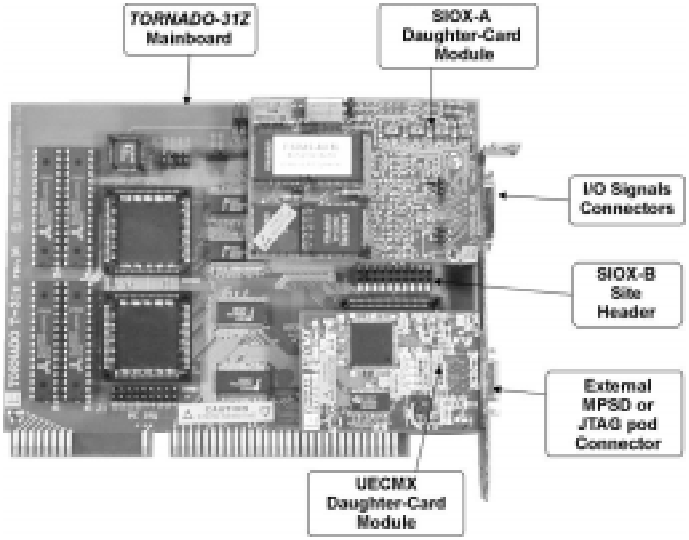


Fig.2-12d. TORNADO-31Z mainboard with SIOX-A and UECMX daughter-card modules..

CAUTION

TORNADO-31M allows only one SIOX daughter-card module being installed at a time into either of on-board SIOX-A or SIOX-B sites.

The horizontal SIOX-A site is used for installation of compatible SIOX daughter-card module in case the *TORNADO-31M* mainboard is installed into the standard desktop PC with external peripherals connection via rear panel of PC chassis.

The vertical SIOX-B site is used for installation of compatible SIOX daughter-card module in case the *TORNADO-31M* mainboard is installed into industrial MicroPC chassis and the external peripherals connects via top panel of MicroPC™ chassis.

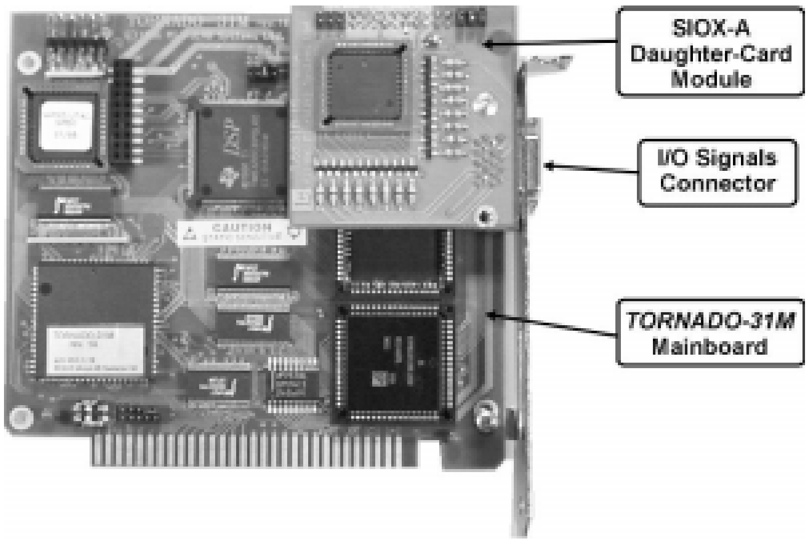


Fig.2-12e. TORNADO-31M mainboard with SIOX daughter-card module for installation into standard desktop PC chassis.

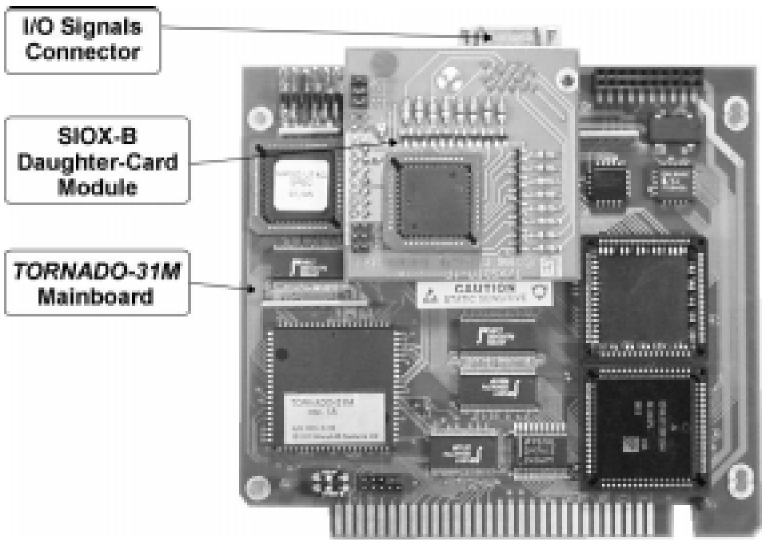


Fig.2-12f. TORNADO-31M mainboard with SIOX daughter-card module for installation into industrial MicroPC™ chassis.

SIOX site connector

SIOX sites connector is an industry standard dual-row 20-pin female header with 0.1"x0.1” pin pattern. SIOX connector pinout is presented at fig.2-13 and signal specifications are listed in table 2-15.

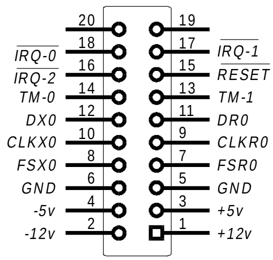


Fig.2-13. SIOX connector pinout (top view).

Table 2-15. SIOX signal specification.

SIOX signal name	signal type	description
		SIO-0 port control
DX0 *FSX0* *CLKX0*	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX site. These signals correspond to the TMS320C31 DSP on-chip serial port transmitter and are wired directly to its pins.
DR0 *FSR0* *CLKR0*	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX site. These signals correspond to the TMS320C31 DSP on-chip serial port receiver and are wired directly to its pins.
		DSP Timers, Reset and Interrupt Requests
TM-0 *TM-0*	I/O/Z	TMS320C31 DSP on-chip TIMER-0 and TIMER-1 control pins.
$\overline{RESET}$	O	Active low reset signal ($\overline{RESET}$ =0) for on-board TMS320C31 DSP.
$\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, $\overline{IRQ\text{-}2}$	I	Falling edge triggered interrupt request lines for the on-board TMS320C31 DSP with the $\overline{IRQ\text{-}0}$ having the highest priority. These inputs have pulled up resistors. Both static and one-shot (with the pulse length longer than 50 ns) are allowed. Actual TMS320C31 DSP external interrupt requests (*INT0..INT2*) will be generated on the falling edge (1→0) of $\overline{IRQ\text{-}0}$ .. $\overline{IRQ\text{-}2}$ signals.
		Power Supplies
GND		Ground.
+5v		+5v power (from ISA-bus).
+12v		+12v power (from ISA-bus).

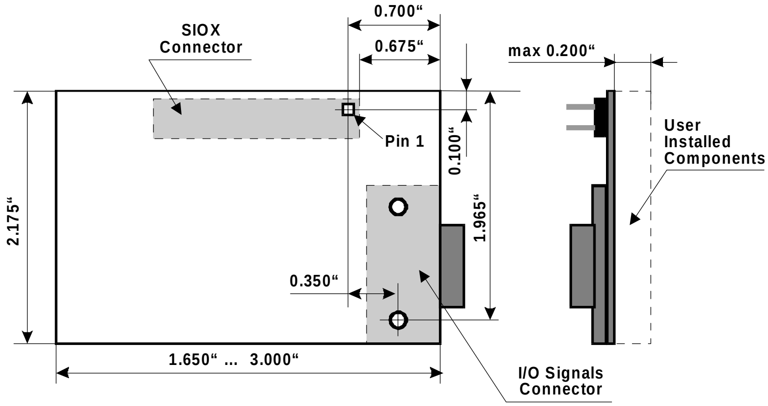
-5v		-5v power (from ISA-bus).
-12v		-12v power (from ISA-bus).

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
1. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

Signal levels for SIOX interface signals correspond to that for the TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

Physical Dimensions for SIOX Daughter-card Modules

Physical dimensions for SIOX daughter-card module are presented at fig.2-14. This information is intended for those *TORNADO* customers, who need to design customized SIOX daughter-card modules.



SIOX connector: 20-pin or 26-pin straight dual-row mail header
(0.025“ Sq., 0.1“x0.1” pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.2-14. Physical dimensions for SIOX daughter-card modules.

2.8 Emulation Tools for *TORNADO-31x*

TORNADO-31x uses scan-path emulation technique in order to debug resident TMS320C31 DSP environment and software.

Scan-path interface of TMS320C31 DSP is known as TI MPSD (modular port scan device), which is similar to the industry standard JTAG port, however allows connection of only one target TMS320C31 per one MPSD emulator channel. Compatible scan-path emulation tools, which can be used with *TORNADO-31x* are as the following:

- external TI XDS510 and MicroLAB’ *MIRAGE-510DX* universal MPSD/JTAG scan-path emulators
- low-cost emulation controller chip (*ECC*) for *TORNADO-31M*, which plugs into the dedicated on-board socket on *TORNADO-31M* mainboard

- low-cost universal emulation control daughter-card module (*UECMX*) for *TORNADO* DSP systems, which plugs into the dedicated site on *TORNADO-31/31Z*. *UECMX* allows emulation of on-board TMS320C31 DSP and also converts *TORNADO-31/31Z* DSP system into universal emulator for all external TMS320 DSP if used with optional external buffer pod, which is compatible with *MIRAGE-510DX* emulator.
- TI HLL Debuggers and GoDSP Code Composer IDE as the debugging environments for TMS320 DSPs, which run with all of the above emulator tools (*ECC*, *UECMX* , TI XDS510 and MicroLAB' *MIRAGE-510DX* universal scan-path emulators).

CAUTION

The MPSD scan-path emulation port of TMS320C31 DSP allows connection of only one TMS320C31 DSP per one MPSD emulator channel and does not allow daisy-chaining as it is available for JTAG based devices.

CAUTION

The DSP must be released from the 'RESET' state and placed into the 'RUN' state prior running TI C3x HLL Debugger or GoDSP C3x/C4x Code Composer IDE (use *-cr0* command line option of *T3CC.EXE* software utility).

It is recommended that the *T3CC.EXE* software utility will be invoked with the *-r* command line option after the host PC power on and after any software trouble situation. This will guarantee that the DSP will be put into known state after the DSP will be released from the 'RESET' state prior running the TI C3x HLL Debugger or GoDSP C3x Code Composer IDE.

On-board MPSD emulation path for TORNADO-31/31Z boards

TORNADO-31/31Z on-board MPSD path is presented at figure 2-15 and comprises of TMS320C31 MPSD emulator port, emulation multiplexer (E-MUX), MPSD-IN connector (JP1) and connector site (JP5) for *UECMX* universal emulation controller daughter-card module.

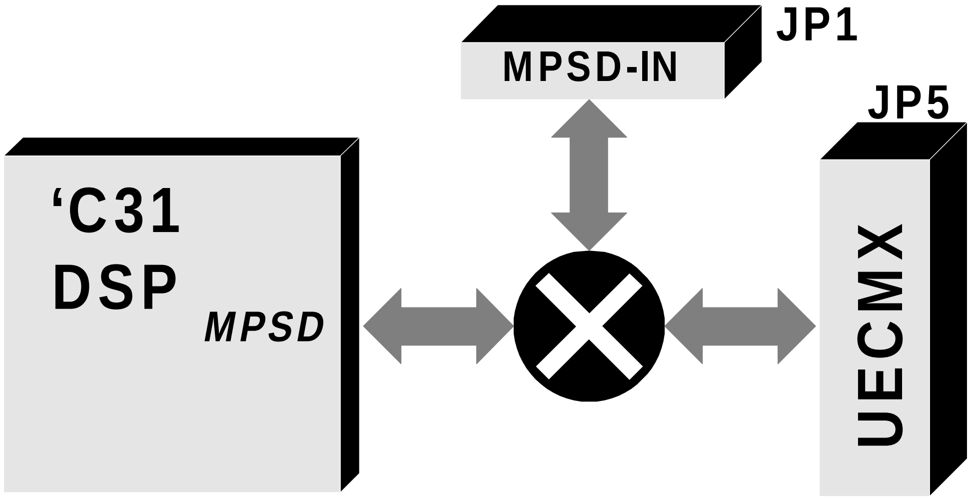


Fig. 2-15. On-board MPSD emulation path of *TORNADO-31/31Z*.

TORNADO-31/31Z on-board emulation multiplexer (EMUX) switches TMS320C31 MPSD emulator port between external emulator and *UECMX* emulator daughter-card module. Emulation multiplexer is controlled either by *T3CC.EXE* software utility software for *TORNADO-31x* or by *UECMXCC.EXE* software utility for *UECMX* emulator module.

The on-board MPSD-IN connector (JP1) should be used for connection to external MPSD emulator, whereas *UECMX* emulator daughter-card module should plug into dedicated *TORNADO-31/31Z* on-board *UECMX* connector site (JP5).

UECMX is the low-cost replacement for external TI XDS510 and MicroLAB' *MIRAGE-510DX* universal MPSD/JTAG emulators, however it does not require external MPSD pod for connection to *TORNADO-31/31Z* board via MPSD-IN connector. Instead, the on-board *TORNADO-31/31Z* hardware provides direct connection of the *UECMX* MPSD port to the on-board TMS320C31 DSP in case *UECMX* is installed and configured for operation with on-board TMS320C31 DSP.

UECMX might be also configured to connect to any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP via optional MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x/C8x) pod, which also connects to target external TMS320 DSP. The MPSD and JTAG pods for *UECMX* are the pods used with MicroLAB' *MIRAGE-510DX* emulator.

UECMX runs under the industry standard TI HLL Debuggers and GoDSP Code Composer IDE. For more details about *UECMX* emulator module refer to "*MIRAGE-510DX/UECMX User's Guide*".

Using external MPSD emulator with TORNADO-31/31Z board

In case external TI XDS510 or MicroLAB' *MIRAGE-510DX* MPSD/JTAG emulator is being used to debug *TORNADO-31/31Z* on-board DSP environment, then this emulator should be connected to MPSD-IN (JP1) on-board connector of *TORNADO-31/31Z* as it is presented at fig.2-16.

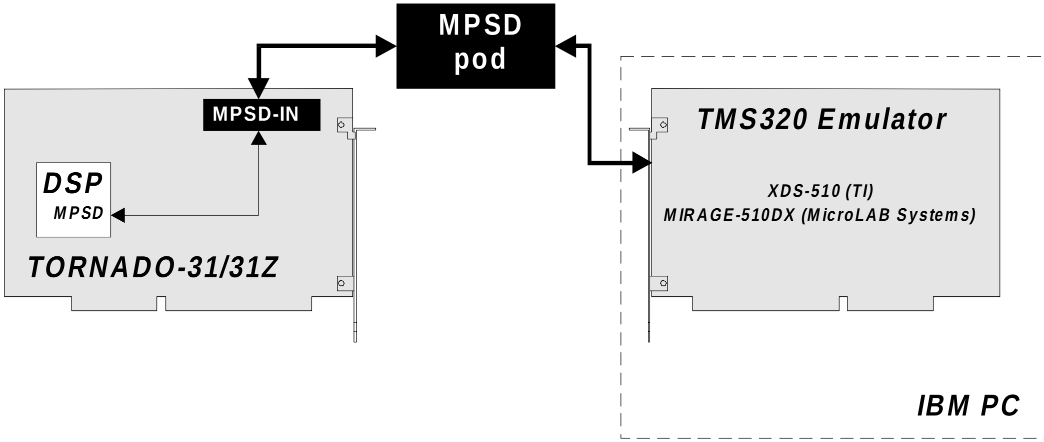


Fig. 2-16. Connection of external MPSD emulator to *TORNADO-31/31Z* board.

Using UECMX with TORNADO-31/31Z

In case external *UECMX* emulator daughter-card module for *TORNADO* emulator is being used to debug *TORNADO-31/31Z* on-board DSP environment, then *UECMX* must plug into on-board *UECMX* site (JP5) as shown at fig.2-17 and configured for operation with on-board DSP.

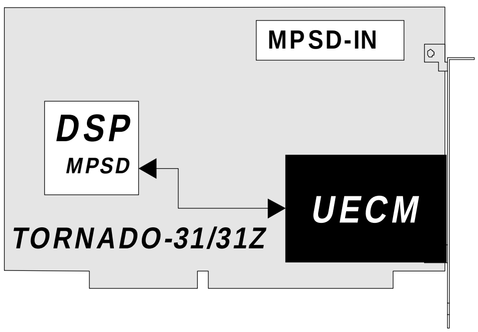


Fig. 2-17. Connection of *UECMX* to MPSD port of *TORNADO-31/31Z* on-board DSP.

CAUTION

Once *UECMX* is installed onto *TORNADO-31/31Z* mainboard and configured for connection to MPSD port of on-board DSP, then the on-board hardware disconnects the MPSD-IN (JP1) connector from on-board MPSD-path.

In this case the external TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator, which is connected to MPSD connector *TORNADO-31/31Z* is ignored and its operation does not effect the functionality of *TORNADO-31/31Z* board.

Using UECMX for emulation external TI TMS320 DSPs

In case *UECMX* is also considered to emulate external TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP, then optional MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x/C8x) pod is required, which connects between *UECMX* and MPSD/JTAG port of target TMS320 DSP as it is presented at fig.2-18. The MPSD and JTAG pods for *UECMX* are the pods used with MicroLAB' *MIRAGE-510DX* emulator.

Selection of target MPSD/JTAG emulation path for *UECMX* is performed either by *T3CC.EXE* software utility software for *TORNADO-31x* or by *UECMXCC.EXE* software utility for *UECMX* emulator module (see chapter 3 for details).

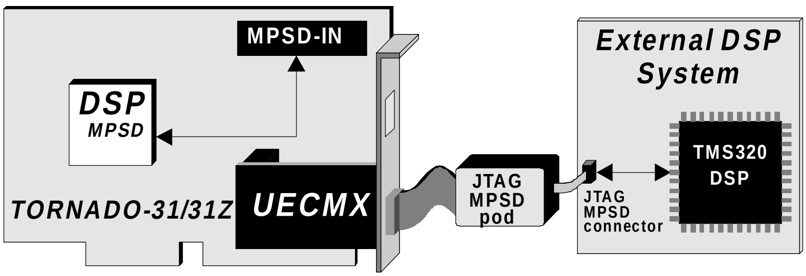


Fig. 2-18. Using *UECMX* for emulation of external TMS320 DSP via optional MPSD/JTAG pod.

When *UECMX* is configured to emulate external TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP via optional MPSD or JTAG pod, then it runs under any of TI C2xx, C3x, C4x, C5x, C54x, C6x, C8x HLL Debuggers or any of Go DSP C2xx/C5x, C3x/C4x, C54x and C6x Code Composer IDE.

CAUTION

Once *UECMX* is installed onto *TORNADO-31/31Z* mainboard and configured to emulate external TMS320 DSP via optional MPSD or JTAG pod, then the on-board hardware disconnects *UECMX* from on-board MPSD path and configures the on-board MPSD path for connection to external TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator via MPSD-IN (JP1) connector.

TORNADO-31M on-board MPSD-path

The on-board MPSD path of *TORNADO-31M* (fig.2-19) comprises of MPSD-IN connector (JP1), TMS320C31 DSP and the *ECC* (emulation control chip, also known as TBC), which is installed into on-board socket site (S6).

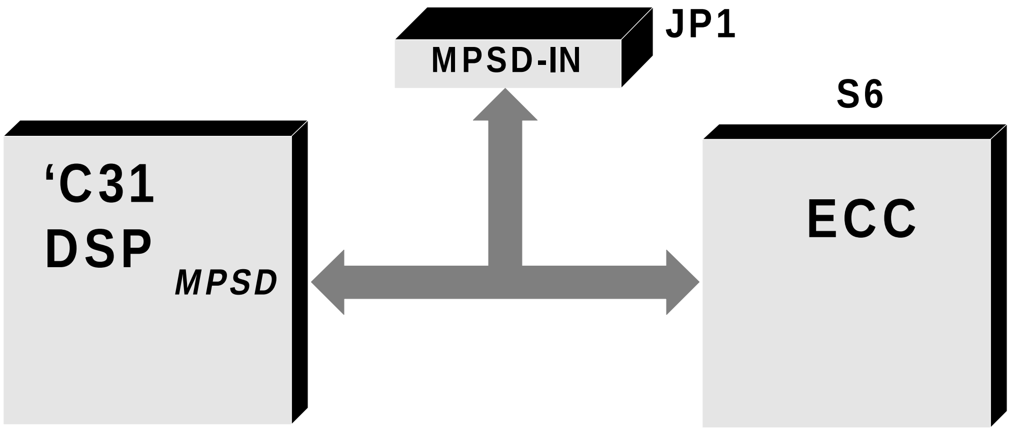


Fig. 2-19. On-board MPSD path of *TORNADO-31M.*

MPSD-IN connector (JP1) should be used for connection of external TI XDS510 or MicroLAB' *MIRAGE-510DX* MPSD emulator, and is paralleled with optional on-board *ECC.*

CAUTION

If TI XDS510 or MicroLAB' *MIRAGE-510DX* universal scan-path emulator is being used with *TORNADO-31M*, then the emulation controller chip (*ECC*) must be switched off using *T3CC.EXE* software utility, and vise-versa.

In case *TORNADO-31M* is used inside the closed computer package, or external TI XDS510 or MicroLAB' *MIRAGE-510DX* universal MPSD/JTAG emulator is not available, then optional *ECC* (emulation controller chip, also known as TBC) is recommended for emulation of *TORNADO-31M* on-board TMS320C31 DSP.

ECC is a low-cost replacement for external TI XDS510 and MicroLAB' *MIRAGE-510DX* universal MPSD/JTAG emulators and installs into the dedicated S6 socket on *TORNADO-31M* mainboard. *ECC* does not require external MPSD pod for connection to *TORNADO-31M* board via MPSD-IN connector. Instead, the on-board *TORNADO-31M* hardware provides direct connection of the *ECC* MPSD port to the on-board TMS320C31 DSP in case *ECC* is installed. *ECC* runs under the industry standard TI C3x HLL Debugger and GoDSP C3x/C4x Code Composer IDE.

Using external MPSD emulator with TORNADO-31M

If external TI XDS510 or MicroLAB' *MIRAGE-510DX* MPSD/JTAG emulator is being used to debug *TORNADO-31M* on-board TMS320C31 DSP environment, then this emulator must connect to the dedicated on-board MPSD-IN connector (JP1) on *TORNADO-31M* mainboard (fig.2-20).

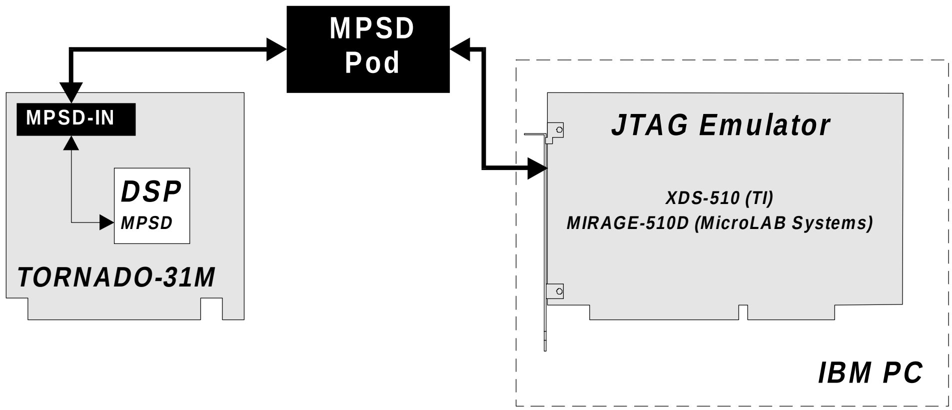


Fig. 2-20. Connection of external MPSD emulator to *TORNADO-31M*.

CAUTION

If TI XDS510 or MicroLAB' *MIRAGE-510DX* universal scan-path emulator is being used with *TORNADO-31M*, then the emulation controller chip (*ECC*) should be switched off using *T3CC.EXE* software utility.

Connection of external XDS510 and *MIRAGE-510DX* emulators to the *TORNADO-31M* on-board MPSD-IN connector while *ECC* is installed and is configured to connect to the on-board TMS320C31 DSP is strongly prohibited and may result in damage of either *ECC* or external XDS510 and *MIRAGE-510DX* emulators.

Using ECC for emulation the TORNADO-31M on-board TMS320C31 DSP

In case *ECC* is being used to emulate *TORNADO-31M* on-board DSP, then *ECC* should be installed into dedicated S6 socket on *TORNADO-31M* mainboard and activated and allocated into host PC-bus I/O address space using *T3CC.EXE* software utility, which is included with the *TORNADO-31M* board (see chapter 3 for details).

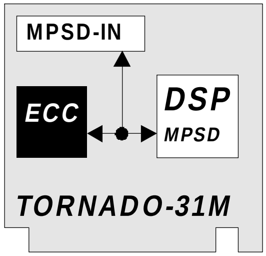


Fig. 2-21. Connection of *ECC* to MPSD port of *TORNADO-31M* on-board DSP.

CAUTION

Once *ECC* is installed and activated, then external XDS510 or *MIRAGE-510DX* emulator should be disconnected from the MPSD-IN connector of *TORNADO-31M*.

Connection of external XDS510 and *MIRAGE-510DX* emulators to the *TORNADO-31M* on-board MPSD-IN connector while *ECC* is installed and is configured to connect to the on-board TMS320C31 DSP is strongly prohibited and may result in damage of either *ECC* or external XDS510 and *MIRAGE-510DX* emulators.

2.9 Software Development Tools

TORNADO-31x is based around TMS320C31 DSP, which is an industry standard DSP and is supported by a variety of software development tools, real-time multitasking tools, DSP algorithm development tools, and application specific function libraries from multiple 3rd party vendors.

Compilers and Debuggers

Software development for *TORNADO-31x* is supported by TI (*www.ti.com*) TMS320 Floating-Point DSP Optimizing C Compiler and Assembly Language Tools.

Debugging of TMS320C31 DSP resident software for *TORNADO-31x* is supported by TI C3x HLL Debugger (*www.ti.com*) and C3x/C4x Code Composer IDE from GoDSP Corp (*www.go-dsp.com*). Both debuggers require either on-board optional emulation controller chip (*ECC*) installed for *TORNADO-31M* or *UECMX* emulation control daughter-card module installed for *TORNADO-31/31Z*.

Hypersignal RIDE Visual DSP Algorithm Development and Simulation Tool

TORNADO-31x DSP systems are supported by DSP algorithm development tools from Hyperception Inc (*www.hyperception.com*), which comprise from Hypersignal Block Diagram, Hypersignal RIDE, Code Generator tools, Happl stand-alone application generator, application specific function libraries and more. Hypersignal RIDE is the visual real-time integrated DSP algorithm development and simulation environment for Windows 95/NT, and allows design entry using high-level function blocks (FIR, FFT, math, etc). The designed DSP algorithm is compiled and loaded into *TORNADO-31x* during design process in order to evaluate the algorithm parameters for real-time execution and to benefit from floating-point performance of *TORNADO-31x* DSP systems.

Real-time Multitasking Operating Systems (RTOS)

TORNADO-31x are supported by multiple industry standard RTOS tools, which provide multitasking capabilities for user application DSP software:

- *VIRTUOSO* from Eonic Systems Inc (*www.eonic.com*) is an industry standard high-performance RTOS and provides full feature multitasking support. *VIRTUOSO* is rated as the best and highest-performance RTOS for DSP. It comes standard with capabilities for host file, keyboard and display I/O from DSP environment via *TORNADO-31x* host ISA-bus interface, and is available with a wide selection of function libraries for DSP, math, matrix, 2D, etc. computations.
- *NUCLEUS PLUS* from Accelerated Technology Inc (*www.atinucleus.com*) is an industry standard single-processor high-performance RTOS and provides full feature multitasking support. Although *NUCLEUS PLUS* is positioned as one of the best RTOS for industrial single-CPU applications and supports virtually any CPU available on the market, is also supports DSP and provide many benefits against other RTOS tools. It features low cost, comes standard with source codes and is royalty free. *NUCLEUS PLUS* also provides many application specific options, including *NUCLEUS FILE*, *NUCLEUS NET*, *NUCLEUS DBUG+* and many more, which also come with source codes.
- *SPOX* from Spectron Microsystems Inc (*www.spectron.com*) was the first industry standard RTOS for DSP that provides multitasking support. It is available with a selection of function libraries for DSP, math, matrix, etc. computations.

Application Software Tools

Application specific tools for *TORNADO-31x* DSP system include a variety of function libraries for DSP, math, vector, image, etc computation, as well as function libraries for vocoder/fax/modem applications and audio multimedia.

Chapter 3. Installation and Configuration

This chapter includes instructions for configuring and installation of *TORNADO-31x* DSP systems into host ISA-bus PC.

3.1 Setting I/O Base Address for Host ISA-bus I/O Interface

You have to setup ISA-bus I/O base address for host ISA-bus I/O interface of *TORNADO-31x* prior installation of *TORNADO-31x* board into ISA-bus slot of host PC. This procedure should be done while host PC power is switched off.

I/O base address for host ISA-bus I/O interface of *TORNADO-31x* is configured by means of on-board DIP-switch SW1 (see fig.A-1) in accordance with configuration setting in table 2-5.

CAUTION

When setting I/O base address for host ISA-bus I/O interface be sure to check I/O base address for other hardware installed in your host PC in order to avoid I/O address conflicts on ISA-bus.

TORNADO-31x is shipped from factory with I/O base address for host ISA-bus I/O interface in accordance with default settings from table 2-5.

3.2 Setting Interrupt Request Line for Host PC

Setting of host PC interrupt request line is optional procedure for *TORNADO-31x* and should be performed in accordance with requirements of application software that you use together with *TORNADO-31x*. This procedure should be done while host PC power is switched off.

Setting of host PC interrupt request line is provided via on-board host PC interrupt request jumper J1 (see fig.A-1). See section 2.5 for details about *TORNADO-31x* host PC interrupt support. *TORNADO-31x* is shipped from factory without PC interrupt request jumper installed.

CAUTION

When setting host CPU interrupt request line be sure to check interrupt requests for other hardware installed in your host PC in order to avoid interrupt request conflicts on ISA-bus.

3.3 Installation of *TORNADO-31x* Mainboard into Host PC

After I/O base address for host ISA-bus I/O interface of *TORNADO-31x* has been configured and host PC interrupt request line has been setup, you can now install *TORNADO-31x* board into 16-bit ISA-bus slot of host PC and screw on-board *TORNADO-31x* mounting bracket to rear panel of host PC. Afterthat, you can safely switch on power of host PC and load operating system of your PC.

3.4 Configuring Memory Base Address for Host ISA-bus Memory Interface

After *TORNADO-31x* has been installed into PC, PC power has been switched on, and PC operating system (DOS or Windows) has been loaded, you can proceed with configuring ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-31x*.

It is recommended to use *T3XCC.EXE* software utility for configuring ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-31x* at DOS prompt.

Setting host PC software environment for accessing host ISA-bus memory interface of TORNADO-31x

Prior you will start working with *TORNADO-31x* host ISA-bus memory interface, you have to configure host PC software environment in accordance with table 2-3 in order it can properly communicate with host ISA-bus memory interface of *TORNADO-31x*.

If memory base address of *TORNADO-31x* host ISA-bus memory interface should be set to *D8000H* hex value, then this requires including the following line into CONFIG.SYS file of host DOS or WINDOWS operating system:

Device=C:\DOS\EMM386.EXE noems x=D800-DFFF

or

Device=C:\WINDOWS\EMM386.EXE noems x=D800-DFFF

The "*x=D800-DFFF*" option for the *EMM386.EXE* memory driver informs *EMM386.EXE* memory driver to reserve the *D8000H..DFFFFH* UMB area, so it will might be used for communication with *TORNADO-31x* host ISA-bus memory interface.

Should you need to set different memory base address of *TORNADO-31x* host ISA-bus memory interface in accordance with table 2-3, then you should setup appropriate ”*x=*“ option for *EMM386.EXE* memory driver in CONFIG.SYS file. Please refer to documentation for DOS and WINDOWS operating system for details.

CAUTION

In case you have PCI PnP cards with UMB mapped memory-based PCI host interface (above 640KB and below 1MB of PC memory address space) installed into your PC along with *TORNADO-31x* board(s), then you have to reserve appropriate UMB area space for *TORNADO-31x* host ISA-bus memory interface via host PC build-in PCI BIOS on PC boot.

Setting Memory Base Address for Host ISA-bus Memory Interface

You have to invoke *T3CC.EXE* software utility with *-imXXXXX* command line option in order to setup ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-31x* at DOS prompt in accordance with table 2-3.

The following example sets *D8000H* memory base address for host ISA-bus memory interface of *TORNADO-31x*:

T3CC -imD8000

In case I/O base address of host ISA-bus I/O interface of *TORNADO-31x* differs from default value specified in table 2-5, then you have also specify *-ipXXX* command line option (where *XXX* denotes I/O base address of host ISA-bus I/O interface for *TORNADO-31x*) in DOS command line when invoking *T3CC.EXE* software utility.

The following example shows how to invoke *T3CC.EXE* software utility for *TORNADO-31x* DSP system with I/O base address for host ISA-bus I/O interface being configured to 300H value:

T3CC -imD8000 -ip300

Switching Off Host ISA-bus Memory Interface

The following example shows how to switch off host ISA-bus memory interface of *TORNADO-31x* DSP system:

T3CC -im0

CAUTION

When setting memory base address for host ISA-bus memory interfaces be sure to check memory base address for other hardware installed in your host PC in order to avoid memory address conflicts on ISA-bus.

3.5 Installation of SRAM banks

TORNADO-31x comes standard with one SRAM memory bank installed and allows expansion of on-board SRAM using memory components as listed below (see section 2.2 and Appendix-A for more details):

- *TORNADO-31* allows installation of up to 2Mx32 0ws of the on-board SRAM, which comprises of four SRAM banks (#0..#3). Each SRAM bank is designed to carry one plug-in SRAM/PLCC chip.
- *TORNADO-31Z* allows installation of up to 1Mx32 0ws of the on-board SRAM, which comprises of two SRAM banks (#0..#1). Each SRAM bank is designed to carry one plug-in SRAM/PLCC chip. SRAM bank #0 can also carry four SRAM/DIP chips in order to provide small on-board SRAM capacity 8K..128Kx32 and to reduce memory cost in case high-density on-board memory is not required for user DSP applications.
- *TORNADO-31M* allows installation of up to 1Mx32 0ws of the on-board SRAM, which comprises of two SRAM banks (#0..#1). Each SRAM bank is designed to carry one plug-in SRAM/PLCC chip.

CAUTION

In case several SRAM banks are installed on *TORNADO-31x* DSP system, then all SRAM banks should have identical SRAM/PLCC chips installed.

CAUTION

You cannot install both SRAM/PLCC chip and SRAM/DIP chips simultaneously into SRAM bank #0 of *TORNADO-31Z*.

Installation of SRAM/PLCC Chips into SRAM Banks

SRAM banks of *TORNADO-31x* DSP systems are designed to accommodate high-density 64K/128K/256K/512Kx32 SRAM/PLCC chips with 15ns data access time and in 68-pin PLCC package (fig.3.1).

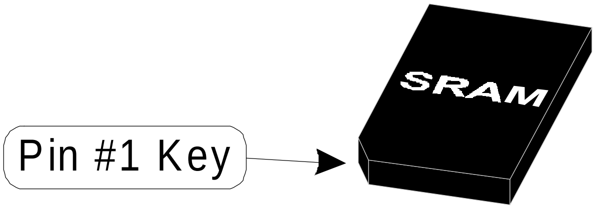


Fig.3-1. SRAM/PLCC chip for *TORNADO-31x*.

SRAM/PLCC chips can be installed into SRAM banks sockets S1..S4 on *TORNADO-31x* mainboard (see fig.A-1 and fig.3-2).

CAUTION

In case several SRAM banks are installed on *TORNADO-31x* DSP system, then all SRAM banks should have identical SRAM/PLCC chips installed.

CAUTION

You have to match correct orientation of SRAM/PLCC chips when installing SRAM/PLCC chips into SRAM banks sockets on *TORNADO-31x* mainboard. If you do not match correct orientation of SRAM/PLCC chips you can damage SRAM/PLCC modules and/or of *TORNADO-31x* on-board hardware.

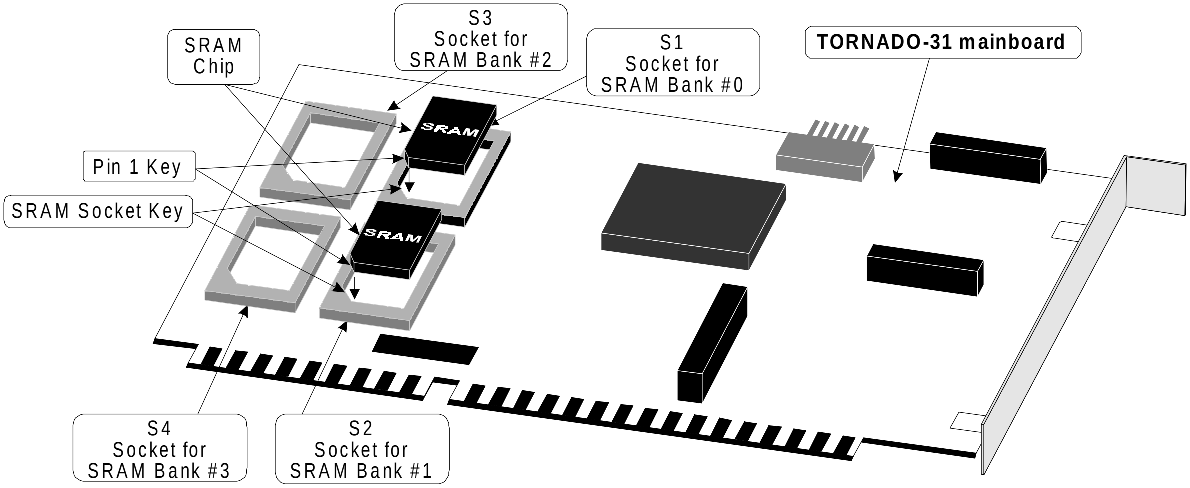


Fig.3-2a. Installation of SRAM/PLCC chip into the SRAM bank socket on *TORNADO-31* mainboard.

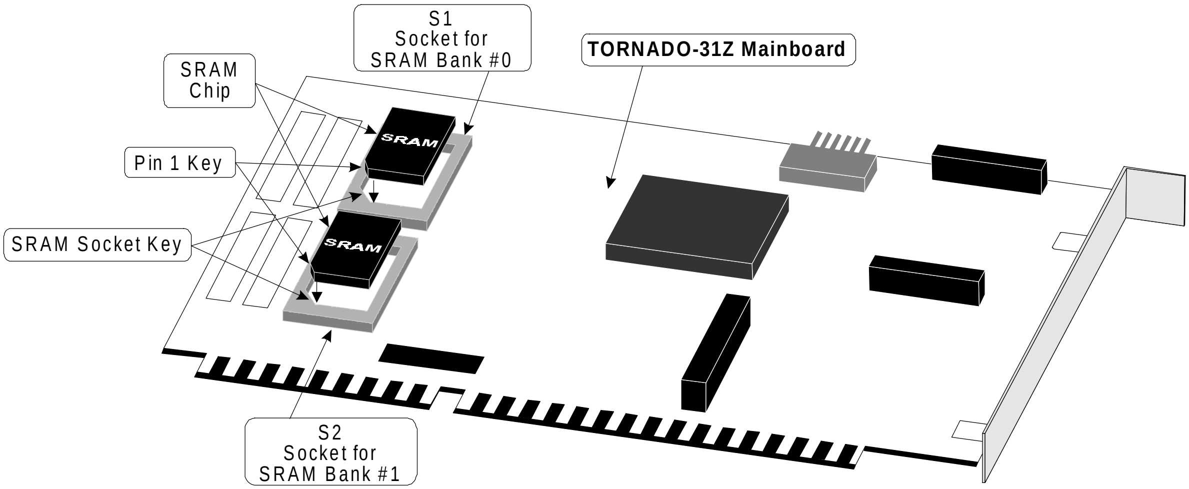


Fig.3-2b. Installation of SRAM/PLCC chip into the SRAM bank socket on *TORNADO-31Z* mainboard.

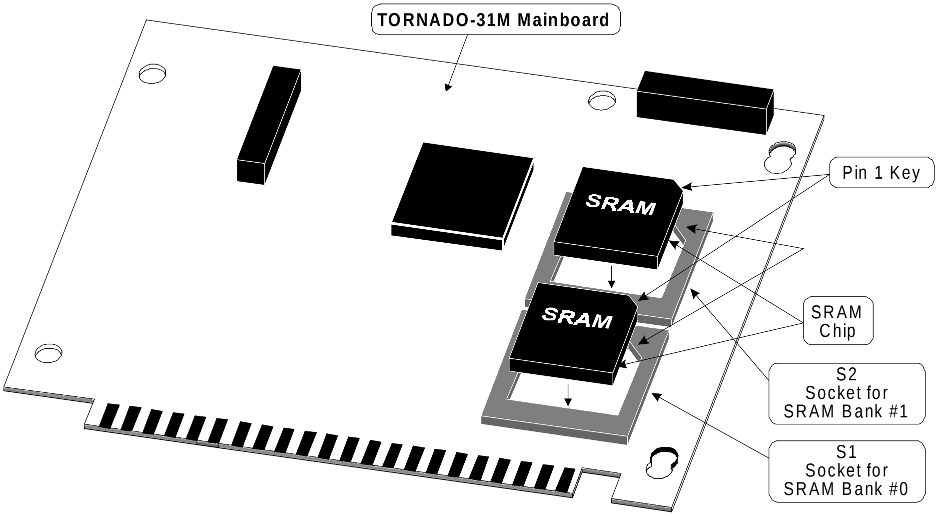


Fig.3-2c. Installation of SRAM/PLCC chip into the SRAM bank socket on *TORNADO-31M* mainboard.

After SRAM/PLCC chips have been installed into SRAM banks on *TORNADO-31x* mainboard, then the on-board jumper set J2, which defines on-board SRAM banks size, must be configured to meet SRAM/PLCC chips capacity (see table 3-1). This is required to have continuous memory address space for all SRAM banks.

Table 3-1a. SRAM bank size for *TORNADO-31*.

SRAM/PLCC chip type	**SRAM bank size**	**installed jumpers from J2 jumper set**
EDI8L3264	*64Kx32*	J2/A-1, J2/B-1
EDI8L32128	*128Kx32*	J2/A-2, J2/B-2
EDI8L32256	*256Kx32*	J2/A-3, J2/B-3
EDI8L32512	*512Kx32*	J2/A-4, J2/B-4

Table 3-1b. SRAM bank size for *TORNADO-31Z/31M*.

SRAM/PLCC chip type	SRAM bank size	installed J2 jumper
EDI8L3264	*64Kx32*	J2-1
EDI8L32128 (TORNADO-31Z/31M) *SRAM/DIP chips are installed in SRAM bank #0 (TORNADO-31Z only)*	*128Kx32*	J2-2
EDI8L32256	*256Kx32*	J2-3
EDI8L32512	*512Kx32*	J2-4

Installation of SRAM/DIP Chips into SRAM Bank #0 of TORNADO-31Z

Along with installation of SRAM/PLCC chips into SRAM banks #0 and #1 of *TORNADO-31Z* DSP system, SRAM bank #0 can also accommodate four SRAM/DIP chips in order to have small 8K..128Kx32 on-board SRAM capacity thus reducing memory cost for those DSP applications, which do not require high-density on-board memory.

CAUTION

You cannot install both SRAM/PLCC chip and SRAM/DIP chips simultaneously into SRAM bank #0 of *TORNADO-31Z*.

Compatible SRAM/DIP chips are the industry standard 8K/32K/64K/128Kx8 SRAM chips with access time 15ns. The package must be either DIP-28 (8K/32Kx8) or DIP-32 (64K/128Kx8) with the package width of 300 MIL.

CAUTION

When installing SRAM/DIP chips into SRAM bank #0 of *TORNADO-31Z*, then four SRAM/DIP chips should be installed simultaneously into sockets S5-1..S5-4 of SRAM bank #0 in order to provide (see fig.A-1 and fig.3-3).

> **CAUTION**
>
> You have to match correct orientation of SRAM/DIP chips when installing SRAM/DIP chips into sockets S4..S8 of *TORNADO-31Z* on-board SRAM bank #0. If you do not match correct orientation of SRAM/DIP chips, you can damage SRAM/DIP chips and/or *TORNADO-31Z* on-board hardware.

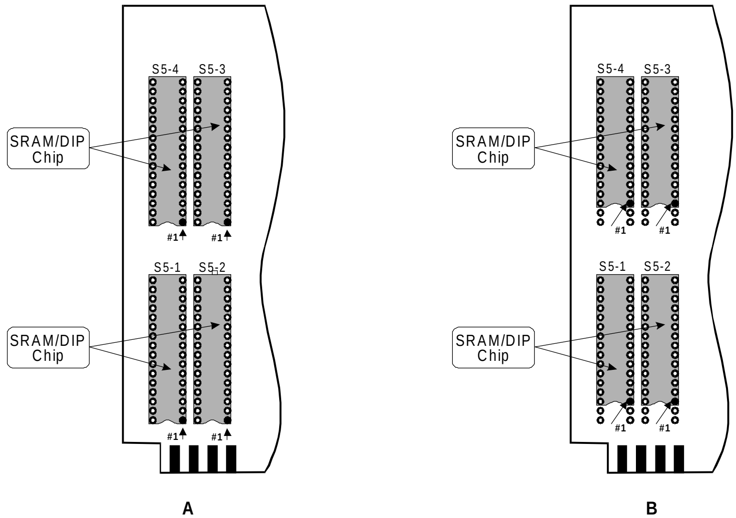


Fig.3-3. Installation of SRAM/DIP chips into sockets S4..S8 of *TORNADO-31Z* on-board SRAM bank #0 (A: - installation of SRAM/DIP chips in DIP-28 package; B: - installation of SRAM/DIP chips in DIP-32 package).

When installing SRAM/DIP chips into sockets S4..S8 of SRAM bank #0, you have to configure on-board *TORNADO-31Z* hardware to recognize those SRAM/DIP chips correctly by means of on-board jumper J3 in accordance with table 3-2 and fig.A-1.

Table 3-2. Setting SRAM/DIP chips type for SRAM bank #0 of *TORNADO-31Z*.

SRAM DIP chips type for SRAM bank #0	**jumper J3**
8Kx8 15ns (DIP-28)	1-2
32Kx8 15ns (DIP-28) *64Kx8 15ns(DIP-32)* *128Kx8 15ns (DIP-32)*	2-3

Note: 1. Highlighted configuration corresponds to default factory settings.

> **CAUTION**
>
> When installing SRAM/DIP chips into sockets S4..S8 of *TORNADO-31Z* on-board SRAM bank #0, you have to set the on-board SRAM banks size to 128Kx32 by means of jumper set J2 in accordance with table 3-1b.

3.6 Installation of *UECMX* Daughter-card Module onto *TORNADO-31/31Z* Mainboard

You have to install *UECMX* module as a daughter-card module (see fig.1-1) into the dedicated on-board site connector JP5 on *TORNADO-31/31Z* mainboard (see fig.1-1 and fig.A-1).

> **CAUTION**
>
> Once you install the *UECMX* daughter card module onto the *TORNADO-31/31Z* mainboard, you cannot use SIOX-B site for installation of SIOX daughter-card modules.

In order to install *UECMX* module onto *TORNADO-31/31Z* mainboard you have to follow the instructions below (see fig.3-4):

- switch off power of host PC and remove *TORNADO-31/31Z* board from ISA-bus slot
- slant *UECMX* module
- insert the on-module connector for active buffer pod into the corresponding hole in the *TORNADO-31/31Z* mounting bracket
- plug in the *UECMX* male header into the dedicated female site connector JP5 on *TORNADO-31/31Z* mainboard
- set ISA-bus I/O base address for the *UECMX* module using the on-module DIP-switch in accordance with "*MIRAGE-510DX/UECMX* User's Guide".

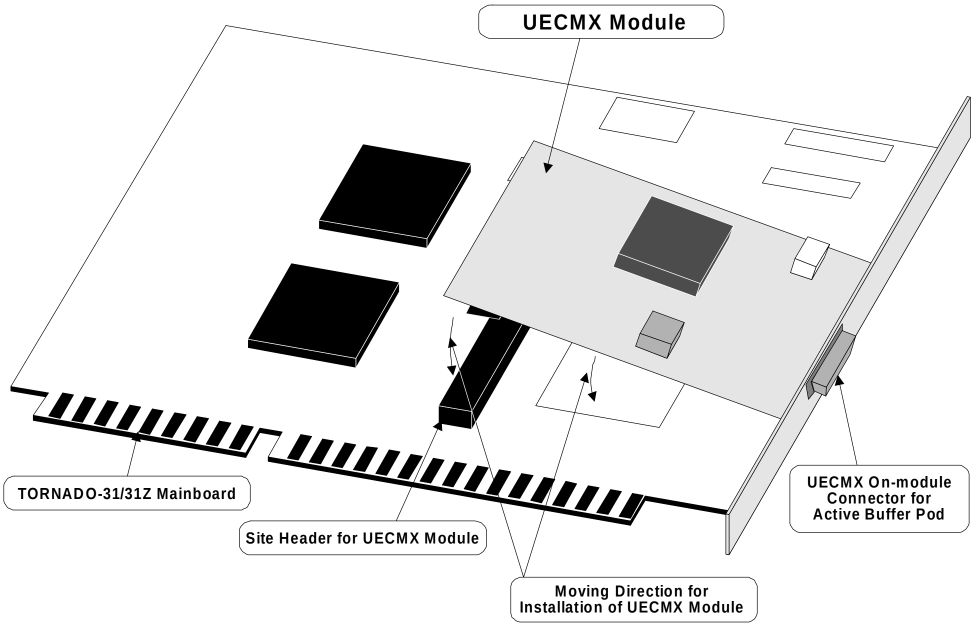


Fig.3-4. Installation of *UECMX* module onto the *TORNADO-31/31Z* mainboard.

UECMX can connect both to the on-board TMS320C31 DSP and to any external TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP via optional MPSD or JTAG pod.

Configuring UECMX to connect to MPSD port of on-board TMS320C31 DSP

After power-on, *UECMX* connects to MPSD port of on-board TMS320C31 DSP. You do not need to use any external MPSD pod for this configuration in order to debug on-board DSP environment.

If you need to configure *UECMX* to connect to MPSD port of on-board TMS320C31 DSP after it was configured to emulate external TMS320 DSP, then you should use *T3CC.EXE* or *UECMXCC.EXE* software utility with '*-ei*' command line option.

If *UECMX* is allocated at the I/O base address, which differs from default 240H I/O base address, then you have to use '*-epXXX*' command line option for *T3CC.EXE* utility and '*-pXXX*' command line option for *UECMXCC.EXE* utility in order to specify I/O base address for *UECMX* (refer to "*MIRAGE-510DX/UECMX* User's Guide" for details).

The following example configures *UECMX*, which is allocated at 280H I/O base address, to connect to MPSD port of on-board TMS320C31 DSP:

T3CC -ei -ep280

UECMXCC -ei -p280

Using UECMX for emulation of external TMS320 DSP

If you want to use *UECMX* to emulate external TMS320C2xx/C3x/C4x/C5x/C54x/C6x/C8x DSP, you have to use optional MPSD (C3x) or JTAG (C2xx/C4x/C5x/C54x/C6x) external pod for connection between the *UECMX* and target TMS320 DSP.

In order to configure the *UECMX* to connect to external TMS320 DSP, you can use either *T3CC.EXE* or *UECMXCC.EXE* software utilities with '*-ex*' command line option and the '*-epXXX*' command line option for *T3CC.EXE* utility and '*-pXXX*' command line option for *UECMXCC.EXE* utility in order to specify I/O base address for *UECMX* (refer to "*MIRAGE-510DX/UECMX* User's Guide" for details), which differs from default 240H I/O base address.

The following example configures *UECMX*, which is allocated at 280H I/O base address, to connect to external TMS320 DSP via optional external buffer MPSD or JTAG pod::

T3CC -ex -ep280

UECMXCC -ex -p280

3.7 Installation of Emulation Controller Chip (*ECC*) onto *TORNADO-31M* Mainboard

Installation of emulation controller chip (*ECC*) into the dedicated socket S6 of *TORNADO-31M* board should be performed while host PC power is off.

Installation of ECC

In order to install emulation controller chip (*ECC*) into the S6 socket onto *TORNADO-31M* board follow recommendations below (see fig. 3-5):

- switch off power of host PC
- remove *TORNADO-31M* board from host PC ISA-bus slot
- take *ECC* by your fingers in such way that its front (labeling) surface is turned to you
- adjust *ECC* to be parallel to the surface of the corresponding S6 PLCC-44 socket on *TORNADO-31M* board
- rotate *ECC* in such way, that the key corner of its PLCC-44 package would match the corresponding corner of on-board S6 PLCC-44 socket
- safely insert *ECC* into on-board S6 PLCC-44 socket
- safely plug and fix *ECC* in the on-board S6 PLCC-44 socket
- install *TORNADO-31M* install into 8-bit ISA-bus slot of host PC
- switch on power of host PC

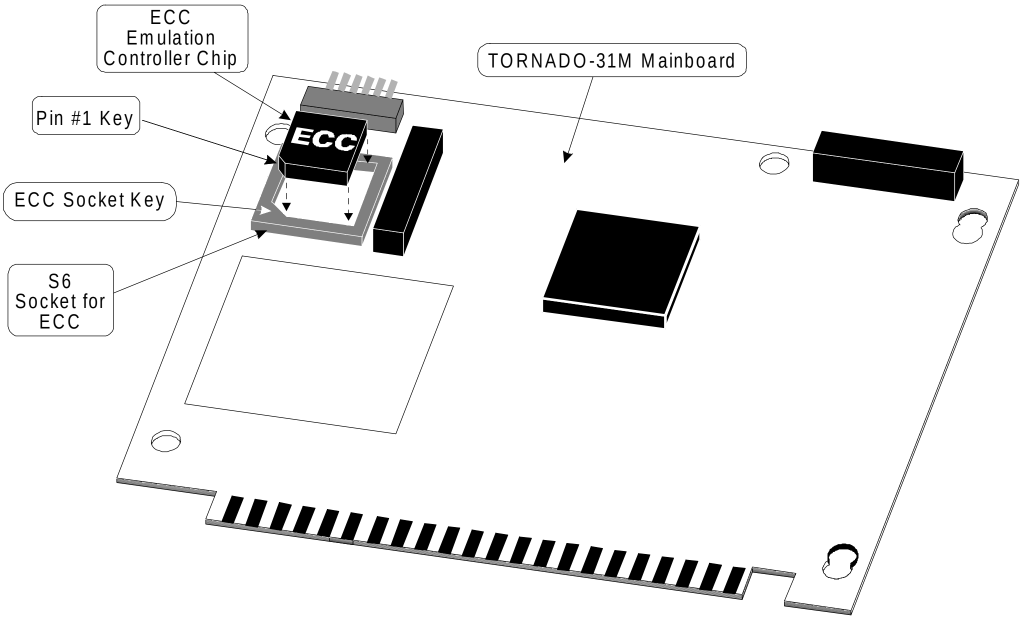


Fig.3-5. Installation of emulation controller chip (*ECC*) onto *TORNADO-31M* board.

Setting I/O Base Address for ECC

You have to invoke *T3CC.EXE* software utility with *-epXXX* command line option in order to activate *ECC* and allocate it at ISA I/O base address in accordance with table 2-11.

The following example activates *ECC* and allocates it default 240H at ISA I/O base address:

T6CC -ep240

In case I/O base address of host ISA-bus I/O interface of *TORNADO-31M* differs from the default value in table 2-5, then you have also specify the *-ipXXX* command line option (where *XXX* denotes I/O base address of host ISA-bus I/O interface for *TORNADO-31M*) when invoking *T3CC.EXE* software utility.

The following example shows how to activate *ECC* and allocate it at default 240H I/O base address for *TORNADO-31M* DSP system, which is configured at 300H ISA-bus I/O base address for its host ISA-bus I/O interface:

T6CC -ep240 -ip300

Switching ECC Off and Deallocating it from ISA-bus I/O Address Space

The following example shows how to switch off *ECC* and deallocate it out from ISA-bus I/O address space:

T3CC -ep0

T3CC -ep0 -ip300

CAUTION

When setting I/O base address for *ECC* be sure to check I/O base address for other hardware installed in your host PC in order to avoid I/O address conflicts on ISA-bus.

Chapter 4. Utility Software

This chapter contains description of utility software for *TORNADO-31x* DSP system.

4.1 *TORNADO-3x* Control Center (T3CC.EXE)

T3CC.EXE (“*TORNADO-3x* Control Center”) software utility program is the DOS command line control software tool for all *TORNADO-3x* DSP systems, which provides easy and powerful user control over *TORNADO-3x* hardware.

T3CC.EXE utility features the following functionality:

- display and sets registers of *TORNADO-31x* host ISA-bus I/O interface
- configures *TORNADO-31x* host ISA-bus memory interface
- reads/writes to on-board SB resources (SRAM and PIOX) via *TORNADO-31x* host ISA-bus memory interface
- configures *UECMX* and *ECC*.

T3CC.EXE utility should be invoked from DOS prompt with up to ten command line options:

T3CC [-*option1*] [-*option2*] [-*option3*] ...

Each command line option corresponds to specific *TORNADO-31x* hardware control operation. The following is a list of available command line options for *T3CC.EXE* utility. Some command line options are specified with reserved command line options in brackets, which correspond to command line options for *T3CC.EXE* utility for old *TORNADO-31x* DSP systems rev.1A/1B, and are provided for compatibility purposes.

System Control via CONTROL REGISTER

-c (-cd)	Display current contents of *CONTROL REGISTER*.
-cc (-ccd)	Display current setting for host SB data cycle format, which is specified by {*SB_CCL-0,SB_CCL-1*} bit field of *CONTROL REGISTER*.
-ccb	Set 8-bit (byte) format for host SB data cycle. Corresponds to setting of {*SB_CCL-0,SB_CCL-1*} bit field of the *CONTROL REGISTER* to the {0,0} state.
-cch	Set 16-bit (halfword) format for host SB data cycle. Corresponds to setting of {*SB_CCL-0,SB_CCL-1*} bit field of *CONTROL REGISTER* to the {1,0} state.
-ccw	Set 32-bit (word) format for host SB data cycle. Corresponds to setting of {*SB_CCL-0,SB_CCL-1*} bit field of *CONTROL REGISTER* to the {0,1} state.
-cg (-cgd)	Display current state of *SB_GLOCK* bit (global SB locking by host ISA-bus memory interface) of *CONTROL REGISTER*.
-cg0	Clear *SB_GLOCK* bit of *CONTROL REGISTER* and unlock SB.

-cg1	Set *SB_GLOCK* bit of *CONTROL REGISTER* for immediate active SB locking.
-cl (-cld)	Display current state of *SB_LOCK* bit (SB locking by host ISA-bus memory interface) of *CONTROL REGISTER*.
-cl0	Clear *SB_LOCK* bit of *CONTROL REGISTER* and unlock SB.
-cl1	Set *SB_LOCK* bit of *CONTROL REGISTER* and issue active SB locking during nearest SB access from host ISA-bus memory interface.
-cie (-cied)	Display current state of *SB_ERROR_IE* bit (host interrupt enable on SB error) of *CONTROL REGISTER*.
-cie0	Clear *SB_ERROR_IE* bit of *CONTROL REGISTER* and disable host interrupts on SB error.
-cie1	Set *SB_ERROR_IE* bit of *CONTROL REGISTER* and enable host interrupts on SB error.
-cim (-cimd)	Display current state of *MH_RQ_IE* bit (host interrupt enable on requests from TMS320C31 DSP) of *CONTROL REGISTER*.
-cim0	Clear *MH_RQ_IE* bit of *CONTROL REGISTER* and disable host interrupts on requests from TMS320C31 DSP.
-cim1	Set *MH_RQ_IE* bit of *CONTROL REGISTER* and enable host interrupts on requests from TMS320C31 DSP.
-cr (-crd)	Display current state of reset signal for TMS320C31 DSP, which is specified by *M_GO* bit of *CONTROL REGISTER*.
-cr0	Remove reset signal for TMS320C31 DSP, i.e. put DSP into "RUN" state. This option sets *M_GO* bit of *CONTROL REGISTER*.
-cr1	Apply reset signal for TMS320C31 DSP, i.e. put DSP into "RESET" state. This option clears *M_GO* bit of *CONTROL REGISTER*.

Flag Registers Control

-fsr	Display contents of *FLAG SELECTOR REGISTER*.
-fsrXX	Select flag register #*XX (hex)*, i.e. load *XX* 8-bit hex data into *FLAG SELECTOR REGISTER*.
-fr	Display contents of currently selected flag register (display *FLAG STATUS REGISTER*). The number of currently selected flag register is defined by the contents of *FLAG SELECTOR REGISTER*.
-frXX	Loads *XX* 8-bit *XX* hex data into the currently selected flag register (load *FLAG CONTROL REGISTER*). The number of currently selected flag register is defined by the contents of *FLAG SELECTOR REGISTER*..
-frs (-fd)	Display contents of *SYS_STATUS_FRG* flag register.

-fe (-fed)	Display current state of *SB_ERROR* flag from *SYS_STATUS_FRG* flag register.
-fe0	Clear *SB_ERROR* flag, i.e. write to *CLEAR_SB_ERROR_FRG* flag register.
-fb (-fbd)	Display current state of *SB_ACK* flag from *SYS_STATUS_FRG* flag register.
-fh (-fhd)	Display current state of *MH_RQ* flag from *SYS_STATUS_FRG* flag register.
-fh0	Clear *MH_RQ* flag, i.e. write to *CLEAR_MH_RQ_FRG* flag register.
-fm1	Generate interrupt request to TMS320C31 DSP, i.e. write to *SET_HM_RQ_FRG* flag register.
-frdi	Display *TORNADO-31x* device ID, i.e. display contents of *DEV_ID0_FRG* and *DEV_ID1_FRG* flag registers.

SB Access Control

-ba (-bad)	Display contents of *SB PAGE MAPPER* register that defines *SMP* SB base address for host-to-SB access.
-balXXXXXX	Load *SB PAGE MAPPER* register with the *SMP* SB base address that corresponds to *XXXXXX* hex SB address of 32-bit SB data word.
-bdSA,EA	Display SB data in 32-bit data format. The *SA* and *EA* parameters specify hex SB starting and ending addresses of 32-bit SB data words correspondingly. Final contents of *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *EA* address.
-bdSA@bS,EA@bE	Display SB data in 8-bit (byte) data format. The *SA* and *EA* parameters specify hex SB starting and ending addresses of 32-bit SB data words correspondingly whereas *bS* and *bE* parameters specify byte offsets (0..3) inside the 32-bit starting and ending data words correspondingly. Final contents of *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *EA* address.
-bdSA@hS,EA@hE	Display SB data in 16-bit (halfword) data format. The *SA* and *EA* parameters specify hex SB starting and ending addresses of 32-bit SB data words correspondingly whereas *hS* and *hE* parameters specify halfword offsets (0..1) inside the 32-bit starting and ending data words correspondingly. Final contents of *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *EA* address.
-bwAAAAAA,XXXXXXXX	Write 32-bit *XXXXXXXX* hex data word at *AAAAAA* hex SB address. The *AAAAAA* parameter defines SB address of 32-bit SB word. *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *AAAAAA* address.

-bwAAAAAA@bS,XX	Write 8-bit *XX* hex data into *bS*-th byte (0..3) of 32-bit SB data word at *AAAAAA* hex SB address. *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *AAAAAA* address.
-bwAAAAAA@hS,XXXX	Write 16-bit *XXXX* hex data (halfword) into *hS*-th halfword (0..1) of 32-bit SB data word at *AAAAAA* hex SB address. *SB PAGE MAPPER* register will be set to the *SMP* SB base address that corresponds to *AAAAAA* address.

Setting I/O and Memory Base Addresses for Host ISA-bus Interface

-im	Display ISA-bus memory base for host ISA-bus memory interface of *TORNADO-31x* in accordance with table 2-3 (display and interprete contents of *ISA_MI_BADDR_FRG* flag register).
-imXXXXX	Set *XXXXX* hex ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-31x* in accordance with table 2-3 (load *ISA_MI_BADDR_FRG* flag register). If *T3CC.EXE* utility is invoked with *-bd* or *-bw* command line options and option *-im* is not specified (or *ISA_MI_BADDR_FRG* flag register was not loaded previously), then the default *D8000H* ISA-bus memory base address will be used for host ISA-bus memory interface during host-to-SB access, and option *-im0* will be automatically executed on exit from *T3CC.EXE* utility in order to deactivate host ISA-bus memory interface afterthat.
-im0	Deactivates host ISA-bus memory interface of *TORNADO-31x*, i.e. removes it from ISA-bus memory address on exit from *T3CC.EXE* utility.
-ipXXX	Specifies *XXX* hex I/O base address for host ISA-bus I/O interface. If this option is omitted, then default factory setting in accordance with table 2-5 will is used.

UECMX and ECC Control

-epXXX	Set the *XXX* hex I/O base address for *UECMX* module or activate and allocate *ECC* chip at *XXX* hex I/O base address. Default setting corresponds to the factory 240H default setting. In case *D_OPTIONS* DOS system variable for TI TMS320C3x HLL Debugger is set and its list includes *-pXXX* option, then *XXX* hex I/O address will be used as default I/O base address for *UECMX/ECC* instead of default setting.
-ei	Connect emulation controller of *UECMX* module to scan-path interface of *TORNADO-31x* on-board TMS320C31 DSP or activate and allocate *ECC* chip at default 240H I/O base address. This option is used for debugging *TORNADO-31x* resident DSP software. No active buffer pod is required for debugging *TORNADO-31x* on-board TMS320C31 DSP if this option is set.
-ex	Connect emulation controller of *UECMX* module to scan-path interface of external TMS320 DSP via optional MPSD or JTAG pod or switch off *ECC*

chip and deallocate it from ISA-bus I/O address area. This option is used to debug external TMS320 DSP and to switch off *ECC* chip. When this option is set, then external TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator can be connected to a dedicated on-board header of *TORNADO-31x* in order to debug on-board TMS320C31 DSP.

-er Perform software reset of *UECMX* module or *ECC* chip. This option is recommended on invocation and exit from TI TMS320C3x HLL Debugger.

General System Control Options

-r Perform software reset of *TORNADO-31x* host ISA-bus interface. All registers of host ISA-bus interface are put into default states, the *ECC* chip of *TORNADO-31M* is reset, DSP is put into 'RESET' state, all error flags are reset, and all host interrupt enable masks are reset. Also, the <NOP> and <B 0x000001> program code is written into reset vector of DSP reset/interrupt table, which guarantees that DSP will be in known state after the DSP reset line will be released prior running the TI C3x HLL Debugger or GoDSP C3x/C4x Code Composer IDE via DSP MPSD emulator interface.

Utility Options

-p Set page-by-page display mode. The "ESC" keypress terminates display output whereas any other keypress results in the next page display.

-? Display help list for the *T3CC.EXE* utility program. Help list is displayed also when the *T3CC.EXE* utility program is invoked without command line options.

T3CC.EXE utility processes command line options in accordance with the following priority list:

1. *CONTROL REGISTER* control options
2. *FLAG STATUS REGISTER* and *FLAG CONTROL REGISTER* control options
3. *UECMX* control options
4. SB access control options.

T3CC.EXE utility returns DOS *exit code* in case it is invoked with *-im*, *-c*, *-cr*, *-cg*, *-cl*, *-cie*, *-cim*, *-fsr*, *-fr*, *-frs*, *-fe*, *-fb*, and *-fh* command line options, which correspond to display of contents of registers, bits and flags of *TORNADO-31x* host ISA-bus interface. The exit code returned corresponds to current value or contents of last displayed bit, bit field, flag or register. Exit code is useful when *T3CC.EXE* utility is integrated into DOS batch (.BAT) file that provides conditional processing. Exit code of *T3CC.EXE* utility program can be analyzed using succeeding '*IF ERRORLEVEL*' DOS batch file commands. The following example of DOS batch file performs conditional processing of *SB_ERROR* flag of *TORNADO-31x*:

```
...
T3CC -fed
IF ERRORLEVEL 1  T32CC -fe0
...
```

When multiple data display options for the *T3CC.EXE* utility are specified, then the returned exit code will correspond to the last processed data display command line option.

In case error is detected by *T3CC.EXE* utility, then the exit code '255' is returned. If *T3CC.EXE* utility is invoked without any data display command line options and no errors is detected, than the exit code '0' is returned.

4.2 Uploading TMS320C3x COFF-files to *TORNADO-31x* via Host ISA-bus Memory Interface

Uploading of TI TMS320C3x COFF-files (output .OUT files from TI Floating-point C/Assembler compilers) into *TORNADO-31x* on-board SB areas and TMS320C31 DSP on-chip environment can be performed by means of *T3COFF.EXE* software utility, that is included with utility software for *TORNADO-31x*. *T3COFF.EXE* utility loads TI TMS320C3x COFF-file into *TORNADO-31x* DSP environment via host ISA-bus memory interface without utilization of emulation controller *ECC* or *UECMX* emulation control daughter-card module.

COFF-file can be uploaded into the *TORNADO-31x* environment using different modes:

- *standard mode*, i.e. when data is uploaded to on-board SB areas via host ISA-bus memory interface without affecting TMS320C31 DSP chip reset line and SB locking
- *reset mode*, i.e. when data is uploaded to on-board SB areas and TMS320C31 DSP on-chip environment via host ISA-bus memory interface while holding TMS320C31 DSP in 'RESET' state
- *global SB locking mode*, i.e. when data is uploaded to on-board SB areas via host ISA-bus memory interface using global SB locking
- *SB locking mode*, i.e. when data is uploaded to on-board SB areas via host ISA-bus memory interface using the SB locking.

All modes except for *reset mode* provide uploading of COFF-file into SB areas only. However, these modes do not effect reset signal for TMS320C31 DSP, and data can be uploaded in parallel with TMS320C31 DSP running.

Reset mode provides uploading of COFF-file into both on-board SB areas and TMS320C31 DSP on-chip environment (including DSP on-chip memory and peripherals). This is performed by means of using run-time TMS320C31 loader that is loaded into on-board SRAM and then removed automatically by *T3COFF.EXE* utility each time loader recognizes that COFF-file data section should be loaded into the DSP on-chip resources.

Uploading of COFF-file into *TORNADO-31x* is performed by invoking *T3COFF.EXE* utility from DOS command line:

T3COFF FILENAME[.OUT] [-*option1*] [-*option2*] [-*option3*] ...

If file extension is missed for source *FILENAME* COFF-file, then .OUT extension is assumed. The following is list of command line options for *T3COFF.EXE* utility, which are grouped into several functional groups.

Upload Mode Control

-lr Set *RESET* mode for uploading of COFF-file. COFF-file is uploaded while holding TMS320C3x DSP in 'RESET' state by means of clearing the

	M_GO bit of *CONTROL REGISTER*. This mode is used for uploading of source program/data modules and supports uploading into both on-board SB areas and TMS320C31 DSP on-chip memory and peripherals. TMS320C31 DSP can be placed into the 'RUN' state on exit from *T3COFF.EXE* utility using *-cr0* command line option. The *-lr* option is assumed as default if none of *-lg*, *-ll* and *-ln* options is specified.
-lg	Set *GLOBAL SB LOCKING* mode for uploading of COFF-file. COFF-file is uploaded into on-board SB areas while holding SB locking by means of setting *SB_GLOCK* bit of *CONTROL REGISTER*. TMS320C31 DSP will not be able to access SB areas until uploading will be finished. TMS320C31 DSP on-chip resources cannot be loaded in this mode. This mode is normally used for uploading of shared data into on-board SB areas while TMS320C31 DSP is executing a program.
-ll	Set *SB LOCKING* mode for uploading of COFF-file. COFF-file is uploaded into on-board SB areas while holding SB locking by means of setting *SB_LOCK* bit of *CONTROL REGISTER*. TMS320C31 DSP will not be able to access SB areas until uploading will be finished. TMS320C31 DSP on-chip resources cannot be loaded in this mode. This mode is normally used for uploading of shared data into on-board SB areas while TMS320C31 DSP is executing a program.
-ln	Set *STANDARD* mode for uploading of COFF-file. COFF-file is uploaded without affecting the 'RESET' state of TMS320C31 DSP and without SB locking. TMS320C31 DSP will be able to access on-board SB areas during uploading of COFF-file. The on-board TMS320C31 DSP on-chip resources cannot be loaded during this mode. This mode is normally used for uploading of run-time program or data into on-board SB areas while on-board TMS320C31 DSP chip is executing a program.
-xi	Exclude uploading of TMS320C31 DSP on-chip memory and peripherals when using the *RESET* mode for uploading. This option should be used together with *-lr* option only.

Restarting TMS320C542 DSP on Exit

-cr0	Restart TMS320C31 DSP on exit from *T3COFF.EXE* utility. This option corresponds to toggling *M_GO* bit from *CONTROL REGISTER*.

Viewing Directory of COFF-file

-d	List directory (sections loading information) for COFF-file. COFF-file will be not loaded into *TORNADO-31x* environment an all other command line options specified will be ignored.

Setting Base Addresses of ISA-bus Memory and I/O Interfaces

-imXXXXX — Set *XXXXX* hex ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-31x* in accordance with table 2-3 (load *ISA_MI_BADDR_FRG* flag register). If *T3CC.EXE* utility is invoked with *-bd* or *-bw* command line options and option *-im* is not specified (or *ISA_MI_BADDR_FRG* flag register was not loaded previously), then the default *D8000H* ISA-bus memory base address will be used for host ISA-bus memory interface during host-to-SB access, and option *-im0* will be automatically executed on exit from *T3CC.EXE* utility in order to deactivate host ISA-bus memory interface afterthat.

-im0 — Deactivates host ISA-bus memory interface of *TORNADO-31x*, i.e. removes it from ISA-bus memory address on exit from *T3CC.EXE* utility.

-ipXXX — Specifies *XXX* hex I/O base address for host ISA-bus I/O interface. If this option is omitted, then default factory setting in accordance with table 2-5 will is used.

Utility Options

-? — Display list of available options for *T3COFF.EXE* utility. Help list is also displayed when *T3COFF.EXE* utility is invoked without command line options and parameters.

In case no errors are detected by *T3COFF.EXE* utility, then exit code '0' will be returned, otherwise exit code '1' will be generated.

CAUTION

If *T3COFF.EXE* utility is used with *-lr* command line option (or when *-lg, -ll* and *-ln* options are not specified) and if either emulation controller (*ECC*) or *UECMX* emulation control daughter card module is installed or any of TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator is attached, then the following error message may appear:

error: missing DSP handshaking

This error message states that the TMS320C31 DSP cannot be initialized correctly during uploading of TMS320C31 DSP on-chip memory or peripherals. This problem is caused by DSP on-chip execution controller that is locked by attached emulator or *ECC/UECMX*.

In order to avoid this problem you have to reset the *ECC/UECMX* or attached emulator. The emulator can be reset using the supplied software reset utility, whereas *ECC/UECMX* can be reset by invoking *T3CC.EXE* utility program with the *-er* command line option.

4.3 *BSF*-files

Along with standard TI COFF-files, *TORNADO-3x* utility software supports binary files with sectional data structure (*binary section format*, *BSF*-files) for high speed program/data upload from host PC disk drive to the on-board SRAM, PIOX and TMS320C31 DSP environment. *BSF*-files also provides security for distribution of user DSP application software since symbolic information is removed from *BSF*-files.

Data transfer for *BSF*-files between host PC disk drive and on-board *TORNADO-31x* SRAM, PIOX and TMS320C31 DSP environment is performed at full speed without utilization of *UECMX* emulation control module or *ECC* emulator chip and TMS320C31 on-chip scan-path interface.

TORNADO-31x utility software tools, which support *BSF*-files, assume conversion of source software program and data modules for TMS320C31 DSP to *BSF*-file format. Source software modules for *BSF*-files can comprise from TI COFF-file (output files from TI floating-point DSP C/Assembly compilers), binary files and hex files. *BSF*-files can be iteratively linked from multiple different source modules.

Structure of BSF-files

BSF-file consists of multiple sequential data sections that are actually the binary data for continuous target memory sections. Each section should be loaded at specified target address. A length of each data section and number of sections are not limited.

BSF-files have smaller total file length due to removal of unused target memory inter-sectional information and due to the binary data format used.

BSF-files have advantages against Intel MCS-86 HEX, Motorola-S, Tektronix HEX, Texas Instruments COFF, etc. file with sectional format since they do not require run-time interpreting and conversion of data, have smaller total length and can be downloaded directly from host disk drive at the highest speed available.

The *BSF*-file comprises of the *global file descriptor* that is located in the very beginning of the *BSF*-file, and of the succeeding binary data sections each containing *section descriptor* and binary data (fig.4-1).

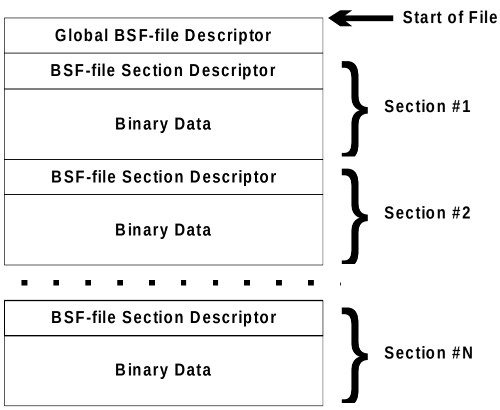


Fig.4-1. Structure of *BSF*-file comprising of *N* sections.

Global *BSF*-file descriptor specifies number of sections in file and includes some security information required for identification and integrity control.

Each *BSF*-file section descriptor specifies data words format, section length in word units, start address and includes some security information required for identification and integrity control.

Tables 4-1 and 4-2 list structures of the global section descriptor for the *BSF*-files.

Table 4-1. Structure of global *BSF*-file descriptor.

byte number	***data type***	***field identifier***	***description***
0	Character	*CS*	Check sum of global file descriptor data starting from the *ID_Rev* field and up to the *File_Length* field. Check sum is defined as the inverse module 256 binary sum of all bytes included.
1-3	Character	*ID_Rev*	Global file descriptor identifier. This field should read and write as 10H, 0H, 1H bytes.
4-7	Long Integer	*Sections*	Number of *BSF*-sections.
8-15	Double Long Integer	*File_Length*	File length in bytes.

Table 4-2. Structure of *BSF*-file section descriptor.

byte number	***data type***	***field identifier***	***description***
0	Character	*CS*	Check sum of section descriptor data starting from the *ID_Rev* field and up to the *Section_Length* field. Check sum is defined as the inverse module 256 binary sum of all bytes included.
1-3	Character	*ID_Rev*	Section descriptor identifier. This field should read and write as 80H, 0H, 1H bytes.
4-5	Integer	*Word_Data_Bits*	Data word length in bits. Values õ8 (8, 16, 24, 32, etc) are valid.
6-13	Double Long Integer	*Load_Address*	Specifies 64-bit target start address of the section data. Address is specified in the word units.
13-21	Double Long Integer	*Section_Length*	Section length in word units.

4.4 Creating and Editing *BSF*-files

BSF-files can be created from source HEX- and BIN-files using *H32BSF.EXE* and *BINBSF.EXE* software converters. You can provide conversion from the following source data files :

- from source *.H32 files that should be in Intel MSC-86 HEX (Extended Intel HEX) with 32-bit address/data words (using the *H32BSF.EXE* software converter)
- from source *.OUT TI COFF files that are generated by TI floating point DSP C and Assembler compilers (using the *H32BSF.EXE* software converter)
- from source *.BIN binary files (using the *BINBSF.EXE* software converter).

All software converters support append mode (command line option *-a*) in order to append new data sections to the end of existing *BSF*-file. This allows to assemble multi-sectional *BSF*-files from different source files with different source data formats.

BSF-file software editor is used in order to list the *BSF*-file directory and to remove undesired data sections.

Conversion of Intel MCS-86 HEX files (.H32) into BSF-files (.BSF)

H32BSF.EXE software converter provides conversion of source .H32 files in Intel MCS-86 HEX (Extended Intel HEX) format with 32-bit address/data words into the corresponding *BSF*-files

$$*.H32 \rightarrow *.BSF$$

Since Intel MCS-86 HEX format is the industry standard format and is supported by almost all compilers, the *H32BSF.EXE* utility may be used for conversion of source program modules generated by different compilers for TMS320C3x DSP chips.

H32BSF.EXE software converter should be invoked from DOS command line:

H32BSF in_file[*.H32*] *out_file*[*.BSF*] [*-a*]

where:

in_file	denotes source Intel MCS-86 HEX (Extended Intel HEX) file with 32-bit address/data words. If file extension is not specified, default .H32 file extension is assumed.
out_file	output *BSF*-file. If file extension is not specified, default .BSF file extension is assumed.
-a	command line option, which specifies that the converted source data sections should be appended to the end of existing *BSF*-file. If output *BSF*-file do not exist, then *-a* option is ignored and new *BSF*-file is created. If *-a* option is not specified, then existing *BSF*-file will be overwritten.

In case no errors are detected by *H32BSF.EXE* software converter, then exit code '0' will be returned, otherwise exit code '1' will be returned.

Conversion of TI COFF files (.OUT) into BSF-files (.BSF)

Conversion of TI COFF files (.OUT), which are generated by TI floating point DSP C/Assembler compilers, into the corresponding *BSF*-files, can be performed by means of intermediate conversion of source COFF files into Intel MCS-86 HEX files .H32 and further conversion into *BSF*-file using TI *H32BSF.EXE* software converter:

**.OUT → *.H32 → *.BSF*

HEX30.EXE utility (version 4.50 or later) must be used to convert source TI COFF files (.OUT) into Intel MCS-86 HEX files (.H32) with 32-bit address/data words:

HEX30 -I -memwidth 32 -romwidth 32 IN_FILE.OUT -o OUT_FILE.H32

HEX30.EXE utility is standard software utility included with TI floating point DSP C/Assembler compiler tools. To get more information about *HEX30.EXE* utility refer to original TI documentation.

Final conversion of .H32 file into the corresponding *BSF*-file must be done by *H32BSF.EXE* software converter (refer to the corresponding subsection earlier in this section).

Conversion of Binary Files (.BIN) into the BSF-files (.BSF)

Conversion of binary source files .BIN with different source data formats (8-bit bytes, 16-bit and 32-bit words) into the corresponding *BSF*-files *.BSF*

**.BIN → *.BSF*

can be performed using *BINBSF.EXE* software converter, which is included with utility software for *TORNADO-31x.*

BINBSF.EXE software converter performs conversion of source .BIN binary file and adds only one section into output *BSF*-file. The *-a* command line option may be used in order to append new sections to existing *BSF*-files.

BINBSF.EXE software converter is useful for including large binary data tables into *BSF*-files, as well as for conversion of source program or data modules in binary format into *BSF*-files for *TORNADO-31x.*

BINBSF.EXE software converter should be invoked from DOS command line:

BINBSF in_file[*.BIN*] *out_file*[*.BSF*] *-fb/-fw16/-fw32 -lXXXXXXX* [*-a*]

where:

in_file	denotes source binary file. If file extension is not specified, default .BIN file extension is assumed.
out_file	output *BSF*-file. If file extension is not specified, default .BSF file extension is assumed.
-fb	specifies that source data are in 8-bit (byte) data word format. This option is alternative to *-fw16* and *-fw32* options.
-fw16	specifies that source data are in 16-bit data word format. In case source data contains non integer number of 16-bit data words, then the generated section for *BSF*-file will be supplied with corresponding number of zero bytes. This option is alternative to *-fb* and *-fw32* options.
-fw32	specifies that source data are in 32-bit data word format. In case source data contains non integer number of 32-bit words, than the generated section for *BSF*-file will be supplied with corresponding number of zero bytes. This option is alternative to *-fb* and *-fw16* options.
-lXXXXXXX	specifies hex starting (loading) address *XXXXXXX* of converted data in the address space of *TORNADO-31x* on-board TMS320C31 DSP chip. Starting address is specified in units of selected data words (defined by *-fb/-fw16/-fw32* options). In case data format is defined as 8-bit (byte) format (option *-fb*), then starting address is the address of first byte of section data in continuous bytes address space. In case data format is defined as 16-bit word format (option *-fw16*), then starting address is the address of first 16-bit word of section data in continuous 16-bit words address space. In case data format is defined as 32-bit word format (option *-fw32*), then starting address is the address of first 32-bit word of section data in continuous 32-bit words address space.
-a	specifies that converted source data section will be appended to the end of existing output *BSF*-file. If output *BSF*-file does not exist, then *-a* option is ignored and new *BSF*-file will be created. If the *-a* option is not specified, then existing *BSF*-file will be overwritten.

In case no errors are detected by *BINBSF.EXE* software converter, then exit code '0' will be returned, otherwise exit code '1' will be returned.

Viewing Directory and Editing BSF-file

When using *BSF*-files you may want to list *BSF*-file directory or to remove undesired data section from *BSF*-file. This may be performed using *BSFEDIT.EXE* software editor that is included with utility software for *TORNADO-31x*.

BSFEDIT in_file[*.BSF*] *-dN*

where:

in_file	denotes source and output *BSF*-file. If file extension is not specified, default .BSF file extension is assumed.
-dN	specifies that *N*-th data section should be removed from *BSF*-file. *N* value should be not greater than number of sections in *BSF*-file.

In order to display directory of *BSF*-file, the *BSFEDIT.EXE* utility should be invoked with source *BSF*-file name specified only.

In case no errors are detected by *BSFEDIT.EXE* utility, then exit code '0' will be returned, otherwise exit code '1' will be generated.

4.5 Uploading *BSF*-files to *TORNADO-31x* via Host ISA-bus Memory Interface

Uploading of *BSF*-files into *TORNADO-31x* on-board SRAM, PIOX and TMS320C31 DSP on-chip environment can be performed by means of *T3BSFLD.EXE* software utility, that is included with utility software for *TORNADO-31x*. *T3BSFLD.EXE* utility loads *BSF*-file into *TORNADO-31x* environment via host ISA-bus memory interface without utilization of *UECMX* module.

BSF-file can be uploaded into the *TORNADO-31x* environment using different modes:

- *standard mode*, i.e. when data is uploaded to on-board SRAM/PIOX via host ISA-bus memory interface without affecting TMS320C31 DSP chip reset line and SB locking
- *reset mode*, i.e. when data is uploaded to on-board SRAM/PIOX and TMS320C31 DSP on-chip environment via host ISA-bus memory interface while holding TMS320C31 DSP in 'RESET' state
- *global SB locking mode*, i.e. when data is uploaded to on-board SRAM/PIOX via host ISA-bus memory interface using global SB locking
- *SB locking mode*, i.e. when data is uploaded to on-board SRAM/PIOX via host ISA-bus memory interface using the SB locking.

All modes except for *reset mode* provide uploading of *BSF*-file into SRAM/PIOX only. However, these modes do not effect reset signal for TMS320C31 DSP, and data can be uploaded in parallel with TMS320C31 DSP running.

Reset mode provides uploading of *BSF*-file into both on-board SRAM/PIOX and TMS320C31 DSP on-chip environment (including DSP on-chip memory and peripherals). This is performed by means of using run-time TMS320C31 loader that is loaded into on-board SRAM/PIOX and then removed automatically by *T3BSFLD.EXE* utility each time loader recognizes that *BSF*-file data section should be loaded into the DSP on-chip resources.

Uploading of *BSF*-file into *TORNADO-31xL* is performed by invoking *T3BSFLD.EXE* utility from DOS command line:

T3BSFLD FILE.BSF [-*option1*] [-*option2*] [-*option3*] *...*

The following is list of command line options for *T3BSFLD.EXE* utility, which are grouped into several functional groups:

Upload Mode Control

-lr Set *RESET* mode for uploading of *BSF*-file. *BSF*-file is uploaded while holding TMS320C31 DSP in 'RESET' state by means of clearing *MRES* bit of *CONTROL REGISTER*. This mode is used for uploading of source program/data modules and supports uploading into both on-board SRAM/PIOX and TMS320C31 DSP on-chip memory and peripherals. TMS320C31 DSP can be placed into the 'RUN' state on exit from *T3BSFLD.EXE* utility using *-cr0* command line option. The *-lg* option is used as default if none of *-lg*, *-ll* and *-ln* options is specified.

-lg Set *GLOBAL SB LOCKING* mode for uploading of *BSF*-file. *BSF*-file is uploaded into on-board SRAM/PIOX while holding SB locking by means of setting *SB_GLOCK* bit of *CONTROL REGISTER*. TMS320C31 DSP will not be able to access SRAM/PIOX until uploading will be finished. TMS320C31 DSP on-chip resources cannot be loaded in this mode. This mode is normally used for uploading of shared data into on-board SRAM/PIOX while TMS320C31 DSP is executing a program.

-ll Set *SB LOCKING* mode for uploading of *BSF*-file. *BSF*-file is uploaded into on-board SRAM/PIOX while holding SB locking by means of setting *SB_LOCK* bit of *CONTROL REGISTER*. TMS320C31 DSP will not be able to access SRAM/PIOX until uploading will be finished. TMS320C31 DSP on-chip resources cannot be loaded in this mode. This mode is normally used for uploading of shared data into on-board SRAM/PIOX while TMS320C31 DSP is executing a program.

-ln Set *STANDARD* mode for uploading of *BSF*-file. *BSF*-file is uploaded without affecting 'RESET' state of TMS320C31 DSP and without SB locking. TMS320C31 DSP will be able to access on-board SRAM/PIOX during uploading of *BSF*-file. The on-board TMS320C31 DSP on-chip resources cannot be loaded during this mode. This mode is normally used for uploading of run-time program or data into on-board SRAM/PIOX while on-board TMS320C31 DSP chip is executing a program.

-xi Exclude uploading of TMS320C31 DSP on-chip memory and peripherals when using *RESET* mode for uploading. This option should be used together with *-lr* option only.

Setting Format of Host SB Data Cycle

-bcb	Set 8-bit (byte) format for host SB data cycle. Corresponds to setting of {*SB_CCL-0,SB_CCL-1*} bit field of the *CONTROL REGISTER* to the {0,0} state. This option is used as default when none of *-bch* and *-bcw* options is specified.
-bch	Set 16-bit (halfword) format for host SB data cycle. Corresponds to setting of {*SB_CCL-0,SB_CCL-1*} bit field of *CONTROL REGISTER* to the {1,0} state.
-bcw	Set 32-bit (word) format for host SB data cycle. Corresponds to setting of {*SB_CCL-0,SB_CCL-1*} bit field of *CONTROL REGISTER* to the {0,1} state.

Restarting TMS320C31 DSP on Exit

-cr0	Remove reset signal for TMS320C31 DSP and put DSP into the program execution state on exit from *T3BSFLD.EXE* utility. This option corresponds to setting *MRES* bit from *CONTROL REGISTER*.

Setting Base Addresses of ISA-bus Memory and I/O Interfaces

-imXXXXX	Set *XXXXX* hex ISA-bus memory base address for host ISA-bus memory interface of *TORNADO-31x* in accordance with table 2-3 (load *ISA_MI_BADDR_FRG* flag register). If *T3CC.EXE* utility is invoked with *-bd* or *-bw* command line options and option *-im* is not specified (or *ISA_MI_BADDR_FRG* flag register was not loaded previously), then the default *D8000H* ISA-bus memory base address will be used for host ISA-bus memory interface during host-to-SB access, and option *-im0* will be automatically executed on exit from *T3CC.EXE* utility in order to deactivate host ISA-bus memory interface afterthat.
-im0	Deactivates host ISA-bus memory interface of *TORNADO-31x*, i.e. removes it from ISA-bus memory address on exit from *T3CC.EXE* utility.
-ipXXX	Specifies *XXX* hex I/O base address for host ISA-bus I/O interface. If this option is omitted, then default factory setting in accordance with table 2-5 will is used.

Utility Options

-?	Display list of available options for *T3BSFLD.EXE* utility. Help list is also displayed when *T3BSFLD.EXE* utility is invoked without command line options and parameters.

In case no errors are detected by *T3BSFLD.EXE* utility, then exit code '0' will be returned, otherwise exit code '1' will be generated.

CAUTION

If *T3BSFLD.EXE* utility is used with *-lr* command line option (or when *-lg*, *-ll* and *-ln* options are not specified) and if either *UECMX* module is installed or any of TI XDS510 or MicroLAB' *MIRAGE-510DX* emulator is attached, then the following error message may appear:

error: missing DSP handshaking

This error message states that the TMS320C31 DSP cannot be initialized correctly during uploading of TMS320C31 DSP on-chip memory or peripherals. This problem is caused by DSP on-chip execution controller that is locked by attached emulator or *UECMX*.

In order to avoid this problem you have to reset *UECMX* or attached emulator. The emulator can be reset using the supplied software reset utility whereas *UECMX* can be reset by invoking *T3CC.EXE* utility program with *-er* command line option.

Appendix A. On-board Jumpers, Connectors and Sockets.

This Appendix includes a summarized description for *TORNADO-31x* on-board configuration jumpers, connectors, switches and sockets.

Layout for different *TORNADO-31x* boards with on-board configuration jumpers, connectors, switches and sockets is presented at fig.A-1.

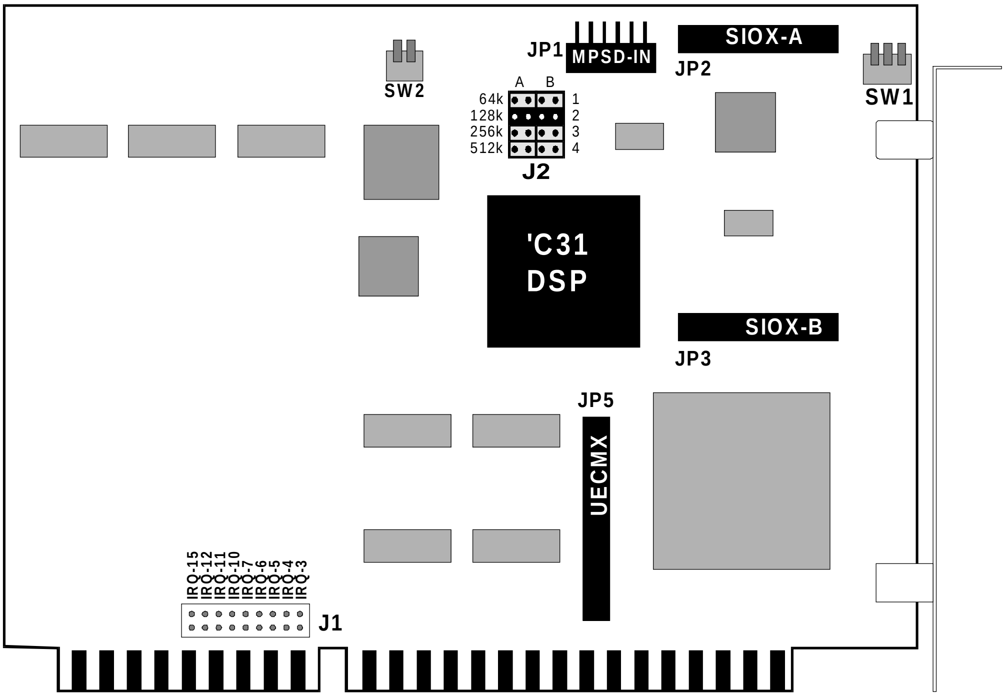


Fig.A-1a. On-board layout for *TORNADO-31*.

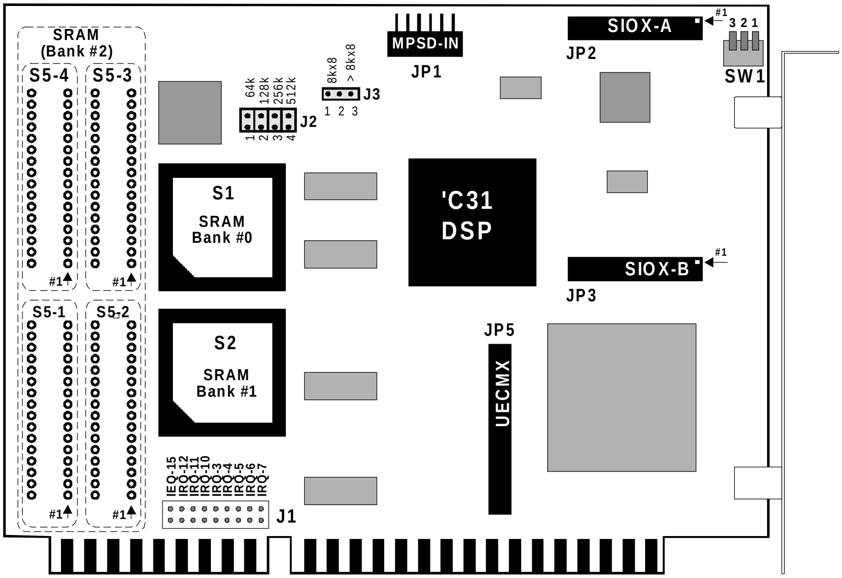


Fig.A-1b. On-board layout for *TORNADO-31Z*.

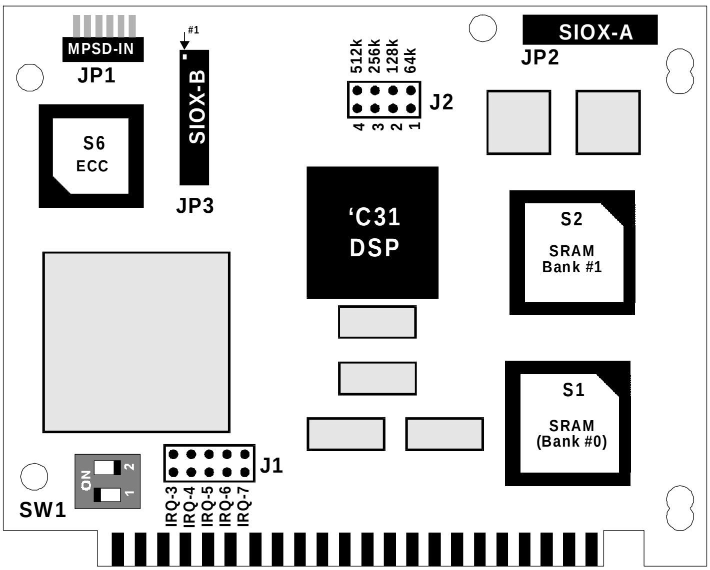


Fig.A-1c. On-board layout for *TORNADO-31M*.

On-board Switches

On-board switches for *TORNADO-31x* DSP systems are summarized in table A-1.

Table A-1. On-board switches for *TORNADO-31x*.

switch #	switch function description	reference information
SW1	ISA -bus I/O base address for host ISA-bus I/O interface.	section 2.5 table 2-5
SW2	PIOX data ready controller operation mode selector (*TORNADO-31* only).	section 2.6 table 2-14

On-board Configuration Jumpers

On-board configuration jumpers for *TORNADO-31x* DSP systems are summarized in table A-2.

Table A-2. On-board configuration jumpers for *TORNADO-31x*.

jumper #	jumper function description	reference information
J1	Host ISA-bus interrupt request line selector.	sections 2.5, 3.2
J2	On-board SRAM banks size selector.	sections 3.5 table 3-1
J3	SRAM/DIP chips type selector (*TORNADO-31Z* only).	section 3.5 table 3-2

On-board Connectors

On-board connectors for *TORNADO-31x* DSP systems are summarized in table A-3.

Table A-3. On-board connectors and headers for *TORNADO-31x*.

connector #	connector function description	reference information
JP1	MPSD-IN connector for connection to external C3x emulator.	section 2.8 fig.2-15, 2-16
JP2 *JP3*	SIOX-A/B expansion interface sites headers.	section 2.7 fig.2-13
JP4	PIOX/PIOX-16 expansion interface site header (*TORNADO-31* only).	section 2.6 fig.2-7, 2-7
JP5	UECMX site header (*TORNADO-31/31Z* only).	sections 2.8 fig.2-15, 2-17, 2-18

On-board Sockets

On-board sockets for *TORNADO-31x* DSP systems are summarized in table A-4.

Table A-4. On-board sockets for *TORNADO-31x*.

socket #	switch function description	reference information
S1 *S2*	PLCC-68 sockets for SRAM/PLCC banks #0 and #1.	section 3.5 fig.3-1, 3-2
S3 *S4*	PLCC-68 sockets for SRAM/PLCC banks #2 and #3 (*TORNADO-31* only).	section 3.5 fig.3-1, 3-2
S5-1 *S5-2* *S5-3* *S5-4*	DIP-28/DIP32 sockets for SRAM/DIP chips for SRAM bank #0 (*TORNADO-31Z* only).	section 3.5 fig.3-3
S6	PLCC-44 socket for *ECC* (*TORNADO-31M* only).	sections 2-8, 3-5; fig.2-19, 2-20, 3-5