MicroLAB Systems

Ultimate DSP Development Solutions

DIGITAL SIGNAL PROCESSING

TORNADO-PX/DDC4

Quad Channel Digital Radio Receiver PIOX-16 Coprocessor/Controller
for *TORNADO* DSP Systems/Controllers

User's Guide

covers:
TORNADO-PX/DDC4 rev.1A

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About this Document

This user's guide contains description for *TORNADO-PX/DDC4* quad channel digital radio receiver (DRR) PIOX-16 Coprocessor and stand-alone controller for *TORNADO* DSP systems/controllers.

This document does not include detail description neither for the on-board components nor for the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C54x. CPU and Peripherals. Reference Guide.*** Texas Instruments Inc, SPRU131D, 1997.
2. ***TMS320VC5410 DSP.*** Texas Instruments Inc, SPRS075, 1999.
3. ***TMS320VC5416 DSP.*** Texas Instruments Inc, SPRS095, 1999.
4. ***TMS320C54x DSP Reference Set. Volume 5: Enhanced Peripherals.*** Texas Instruments Inc, SPRU302, 1999.
5. ***TMS320C5000 DSP Family Functional Overview.*** Texas Instruments Inc, SPRU307, 1999.
6. ***HSP50214 Programmable Down Converter.*** Intersil Inc, 1999.
7. ***PC16552D Dual Universal Asynchronous Receiver/Transmitter with FIFO.*** National Semiconductor Inc, 1995.

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Chapter 1. Introduction

This chapter contains general description for *TORNADO-PX/DDC4* quad-channel digital radio receiver (DRR) PIOX-16 coprocessor/controller.

1.1 General Information

TORNADO-PX/DDC4 is a quad-channel DRR coprocessor PIOX-16 (parallel I/O expansion) daughter-card module (DCM) (fig.1-1) for *TORNADO* DSP systems (*TORNADO-3x/54x/6x/P3x/P6x/etc*) and *TORNADO-E* stand-alone DSP controllers (*TORNADO-E3x/E6x/etc*) from MicroLAB Systems Ltd.

TORNADO-PX/DDC4 can be also used as stand-alone DRR application specific controller with on-board DSP facility and serial communication with host computer.

TORNADO-PX/DDC4 DCM has been designed for multi-channel high-frequency and high-accuracy DRR telecom applications, however it can be used for many other applications with similar signal processing algorithm.

Fig. 1-1. TORNADO-PX/DDC4 DCM.

Installation onto TORNADO DSP System/Controller

TORNADO-PX/DDC4 DCM installs as PIOX-16 DCM (fig.1-2) into the PIOX-16 site onto *TORNADO* DSP system/controller mainboard.

Fig. 1-2. TORNADO-PX/DDC4 DCM installed onto *TORNADO-31* mainboard.

Using TORNADO-PX/DDC4 as Stand-alone Controller

In case *TORNADO-PX/DDC4* DCM is considered to be used as stand-alone multi-channel DRR application specific controller, then PIOX-16 connector is not used and external power must be applied via the dedicated on-board connector. Communication with external host computer can be performed either via RS232 port or via on-chip McBSP serial port of on-board DSP.

Overview

TORNADO-PX/DDC4 DCM features the following main on-board components:

- two 12-bit 65 Msps analog-to-digital converters (ADC)
- ADC streams multiplexer
- four 65 MSPS programmable down converters (PDC)
- bypass FIFO
- set of programmable peripherals
- 100 MIPS (or 160 MIPS) 16-bit fixed-point DSP
- host PIOX-16 interface.

On-board ADC feature 12-bit resolution at up to 65 MHz sampling frequency with excellent linearity, which guarantee minimum signal distortion during sampling of RF inputs. Also, input analog circuits and ADC allow undersampling of input RF signal.

Output ADC streams are routed to four Harris HSP50214 programmable down converters (PDC) and bypass FIFO via programmable ADC streams multiplexer. Four on-board PDC are organized as two groups of two PDC each, with each PDC group sharing common input data stream. Harris HSP50214 PDC is extremely flexible telecom oriented PDC chip, which provides high-resolution tuning and mixing of input digital stream with further decimation, filtering, resampling and demodulation of input digital data. The PDC parallel outputs can be software configured to comprise of different output data. On-board 256 KW high-density bypass FIFO is useful for monitoring and spectral analysis of ADC output data.

PDC parallel output data along with the output of bypass FIFO are available for read by the on-board high performance 16-bit fixed-point 100 MIPS TMS320VC5410 DSP (or 160 MIPS TMS320VC5416 DSP). DSP can be used for processing of PDC real-time output data, reading/analyzing FIFO output data, programming of PDC/FIFO and on-board peripherals, system control, communication via host PIOX-16 interface and for communication with external equipment. On-board DSP environment also includes 128K FLASH memory for stand-alone operation, and 32K dual-port RAM (DPRAM) for data storage and communication with host *TORNADO* DSP system/controller via PIOX-16 interface.

Host PIOX-16 interface provides access to on-board DRPAM, HPI port of on-board DSP, and contains a set of control registers for DSP reset and bootmode control, host interrupt selection, and for error processing.

TORNADO-PX/DDC4 DCM also contains a set of on-board peripherals, which are controlled by the on-board DSP and required for design a complete single-channel programmable DRR system with a minimum of external components. These on-board peripherals comprise of two high-resolution sampling frequency generators, dual UART with RS232C interfaces for external tuner control, two 12-bit DAC for gain control of external RF amplifiers or general purpose analog output, 16-bit audio-DAC for either external phones or general purpose analog output, two external serial links for either digital gain control of external RF amplifiers or general purpose serial digital output, digital I/O, and DSP reset controller with watchdog timer.

TORNADO-PX/DDC4 DCM can be also used as stand-alone multi-channel DRR application specific controller without installation onto host *TORNADO* DSP system/controller. In this case the external power must be applied via the dedicated on-board connector, and on-board DSP is able to boot from the on-board FLASH memory. Communication with external host computer can be performed either via RS232 port or via on-chip McBSP serial port of on-board DSP.

External signal I/O

Connection of *TORNADO-PX/DDC4* DCM to external analog and digital I/O world is performed either via on-board I/O connectors or by means of external I/O board (*T/X-XIOB/DDC4*) (fig.1-3).

T/X-XIOB/DDC4 external I/O board splits *TORNADO-PX/DDC4* on-board I/O connectors into two logical groups (channels) with I/O connector specifications of that for *T/SDAS-DDC1* single-channel DRR SIOX DCM for *TORNADO* DSP systems/controllers. This allows *TORNADO-PX/DDC4* PIOX-16 DCM and *T/SDAS-DDC1* SIOX DCM to use identical cables and options for connection to external equipment.

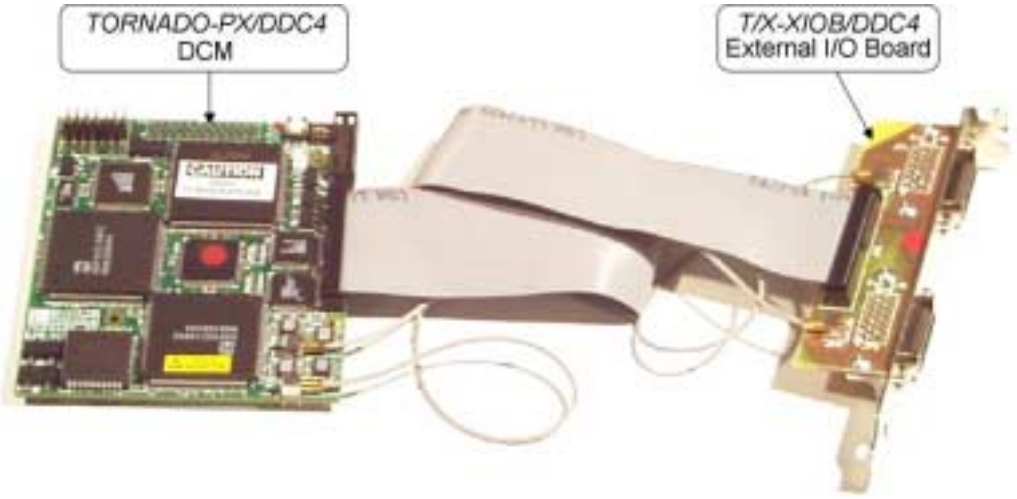


Fig. 1-3. TORNADO-PX/DDC4 DCM and *T/X-XIOB/DDC4* external I/O board.

T/X-XIOB/DDC4 external I/O board installs either to the rear mounting bracket of host *TORNADO* DSP system in case *TORNADO-PX/DDC4* DCM is installed onto *TORNADO* DSP system for PC (fig.1-4), or can install directly at the rear panel of host PC.

Fig. 1-4. TORNADO-PX/DDC4 DCM with *T/X-XIOB/DDC4* external I/O board installed onto *TORNADO-62* PC plug-in DSP system.

External options

TORNADO-PX/DDC4 DCM can be used with several I/O options when connecting to external signal I/O equipment:

- *T/X-DDC1/C* external I/O cable set (fig.1-5 and Appendix C), which provides separate industry standard connectors for RF analog input, analog outputs, RS232C interface and auxiliary I/O (refer to Appendix C for more details)
- *T/X-DDC/AFE-xx* external RF amplifier (fig.1-5), which is optional for *TORNADO-PX/DDC4* DCM.

Fig. 1-5. TORNADO-62 PC plug-in DSP system with *TORNADO-PX/DDC4* DCM, *T/X-XIOB/DDC4* external I/O board, *T/X-DDC1/C* external I/O cable set and *T/X-DDC/AFE-xx* external RF amplifier.

Two *T/X-DDC1/C* external cable sets (Appendix C, fig.1-3) come standard with *TORNADO-PX/DDC4* DCM and provide direct connection to any external RF signal source, external host computer or peripheral via RS232C interface, and auxiliary analog and digital I/O via separate industry-standard connectors. *T/X-DDC1/C* external cable sets connect to *T/X-XIOB/DDC4* external I/O board for *TORNADO-PX/DDC4* DCM.

The *T/X-DDC/AFE-xx* external RF amplifier (fig.1-3) is optional for *TORNADO-PX/DDC4* DCM and provides software programmable gain and factory defined RF signal bandwidth. This option can connect to any of two channels of *T/X-XIOB/DDC4* external I/O board for *TORNADO-PX/DDC4* DCM and is useful in case external RF tuner provides small RF output signal, which is a typical situation with the most industry standard tuners. The *T/X-DDC/AFE-xx* option is available with different bandwidth and gain parameters, and it is also possible to customize the bandwidth and gain parameters of this option in order to meet requirements of customer application (contact MicroLAB Systems for more details). The RS232C interface I/O, analog output and auxiliary I/O are available on separate connectors at the *T/X-DDC/AFE-xx* device package.

Applications

TORNADO-PX/DDC4 DCM has been designed for high-accuracy multi-channel DRR telecommunication applications, as well as for other industrial and general signal processing applications, which assumes similar signal processing and demodulation techniques and meets the frequency specifications of *TORNADO-PX/DDC4* DCM.

1.2 Technical Specification

The following are detail technical specifications for *TORNADO-PX/DDC4* quad DRR coprocessor/controller for *TORNADO* DSP systems/controllers.

CAUTION

Some of on-board components of *TORNADO-PX/DDC4* DCM may appear very hot during operation and can deliver skin sore in case of direct contact.

Although it is generally not required for normal operation of the *TORNADO-PX/DDC4* DCM, it is recommended to provide airflow over *TORNADO-PX/DDC4* DCM board surface by means of optional fan/blower in order to exclude excessive heating of *TORNADO-PX/DDC4* DCM and of the neighbor boards installed into the same chassis compartment.

Parameter description	*parameter value*
RF inputs and ADCs	
number of RF input channels	2
input RF signal range	± (0.5 V ± 30 mV (typ))
input impedance for RF inputs	50 Ohm
input signal bandwidth	5 kHz .. 150 MHz
Resolution	12 bits
SNR (Fs=31MHz)	67 dB (typ)
maximum sampling frequency	65 MHz
input DC bias	± 1 V max
other ADC options	overflow control
ADC streams multiplexer	
number of input streams	2
number of output streams	3
number of data bits in each I/O stream	12
Programmable Down-Converter Chips (PDC)	

number of PDC channels	4
input PDC data streams organization	2x2
PDC type	Intersil HSP50214 PDC
maximum CLKIN sampling frequency (either set by on-board PFG-1/2 or sourced from external XFS-1/2 inputs)	65 MHz
PROCLK frequency	50 MHz
decimation factor	4..16384
build-in hardware demodulators	AM, FM, ASK, FSK ready for PM/PSK
output signal bandwidth	≤ 982 kHz

Bypass ADC data FIFO

FIFO depth	256 KW (256Kx12)
programmable end-of-acquisition condition	PAF/FF

Programmable Sampling Frequency Generators (PFG)

number of PFG channels	2
output frequency range	0.09765 MHz .. 65 MHz
reference clock frequency	10 MHz
Stability of reference clock frequency	± 50 PPM
PLL lock time to within 1% of output frequency	< 200 uS
period jitter	± 40 pS (MSV) ± 120 pS (absolute)

External Sampling Frequency (XFS) inputs

number of XFS inputs	2
maximum XFS frequency	65 MHz
logical input level	3v/5v TTL
input impedance	110 Ohm

general purpose DAC (XDAC)

number of DAC channels	2
resolution	12 bits
software programmable output signal range	0..2.048 VDC 0..4.096 VDC
minimum load resistance	2 kOhm
output settling time	≤ 3.5 uS

phone DAC (PHDAC)

number of phone DAC channels	1
resolution	16 bits
output signal range	± 3 VDC
minimum load resistance	≥ 600 Ohm
output settling time	≤ 3 uS

External Serial Links (XSL)

number of XSL output channels (XSL output frame synchronization pulses)	2
number of output data bits	software selectable from: 8, 16, 24, 30 bits
output serial clock frequency	< 20 MHz
output serial clock features	programmable polarity programmable framing
output signals level	3v/5v TTL
output load current	< 3.2 mA

Dual-channel UART (DUART)

number of UART channels	2
DUART chip	PC16552D from National Semiconductor Inc (each channel is hardware/software compatible with PC COM-port)
external I/O interface	RS232C
source clock frequency	1.8432 MHz

maximum communication speed	115 kBaud
External Digital I/O	
number of programmable digital I/O bits	2 I/O bits with programmable direction
I/O signal level	3v/5v TTL
output load current	< 3.2 mA
Watchdog timer (WDT) and DSP reset controller (RC)	
WDT latency period	1.6 sec typ
duration of external reset input signal	>500 ns
duration of the output DSP reset signal	>0.2 sec
DSP	
DSP type	100 MIPS TMS320VC5410 or 160 MIPS TMS320VC5416
FLASH memory	
FLASH memory capacity	128Kx8
FLASH memory options	on-board write protection
Host PIOX-16 Interface	
number of occupied I/O ports	65K=65,536 (2^{16}) organized as 32K DPRAM area and 32K I/O ports
dual-port RAM (DPRAM) capacity	32Kx16
dual-port semaphores (DPSEM)	8
DPRAM options	Host-to-DSP and DSP-to-Host interrupt generation
PIOX-16 interrupt request inputs	software selectable from IRQ-0, XIRQ-1, XIRQ-2
I/O ports	control registers, DSP HPI port
access time	< 20 ns (control register access) < 31ns..140ns (HPI access) < 36 ns (DPRAM/DPSEM access)
physical and power:	

dimensions	65 mm (2.55") x 85 mm (3.34")
power consumption via host PIOX I/F	+5v @ 1.5 A +12v @ 0.43 A -12v @ 0.1 A
external operating temperature	0°C .. +55°C
recommended fan/blower airflow	>0.2 m^3/min

Chapter 2. System Architecture and Construction

This chapter contains detail technical description for architecture and construction of *TORNADO-PX/DDC4* PIOX-16 coprocessor/controller.

2.1 System Architecture

System architecture and construction for *TORNADO-PX/DDC4* PIOX-16 coprocessor/controller are presented at fig.2-1 and fig.2-1.

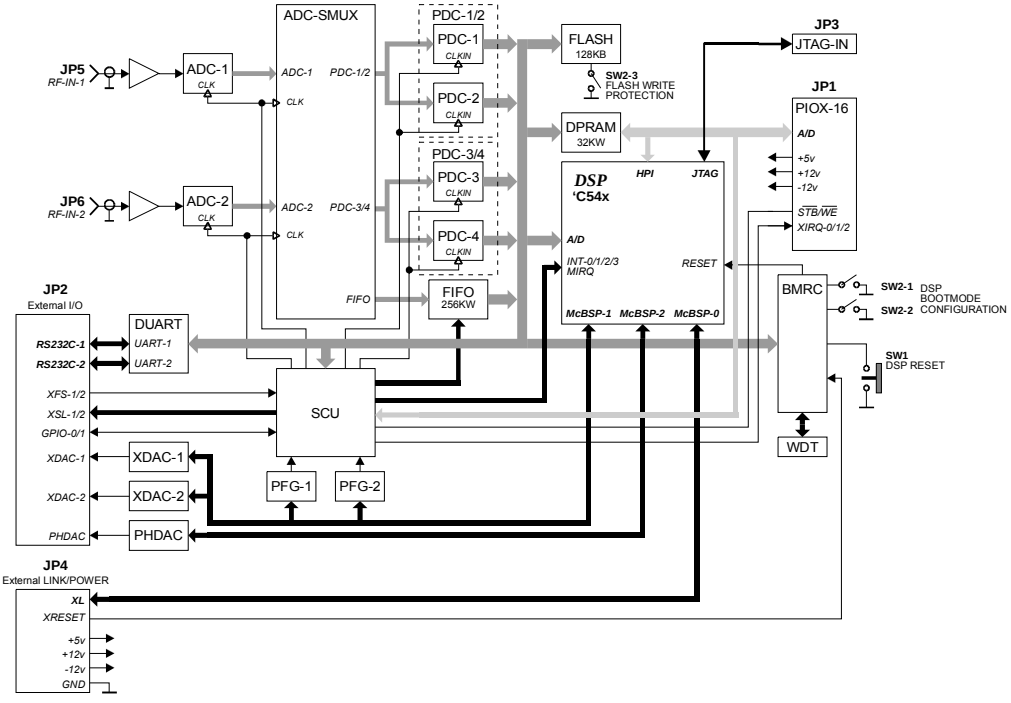


Fig.2-1. Block diagram of *TORNADO-PX/DDC4* DCM.

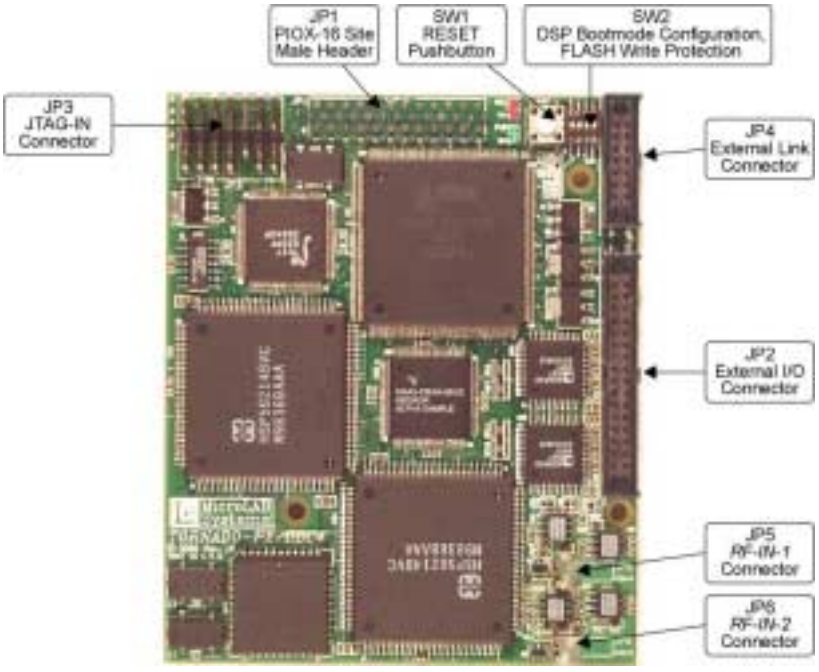


Fig.2-2. Construction of *TORNADO-PX/DDC4* DCM.

TORNADO-PX/DDC4 can either install as PIOX-16 DCM onto host *TORNADO* DSP system/controller, or can be used as stand-alone application specific controller.

TORNADO-PX/DDC4 DCM comprises of the following components:

- RF analog input section, which includes two 12-bit 65 Msps ADCs (ADC-1..2) and two RF input amplifiers with RF input connectors (JP5 and JP6)
- programmable 2:3 ADC streams multiplexer (ADC-SMUX)
- four 65 MSPS Intersil HSP50214 PDC chips (PDC-1..4)
- two programmable sampling frequency generators (PFG-1..2)
- 256 KW bypass FIFO
- either 100 MIPS TMS320VC5410 DSP or 160 MIPS TMS320VC5416 DSP
- 128 KB FLASH memory with on-board write protection feature
- analog output section, which comprises of two 12-bit 300ksps DAC (XDAC-1..2) for either gain control of external RF amplifiers or general purpose analog outputs, and of 16-bit 300ksps phone DAC (PH-DAC) for either audio monitoring or general purpose analog output
- two programmable external serial output links (XSL-1..2) for either digital gain control of external RF amplifier or general purpose serial output
- dual-channel 115 kBaud UART (DUART with UART-1..2 channels) with RS232C interfaces for either external tuner control, or for communication with host computer and external peripherals via the industry standard asynchronous serial protocol
- 2-bit general purpose programmable digital I/O (GPIO-0..1)

- DSP bootmode and reset controller (BMRC) with watch-dog timer (WDT), DSP reset pushbutton (SW1) and DSP bootmode configuration switch (SW2)
- 32 KW dual-port RAM (DPRAM) with 8 dual-port semaphores (DPSEM) and bi-directional interrupt generation
- synchronization and control unit (SCU)
- DSP JTAG-IN connector (JP3) for connection to external MPSD/JTAG emulator
- external I/O connector (JP2)
- external link and power connector (JP4)
- host PIOX-16 interface header (JP1) for installation onto *TORNADO* DSP systems/controllers.

ADC and RF input amplifiers

TORNADO-PX/DDC4 DCM provides two on-board RF analog input channels each comprising of RF input amplifier and ADC.

RF input amplifiers connect to external analog world via mini-coax on-board JP5 and JP6 connectors, and provide 50 Ohm input impedance and wide signal-pass bandwidth.

On-board ADC feature 12-bit resolution at up to 65 MHz sampling frequency and excellent linearity, which guarantee minimum signal distortions during conversion of RF input signal. ADC allow undersampling of RF input signals. ADC sampling frequency can be individually configured by on-board DSP software to come from any of two on-board programmable sampling frequency generators (PFG-1 and PFG-2) or from any of two external sampling frequency inputs (XFS-1 and XFS-2).

On-board hardware also provides real-time overflow control for each ADC in order to guarantee that no distortions have been occurred during A/D conversion of RF input signal and that the signal processing inside PDC is performed properly. Overflow flags can generate interrupts to DSP and are also available for software polling.

For more details about ADC refer to section “RF Signal Processing” later in this chapter.

ADC streams multiplexer (ADC-SMUX)

Each of two ADC output data streams can be routed to the input data streams for two PDC sets (PDC-1/2 and PDC-3/4) chips and bypass FIFO via programmable ADC streams multiplexer (ADC-SMUX). ADC-SMUX is controlled by DSP software and delivers outstanding flexibility for run-time configuring of RF digital signal processing paths.

For more details about ADC-SMUX refer to section “RF Signal Processing Control” later in this chapter.

PDC

On-board PDC pool comprises of four Intersil HSP50214 PDC chips, which provide digital down conversion of high-bandwidth parallel ADC output stream to the low-band PDC output data stream. PDC output data can be read and processed by on-board DSP. Each PDC chip provides one DRR signal processing channel.

Intersil HSP50214 PDC chip is the industry most flexible and powerful 16-bit 65 Msps PDC chip, which is oriented for telecommunication applications. It features on-chip digital mixer/NCO, digital filters/decimators, resampler, automatic digital gain control, and output digital demodulator. It provides up to 16384 decimation factor, built-in AM/FM/ASK/FSK demodulator (ready for PH/PSK demodulation), and programmable output data in order to meet requirements of different telecommunication applications. NCO, mixer, filter and

decimator parameters along with 16-bit output data selectors of Intersil HSP50214 PDC chips can be programmed by the on-board DSP.

On-board PDC pool is organized as two sets of two PDC chips each (PDC-1/2 and PDC-3/4). Both PDC chips within one PDC set share common 12-bit input data stream, which is the ADC output data stream coming out from the corresponding output of ADC-SMUX.

For more details about PDC refer to section "RF Signal Processing Control" later in this chapter.

Bypass FIFO

On-board 256 KW (256Kx12) high-density bypass FIFO can be used for monitoring and spectral analysis of ADC output data. 12-bit input data stream for bypass FIFO is the ADC output data stream coming out from the FIFO output of ADC-SMUX.

Bypass FIFO can acquire any programmable number of ADC output data samples, whereas on-board DSP software must read and analyze FIFO data in order to detect 'active' sub-bands within the full input signal bandwidth and to tune PDC to particular active sub-band.

For more details about bypass FIFO refer to section "RF Signal Processing Control" later in this chapter.

sampling frequency generators (PFG-1 and PFG-2)

TORNADO-PX/DDC4 DCM provides two programmable sampling frequency generators (PFG-1 and PFG-2). Each PFG allows accurate setting of virtually any sampling frequency value for the on-board ADC-PDC and ADC-FIFO paths within the 97 kHz .. 65 MHz frequency range. The sampling frequency, which value is out of this frequency range, must be supplied from external sampling frequency inputs (XFS-1 and XFS-2).

For more details about PFG-1 and PFG-2 programmable sampling frequency generators refer to section "Serial Peripherals" later in this chapter.

TMS320C54x DSP

On-board DSP is 16-bit fixed-point high-performance either 100 MIPS TMS320VC5410 DSP or 160 MIPS TMS320VC5416 DSP with large on-chip memory (64 KW for TMS320VC5410 DSP and 128 KW for TS320VC5416 DSP), six programmable DMA channels, three multi-channel buffered serial ports (McBSP), and HPI port.

On-board DSP can be used to process of PDC real-time output data, to read and analyze of FIFO output data, to program PDC/FIFO and on-board peripherals, for system control, for communication with host DSP of host *TORNADO* DSP system/controller, and for communication with external equipment.

On-board DSP environment also includes 128K FLASH memory for stand-alone operation and 32K dual-port RAM (DPRAM) for data storage and communication with host *TORNADO* DSP system/controller via PIOX-16 interface.

On-board TMS320C54x DSP can run either in stand-alone or host mode under control of host *TORNADO* DSP system/controller via host PIOX-16 interface. When running in stand-alone mode, DSP can start either in the 'microprocessor' mode without boot (used for DSP software debugging), or boot from the on-board FLASH memory. When *TORNADO-PX/DDC4* DCM is installed onto host *TORNADO* DSP system/controller and is running in host mode, then DSP can start either in either in the 'microprocessor' mode without boot (used for DSP software debugging), or boot from either HPI port or from on-board FLASH memory.

For more details about on-board DSP refer to section “DSP Environment” later in this chapter.

FLASH

TORNADO-PX/DDC4 provides 128Kx8 of on-board FLASH memory for boot code and/or for non-volatile data. On-board FLASH memory has multi-page 4x32K organization in order to fit external data memory area of on-board TMS320C54x DSP. Also provided is the on-board write protection facility in order to ensure data safety and integrity for FLASH contents in case the FLASH data shall not be altered.

For more details about on-board DSP refer to sections “DSP Environment” later in this chapter and Appendix D “FLASH Memory Programming”.

DPRAM

TORNADO-PX/DDC4 provides 32K dual-port RAM (DPRAM) for data storage and communication with host *TORNADO* DSP system/controller via PIOX-16 interface.

On-board DPRAM extends memory environment of on-board DSP, and allows quick random access to shared data from host *TORNADO* DSP system/controller via PIOX-16 interface (DSP on-chip HPI port requires preliminary address load prior accessing actual data), which is required for high-performance communication and synchronization between DSP and host *TORNADO* DSP system/controller environment.

DPRAM can also generate DSP-to-HOST and HOST-to-DSP interrupts, and includes eight dual-port semaphores for software synchronization between DSP and host *TORNADO* DSP system/controller when accessing shared resources.

For more details about on-board DSP refer to section “DSP Environment” later in this chapter.

Dual-channel UART with RS232C interface

On-board dual-channel universal asynchronous receiver/transceiver (DUART) with RS232C interface has been designed for external RF tuner control, interfacing to general purpose peripherals or for communication with host computer using industry standard asynchronous protocol and RS232C interface. Most of the industry standard RF tuners (AOR, ICOM, etc), which can be used with the *TORNADO-PX/DDC4* DCM, provide RS232C input port for remote control.

On-board DUART is based around the industry standard PC16552D chip from National Semiconductor Corp. Each DUART channel (UART-1 and UART-2) is hardware compatible with PC COM port and can communicate at up to 115 kBaud via RS232C interfaces, which are available at JP2 external I/O connector. The DUART is sourced by 1.8432 MHz clock, which allows communication at all industry standard baud rates up to 115 kBaud.

For more details about DUART refer to section “DSP Environment” later in this chapter.

Analog output section

Analog output section of *TORNADO-PX/DDC4* DCM comprises of two 12-bit 300ksps digital-to-analog converters (XDAC-1 and XDAC-2) for either gain control of external RF amplifiers or general purpose analog outputs, and of 16-bit 300ksps phone DAC (PHDAC) for either audio monitoring or general purpose analog output. XDAC-1, XDAC-2 and PHDAC outputs are DC coupled and are available at JP2 external I/O connector.

For more details about XDAC-1, XDAC-2 and PHDAC peripherals refer to section "Serial Peripherals" later in this chapter.

External serial links (XSL)

External programmable serial links (XSL-1 and XSL-2) of *TORNADO-PX/DDC4* DCM are provided for digital gain control of external RF amplifiers, however they can be also used for general purpose serial data output. XSL-1/2 output signals are available at JP2 external I/O connector.

XSL feature programmable data format (8/16/24/30 data bits), programmable serial clock polarity, and programmable serial clock framing feature.

For more details about XSL-1 and XSLC-2 peripherals refer to section "Serial Peripherals" later in this chapter.

Programmable general purpose I/O

TORNADO-PX/DDC4 provides two programmable general purpose I/O bits (GPIO-0 and GPIO-1), which are available at JP2 external I/O connector. GPIO-0/1 I/O pins are 3v/5v TTL compatible and can be used as general purpose I/O for control and interfacing to external peripherals.

Direction and input/output data for GPIO-0/1 pins are programmable by the on-board DSP. Active low condition at GPIO-0/1 I/O pins can also generate interrupt requests to the on-board DSP.

For more details about GPIO refer to section "DSP Environment" later in this chapter.

Host PIOX-16 interface

Host 16-bit PIOX-16 interface (JP1 connector) provides access to on-board DRPAM, DSP on-chip HPI port, and contains a set of control registers for DSP reset and bootmode control, host interrupt selection, and for error processing.

For more details about host PIOX-16 interface refer to section "Host PIOX-16 Interface" later in this chapter.

DSP Bootmode and Reset Controller (BMRC)

The DSP reset and bootmode control are provided by *TORNADO-PX/DDC4* on-board DSP bootmode and reset controller (BMRC). BMRC is controlled by on-board SW2 configuration switch, SW1 reset pushbutton, watch-dog time, *XRESET* signal from JP4 external link/power connector, and by host *TORNADO* DSP system/controller via host PIOX-16 interface.

The DSP reset signal can be either controlled by host *TORNADO* DSP system/controller in case *TORNADO-PX/DDC4* DCM is running in host PIOX-16 mode, or is generated on-board in case DSP is running in stand-alone mode.

Watchdog timer (WDT)

TORNADO-PX/DDC4 features on-board watch-dog timer (WDT) in order to increase reliability of DSP operation in stand-alone operation. In case DSP is running in stand-alone mode with the WDT feature enabled, and while the DSP is operating properly, it should perform reset of WDT every 1.6 sec, otherwise the WDT will generate the DSP reset signal and will restart *TORNADO-PX/DDC4*.

Stand-alone operation

TORNADO-PX/DDC4 DCM has been designed with support for stand-alone operation also, which is required for embedded applications.

In stand-alone operation, on-board DSP can boot from the on-board FLASH memory and can communicate with external world either via on-board DUART with RS232C interfaces, or via DSP on-chip McBSP-0 port, which is available via JP4 external link/power connector. Host PIOX-16 interface is switched off during stand-alone operation.

The external power and external DSP reset signal (*XRESET*) for stand-alone operation can be applied either via the power pins of host PIOX-16 interface, or via the power pins of JP4 external link/power connector.

For more details about stand-alone operation and JP4 connector specifications refer to section "DSP Environment" later in this chapter and to Appendix A.

Debugging TMS320C54x DSP software

On-board TMS320C54x DSP software for *TORNADO-PX/DDC4* can be developed and debugged using either TI XDS510 or MicroLAB' *MIRAGE-510DX* scan-path emulators via on-board JTAG-IN connector (JP3) and using TI C5000 Code Composer Studio IDE.

2.2 DSP Environment

TORNADO-PX/DDC4 DCM on-board DSP environment is based around the TMS320C54x high-performance 16-bit fixed point DSP from TI, which must be used for processing of PDC real-time output data, reading and analyzing FIFO output data, programming PDC/FIFO and on-board peripherals, system control, for communication with host DSP of host *TORNADO* DSP system/controller, and for communication with external equipment.

DSP

TORNADO-PX/DDC4 DCM has been designed to utilize any of following 16-bit high-performance TMS320C54x fixed-point DSP from TI:

- 100 MIPS TMS320VC5410 DSP
- 160 MIPS TMS320VC5416 DSP.

Each of the above DSP features large on-chip memory (64 KW for TMS320VC5410 DSP and 128 KW for TS320VC5416 DSP), six programmable DMA channels, three multi-channel buffered serial ports (McBSP), and on-chip HPI port.

CAUTION

This manual does not contain description and programming details
for on-board TI TMS320C54x DSP.

For more information refer to original TI datasheets and user's guides for TMS320C54x DSP,
which are supplied in either paper or electronic form together with this manual.

DSP bootmode configurations and reset control

The DSP bootmode configuration is defined by on-board SW2 switch (fig.2-1 and A-1) and by bits {*BMODE-1, BMODE-0*}of *HOST_CNTR2_RG* register (refer to section "Host PIOX-16 Interface" later in this chapter) from host *TORNADO* DSP system/controller via host PIOX-16 interface.

The DSP reset signal source is defined by current DSP bootmode configuration and is controlled by on-board SW1 reset pushbutton (fig.2-1 and A-1), by *XRESET* signal from on-board JP4 external link/power connector, by on-board WDT expiration event (in case the WDT feature is enabled), and by *M_GO* bit of *HOST_CNTR1_RG* register (refer to section "Host PIOX-16 Interface" later in this chapter) from host *TORNADO* DSP system/controller via host PIOX-16 interface.

Refer to table 2-1 for the summary of DSP bootmode configurations and for the DSP reset conditions.

Table 2-1. DSP Bootmode Configurations.

SW2 on-board switch		***HOST_CNTR2_RG* register bits of host PIOX-16 interface**		**bootmode**	**description**
SW2-1	**SW2-2**	***BMODE-1***	***BMODE-0***		
ON	ON	X	x	*SA/NO-BMODE*	*Corresponds to DSP stand-alone operation with Microprocessor (MP) start-up mode without boot process. DSP reset is controlled by on-board SW1 reset pushbutton, XRESET signal from JP4 external link/power connector, and WDT expiration event in case WDT feature is enabled via DSP_WDT_EN_RG register.* *After DSP reset will be released, DSP will fetch the reset vector from address FF80H of program RAM, which is mapped to DPRAM.*
ON	OFF	X	x	*SA/FLASH8-BMODE*	*Corresponds to DSP stand-alone operation with Microcontroller (MC) start-up mode and boot from the on-board 8-bit FLASH page #0 starting at DSP data memory address 8000H. DSP reset is controlled by on-board SW1 reset pushbutton, XRESET signal from JP4 external link/power connector, and WDT expiration event in case WDT feature is enabled via DSP_WDT_EN_RG register.*
OFF	x	0	0	*HOST/NO-BMODE*	*Corresponds to DSP host operation with Microprocessor (MP) start-up mode without boot process. DSP reset is controlled by M_GO bit of HOST_CNTR1_RG register of host PIOX-16 interface.* *After DSP reset will be released, DSP will fetch the reset vector from address FF80H of program RAM, which is mapped to DPRAM.*
OFF	x	0	1	*HOST/FLASH8-BMODE*	*Corresponds to DSP host operation with Microcontroller (MC) start-up mode and boot from the on-board 8-bit FLASH page #0 starting at DSP data memory address 8000H. DSP reset is controlled by M_GO bit of HOST_CNTR1_RG register of host PIOX-16 interface.*
OFF	x	1	0	*HOST/HPI-BMODE*	*Corresponds to DSP host operation with Microcontroller (MC) start-up mode and boot from the DSP on-chip HPI port. DSP reset is controlled by M_GO bit of HOST_CNTR1_RG register of host PIOX-16 interface.* *After DSP reset will be released, DSP will begin execution from address 1000H of DSP on-chip RAM.*
OFF	x	1	1	-	*Reserved. Do not use.*

Note: 1. Highlighted configuration corresponds to the factory setting.

On-board TMS320C54x DSP can run either in *stand-alone* or *host* operation mode under control of host *TORNADO* DSP system/controller via host PIOX-16 interface.

When running in *stand-alone* operation mode, activity of host PIOX-16 interface is ignored, and DSP bootmode is defined by on-board SW2 configuration switch. In stand-alone mode the DSP power can be applied either via the power pins of host PIOX-16 interface, or via on-board JP4 external link/power connector. In stand-alone mode DSP reset signal is controlled by on-board SW1 DSP reset pushbutton, by *XRESET* signal of on-board JP4 external link/power connector, and by the WDT expiration event in case the WDT feature is enable by DSP software.

When running in *host* operation mode, the DSP bootmode and DSP reset signal are controlled by host *TORNADO* DSP system/controller via control registers of host PIOX-16 interface.

The *SA/NO-BMODE* bootmode configuration corresponds to stand-alone operation mode of on-board DSP with microprocessor (MC) start-up mode without boot process. DSP reset vector mapped to FF80H address of the DSP external program memory, which is mapped to the on-board dual-port RAM memory area.

The *SA/FLASH8-BMODE* DSP bootmode configuration corresponds to stand-alone operation mode of on-board DSP with microcontroller (MC) start-up mode and boot from the on-board 8-bit FLASH page #0 starting at the DSP data memory address 8000H. The contents of FLASH must meet the format of the TMS320C54x DSP on-chip ROM bootloader for 8-bit external ROM.

CAUTION

The application boot code must be allocated into the FLASH page #0, since this is the FLASH page, which is selected automatically during FLASH boot procedure.

In case the boot code exceeds the FLASH memory page limits (32KB), then the application must provide the start-up kernel of boot code at FLASH page #0, which will be run after the boot of FLASH page #0 completes. This start-up kernel must load FLASH pages #1..#3 into the DSP on-chip memory depending upon the customer application.

The *HOST/NO-BMODE* bootmode configuration corresponds to host operation mode of on-board DSP with microprocessor start-up mode without boot process. DSP reset vector mapped to FF80H address of the DSP external program memory, which is mapped to the on-board dual-port RAM memory area.

The *HOST/FLASH8-BMODE* DSP bootmode configuration corresponds to host operation mode of on-board DSP with microcontroller start-up mode and boot from the on-board 8-bit FLASH page #0 starting at the DSP data memory address 8000H. The contents of FLASH must meet the format of the TMS320C54x DSP on-chip ROM bootloader for 8-bit external ROM.

The *HOST/HPI-BMODE* DSP bootmode configuration corresponds to host operation mode of on-board DSP with microcontroller start-up mode and boot via DSP on-chip HPI port. Host *TORNADO* DSP system/controller must load code to the DSP on-chip memory while holding DSP in the reset state. After the DSP reset will be released, DSP will begin program execution from the 1000H on-chip memory address.

DSP memory and I/O map

TORNADO-PX/DDC4 on-board TMS320C54x DSP address area comprises of program, data and I/O areas. Note, that the DSP on-chip memory capacity depends upon the particular DSP chip type installed. Table 2-2 specifies the DSP memory and I/O maps.

Table 2-2. DSP memory and I/O map.

address area of TMS320C54x DSP	value on DSP RESET	access mode	address range (in 16-bit words)	access wait states
DSP on-chip PROGRAM memory *(refer to TMS320VC5410/VC5416 DSP datasheets for more details)*	-	r/w	0000H...7FFFH @PROG (OVLY=1) 18000H...1FFFFH @PROG (all MC-modes) 28000H...2FFFFH 38000H...3FFFFH @PROG (all MC-modes, TMS320VC5416 only)	0ws
external PROGRAM memory *(refer to TMS320VC5410/VC5416 DSP datasheets for more details)*	-	r/w	8000H...FFFFH @PROG (all MP bootmodes) 8000H...BFFFH @PROG (all MC bootmodes)	2ws (mapped to on-board DPRAM)
DSP on-chip DATA memory *(refer to TMS320VC5410/VC5416 DSP datasheets for more details)*	-	r/w	0000H...7FFFH @DATA 8000H...F7FFFH @DATA (DROM=1)	0ws
external DATA memory *(refer to TMS320VC5410/VC5416 DSP datasheets for more details)*	-	r/w	8000H...FFFFH @DATA (DROM=0) (bits D0..D7 for FLASH) (bits D0..D15 for DPRAM)	(2ws+*DP_RDY*) (DPRAM) 5ws (FLASH) (mapped to either DPRAM or FLASH depending upon the *XDM_SEL* bit of *DSP_XDMP_RG* register)
external DATA memory (DPRAM): *DSP_DPRAM_HM_RQ* *(Host-to-DSP interrupt request via DPRAM* in case DPRAM is selected via *XDM_SEL* bit of *DSP_XDMP_RG)*	-	r/w	FFFFH @DATA (DROM=0)	(2ws+*DP_RDY*) (mapped to DPRAM)

external DATA memory (DPRAM): *DSP_DPRAM_MH_RQ* *(DSP-to-Host interrupt request via DPRAM* in case DPRAM is selected via *XDM_SEL* bit of *DSP_XDMP_RG)*	-	r/w	FFFEH @DATA (DROM=0)	(2ws+*DP_RDY*) (mapped to DPRAM)
I/O area: UART channel #2 register set (refer to DUART user's guide) *DSP_UART2_RDATA_RG* *DSP_UART2_TDATA_RG* *DSP_UART2_DIVL_RG* *DSP_UART2_IE_RG* *DSP_UART2_DIVH_RG* *DSP_UART2_FIFOCNTR_RG* *DSP_UART2_IID_RG* *DSP_UART2_ALTFUNC_RG* *DSP_UART2_LCNTR_RG* *DSP_UART2_MCNTR_RG* *DSP_UART2_LSTAT_RG* *DSP_UART2_MSTAT_RG* *DSP_UART2_SCRATCH_RG*	-	r/w	0000H..0007H @I/O (bits D0..D7 only) 0000H@I/O 0000H@I/O 0000H@I/O 0001H@I/O 0001H@I/O 0002H@I/O 0002H@I/O 0002H@I/O 0003H@I/O 0004H@I/O 0005H@I/O 0006H@I/O 0007H@I/O	3ws
I/O area: UART channel #1 register set (refer to DUART user's guide) *DSP_UART1_RDATA_RG* *DSP_UART1_TDATA_RG* *DSP_UART1_DIVL_RG* *DSP_UART1_IE_RG* *DSP_UART1_DIVH_RG* *DSP_UART1_FIFOCNTR_RG* *DSP_UART1_IID_RG* *DSP_UART1_ALTFUNC_RG* *DSP_UART1_LCNTR_RG* *DSP_UART1_MCNTR_RG* *DSP_UART1_LSTAT_RG* *DSP_UART1_MSTAT_RG* *DSP_UART1_SCRATCH_RG*	-	r/w	0008H..000FH @I/O (bits D0..D7 only) 0008H@I/O 0008H@I/O 0008H@I/O 0009H@I/O 0009H@I/O 000AH@I/O 000AH@I/O 000AH@I/O 000BH@I/O 000CH@I/O 000DH@I/O 000EH@I/O 000FH@I/O	3ws
I/O area: *DSP_DPSEM0_RG* .. *DSP_DPSEM7_RG* (DPSEM dual-port semaphores)	-	r/w	0010H..0017H @I/O (bit D0 only)	2ws
I/O area: *DSP_FIFO_DATA_RG* register (bypass FIFO read data and FIFO serial-in data)	-	r/w	003CH @I/O (r: D0..D11 only w: D0 only))	2ws
I/O area: *DSP_FIFO_RES_RG* register (FIFO reset)	-	w	003DH @I/O (data ignored)	2ws

I/O area: *DSP_WDT_RES_RG* register (WDT reset)	-	w	003EH @I/O (data ignored)	2ws
I/O area: *DSP_CLR_ADC_OVF_RG* register (clear ADC overflow flags)	-	w	003FH @I/O (data ignored)	2ws
I/O area: PDC-1 microprocessor port (refer to HSP50214 PDC user's guide) *DSP_PDC1_HLD0_RG* *DSP_PDC1_HLD1_RG* *DSP_PDC1_HLD2_RG* *DSP_PDC1_HLD3_RG* *DSP_PDC1_WRADDR_RG* *DSP_PDC1_RDARRD_RG*	-	r/w	0040H..0047H @I/O (bits D0..D7 only) 0040H@I/O 0041H@I/O 0042H@I/O 0043H@I/O 0044H@I/O 0045H@I/O	2ws
I/O area: PDC-2 microprocessor port (refer to HSP50214 PDC user's guide) *DSP_PDC2_HLD0_RG* *DSP_PDC2_HLD1_RG* *DSP_PDC2_HLD2_RG* *DSP_PDC2_HLD3_RG* *DSP_PDC2_WRADDR_RG* *DSP_PDC2_RDARRD_RG*	-	r/w	0048H..004FH @I/O (bits D0..D7 only) 0048H@I/O 0049H@I/O 004AH@I/O 004BH@I/O 004CH@I/O 004DH@I/O	2ws
I/O area: PDC-3 microprocessor port (refer to HSP50214 PDC user's guide) *DSP_PDC3_HLD0_RG* *DSP_PDC3_HLD1_RG* *DSP_PDC3_HLD2_RG* *DSP_PDC3_HLD3_RG* *DSP_PDC3_WRADDR_RG* *DSP_PDC3_RDARRD_RG*	-	r/w	0050H..0057H @I/O (bits D0..D7 only) 0050H@I/O 0051H@I/O 0052H@I/O 0053H@I/O 0054H@I/O 0055H@I/O	2ws
I/O area: PDC-4 microprocessor port (refer to HSP50214 PDC user's guide) *DSP_PDC4_HLD0_RG* *DSP_PDC4_HLD1_RG* *DSP_PDC4_HLD2_RG* *DSP_PDC4_HLD3_RG* *DSP_PDC4_WRADDR_RG* *DSP_PDC4_RDARRD_RG*	-	r/w	0058H..005FH @I/O (bits D0..D7 only) 0058H@I/O 0059H@I/O 005AH@I/O 005BH@I/O 005CH@I/O 005DH@I/O	2ws
I/O area: *DSP_PDC1_AOUT0_RG..* *DSP_PDC1_AOUT7_RG* registers (PDC-1 AOUT-0..7 ports; refer to HSP50214 PDC user's guide)	-	r	0080H..0087H @I/O	2ws

I/O area: *DSP_PDC1_BOUT0_RG..* *DSP_PDC1_BOUT7_RG* registers (PDC-1 BOUT-0..7 ports; refer to HSP50214 PDC user's guide)	-	r	0088H..008FH @I/O	2ws
I/O area: *DSP_PDC2_AOUT0_RG..* *DSP_PDC2_AOUT7_RG* registers (PDC-2 AOUT-0..7 ports; refer to HSP50214 PDC user's guide)	-	r	0090H..0097H @I/O	2ws
I/O area: *DSP_PDC2_BOUT0_RG..* *DSP_PDC2_BOUT7_RG* registers (PDC-2 BOUT-0..7 ports; refer to HSP50214 PDC user's guide)	-	r	0098H..009FH @I/O	2ws
I/O area: *DSP_PDC3_AOUT0_RG..* *DSP_PDC3_AOUT7_RG* registers (PDC-3 AOUT-0..7 ports; refer to HSP50214 PDC user's guide)	-	r	00A0H..00A7H @I/O	2ws
I/O area: *DSP_PDC3_BOUT0_RG..* *DSP_PDC3_BOUT7_RG* registers (PDC-3 BOUT-0..7 ports; refer to HSP50214 PDC user's guide)	-	r	00A8H..00AFH @I/O	2ws
I/O area: *DSP_PDC4_AOUT0_RG..* *DSP_PDC4_AOUT7_RG* registers (PDC-4 AOUT-0..7 ports; refer to HSP50214 PDC user's guide)	-	r	00B0H..00B7H @I/O	2ws
I/O area: *DSP_PDC4_BOUT0_RG..* *DSP_PDC4_BOUT7_RG* registers (PDC-4 BOUT-0..7 ports; refer to HSP50214 PDC user's guide)	-	r	00B8H..00BFH @I/O	2ws
I/O area: *DSP_FIFO_CNTR_RG* register (bypass FIFO control)	01H (FIFO DAQ mode)	r/w	00C8H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_ADC_CLKSEL_RG* register (ADC clock selectors)	00H (PFG-1 is selected for ADC-1/2)	r/w	00CAH @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_PDC_FIFO_ISEL_RG* register (PDC and bypass FIFO input stream selectors)	00H (ADC-1 output stream is selected as input stream for PDC-1/2/3/4 and bypass FIFO)	r/w	00CBH @I/O (bits D0..D7 only)	2ws

I/O area: *DSP_ADC_FIFO_STAT_RG* register (ADC/FIFO status)	-	r	00CCH @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_PDC_STAT_RG* register (PDC status)	-	r	00CDH @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_MIRQ0_SEL_RG* register (DSP INT-0 source selector)	00H (no interrupt source)	r/w	00D0H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_MIRQ1_SEL_RG* register (DSP INT-1 source selector)	00H (no interrupt source)	r/w	00D1H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_MIRQ2_SEL_RG* register (DSP INT-2 source selector)	00H (no interrupt source)	r/w	00D2H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_MIRQ3_SEL_RG* register (DSP INT-3 source selector)	00H (no interrupt source)	r/w	00D3H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_MNMI_SEL_RG* register (DSP NMI source selector)	00H (no interrupt source)	r/w	00D4H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_AUX_IRQ_STAT_RG* register (auxiliary interrupt status)	-	r	00D8H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_XDMP_RG* register (external data memory page selector)	00H for *SA/NO-BMODE* *HOST/NO-BMODE* *HOST/HPI-BMODE* bootmodes (DPRAM is selected) 80H for *SA/FLASH8-BMODE* *HOST/FLASH8-BMODE* bootmodes (FLASH page#0 is selected)	r/w	00E0H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_GPIO_DATA_RG* register (general purpose I/O data)	00H	r/w	00E2H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_GPIO_DIR_RG* register (general purpose I/O direction control)	00H (*GPIO-0/1* are configured as inputs)	r/w	00E3H @I/O (bits D0..D7 only)	2ws

I/O area: *DSP_WDT_EN_RG* register (WDT enable control)	00H (WDT is disabled)	r/w	00E4H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_XSL_FMT_RG* register (external serial links format)	20H (XSL clock framing, 8 data bits, positive clock polarity)	r/w	00E6H @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_SYS_STAT_RG* register (DSP boot status)	-	r	00EEH @I/O (bits D0..D7 only)	2ws
I/O area: *DSP_BRS_RG* register (BRS LSB for DSP on-chip bootloader)	81H (boot from FLASH8 at 8000H address)	r	FFFFH @I/O (bits D0..D7 only)	2ws

Notes:
1. @PROG denotes PROGRAM memory DSP area; @DATA denotes DATA memory DSP area, @IO denotes I/O DSP area.
2. The DROM bit of DSP on-chip PMST register must be set to DROM=0 value (default value on DSP reset) in order to enable access to on-board DPRAM/FLASH memory.
3. The OVLY bit of DSP on-chip PMST register must be set to OVLY=1 value in order to allocate PROGRAM memory within 0000H..7FFFH address range to the DSP on-chip memory.
4. Access modes: *r* - read only, *w* - write only, *r/w* - read/write.

Setting SWWSR, SWCR, BSCR and CLKMD Control Registers of TMS320C54x DSP

In order to benefit of full performance of TMS320C54x DSP and to provide correct operation of on-board hardware, user TMS320C54x DSP application must set TMS320C54x on-chip *SWWSR*, *SWCR*, *BSCR* and *CLKMD* control registers as the following:

- The SWWSR register (hex address 0028H) of TMS320C54x DSP must be programmed to 2410H hex value. This corresponds to access of on-board memory and peripherals with minimum 2ws and under control of on-board hardware wait states controller.
- The SWCR register (hex address 002BH) of TMS320C54x DSP must be programmed to 0000H hex value.
- The BSCR register (hex address 0029H) must be programmed to 8000H hex value for TMS320VC5410 DSP and to the A000H value for TMS320VC5416 DSP. This corresponds to 100 MHz DSP output clock for TMS320VC5410 DSP and to 80 MHz DSP output clock for TMS320VC5416 DSP.
- The *CLKMD* register (hex address 0058H) of TMS320C54x DSP must be programmed to 07F7H hex value for TMS320VC5410 DSP and to the 17F7H value for TMS320VC5416 DSP. This corresponds to the PLLx1 mode for TMS320VC5410 DSP and PLLx2 mode for TMS320VC5416 DSP.

FLASH memory area

TORNADO-PX/DDC4 on-board 128Kx8 FLASH memory can be used to store non-volatile data and/or DSP boot code. The FLASH boot code is reloaded to DSP on-chip memory during *SA/FLASH8-BMODE* and *HOST/FLASH8-BMODE* bootmodes.

TORNADO-PX/DDC4 on-board 128Kx8 FLASH memory is available for the on-board DSP as 8-bit external data memory (allocated as least-significant byte of DSP 16-bit data words) at the addresses 8000H..FFFFH in case FLASH memory is selected via *XDM_SEL* selector bit (*XDM_SEL*=1) of *DSP_XDMP_RG* register and in case the DROM bit of DSP on-chip PMST register is set to DROM=0 state (this condition allows external

data memory at 8000H..FFFFH data memory address). Since capacity of FLASH exceeds the 32K external data memory area of TMS320C54x DSP, then *DSP_XDMP_RG* register is provided in order address external FLASH memory in 32KB pages (refer to the corresponding subsection below for more details).

TORNADO-PX/DDC4 on-board FLASH memory can be programmed by on-board DSP, and there is also a possibility to inhibit FLASH writes in order to maintain integrity and safety of FLASH contents.

TORNADO-PX/DDC4 DCM provides FLASH memory write protection in order to exclude unauthorized FLASH memory data update and to guarantee FLASH memory integrity. The FLASH write protection feature is controlled by on-board SW2-3 switch (fig.2-2 and A-1) in accordance with table 2-3.

Table 2-3. FLASH write protection control.

SW2-3 state	Description
ON	FLASH writes are enabled. Application DSP software must meet FLASH programming algorithm requirements in order to program FLASH memory (refer to FLASH memory user's guide for more details).
OFF	FLASH writes are disabled.

Note: 1. Highlighted configuration corresponds to the factory setting.

For more details about programming FLASH memory refer to Appendix D "FLASH Memory Programming".

DPRAM area

TORNADO-PX/DDC4 on-board 32Kx16 DPRAM can be used for both to store DSP program code and for communication between the on-board DSP and host DSP of host *TORNADO* DSP system/controller via host PIOX-16 interface. DPRAM can be accessed by both on-board DSP and host PIOX-16 interface.

In case *TORNADO-PX/DDC4* DCM is being used in stand-alone mode, then DPRAM can be used to store data and/or program code. DPRAM appears as standard 16-bit asynchronous memory and can be accessed by both DSP and host PIOX-16 interface.

CAUTION

Instead of communication between on-board DSP and host PIOX-16 interface via DSP on-chip HPI port, DPRAM allows fast random access to 16-bit memory location from host *TORNADO* DSP system/controller without need to write and store address of the memory location prior accessing the contents of this memory location.

Host-to-DPRAM accesses is performed 4 times faster than that via the DSP on-chip HPI port in case random DPRAM locations are being accessed, and is performed 2 times faster in case autoincremented addressing or preset DPRAM location are being accessed.

TORNADO-PX/DDC4 on-board 32Kx16 DPRAM is available for on-board DSP as both external program and data memory in accordance with the following conditions:

- external data memory at the addresses 8000H..FFFFH in case DPRAM is selected via *XDM_SEL* selector bit (*XDM_SEL*=0) of *DSP_XDMP_RG* register and in case the DROM bit of DSP on-chip PMST register is set to DROM=0 state (this condition allows external data memory at 8000H..FFFFH data memory address)
- external program memory at the addresses 8000H..FFFFH in case DSP starts-up in any of the Microprocessor (MP) bootmodes (*SA/NO-BMODE* and *HOST/NO-BMODE* bootmodes)
- external program memory at the addresses 8000H..BFFFH in case DSP starts-up in any of the Microcontroller (MC) bootmodes (*SA/FLASH8-BMODE*, *HOST/FLASH8-BMODE* and *HOST/HPI-BMODE* bootmodes)

Access to DPRAM feature no arbitration delays for DSP and host PIOX-16 interface unless both on-board DSP and host PIOX-16 interface are addressing the same DPRAM memory location. In the latter case there is no arbitration preferences, and the first active accessing port will proceed without any arbitration delays, whereas the other port will be pending until the first port will finish the access cycle.

DPRAM area of on-board DSP environment has two specific memory locations, which are known as *DSP_DPRAM_HM_RQ* and *DSP_DPRAM_MH_RQ*. These DPRAM locations match *HOST_DPRAM_HM_RQ* and *HOST_DPRAM_MH_RQ* DPRAM locations from on-board DSP environment (refer to section “Host PIOX-16 Interface” later in this chapter). These DPRAM locations provide Host-to-DSP and DSP-to-Host interrupt generation along with standard common memory functionality. Refer to the corresponding subsection below for more details.

Generating Host-to-DSP and DSP-to-Host Interrupt Requests via DPRAM

DPRAM area of on-board DSP environment has two specific memory locations, which are called as *DSP_DPRAM_HM_RQ* and *DSP_DPRAM_MH_RQ* and provide Host-to-DSP and DSP-to-Host interrupt generation along with standard common memory functionality. These DPRAM locations match *HOST_DPRAM_HM_RQ* and *HOST_DPRAM_MH_RQ* memory locations from on-board DSP environment (refer to section “Host PIOX-16 Interface” later in this chapter).

DSP_DPRAM_HM_RQ and *DSP_DPRAM_MH_RQ* DSPRAM memory locations are allocated at the DPRAM addresses in accordance with table 2-2 and are the useful tool for communication between host DSP of host *TORNADO* DSP system/controller and *TORNADO-PX/DDC4* on-board DSP using interrupt request method combined with the 16-bit interrupt request code, which might be simultaneously passed via these DPRAM memory cells.

CAUTION

When host DSP of host *TORNADO* DSP system/controller writes to the *HOST_DPRAM_HM_RQ* DPRAM location via host PIOX-16 interface (refer to section "Host PIOX-16 Interface later in this chapter), then active *DSP_DPRAM_IRQ* interrupt request is generated to the DSP environment and on-board DSP can read data written by host via *DSP_DPRAM_HM_RQ* DPRAM location of on-board DSP environment. This interrupt request remains active until DSP will read contents of this DPRAM memory location. Writing to *DSP_DPRAM_HM_RQ* DPRAM location from the DSP side does not effect the state of *DSP_DPRAM_IRQ* interrupt request.

The *DSP_DPRAM_IRQ* interrupt request can generate active DSP interrupt request in case it is routed via the corresponding interrupt request selector to any of DSP external interrupt requests or DSP NMI. Refer to the corresponding subsection later in this section for more details about external DSP interrupt generation.

CAUTION

When DSP writes to the *DSP_DPRAM_MH_RQ* address, then active *HOST_DPRAM_IRQ* interrupt request is generated to host *TORNADO* DSP system/controller via host PIOX-16 interface and host *TORNADO* DSP system/controller can read data written by DSP via *HOST_DPRAM_HM_RQ* DPRAM location of host PIOX-16 interface. This interrupt request remains active until host DSP of host *TORNADO* DSP system/controller will read contents of this DPRAM memory location. Writing to *HOST_DPRAM_HM_RQ* DPRAM location from host *TORNADO* DSP system/controller side does not effect the state of *HOST_DPRAM_IRQ* interrupt request.

HOST_DPRAM_IRQ interrupt request can generate active interrupt request to host *TORNADO* DSP system/controller via host PIOX-16 interface in case it is enabled via the *HOST_IE_RG* interrupt enable register and particular host interrupt request line is selected via *HOST_HIRQ_SEL_RG* interrupt line selector register. Refer to section "Host PIOX-16 Interface" later in this chapter for more details.

DPSEM area

TORNADO-PX/DDC4 on-board DSP environment provides on-board dual-port hardware semaphores (DPSEM), which is accessible by both on-board DSP and host DSP of host *TORNADO* DSP system/controller via PIOX-16 interface.

Hardware semaphores are extremely useful tool for synchronization of access to any shared resources (DPRAM, HPI port memory locations, etc) and setting synchro-events between DSP and host PIOX-16 interface. DPSEM area comprises of eight dual-port semaphores, which appear as *DSP_DPSEM0_RG* .. *DSP_DPSEM7_RG*

registers within the DSP I/O area (table 2-2).. Access to DPSEM area is performed without any arbitration delays on both DSP and host PIOX-16 interface sides.

Each semaphore occupies least significant bit D0 only within 16-bit data word with bits D1..D15 being an extended copy of bit D0. Semaphore has only two valid states: '0' and '1'. The semaphore logic is active low, and the '0' state is called as 'open state' of semaphore (semaphore token), whereas the '1' state is called as 'closed state' of semaphore. Hardware semaphore logic guarantees that both ports will never get enable state (or semaphore token) simultaneously. Table 2-4 provides example of sample procurement sequence for dual-port semaphores.

Table 2-4. Example of the DPSEM semaphore procurement sequence.

Function	semaphore data at host PIOX-16 interface side	semaphore data at the DSP side	Description
No action.	1	1	Semaphores are closed.
Host PIOX-16 interface writes '0' to semaphore.	0	1	Host PIOX-16 interface receives open semaphore.
DSP writes '0' to semaphore.	0	1	No change. DSP has to wait for semaphore to be released by host PIOX-16 interface.
Host PIOX-16 interface writes '1' to semaphore.	1	0	Host PIOX-16 interface releases semaphore, and DSP receives open semaphore.
Host PIOX-16 interface writes '0' to semaphore.	1	0	No change. Host PIOX-16 interface has to wait for semaphore to be released by the DSP.
DSP writes '1' to semaphore.	0	1	DSP releases semaphore, and host PIOX-16 interface receives open semaphore.
Host PIOX-16 interface writes '1' to semaphore.	1	1	Host PIOX-16 interface releases semaphore, and semaphores are now closed.

DUART

Each DUART channel (UART-1 and UART-2) of On-board PC16552D DUART chip from National Semiconductor Corp can communicate at up to 115 kBaud via RS232C interfaces, which are available at JP2 external I/O connector. DUART is sourced by 1.8432 MHz clock, which allows communication at all industry standard baud rates up to 115 kBaud.

The 8-bit registers set for each DUART channel is compatible with that for PC COM port and is allocated to the DSP I/O area at the base addresses in accordance with table 2-2. DUART register set is allocated to the least significant byte of DSP 16-bit data word.

CAUTION

This manual does not provide information about architecture and programming of PC16552D DUART chip from National Semiconductor Corp.

For more details about PC16552D DUART refer to pages #10..#20 of the corresponding datasheet, which is enclosed in either electronic or paper form with this manual.

HSP50214 PDC data ports

Each of four on-board HSP50214 PDC chips appears in the DSP environment as 8-bit PDC microprocessor read/write port and two 16-bit read-only PDC real-time output data ports (AOUT and BOUT). All ports are available via DSP I/O area (table 2-2).

CAUTION

This manual does not provide information about architecture and programming of Intersil HSP50214 PDC chip.

For more details about Intersil HSP50214 PDC chip refer to original datasheet, which is supplied in either electronic or paper form with this user's guide.

PDC microprocessor port comprises of six 8-bit registers (*DSP_PDCx_HLD0_RG, DSP_PDCx_HLD1_RG, DSP_PDCx_HLD2_RG, DSP_PDCx_HLD3_RG, DSP_PDCx_WRADDR_RG* and *DSP_PDCx_RDARRD_RG*) and must be used o configure PDC on-chip NCO, mixer, digital filters, decimators, demodulators and output data selectors. PDC microprocessor port registers are allocated to the least significant byte of DSP 16-bit data word.

PDC AOUT/BOUT 16-bit output data ports shall be used for reading real-time PDC output data. Each of AOUT and BOUT output data ports comprises of eight 16-bit output data registers (*DSP_PDCx_AOUT0_RG .. DSP_PDCx_AOUT7_RG* and *DSP_PDCx_BOUT0_RG .. DSP_PDCx_BOUT7_RG*). The read contents of these output ports depend upon the PDC output operation mode: either *PARALLEL DIRECT OUTPUT MODE* or PDC *BUFFER RAM PARALLEL OUTPUT MODE* .

For details about PDC control refer to the corresponding subsection below and to section "RF Signal Processing Control" later in this chapter.

Bypass FIFO data port register

Bypass FIFO can be both read and configured by DSP software via *DSP_FIFO_DATA_RG* data read/write port, which is mapped to DSP I/O area (table 2-2).

Reading from *DSP_FIFO_DATA_RG* register will result in reading bypass FIFO data with incrementing FIFO read pointer and updating FIFO EF/PAE/PAF/FF flags. The 12-bit bypass FIFO data are aligned to the least significant bit of DSP 16-bit data word with the upper four bits left undefined.

DSP_FIFO_DATA_RG register (r)

x	X	x	X	FIFO_READ_DATA-11.. FIFO_READ_DATA-0 (r)
bit 15	bit-14	bit-13	Bit-12	bits-11..0

Writing to *DSP_FIFO_DATA_RG* register will take effect only in FIFO configuration mode (which is set when *FIFO_MODE* bit of *DSP_FIFO_CNTR_RG* register is set to *FIFO_MODE* =0 state) and must be used for serial programming of FIFO PAF/PAE programmable flags. When writing to *DSP_FIFO_DATA_RG* register, only bit #0 is valid, which is FIFO serial-in data.

DSP_FIFO_DATA_RG register (w)

X	x	X	X	x	X	X	x	FIFO_SIN (w)
Bits 15..8	bit-7	bit-6	Bit-5	bit-4	bit-3	Bit-2	bit-1	bit-0

For details about FIFO operation refer to the corresponding subsection below and to section "RF Signal Processing Control" later in this chapter.

ADC, ADC-SMUX, bypass FIFO and PDC operation control registers

On-board RF signal processing is configured and controlled via a set of control registers, which are mapped to DSP I/O area (table 2-2) and comprises of control for ADC, ADC-SMUX, bypass FIFO and PDC:

- *DSP_ADC_CLKSEL_RG* register, which is used to select ADC sampling frequency
- *DSP_PDC_FIFO_ISEL_RG* register, which is used to configure ADC-SMUX, i.e. to select input data streams for PDC and FIFO
- *DSP_FIFO_CNTR_RG* register, which is used to control bypass FIFO operation
- read-only *DSP_ADC_FIFO_STAT_RG* register, which is used to read current status of ADC overflow flags and FIFO flags
- read-only *DSP_PDC_STAT_RG* register, which is used to read current status of PDC ready flags
- write-only *DSP_CLR_ADC_OVF_RG* register, which is used to clear ADC overflow flags
- write-only *DSP_FIFO_RES_RG* register, which is used to reset bypass FIFO read/write pointers and FIFO flags.

For details about ADC, PDC and FIFO operation refer to section "RF Signal Processing Control" later in this chapter, whereas this subsection will describe control registers details.

DSP_ADC_CLKSEL_RG register must be used to select sampling frequency source for each ADC channel (ADC-1 and ADC-2) and the corresponding FIFO or PDC-12/34 resources, which are linked to the ADC-1/2 output data streams. *DSP_ADC_CLKSEL_RG* register is available for read/write and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area.

DSP_ADC_CLKSEL_RG register (r/w)

x	0	0	PFG2_ FDIV8_EN (r/w, 0+)	PFG1_ FDIV8_EN (r/w, 0+)	ADC2_ CLKSEL-1 (r/w, 0+)	ADC2_ CLKSEL-0 (r/w, 0+)	ADC1_ CLKSEL-1 (r/w, 0+)	ADC1_ CLKSEL-0 (r/w, 0+)
bits 15..8	Bit-7	bit-6	Bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

The sampling frequency source for ADC-1 and ADC-2 are defined by bits {*ADC1_CLKSEL-1*, *ADC1_CLKSEL-0*} and {*ADC2_CLKSEL-1*, *ADC2_CLKSEL-0*} correspondingly, and can be selected from either on-board PFG-1/2 programmable sampling frequency generators, or from XFS-1/2 external frequency inputs, which are available via on-board JP2 connector.

DSP_ADC_CLKSEL_RG register also includes *PFG1_FDIV8_EN* and *PFG2_FDIV8_EN* bits, which enable optional 1:8 frequency dividers at the outputs of on-board PFG-1 and PFG-2 sampling frequency generators correspondingly in accordance with tables 2-6a and 2-6b. Optional 1:8 frequency dividers at the PFG-1/2 outputs allow to decrease the minimum PFG-1/2 output frequencies from 0.78 MHz to 0.09765 MHz, and to extend programmable ADC sampling frequency range to 0.09765 MHz .. 65 MHz, which meets requirements of virtually any DRR application. For details about programming of PFG-1/2 on-board sampling frequency generators refer to section "Serial Peripherals" later in this chapter.

Table 2-5 provides details about *DSP_ADC_CLKSEL_RG* register bits.

Table 2-5. Register bits of *DSP_ADC_CLKSEL_RG* register.

register bits or bit fields	access mode	value on DSP reset	Description
{*ADC1_CLKSEL-1*, *ADC1_CLKSEL-0*}	r/w	{0,0}	Defines sampling frequency source for ADC-1. {*ADC1_CLKSEL-1*, *ADC1_CLKSEL-0*}= {0,0} corresponds to the on-board PFG-1 programmable sampling frequency generator selected as the sampling frequency source for ADC-1. {*ADC1_CLKSEL-1*, *ADC1_CLKSEL-0*}= {0,1} corresponds to the on-board PFG-2 programmable sampling frequency generator selected as the sampling frequency source for ADC-1. {*ADC1_CLKSEL-1*, *ADC1_CLKSEL-0*}= {1,0} corresponds to the external XFS-1 input from JP2 external I/O connector selected as the sampling frequency source for ADC-1. {*ADC1_CLKSEL-1*, *ADC1_CLKSEL-0*}= {1,1} corresponds to the external XFS-2 input from JP2 external I/O connector selected as the sampling frequency source for ADC-1.
{*ADC2_CLKSEL-1*, *ADC2_CLKSEL-0*}	r/w	{0,0}	Defines sampling frequency source for ADC-2. {*ADC2_CLKSEL-1*, *ADC2_CLKSEL-0*}={0,0} corresponds to the on-board PFG-1 programmable sampling frequency generator selected as the sampling frequency source for ADC-2. {*ADC2_CLKSEL-1*, *ADC2_CLKSEL-0*}={0,1} corresponds to the on-board PFG-2 programmable sampling frequency generator selected as the sampling frequency source for ADC-2. {*ADC2_CLKSEL-1*, *ADC2_CLKSEL-0*}={1,0} corresponds to the external XFS-1 input from JP2 external I/O connector selected as the sampling frequency source for ADC-2. {*ADC2_CLKSEL-1*, *ADC2_CLKSEL-0*}={1,1} corresponds to the external XFS-2 input from JP2 external I/O connector selected as the sampling frequency source for ADC-2.
PFG1_FDIV8_EN	r/w	0	Defines output frequency, which is generated by the PFG-1 programmable sampling frequency generator. *PFG1_FDIV8_EN*=0 corresponds to direct PFG-1 output without optional 1:8 frequency divider selected as the output of PFG-1 sampling frequency generator. *PFG1_FDIV8_EN*=1 corresponds to the output of optional 1:8 frequency divider at the PFG-1 selected as the output of PFG-1 sampling frequency generator.

PFG2_FDIV8_EN	r/w	0	Defines output frequency, which is generated by the PFG-2 programmable sampling frequency generator. *PFG2_FDIV8_EN* =0 corresponds to direct PFG-2 output without optional 1:8 frequency divider selected as the output of PFG-2 sampling frequency generator. *PFG2_FDIV8_EN* =1 corresponds to the output of optional 1:8 frequency divider at the PFG-2 selected as the output of PFG-2 sampling frequency generator.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP_PDC_FIFO_ISEL_RG register must be used to configure on-board RF digital signal processing paths for ***TORNADO-PX/DDC4*** DCM, i.e. input data stream sources for PDC-1/2 and PDC-3/4 PDC sets, and for bypass FIFO. ***DSP_PDC_FIFO_ISEL_RG*** register is available for read/write and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area.

DSP_PDC_FIFO_ISEL_RG register (r/w)

x	*0*	*0*	*0*	*0*	*0*	*FIFO_ISEL (r/w, 0+)*	*PDC34_ISEL (r/w, 0+)*	*PDC12_ISEL (r/w, 0+)*
bits 15..8	bit-7	Bit-6	Bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

Input data stream source for PDC-1/2, PDC-3/4 and bypass FIFO are defined by bits ***PDC12_ISEL***, ***PDC34_ISEL*** and ***FIFO_ISEL*** correspondingly from either ADC-1 or ADC-2 output data streams in accordance with table 2-6.

Table 2-6. Register bits of *DSP_PDC_FIFO_ISEL_RG* register.

register bits	access mode	value on DSP reset	Description
PDC12_ISEL	r/w	0	Selects input data stream and CLKIN frequency for PDC-1 and PDC-2. *PDC12_ISEL* =0 corresponds to ADC-1 output data stream selected as input data stream for PDC-1 and PDC-2, and CLKIN inputs of PDC-1 and PDC-2 are set to the ADC-1 sampling frequency source. *PDC12_ISEL* =1 corresponds to ADC-2 output data stream selected as input data stream for PDC-1 and PDC-2, and CLKIN inputs of PDC-1 and PDC-2 are set to the ADC-2 sampling frequency source.
PDC34_ISEL	r/w	0	Selects input data stream and CLKIN frequency for PDC-3 and PDC-4. *PDC34_ISEL* =0 corresponds to ADC-1 output data stream selected as input data stream for PDC-3 and PDC-4, and CLKIN inputs of PDC-3 and PDC-4 are set to the ADC-1 sampling frequency source. *PDC34_ISEL* =1 corresponds to ADC-2 output data stream selected as input data stream for PDC-3 and PDC-4, and CLKIN inputs of PDC-3 and PDC-4 are set to the ADC-2 sampling frequency source.
FIFO_ISEL	r/w	0	Selects input data stream and write clock for bypass FIFO. *FIFO_ISEL* =0 corresponds to ADC-1 output data stream selected as input data stream for bypass FIFO, and write clock of bypass FIFO is set to the ADC-1 sampling frequency source. *FIFO_ISEL* =1 corresponds to ADC-2 output data stream selected as input data stream for bypass FIFO, and write clock of bypass FIFO is set to the ADC-2 sampling frequency source.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

CAUTION

In case ADC-1 output data stream is selected as the input data stream for PDC-1/2, and/or PDC-3/4, and/or bypass FIFO, then the CLKIN input clock frequency input for PDC-1/2 and/or PDC-3/4, and/or the write clock input for bypass FIFO are connected to the ADC-1 sampling frequency source.

In case ADC-2 output data stream is selected as the input data stream for PDC-1/2, and/or PDC-3/4, and/or bypass FIFO, then the CLKIN input clock frequency input for PDC-1/2 and/or PDC-3/4, and/or the write clock input for bypass FIFO are connected to the ADC-2 sampling frequency source.

DSP_FIFO_CNTR_RG register must be used to set FIFO mode and to control operation of bypass FIFO in FIFO data acquisition mode. *DSP_FIFO_CNTR_RG* register is available for read/write and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area.

DSP_FIFO_CNTR_RG register (r/w)

x	*0*	*0*	*FIFO_ DAQ_END (r,0+)*	*FIFO_ DAQ_ABORT (w, 0+)*	*0*	*FIFO_ DAQTF_SEL (r/w, 0+)*	*FIFO_ DAQ_RUN (r/w, 0+)*	*FIFO_ MODE (r/w, 1+)*
bits 15..8	bit-7	Bit-6	Bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-7 provides details about *DSP_FIFO_CNTR_RG* register bits.

Table 2-7. Register bits of *DSP_FIFO_CNTR_RG* register.

register bits	access mode	value on DSP reset	Description
FIFO_MODE	r/w	1	Defines operation mode for bypass FIFO. Refer to section “RF Signal Processing Control” later in this chapter for more details about operation of bypass FIFO. *FIFO_MODE* =0 corresponds to FIFO configuration mode, which must be used to program FIFO PAE/PAF flags offsets by writing to *DSP_FIFO_RG* register. *FIFO_MODE* =1 corresponds to FIFO data acquisition mode, which must be used to store FIFO input stream data in accordance with bit *FIFO_ISEL* bit of *DSP_PDC_FIFO_ISEL_RG* register. FIFO data acquisition process can be initialized via setting bit *FIFO_DAQ_RUN* of *DSP_FIFO_CNTR_RG* register to the *FIFO_DAQ_RUN* =1 state. FIFO data acquisition process can be either terminated normally on the FIFO termination flag event, or can be aborted either by setting bit *FIFO_DAQ_ABORT* bit of *DSP_FIFO_CNTR_RG* register to the ‘1’ state or by writing to *DSP_FIFO_RES_RG* register.
FIFO_DAQ_RUN	r/w	0	Initializes FIFO data acquisition process in case FIFO data acquisition mode is selected via bit *FIFO_MODE* of *DSP_FIFO_CNTR_RG* register. Refer to section “RF Signal Processing Control” later in this chapter for more details about operation of bypass FIFO. *FIFO_DAQ_RUN* =0 corresponds to no active FIFO data acquisition process. *FIFO_DAQ_RUN* =1 corresponds to active FIFO data acquisition process. Writing ‘1’ to *FIFO_DAQ_RUN* bit will initialize FIFO data acquisition process. FIFO data acquisition process can be either terminated normally on the FIFO termination flag event, or can be aborted by setting bit *FIFO_DAQ_ABORT* bit of *DSP_FIFO_CNTR_RG* register. Writing ‘0’ to *FIFO_DAQ_RUN* bit while *FIFO_DAQ_RUN*=1 will have no effect.
FIFO_DAQTF_SEL	r/w	0	Select termination flag for FIFO data acquisition process. Refer to section “RF Signal Processing Control” later in this chapter for more details about operation of bypass FIFO. *FIFO_DAQTF_SEL* =0 corresponds to FIFO FF flag is selected to terminate FIFO data acquisition process normally. *FIFO_DAQTF_SEL* =1 corresponds to FIFO PAF programmable flag is selected to terminate FIFO data acquisition process normally.

FIFO_DAQ_ABORT	W	0	Write-only bit, which must be used to abort active FIFO data acquisition process in case FIFO data acquisition mode is selected via bit *FIFO_MODE* of *DSP_FIFO_CNTR_RG* register. Bit *FIFO_DAQ_ABORT* always reads as '0'. Refer to section "RF Signal Processing Control" later in this chapter for more details about operation of bypass FIFO. Setting *FIFO_DAQ_ABORT* =0 will have no effect on FIFO data acquisition process. Setting *FIFO_DAQ_ABORT* =1 will abort currently active FIFO data acquisition process and will clear bits *FIFO_DAQ_RUN* and *FIFO_DAQ_END* of *DSP_FIFO_CNTR_RG* register.
FIFO_DAQ_END	R	0	Read-only bit, which indicates normal termination of FIFO data acquisition process on selected termination flag event. *FIFO_DAQ_END* flag can generate DSP external interrupts INT-0..3 and NMI. Refer to section "RF Signal Processing Control" later in this chapter for more details about operation of bypass FIFO. *FIFO_DAQ_END* =0 can be interpreted as either FIFO data acquisition process is in progress (in case *FIFO_DAQ_RUN*=1), or as *FIFO_DAQ_ABORT* command has been issued to clear FIFO data acquisition controller. *FIFO_DAQ_END* =1 corresponds to normal termination of FIFO data acquisition process on the selected FIFO data acquisition termination flag event. Termination flag for FIFO data acquisition process must be selected via bit *FIFO_DAQTF_SEL*.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP_ADC_FIFO_STAT_RG register must be used to read current state of FIFO EF/PAE/FF/PAF flags and ADC overflow flags. ***DSP_ADC_FIFO_STAT_RG*** register is available for read-only and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area. Table 2-8 provides details about ***DSP_ADC_FIFO_STAT_RG*** register bits.

DSP_ADC_FIFO_STAT_RG register (r)

x	*ADC12_OVF (r)*	*ADC2_OVF (r)*	*ADC1_OVF (r)*	*0*	*FIFO_PAF (r,0+)*	*FIFO_FF (r,0+)*	*FIFO_PAE (r,1+)*	*FIFO_EF (r,1+)*
bits 15..8	bit-7	bit-6	Bit-5	bit-4	bit-3	bit-2	Bit-1	bit-0

Table 2-8. Register bits of *DSP_ADC_FIFO_STAT_RG* register.

register bits	access mode	value on DSP reset	Description
FIFO_EF	r	1	Read-only FIFO empty flag (EF). FIFO EF flag is non-programmable. *FIFO_EF* flag can generate DSP external interrupts INT-0..3 and NMI. Refer to section “RF Signal Processing” later in this chapter for more details about operation of bypass FIFO. *FIFO_EF* =0 corresponds to non-empty condition of bypass FIFO. *FIFO_EF* =1 corresponds to empty condition of bypass FIFO.
FIFO_PAE	r	1	Read-only FIFO partially empty flag (PAE). Programmable offset value for FIFO PAE flag can be programmed during FIFO configuration mode. Refer to section “RF Signal Processing Control” later in this chapter for more details about operation of bypass FIFO. *FIFO_PAE* =0 corresponds to more than N unread samples inside bypass FIFO (N is the programmed offset for FIFO PAE flag). *FIFO_PAE* =1 corresponds to N or less number of unread samples inside bypass FIFO (N is the programmed offset for FIFO PAE flag).
FIFO_FF	r	0	Read-only FIFO full flag (FF). FIFO FEF flag is non-programmable. FIFO FF flag can be selected as the termination flag for FIFO data acquisition process via setting bit *FIFO_DAQTF_SEL*=0 in *DSP_FIFO_CNTR_RG* register. *FIFO_FF* flag can generate DSP external interrupts INT-0..3 and NMI. Refer to section “RF Signal Processing Control” later in this chapter for more details about operation of bypass FIFO. *FIFO_FF* =0 corresponds to non-full condition of bypass FIFO. *FIFO_FF* =1 corresponds to full condition of bypass FIFO.
FIFO_PAF	r	0	Read-only FIFO partially full flag (PAF). Programmable offset value for FIFO PAF flag can be programmed during FIFO configuration mode. FIFO PAF flag can be selected as the termination flag for FIFO data acquisition process via setting bit *FIFO_DAQTF_SEL*=1 in *DSP_FIFO_CNTR_RG* register. Refer to section “RF Signal Processing Control” later in this chapter for more details about operation of bypass FIFO. *FIFO_PAF* =0 corresponds to (2^{18}-M-1) or less number of unread samples inside bypass FIFO (M is the programmed offset for FIFO PAF flag). *FIFO_PAF* =1 corresponds to (2^{18}-M) or more number of unread samples inside bypass FIFO (M is the programmed offset for FIFO PAF flag).

ADC1_OVF	r	-	Read-only ADC-1 overflow flag. *ADC1_OVF* flag can generate DSP external interrupts INT-0..3 and NMI. Refer to section "RF Signal Processing Control" later in this chapter for more details about operation of bypass FIFO. *ADC1_OVF* =0 corresponds to no overflow event has been detected for ADC-1. *ADC1_OVF*=1 corresponds to the overflow event has been detected for ADC-1. *ADC1_OVF* flag can be reset by writing to the *DSP_CLR_ADC_OVF_RG* register.
ADC2_OVF	r	-	Read-only ADC-2 overflow flag. *ADC2_OVF* flag can generate DSP external interrupts INT-0..3 and NMI. Refer to section "RF Signal Processing Control" later in this chapter for more details about operation of bypass FIFO. *ADC2_OVF* =0 corresponds to no overflow event has been detected for ADC-2. *ADC2_OVF*=1 corresponds to the overflow event has been detected for ADC-2. *ADC2_OVF* flag can be reset by writing to the *DSP_CLR_ADC_OVF_RG* register.
ADC12_OVF	r	-	Read-only ADC-1 and/or ADC-2 overflow flag. *ADC12_OVF* flag can generate DSP external interrupts INT-0..3 and NMI. This flag can be useful in saving DSP computing time when analyzing overflow event for any of the ADC-1 and ADC-2 data. Refer to section "RF Signal Processing Control" later in this chapter for more details about operation of bypass FIFO. *ADC12_OVF* =0 corresponds to no overflow event has been detected neither for ADC-1 nor for ADC-2. *ADC12_OVF*=1 corresponds to the overflow event has been detected either for ADC-1 and/or for ADC-2. *ADC12_OVF* flag can be reset by writing to the *DSP_CLR_ADC_OVF_RG* register.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP_PDC_STAT_RG register must be used to read current state of PDC data ready and interrupt request flags. *DSP_PDC_STAT_RG* register is available for read-only and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area. Table 2-9 provides details about *DSP_PDC_CNTR_RG* register bits.

DSP_PDC_STAT_RG register (r)

X	*PDC4_INT (r)*	*PDC3_INT (r)*	*PDC2_INT (r)*	*PDC1_INT (r)*	*PDC4_RDY (r)*	*PDC3_RDY (r)*	*PDC2_RDY (r)*	*PDC1_RDY (r)*
bits 15..8	bit-7	bit-6	Bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-9. Register bits of *DSP_PDC_STAT_RG* register.

register bits	access mode	value on DSP reset	Description
PDC1_RDY *PDC2_RDY* *PDC3_RDY* *PDC4_RDY*	r	-	Read-only PDC-x data ready flag, which is valid for PDC PARALLEL DIRECT OUTPUT MODE of the corresponding PDC chip. *PDCx_RDY* flags can generate DSP external interrupts INT-0..3. Refer to the HSP50214 documentation and to section “RF Signal Processing Control” later in this chapter for more details about operation of bypass FIFO. *PDCx_RDY* =0 corresponds to no valid data at the AOUT/BOUT 16-bit output ports presents for the corresponding PDC chip. *PDCx_RDY* =1 corresponds to the valid data has been loaded by the corresponding PDC chip to its AOUT/BOUT 16-bit output ports. *PDCx_RDY* flag will stay in the *PDCx_RDY* =1 state until DSP will read either AOUT or BOUT port of the corresponding PDC chip.
PDC1_INT *PDC2_INT* *PDC3_INT* *PDC4_INT*	r	-	Read-only PDC-x interrupt request flag, which is valid for PDC BUFFER RAM PARALLEL OUTPUT MODE of the corresponding PDC chip. *PDCx_INT* interrupt signal can be configured by DSP software to certain PDC FIFO depth threshold (via bits #12..#14 of PDC Control Word #21). *PDCx_INT* flags can generate DSP external interrupts INT-0..3. Refer to the HSP50214 documentation and to section “RF Signal Processing Control” later in this chapter for more details about operation of bypass FIFO. *PDCx_INT* =0 corresponds to the number of valid FIFO data frames is less than the programmed PDC FIFO depth threshold. *PDCx_INT* =1 corresponds to the number of valid FIFO data frames is equal or larger than the programmed PDC FIFO depth threshold. PDC FIFO data frames can be reconstructed by DSP software from least significant bytes of the PDC AOUT and PDC BOUT output data. *PDCx_INT* signal will stay in the *PDCx_INT* =1 state during eight PDC PROCLK cycles (160 ns) only, and will go to the *PDCx_INT* =0 state afterthat. DSP software must read PDC FIFO data as quick as possible in order to free space for the next FIFO data frame, which will be filled-in on the next PDC output sampling frequency event.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP_CLR_ADC_OVF_RG register must be used to clear overflow flags for ADC-1 and ADC-2. All *ADC1_OVF*, *ADC2_OVF* and *ADC12_OVF* flags, which are available via *DSP_ADC_FIFO_STAT_RG* register (fig.2-8) will be cleared on write to *DSP_CLR_ADC_OVF_RG* register. *DSP_CLR_ADC_OVF_RG* register is available within the DSP I/O area for write-only with the data written ignored.

DSP_CLR_ADC_OVF_RG register (w)

bits 15..8	bit-7	bit-6	Bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
x	*x (w)*	*X (w)*	*x (w)*	*x (w)*	*X (w)*	*x (w)*	*x (w)*	*x (w)*

DSP_FIFO_RES_RG register must be used to reset bypass FIFO data acquisition controller and to clear FIFO EF/PAE/PAF/FF flags. Bits *FIFO_DAQ_RUN* and *FIFO_DAQ_END* of *DSP_FIFO_CNTR_RG* register (table 2-7) will be also cleared on write to *DSP_FIFO_RES_RG* register. *DSP_FIFO_RES_RG* register is available within the DSP I/O area for write-only with written data ignored.

DSP_FIFO_RES_RG register (w)

bits 15..8	bit-7	bit-6	Bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
x	*x (w)*	*x (w)*	*X (w)*	*x (w)*	*x (w)*	*x (w)*	*x (w)*	*x (w)*

DSP_XDMP_RG register for selection of accessed external data memory

DSP_XDMP_RG register must be used by the on-board TMS320C54x DSP software in order to switch between the on-board DPRAM and FLASH memories when accessing external data memory (refer to table 2-2), and to select the 32KB page of FLASH memory, which is allocated to the DSP external data memory address range in case FLASH has been selected by the DSP.

DSP_XDMP_RG register is available for read/write and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area. Table 2-10 provides details about *DSP_XDMP_RG* register bits.

DSP_XDMP_RG Register (r/w)

bits 15..8	bit-7	Bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
X	*XDMEM_SEL (r/w)*	*0*	*0*	*0*	*0*	*0*	*FPAGE-1 (r/w, 0+)*	*FPAGE-0 (r/w, 0+)*

Table 2-10. Register bits of *DSP_XDMP_RG* register.

register bits	access mode	value on DSP reset	Description
XDMEM_SEL	r/w	0 (for *SA/NO-BMODE HOST/NO-BMODE HOST/HPI-BMODE* bootmodes) 1 (for *SA/FLASH8-BMODE HOST/FLASH8-BMODE* bootmodes)	Defines the memory (DPRAM or FLASH), which is mapped to the [8000H..FFFFH] external data memory address space of on-board TMS320C54x DSP in case bit DROM of DSP on-chip PMST register is set to the DROM=0 state. *XDMEM_SEL* =0 corresponds to DPRAM memory is mapped to the DSP external data memory area. *XDMEM_SEL* =1 corresponds to FLASH memory is mapped to the DSP external data memory area.
{*FPAGE-1, FPAGE-0*}	r/w	{0,0}	Selects particular 32K page of 128K FLASH memory, which is mapped to the [8000H..FFFFH] external data memory address space of on-board TMS320C54x DSP in case bit *XDMEM_SEL* of *DSP_XDMP_RG* register is set to the XDMEM_SEL=1 state and DROM of DSP on-chip PMST register is set to the DROM=0 state.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

CAUTION

DSP_XDMP_RG register defaults to the DPRAM memory selected as external data memory for on-board DSP on the DSP reset condition in case DSP starts in either *SA/NO-BMODE*, or *HOST/NO-BMODE*, or *HOST/HPI-BMODE* bootmode.

DSP_XDMP_RG register defaults to the FLASH memory page #0 selected as external data memory for on-board DSP on the on the DSP reset condition in case DSP starts in either *SA/FLASH8-BMODE* or *HOST/FLASH8-BMODE* bootmode.

DSP_SYS_STAT_RG register

DSP_SYS_STAT_RG register contains information about the operation mode and DSP bootmode. *DSP_SYS_STAT_RG* register is available for read-only and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area. Table 2-11 provides details about *DSP_SYS_STAT_RG* register bits.

DSP_SYS_STAT_RG register (r)

X	*0*	*0*	*0*	*0*	*0*	*SA_MODE (r)*	*BMODE-1 (r)*	*BMODE-0 (r)*
bit-15...bit-8	Bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-11. Register bits of *DSP_SYS_STAT_RG* register.

register bits	access mode	Description
SA_MODE	r	Returns the DSP start up operation mode. *SA_MODE* bit does not change during DSP running until DSP reset signal will be applied. *SA_MODE* =0 corresponds to the on-board DSP running under the control of host PIOX-16 interface (*HOST/NO-BMODE*, *HOST/FLASH8-BMODE* and *HOST/HPI-BMODE* bootmodes in accordance with table 2-1). *SA_MODE* =1 corresponds to the on-board DSP running in stand-alone mode (*SA/NO-BMODE* and *SA/FLASH-BMODE* bootmodes in accordance with table 2-1).
{*BMODE-1, BMODE-0*}	r	Returns DSP boot mode. *BMODE-1/0* bits do not change during DSP running until DSP reset signal will be applied. {*BMODE-1, BMODE-0*} ={0,0} corresponds to the microprocessor start-up modes without boot process (*SA/NO-BMODE* and *HOST/NO-BMODE* bootmodes in accordance with table 2-1). {*BMODE-1, BMODE-0*} ={0,1} corresponds to the microcontroller start-up modes with boot from 8-bit FLASH memory (*SA/FLASH8-BMODE* and *HOST/FLASH8-BMODE* bootmodes in accordance with table 2-1). {*BMODE-1, BMODE-0*} ={0,1} corresponds to the microcontroller start-up modes with boot via HPI port (*HOST/HPI-BMODE* bootmodes in accordance with table 2-1). {*BMODE-1, BMODE-0*} ={1,1} is reserved and should not be read.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP_BRS_RG register

DSP_BRS_RG read-only register has been included for compatibility with the TMS320C54x DSP on-chip bootloader, and makes the DSP bootloader to select the boot from the on-board 8-bit FLASH memory starting from the 8000H DSP external data memory address in case boot from FLASH has been selected via on-board SW2-1 button. This register is allocated at the FFFFH DSP I/O address and has the following data format:

DSP_BRS_RG register (r)

X	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*1*
bit-15...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Watchdog timer (WDT) control

TORNADO-PX/DDC4 provides on-board watchdog timer (WDT), which can generate output pulse in case it has been not reset by DSP software within the latency period (typically 1.6 sec) after the last WDT reset event. In case DSP is running in stand-alone mode with the WDT feature enabled, then the DSP software must

periodically reset WDT (with the period about 0.8 sec) in order to exclude automatic DSP restart via on-board DSP bootmode and reset controller (BMRC). WDT feature increases the reliability of stand-alone DSP operation in embedded environment and allows to restart the on-board DSP in case of the DSP idling or software crash

DSP reset on the WDT expiration event is enabled by the ***WDT_EN*** bit of ***DSP_WDT_EN_RG*** register, which is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area. Table 2-12 provides details about ***DSP_WDT_EN_RG*** register bits.

DSP_WDT_EN_RG register (r/w)

X	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*WDT_EN (r/w, 0+)*
bit-15...bit-8	Bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-12. Register bits of *DSP_WDT_EN_RG* register.

Register bits	access mode	value on DSP reset	Description
WDT_EN	r/w	0	Enables WDT feature for DSP stand-alone operation (*SA/NO-BMODE* and *SA/FLASH-BMODE* bootmodes in accordance with table 2-1). *WDT_EN* =0 corresponds to the WDT feature disabled. The DSP reset on the WDT expiration event is disabled, and WDT output is ignored by on-board BMRC. *WDT_EN* =1 corresponds to the WDT feature enabled. DSP software must periodically (with the period about 0.8 sec) reset WDT by means of writing to the *DSP_WDT_RES_RG* register (written data is ignored) in order to exclude automatic DSP restart.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP_WDT_RES_RG register must be used to reset WDT in case WDT feature is enabled and DSP is running in stand-alone bootmode (refer to tables 2-1 and 2-12). ***DSP_WDT_RES_RG*** register is available within the DSP I/O area for write-only with written data ignored.

DSP_WDT_RES_RG register (w)

x	*X (w)*	*X (w)*	*X (w)*	*X (w)*	*x (w)*	*X (w)*	*x (w)*	*x (w)*
bits 15..8	bit-7	Bit-6	Bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

CAUTION

The time period between sequential WDT resets must not exceed 0.8 sec, otherwise the WDT output will activate the DSP reset.

General Purpose I/O pins

GPIO-0/1 are general purpose I/O pins, which are routed to JP2 external I/O connector. *GPIO-0/1* I/O pins are controlled by two control registers (refer to table 2-2):

- *DSP_GPIO_DIR_RG* register (*GPIO* direction register)
- *DSP_GPIO_DATA_RG* register (*GPIO* data register)

DSP_GPIO_DIR_RG register configures direction for *GPIO-0/1* I/O pins and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area. Table 2-13 provides details about *DSP_GPIO_DIR_EN_RG* register bits.

DSP_GPIO_DIR_RG register (r/w)

X	*0*	*0*	*0*	*0*	*0*	*0*	*GPIO-1_DIR (r/w, 0+)*	*GPIO-0_DIR (r/w, 0+)*
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

DSP_GPIO_DATA_RG register defines the current state of *GPIO-0/1* I/O pins and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area.

DSP_GPIO_DATA_RG IOX register (r/w)

X	*0*	*0*	*0*	*0*	*0*	*0*	*GPIO-1 (r/w, 0+)*	*GPIO-0 (r/w, 0+)*
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-13. Register bits of *DSP_GPIO_DIR_RG* register.

Register bits	access mode	value on DSP reset	Description
GPIO-0_DIR	r/w	0	Controls direction of the *GPIO-0* I/O pin, which is available at JP2 external I/O connector. *GPIO-0_DIR* =0 corresponds to the input direction for *GPIO-0* I/O pin. In this case the current state of *GPIO-0* input pin can be read by DSP software via the *GPIO-0* bit of *DSP_GPIO_DATA_RG* register. Writes to the *GPIO-0* bit of *DSP_GPIO_DATA_RG* register are ignored. *GPIO-0_DIR* =1 corresponds to the input direction for *GPIO-0* I/O pin. In this case the output state of *GPIO-0* output pin can be set by writing to the *GPIO-0* bit of *DSP_GPIO_DATA_RG* register, whereas current state of *GPIO-0* pin can be read by DSP software via the *GPIO-0* bit of *DSP_GPIO_DATA_RG* register.
GPIO-1_DIR	r/w	0	Controls direction of the *GPIO-1* I/O pin, which is available at JP2 external I/O connector. *GPIO-1_DIR* =0 corresponds to the input direction for *GPIO-1* I/O pin. In this case the current state of *GPIO-1* input pin can be read by DSP software via the *GPIO-1* bit of *DSP_GPIO_DATA_RG* register. Writes to the *GPIO-1* bit of *DSP_GPIO_DATA_RG* register are ignored. *GPIO-1_DIR* =1 corresponds to the input direction for *GPIO-1* I/O pin. In this case the output state of *GPIO-1* output pin can be set by writing to the *GPIO-1* bit of *DSP_GPIO_DATA_RG* register, whereas current state of *GPIO-1* pin can be read by DSP software via the *GPIO-1* bit of *DSP_GPIO_DATA_RG* register.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

Note, that in case any of *GPIO-0/1* I/O flags is configured as input, then writing to the corresponding bit of *DSP_GPIO_DATA_RG* register is ignored, however data written will be hold in *DSP_GPIO_DATA_RG* register and will appear on *GPIO-0/1* output as soon as it will be configured as the output.

Interrupt source selectors for DSP INT0..3 and NMI external interrupt inputs

The DSP environment of *TORNADO-PX/DDC4* offers software programmable selectors for each of the DSP external interrupts (INT0..INT3) and for DSP non-maskable interrupt (NMI). Since the number of possible external DSP interrupt sources for *TORNADO-PX/DDC4* is well above five sources, then this allows outstanding flexibility for run-time selection from multiple DSP interrupt sources for *TORNADO-PX/DDC4* in order to meet requirements of virtually any DSP application.

CAUTION

This manual does not provide information about using and programming of TMS320C54x DSP external INT0..3 and NMI interrupts.

For more details refer to the TMS320C54x user's guide, which is enclosed in either electronic or paper form with this manual.

Setting the interrupt source for DSP external interrupts INT0..3 and for DSP NMI is performed by the DSP software by means of programming the ***DSP_MIRQ0_SEL_RG..DSP_MIRQ3_SEL_RG*** and to the ***DSP_MNMI_SEL_RG*** registers (refer to table 2-2), which are allocated to the least significant byte of DSP 16-bit data words within the DSP I/O area.

DSP_MIRQ0_SEL_RG register (r/w)

bit-15...8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
x	*0*	*0*	*0*	*MIRQ0_SEL-4 (r/w, 0+)*	*MIRQ0_SEL-3 (r/w, 0+)*	*MIRQ0_SEL-2 (r/w, 0+)*	*MIRQ0_SEL-1 (r/w, 0+)*	*MIRQ0_SEL-0 (r/w, 0+)*

DSP_MIRQ1_SEL_RG register (r/w)

bit-15...8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
x	*0*	*0*	*0*	*MIRQ1_SEL-4 (r/w, 0+)*	*MIRQ1_SEL-3 (r/w, 0+)*	*MIRQ1_SEL-2 (r/w, 0+)*	*MIRQ1_SEL-1 (r/w, 0+)*	*MIRQ1_SEL-0 (r/w, 0+)*

DSP_MIRQ2_SEL_RG register (r/w)

bit-15...8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
x	*0*	*0*	*0*	*MIRQ2_SEL-4 (r/w, 0+)*	*MIRQ2_SEL-3 (r/w, 0+)*	*MIRQ2_SEL-2 (r/w, 0+)*	*MIRQ2_SEL-1 (r/w, 0+)*	*MIRQ2_SEL-0 (r/w, 0+)*

DSP_MIRQ3_SEL_RG register (r/w)

bit-15...8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
x	*0*	*0*	*0*	*MIRQ3_SEL-4 (r/w, 0+)*	*MIRQ3_SEL-3 (r/w, 0+)*	*MIRQ3_SEL-2 (r/w, 0+)*	*MIRQ3_SEL-1 (r/w, 0+)*	*MIRQ3_SEL-0 (r/w, 0+)*

DSP_MNMI_SEL_RG Register (r/w)

x	0	0	0	0	NMI_SEL-3 (r/w, 0+)	NMI_SEL-2 (r/w, 0+)	NMI_SEL-1 (r/w, 0+)	NMI_SEL-0 (r/w, 0+)
bit-15...8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

CAUTION

DSP_MIRQ0_SEL_RG..DSP_MIRQ3_SEL_RG interrupt selector registers allow selection of interrupt source for TMS320C54x DSP INT0..3 external interrupt inputs.

DSP_NMI_SEL_RG interrupt selector register allow selection of interrupt source for TMS320C54x DSP NMI external interrupt input.

Each of the DSP INT0..3 external interrupt selector registers of *TORNADO-PX/DDC4* allows selection of one interrupt source from 20 available interrupt sources in accordance with table 2-14a, whereas DSP NMI interrupt selector register allows selection of one interrupt source from 12 available interrupt sources in accordance with table 2-14b.

Table 2-14a. Interrupt sources for DSP INT0..3 external interrupt selectors.

bits #4..#0 of DSP_MIRQ0_SEL_RG, DSP_MIRQ1_SEL_RG DSP_MIRQ2_SEL_RG, DSP_MIRQ3_SEL_RG					**DSP Interrupt source**
bit #4	**bit #3**	**bit #2**	**bit #1**	**bit #0**	
0	*0*	*0*	*0*	*0*	Interrupt is disabled. This is the default value on the DSP reset condition.
0	*0*	*0*	*0*	*1*	Interrupt on interrupt request from DPRAM (active *DSP_DPRAM_IRQ* interrupt request).
0	*0*	*0*	*1*	*0*	Interrupt on interrupt request from the UART-1 channel of DUART.
0	*0*	*0*	*1*	*1*	Interrupt on interrupt request from the UART-2 channel of DUART.
0	*0*	*1*	*0*	*0*	Interrupt on the falling edge (1→0 transition) at the *GPIO-0* I/O pin.
0	*0*	*1*	*0*	*1*	Interrupt on falling edge (1→0 transition) at the *GPIO-1* I/O pin.
0	*0*	*1*	*1*	*0*	Interrupt on ADC-1 overflow (active *ADC1_OVF* flag).
0	*0*	*1*	*1*	*1*	Interrupt on ADC-2 overflow (active *ADC2_OVF* flag).
0	*1*	*0*	*0*	*0*	Interrupt on either ADC-1 or ADC-2 overflow (active *ADC12_OVF* flag).
0	*1*	*0*	*0*	*1*	Interrupt on the end of FIFO data acquisition (active *FIFO_DAQ_END* flag).
0	*1*	*0*	*1*	*0*	Interrupt on FIFO empty condition (active FIFO EF flag).
0	*1*	*0*	*1*	*1*	Interrupt on FIFO partially empty condition (active FIFO PAE flag).
0	*1*	*1*	*0*	*0*	Interrupt on PDC-1 interrupt request (active *PDC1_IRQ* flag).
0	*1*	*1*	*0*	*1*	Interrupt on PDC-2 interrupt request (active *PDC2_IRQ* flag).
0	*1*	*1*	*1*	*0*	Interrupt on PDC-3 interrupt request (active *PDC3_IRQ* flag).
0	*1*	*1*	*1*	*1*	Interrupt on PDC-4 interrupt request (active *PDC4_IRQ* flag).
1	*0*	*0*	*0*	*0*	Interrupt on PDC-1 ready condition (active *PDC1_RDY* flag).
1	*0*	*0*	*0*	*1*	Interrupt on PDC-2 ready condition (active *PDC2_RDY* flag).
1	*0*	*0*	*1*	*0*	Interrupt on PDC-3 ready condition (active *PDC3_RDY* flag).
1	*0*	*0*	*1*	*1*	Interrupt on PDC-4 ready condition (active *PDC4_RDY* flag).

Notes:
1. Unlisted combinations are reserved and will result in no interrupt selection.
2. Highlighted selection corresponds to default setting on the DSP reset condition.

Table 2-14b. Interrupt sources for DSP NMI external interrupt selector.

bits #4..#0 of DSP_MNMI_SEL_RG					**DSP Interrupt source**
bit #4	**bit #3**	**bit #2**	**bit #1**	**bit #0**	
0	*0*	*0*	*0*	*0*	Interrupt is disabled. This is the default value on the DSP reset condition.
0	*0*	*0*	*0*	*1*	Interrupt on interrupt request from DPRAM (active *DSP_DPRAM_IRQ* interrupt request).
0	*0*	*0*	*1*	*0*	Interrupt on interrupt request from the UART-1 channel of DUART.
0	*0*	*0*	*1*	*1*	Interrupt on interrupt request from the UART-2 channel of DUART.
0	*0*	*1*	*0*	*0*	Interrupt on the falling edge (1→0 transition) at the *GPIO-0* I/O pin.
0	*0*	*1*	*0*	*1*	Interrupt on the falling edge (1→0 transition) at the *GPIO-1* I/O pin.
0	*0*	*1*	*1*	*0*	Interrupt on ADC-1 overflow (active *ADC1_OVF* flag).
0	*0*	*1*	*1*	*1*	Interrupt on ADC-2 overflow (active *ADC2_OVF* flag).
0	*1*	*0*	*0*	*0*	Interrupt on either ADC-1 or ADC-2 overflow (active *ADC12_OVF* flag).
0	*1*	*0*	*0*	*1*	Interrupt on the end of FIFO data acquisition (active *FIFO_DAQ_END* flag).
0	*1*	*0*	*1*	*0*	Interrupt on FIFO empty condition (active FIFO EF flag).
0	*1*	*0*	*1*	*1*	Interrupt on FIFO partially empty condition (active FIFO PAE flag).

Notes:
1. Unlisted combinations are reserved and will result in no interrupt selection.
2. Highlighted selection corresponds to default setting on the DSP reset condition.

CAUTION

All DSP external interrupt source selector registers default to the 00H state on the DSP reset condition, which corresponds to no selected interrupt source, i.e. the corresponding external interrupt is disabled.

DSP_AUX_IRQ_STAT_RG register

DSP_AUX_IRQ_STAT_RG register contains status information for some interrupt requests, which is not available via on-board read-back peripherals and registers. *DSP_AUX_IRQ_STAT_RG* register might be useful in case user DSP application would appreciate to perform software polling of peripherals ready condition rather then to use interrupts.

DSP_AUX_IRQ_STAT_RG register is available for read-only and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area. Table 2-15 provides details about *DSP_AUX_IRQ_STAT_RG* register bits.

DSP_AUX_IRQ_STAT_RG register (r)

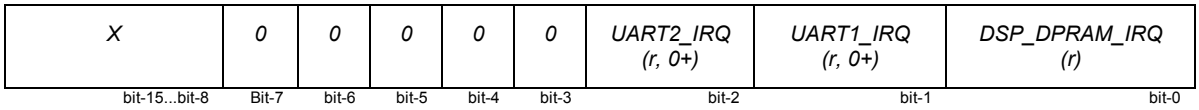


Table 2-15. Register bits of *DSP_AUX_IRQ_STAT_RG* register.

register bits	access mode	Description
DSP_DPRAM_IRQ	r	Returns current status of interrupt request from DPRAM. DPRAM interrupt is set active when host *TORNADO* DSP system/controller writes to the *DSP_DPRAM_HM_RQ* DPRAM memory location via host PIOX-16 interface. This interrupt request is valid for host operation mode only. *DSP_DPRAM_IRQ* =0 corresponds to no active interrupt request from DPRAM. *DSP_DPRAM_IRQ* =1 corresponds to active interrupt request from DPRAM, i.e. host *TORNADO* DSP system/controller has written data to the *DSP_DPRAM_HM_RQ* DPRAM memory location via host PIOX-16 interface. DSP software has to read from *DSP_DPRAM_HM_RQ* DPRAM memory location in order to clear DPRAM interrupt request.
UART1_IRQ *UART2_IRQ*	r	Return interrupt current status of interrupt requests from UART-1 and UART-2 channels of DUART.. *UARTx_IRQ* =0 corresponds to no active interrupt request from the corresponding channel of DUART. This is the default value on the DSP reset condition. *UARTx_IRQ* =1 corresponds to active interrupt request from the corresponding channel of DUART. DSP software has to identify UART interrupt source via reading UART registers and to perform either write to or read from UART in order to clear interrupt request. For more detail refer to the PC16552D DUART documentation.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP_XSL_FMT_RG register for programming XSL configuration

DSP_XSL_FMT_RG register must be used by on-board TMS320C54x DSP software in order to configure data format and serial clock features for XSL-1 and XSL-2 external output serial links are serial peripherals, which can be loaded via DSP on-chip McBSP-1 port. XSL-1 and XSL-2 have been included for digital gain control of external RF amplifiers, however they can be also used for general purpose serial data output.

For more details about XSL-1 and XSL-2 external output serial links refer to section "Serial Peripherals" later in this chapter.

DSP_XSL_FMT_RG register is available for read/write and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area. Table 2-16 provides details about ***DSP_XSL_FMT_RG*** register bits.

DSP_XSL_FMT_RG Register (r/w)

X	*0*	*0*	*XSL-CLK_FRM (r/w, 1+)*	*XSL-CLK_POL (r/w,0+)*	*XSL2-DF1 (r/w,0+)*	*XSL2-DF0 (r/w,0+)*	*XSL1-DF1 (r/w, 0+)*	*XSL1-DF0 (r/w, 0+)*
bits 15..8	bit-7	Bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-16. Register bits of *DSP_XSL_FMT_RG* register.

register bits	access mode	value on DSP reset	Description
{*XSL1-DF1, XSL1-DF0*}	r/w	{0,0}	Defines serial data format for XSL-1 external output serial link. {*XSL1-DF1, XSL1-DF0*}= {0,0} corresponds to 8-bit data transmission over XSL-1. This value is set as default on the DSP reset condition. {*XSL1-DF1, XSL1-DF0*}= {0,1} corresponds to 16-bit data transmission over XSL-1. {*XSL1-DF1, XSL1-DF0*}= {1,0} corresponds to 24-bit data transmission over XSL-1. {*XSL1-DF1, XSL1-DF0*}= {1,1} corresponds to 30-bit data transmission over XSL-1.
{*XSL2-DF1, XSL2-DF0*}	r/w	{0,0}	Defines serial data format for XSL-2 external output serial link. {*XSL2-DF1, XSL2-DF0*}={0,0} corresponds to 8-bit data transmission over XSL-2. This value is set as default on the DSP reset condition. {*XSL2-DF1, XSL2-DF0*}={0,1} corresponds to 16-bit data transmission over XSL-2. {*XSL2-DF1, XSL2-DF0*}={1,0} corresponds to 24-bit data transmission over XSL-2. {*XSL2-DF1, XSL2-DF0*}={1,1} corresponds to 30-bit data transmission over XSL-2.
XSL-CLK_POL	r/w	0	Defines polarity for XSL serial clock output (*XSL-CLK*), which is common for both XSL-1 and XSL-2 external output serial links. *XSL-CLK_POL*=0 corresponds to positive polarity of *XSL-CLK* output, i.e. both XSL data frame synchronization outputs (*XSL1-FSYNC* and *XSL2-FSYNC*) output data are updated at the rising edges of *XSL-CLK* output signal. This value is set as default on the DSP reset condition. *XSL-CLK_POL*=1 corresponds to negative polarity of *XSL-CLK* output, i.e. both XSL data frame synchronization outputs (*XSL1-FSYNC* and *XSL2-FSYNC*) output data are updated at the falling edges of *XSL-CLK* output signal.

XSL-CLK_FRM	r/w	1	Defines framing feature for XSL serial clock output (*XSL-CLK*), which is common for both XSL-1 and XSL-2 external output serial links. *XSL-CLK_FRM*=0 disables framing for *XSL-CLK* output, i.e. *XSL-CLK* output is continuous and is not effected by the XSL-1 and XSL-2 frame synchronization outputs (*XSL1-FSYNC* and *XSL2-FSYNC*). This value is set as default on the DSP reset condition. *XSL-CLK_FRM*=1 enables framing for *XSL-CLK* output, i.e. *XSL-CLK* output is not continuous and is enabled only during active XSL-1 and XSL-2 frame synchronization outputs (*XSL1-FSYNC* and *XSL2-FSYNC*). This feature is useful in case XSL are used for digital gain control of external RF amplifiers and it is desirable to reduce digital noise level.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP on-chip McBSP ports

TORNADO-PX/DDC4 on-board TMS320C54x DSP features three on-chip McBSP ports, which can be used to communicate with on-board peripherals and external devices.

McBSP-0 port is available via on-board JP4 external link/power connector for communication with compatible external peripherals (refer to Appendix A for connector specifications)

McBSP-1 port is used for programming on-board serial peripherals, which comprise of XDAC-1 and XDAC-2 digital-to-analog converters, PFG-1 and PFG-2 sampling frequency generators, and of XSL-1 and XSL-2 external serial links (for more details refer to section “Serial Peripherals” later in this chapter)

McBSP-2 port is used for output to on-board programming on-board PHDAC phone DAC (for more details refer to section “Serial Peripherals” later in this chapter).

2.3 RF Signal Processing Control

TORNADO-PX/DDC4 DCM provides multi-path software configurable on-board RF digital signal processing, which comprises of the following on-board components (fig.2-1):

- RF analog input section, which includes two 12-bit 65 Msps ADCs (ADC-1 and ADC-2) and two RF input amplifiers with RF input connectors
- programmable 2:3 ADC streams multiplexer (ADC-SMUX)
- four 65 MSPS Intersil HSP50214 PDC chips (PDC-1, PDC-2, PDC-3 and PDC-4)
- 256 KW bypass FIFO
- TMS320VC5410 DSP or TMS320VC5416 DSP.

TORNADO-PX/DDC4 on-board RF signal processing paths are configured and controlled via a set of control registers, which are mapped to DSP I/O area (refer to section “DSP Environment” earlier in this chapter and to table 2-2):

- *DSP_ADC_CLKSEL_RG* register, which is used to select ADC sampling frequency
- *DSP_PDC_FIFO_ISEL_RG* register, which is used to configure ADC-SMUX, i.e. to select input data streams for PDC and FIFO
- *DSP_FIFO_CNTR_RG* register, which is used to control bypass FIFO operation

- *DSP_FIFO_DATA_RG* read/write register, which is used to read FIFO data and to program FIFO flags
- read-only *DSP_ADC_FIFO_STAT_RG* register, which is used to read current status of ADC overflow flags and FIFO flags
- read-only *DSP_PDC_STAT_RG* register, which is used to read current status of PDC ready flags
- write-only *DSP_CLR_ADC_OVF_RG* register, which is used to clear ADC overflow flags
- write-only *DSP_FIFO_RES_RG* register, which is used to reset bypass FIFO read/write pointers and FIFO flags.

This section will provide details about *TORNADO-PX/DDC4* on-board RF signal processing components and how to configure and control RF digital signal processing paths.

RF analog input section

RF analog input section (fig.2-3) of *TORNADO-PX/DDC4* DCM includes two identical channels, each comprising of RF input amplifier, ADC, ADC sampling frequency selector and ADC overflow controller.

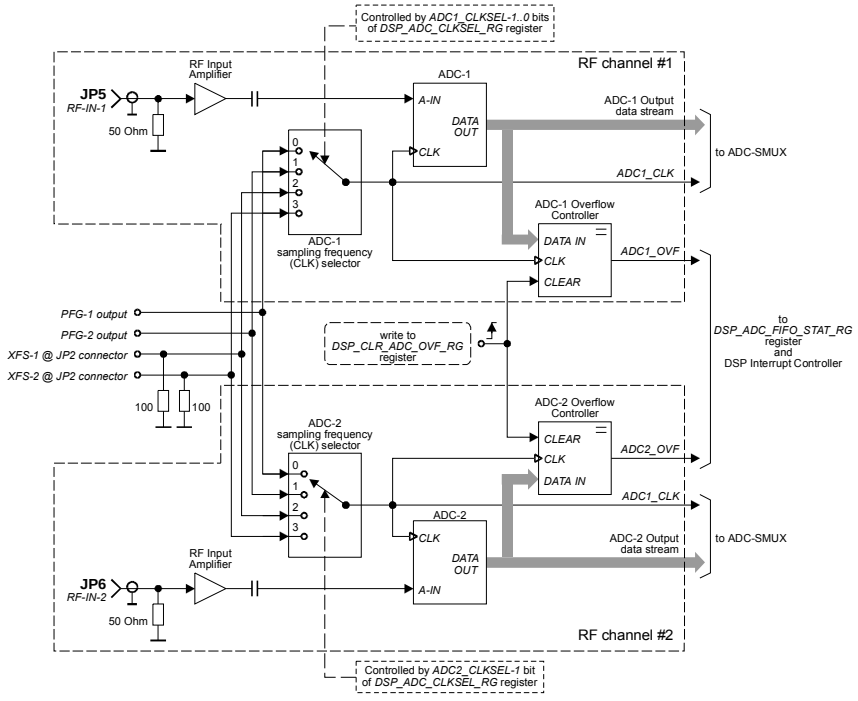


Fig.2-3. RF analog input section.

RF input amplifiers

RF input amplifiers connect to external analog world via mini-coax on-board JP5 and JP6 connectors, and provide 50 Ohm input impedance and wide signal-pass bandwidth.

RF input amplifiers are DC coupled with input RF signals and allow small DC input bias at RF inputs. Outputs of RF input amplifiers are DC decoupled from ADC inputs.

The signal-pass bandwidth of RF input amplifiers is limited at the low end only by means of the 1st order high-frequency pass filter at approximately 5 kHz, which is actually defined by the parameters of the DC decoupling between RF input amplifies and the corresponding ADC inputs.

The upper bandpass frequency of input RF input amplifiers well exceeds the 32.5 MHz bandwidth for 65 MHz maximum sampling frequency value for on-board ADC in order to allow undersampling of input RF signal via ADC.

ADC and ADC sampling frequency selector

On-board ADC feature 12-bit resolution at up to 65 MHz sampling frequency and excellent linearity, which guarantee minimum signal distortions during conversion of RF input signal.

On-board ADC feature wide signal bandwidth and along with RF input amplifiers allow undersampling of RF input signals within the frequency range below approximately 150 MHz.

12-bit real-time output data stream of each ADC can be further routed to the input data streams for PDC and FIFO via on-board ADC-SMUX stream multiplexer.

Each ADC has its own sampling frequency input, which can be configured by on-board DSP software via *DSP_ADC_CLKSEL_RG* register to come from any of the following sources (table 2-5):

- any of two on-board sampling frequency generators (PFG-1 and PFG-2)
- any of two external sampling frequency inputs (XFS-1 and XFS-2).

The on-board PFG-1 and PFG-2 sampling frequency generators can be programmed by DSP software to any frequency value within the 0.09765 MHz .. 65 MHz frequency range. For more details about PFG refer to section “Serial Peripherals” later in this chapter.

External sampling frequency inputs XFS-1 and XFS-2 are available at the JP2 external I/O connector. Both XFS-1 and XFS-2 inputs are low impedance 100 Ohm logical inputs in order to minimize signal distortions when connecting to external signal sources.

ADC overflow controller

One of the important requirements for perfect RF digital signal processing using PDC chips is to ensure no input data overflow (saturation), which can result in significant output distortions after digital signal mixing, digital filtering and digital demodulation. In order to meet this requirement, *TORNADO-PX/DDC4* DCM provides real-time overflow control for each of the on-board ADC.

ADC overflow flags (*ADC1_OVF* and *ADC2_OVF*) are set in case the corresponding ADC output digital data reaches its either positive maximum or negative minimum value and can be cleared by DSP software by means of writing to the *DSP_CLR_ADC_OVF_RG* register (refer to section “DSP Environment” earlier in this chapter) after DSP will recognize and process ADC overflow event(s).

CAUTION

Writing to the *DSP_CLR_ADC_OVF_RG* register clears both *ADC1_OVF* and *ADC2_OVF* ADC overflow flags.

ADC overflow events can generate external DSP interrupt in case the corresponding *ADC1_OVF* and *ADC2_OVF* ADC overflow flag is selected via *DSP_MIRQ0_SEL_RG..DSP_MIRQ3_SEL_RG* and *DSP_MNMI_SEL_RG* registers to generate either DSP external INT0..3 or NMI interrupt (tables 2-14a and 2-14b).

ADC1_OVF and *ADC2_OVF* ADC overflow flags are also available for software polling via *DSP_ADC_FIFO_STAT_RG* register (table 2-8).

TORNADO-PX/DDC4 DCM also provides *ADC12_OVF* summary ADC overflow flag, which is a logical OR between the *ADC1_OVF* and *ADC2_OVF* ADC overflow flags, and is set in case any of the *ADC1_OVF* and *ADC2_OVF* flags is set. *ADC12_OVF* summary ADC overflow flag is available both for software polling via *DSP_CLR_ADC_OVF_RG* register and as the source for DSP external INT0..3 and NMI interrupts.

CAUTION

ADC12_OVF summary ADC overflow flag is useful to reduce the number of the DSP external interrupts utilized for ADC overflow tracking and/or to save DSP time for detection of the ADC overflow events by means of software polling via *DSP_CLR_ADC_OVF_RG* register.

ADC streams multiplexer (ADC-SMUX)

Each of two 12-bit ADC output data streams can be routed to the input streams for PDC-1/2 and PDC-3/4 PDC sets, and for bypass FIFO via programmable ADC-SMUX ADC streams multiplexer (fig.2-4).

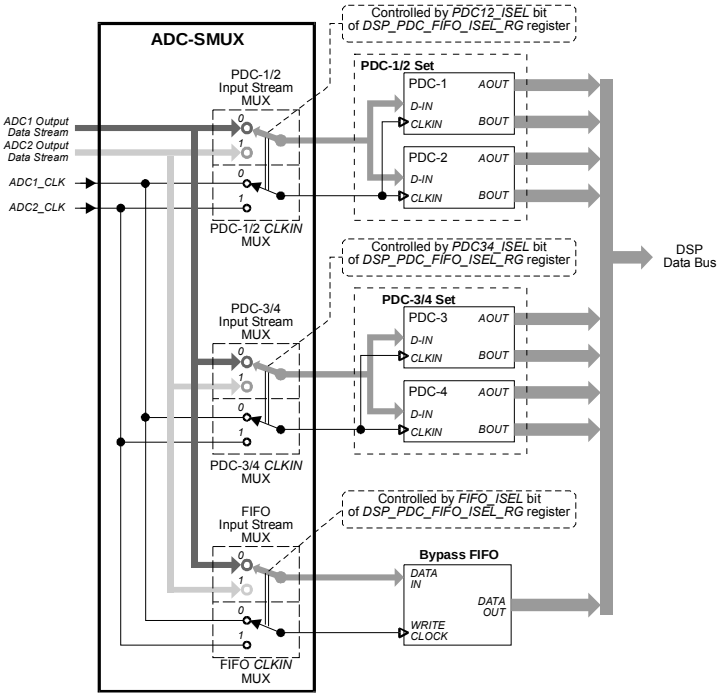


Fig.2-4. ADC output data stream multiplexer.

ADC-SMUX is controlled by DSP software via ***DSP_PDC_FIFO_ISEL_RG*** register (table 2-6) and delivers outstanding flexibility for run-time configuring of RF digital signal processing paths.

ADC-SMUX comprises of three independent data streams multiplexers for PDC-1/2, PDC-3/4 and FIFO inputs, which are combined with the corresponding clock multiplexers. The PDC-1/2 combined data stream and clock multiplexer is controlled by the ***PDC12_ISEL*** bit of via ***DSP_PDC_FIFO_ISEL_RG*** register, whereas the ***PDC34_ISEL*** and ***FIFO_ISEL*** bits of ***DSP_PDC_FIFO_ISEL_RG*** register control the corresponding combined data stream and clock multiplexers for PDC-3/4 set and bypass FIFO.

Should this be important for user application, each data stream multiplexer of ADC-SMUX introduces 2 clocks delay to the corresponding digital data stream path.

PDC pool

On-board PDC pool comprises of four Intersil HSP50214 PDC chips each providing one DRR signal processing channel. PDC perform digital down conversion of high-bandwidth parallel ADC output stream to the low-band PDC output data stream, which can be read and processed by on-board DSP.

On-board PDC pool is organized as two sets of two PDC chips each (PDC-1/2 and PDC-3/4). Both HSP50214 PDC chips within one PDC set share common 12-bit input data stream and common CLKIN clock frequency, which are the output data stream and clock output of the corresponding combined data stream and clock multiplexer of ADC-SMUX (fig.2-4).

CAUTION

Input PDC data streams from the corresponding ADC-SMUX outputs are aligned at the PDC most significant bit at the PDC input data port with four least significant bits being 'zeroed'.

The PDC external gain adjustment inputs are not used, and are externally grounded in order to provide optional 0dB gain factor.

Each on-board HSP50214 PDC chips comprises of 8-bit PDC microprocessor read/write port, which must be used to configure and control the PDC chip, and two 16-bit read-only PDC real-time output data ports (AOUT and BOUT). All ports are available via DSP I/O area (table 2-2).

CAUTION

This manual does not provide information about architecture and programming of Intersil HSP50214 PDC chip.

For more details about Intersil HSP50214 PDC chip refer to original datasheet, which is supplied in either electronic or paper form with this user's guide.

configuring PDC via microprocessor port

PDC microprocessor port must be used to configure PDC on-chip NCO, mixer, digital filters, decimators, demodulators and output data selectors. PDC microprocessor port comprises of six 8-bit registers, which are allocated to the least significant byte of the DSP 16-bit data word:

- *DSP_PDCx_HLD0_RG, DSP_PDCx_HLD1_RG, DSP_PDCx_HLD2_RG* and *DSP_PDCx_HLD3_RG* registers, which shall be used to compose and latch the 32-bit data word during writes to the PDC chip and to read requested data from the PDC chip
- *DSP_PDCx_WRADDR_RG* register, which must be used to define the write address for 32-bit data word, which is composed and latched by *DSP_PDCx_HLD0_RG, DSP_PDCx_HLD1_RG, DSP_PDCx_HLD2_RG* and *DSP_PDCx_HLD3_RG* registers
- *DSP_PDCx_RDARRD_RG* register, which must be used to define the address of data to be read from the PDC chip.

For example, the write procedure of 32-bit 0x12345678 data word to the PDC-3 on-chip control register #A via PDC microprocessor port is performed in five steps:

- write byte #1 (least significant byte) of 32-bit data word (0x78) to *DSP_PDC3_HLD0_RG* register
- write byte #2 of 32-bit data word (0x56) to *DSP_PDC3_HLD1_RG* register
- write byte #3 of 32-bit data word (0x34) to *DSP_PDC3_HLD2_RG* register
- write byte #4 (most significant byte) of 32-bit data word (0x12) to *DSP_PDC3_HLD3_RG* register
- write address #A to *DSP_PDCx_WRADDR_RG* register.

PDC has been designed to read-back only few predefined data via PDC microprocessor port. This predefined data includes buffer RAM contents (I, Q, magnitude, phase and frequency), input level detector, AGC timing

and error, and status information. For example, the read procedure of I/Q data from the buffer RAM of PDC-3 chip is performed in five steps:

- write 00H data to the *DSP_PDC3_RDARRD_RG* register, i.e. select I/Q data for read-back
- read byte #1 (least significant byte) of 16-bit I-data from the *DSP_PDC3_HLD0_RG* register
- read byte #2 (most significant byte) of 16-bit I-data from the *DSP_PDC3_HLD1_RG* register
- read byte #1 (least significant byte) of 16-bit Q-data from the *DSP_PDC3_HLD2_RG* register
- read byte #2 (most significant byte) of 16-bit Q-data from the *DSP_PDC3_HLD3_RG* register.

Refer to original documentation for HSP50214 PDC for more details about how to use the PDC microprocessor port and how to configure HSP50214 PDC chip.

reading PDC real-time data via 16-bit AOUT/BOUT output ports

Real-time output PDC data are available for read by DSP software via the AOUT and BOUT 16-bit output data ports (table 2-2).

Each of 16-bit AOUT and BOUT output data ports comprises of eight 16-bit output data registers:

- *DSP_PDCx_AOUT0_RG .. DSP_PDCx_AOUT7_RG* internal PDC registers available via AOUT port
- *DSP_PDCx_BOUT0_RG .. DSP_PDCx_BOUT7_RG* internal PDC registers available via BOUT port,

whereas data, which is read via AOUT/BOUT PDC output ports, shall be interpreted upon the PDC output operation mode:

- *PARALLEL DIRECT OUTPUT MODE*
- *BUFFER RAM PARALLEL OUTPUT MODE*

In case *PARALLEL DIRECT OUTPUT MODE* (fig.2-5) is selected (via bit #25 of PDC Control Word #20), then output data shall be read from *DSP_PDCx_AOUT0_RG* and *DSP_PDCx_BOUT0_RG* registers only. Two 16-bit real-time data words, which are routed to PDC AOUT/BOUT output ports (*DSP_PDCx_AOUT0_RG* and *DSP_PDCx_BOUT0_RG* registers) in this mode are selected by bits #22..#23 and bits #20..#21 correspondingly of PDC Control Word #20. When new PDC output data comes available via PDC AOUT/BOUT output ports, then the corresponding *PDCx_RDY* ready signal is set active by PDC. *PDCx_RDY* ready signal can be either polled via *DSP_PDC_STAT_RG* register or can generate DSP external interrupt INT-0..3 in case *PDCx_RDY* input is selected as the interrupt source via the interrupt selector registers *DSP_MIRQ0_SEL_RG .. DSP_MIRQ3_SEL_RG*. *PDCx_RDY* signal remains in active state until on-board DSP will read from any of the PDC AOUT/BOUT output ports.

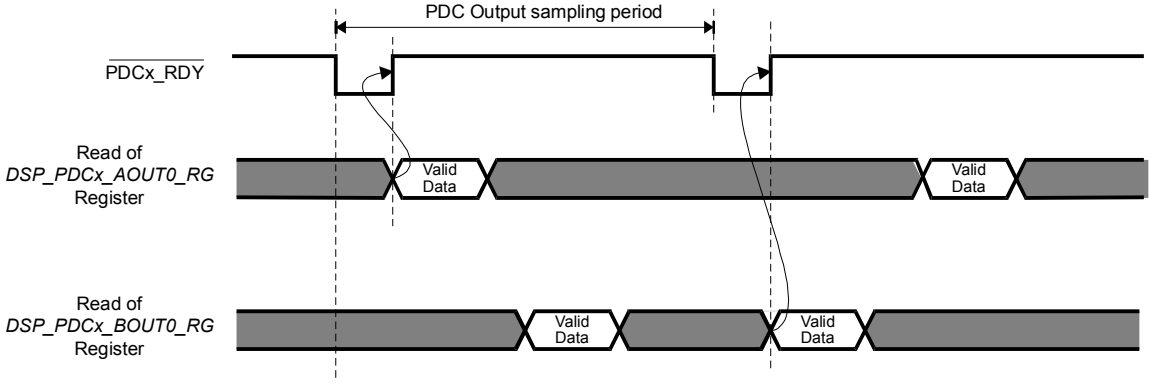


Fig.2-5. Timing diagram for PDC *PARALLEL DIRECT OUTPUT MODE*.

In case *BUFFER RAM PARALLEL OUTPUT MODE* (fig.2-6) is selected (via bit #15 of PDC Control Word #21), then actual 16-bit PDC FIFO output data word must be reconstructed by on-board DSP software using LSB of PDC AOUT and LSB of PDC BOUT output data ports. The LSB of AOUT data must be treated as MSB of 16-bit PDC FIFO output data word, whereas the LSB of BOUT must be treated as LSB of 16-bit PDC FIFO output data word. MSBs of both PDC AOUT and PDC BOUT data words shell be ignored. Particular reconstructed 16-bit FIFO data word (I, Q, Magnitude, Phase, Frequency), or FIFO status/control register is selected by the corresponding addressed words within AOUT/BOUT data ports (*DSP_PDCx_AOUT0_RG* .. *DSP_PDCx_AOUT7_RG* and *DSP_PDCx_BOUT0_RG* .. *DSP_PDCx_BOUT7_RG*). Data transfer in this mode is synchronized by PDC output *PDCx_INT* interrupt signal, which can be can be either polled via *DSP_PDC_STAT_RG* register or generate DSP external interrupt INT-0..3 in case *PDCx_INT* input is selected as the interrupt source via the interrupt selector registers *DSP_MIRQ0_SEL_RG* .. *DSP_MIRQ3_SEL_RG*. *PDCx_INT* interrupt signal can be configured by DSP software to certain PDC FIFO depth threshold (via bits #12..#14 of PDC Control Word #21).

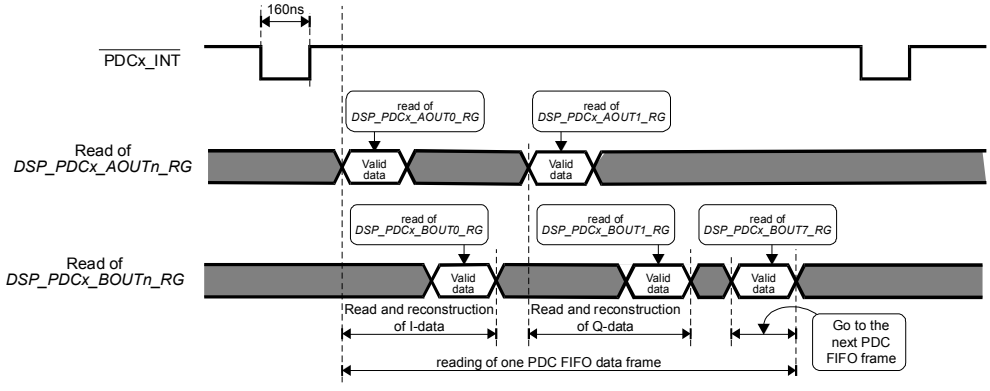


Fig.2-6. Timing diagram for PDC *BUFFER RAM PARALLEL OUTPUT MODE*.

CAUTION

PDCx_INT signal will remain in the *PDCx_INT* =1 state during eight PDC PROCLK cycles (160 ns) only, and will go to the *PDCx_INT* =0 state afterthat.

It is recommended to use *PDCx_INT* signal to interrupt DSP in order to ensure that the *PDCx_INT*=1 condition is not missed by your software.

DSP application software must read PDC FIFO data as quick as possible in order to free space for the next FIFO data frame, which will be filled-in on the next PDC output sampling frequency period, and to ensure correct PDC FIFO operation.

Refer to original documentation for HSP50214 PDC for more details about PDC output data modes and how to use PDC AOUT and BOUT 16-bit output data ports.

Bypass FIFO

On-board 256 KW (256Kx12) high-density synchronous bypass FIFO (fig.2-7) has been included for monitoring and spectral analysis of direct ADC output data.

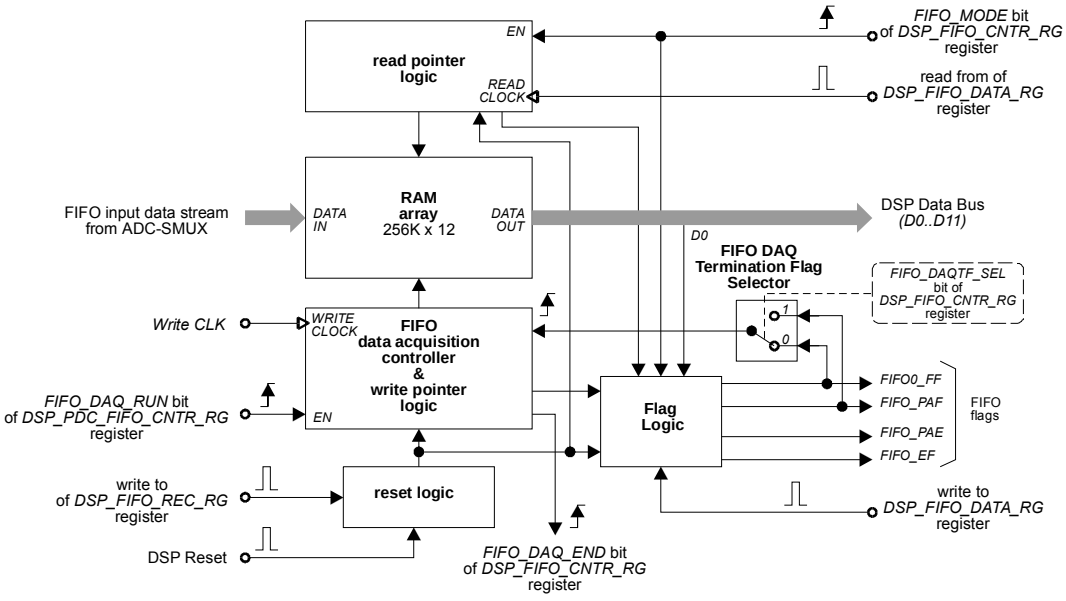


Fig.2-7. Bypass FIFO.

Bypass FIFO comprises of (256K=262,144)x12 static RAM array with read/write pointer logic, FIFO data acquisition controller, and programmable FIFO flag logic.

Bypass FIFO is controlled via *DSP_FIFO_CNTR_RG* register (table 2-7), and can operate in the following modes, which are selected by *FIFO_MODE* bit:

- *FIFO CONFIGURATION MODE*, which is used to program offsets for FIFO partially empty (PAE) and partially full (PAF) flags, which are used in *FIFO DATA ACQUISITION MODE*
- *FIFO DATA ACQUISITION MODE*, which is used to acquire and store input ADC data stream in FIFO RAM array, and further read stored FIFO data by on-board DSP.

FIFO read/write pointer logic and FIFO data acquisition controller are activated in *FIFO DATA ACQUISITION MODE* and are used to control write to FIFO, read from FIFO from on-board DSP, and to activate and terminate data acquisition process.

FIFO flag logic

FIFO flag logic is used in *FIFO DATA ACQUISITION MODE* to terminate FIFO data acquisition process and to monitor FIFO data fill-in conditions. FIFO flag logic comprises of the following flags:

- FIFO empty flag (EF)
- FIFO partially empty flag (PAE)
- FIFO full flag (FF)
- FIFO partially full flag (PAF).

FIFO empty flag (EF), which appears as *FIFO_EF* bit for software polling in read-only *DSP_ADC_FIFO_STAT_RG* register (table 2-8). FIFO EF flag is non-programmable and indicates FIFO empty condition. FIFO EF flag can also generate DSP external interrupts INT-0..3 and NMI (tables 2-14a and 2-14b).

FIFO partially empty flag (PAE), which appears as *FIFO_PAE* bit for software polling in read-only *DSP_ADC_FIFO_STAT_RG* register. FIFO PAE flag can be programmed *FIFO CONFIGURATION MODE*. FIFO PAE flag can also generate DSP external interrupts INT-0..3 and NMI (tables 2-14a and 2-14b). In case FIFO PAE flag is not set, then there is more than N unread samples inside bypass FIFO (N is the programmed offset for FIFO PAE flag). In case FIFO PAE flag is set, then there is N or less number of unread samples inside bypass FIFO.

CAUTION

Offset value for FIFO PAE flag is set to default N=1,023 value on the DSP reset condition, and can be reprogrammed to any value below 256K=262,144 in *FIFO CONFIGURATION MODE*.

FIFO full flag (FF), which appears as *FIFO_FF* bit for software polling in read-only *DSP_ADC_FIFO_STAT_RG* register (table 2-8). FIFO FF flag is non-programmable and indicates FIFO full condition. FIFO FF flag is used as the termination event for FIFO data acquisition controller in *FIFO DATA ACQUISITION MODE* and can also generate DSP external interrupts INT-0..3 and NMI (tables 2-14a and 2-14b).

FIFO partially full flag (PAF), which appears as *FIFO_PAF* bit for software polling in read-only *DSP_ADC_FIFO_STAT_RG* register. FIFO PAE flag can be programmed *FIFO CONFIGURATION MODE*. FIFO PAF flag is used as the termination event for FIFO data acquisition controller in *FIFO DATA ACQUISITION MODE* and can also generate DSP external interrupts INT-0..3 and NMI (tables 2-14a and 2-14b). In case FIFO PAF flag is not set, then there is (2^{18}-M-1) or less number of unread samples inside bypass

FIFO (M is the programmed offset for FIFO PAF flag). In case FIFO PAF flag is set, then there is (2^{18}-M) or more number of unread samples inside bypass FIFO (M is the programmed offset for FIFO PAF flag).

CAUTION

Offset value for FIFO PAF flag is set to default M=1,023 value on the DSP reset condition, and can be reprogrammed to any value below 256K=262,144 in *FIFO CONFIGURATION MODE*.

CAUTION

Offset values for FIFO PAE and PAF flags will not change when performing reset of FIFO logic and read/write pointer by means of writing to ***DSP_FIFO_RES_RG*** register.

Table 2-17 contains description for operation of flag logic of bypass FIFO in *FIFO DATA ACQUISITION MODE*.

Table 2-17. Flag logic of bypass FIFO.

number of words in bypass FIFO	FIFO FF	FIFO PAF	FIFO PAE	FIFO EF
0	0	0	1	1
1 to N	0	0	1	0
(N+1) to (262,144-(M+1)	0	0	0	0
(262,144-M) to 262,143	0	1	0	0
262,144	1	1	0	0

Notes: 1. '*N* ' denotes offset value for FIFO PAE flag.
2. '*M* ' denotes offset value for FIFO PAF flag.

FIFO Configuration Mode

FIFO CONFIGURATION MODE is selected in case ***FIFO_MODE*** bit of ***DSP_FIFO_CNTR_RG*** register (table 2-7) is set to the ***FIFO_MODE*** =0 state. *FIFO CONFIGURATION MODE* must be used to program offsets for FIFO partially empty (PAE) and FIFO partially full (PAF) flags in case default offset values of FIFO PAE/PAF flags, which are set on the DSP reset condition, are not desired for user application.

FIFO PAE and PAF flags shall be programmed by DSP software by means of serial writing to ***DSP_FIFO_DATA_RG*** register (fig.2-8).

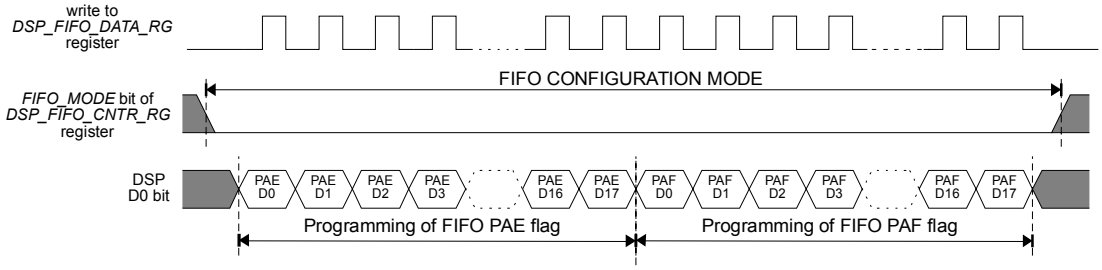


Fig.2-8. Programming of FIFO PAE/PAF flags.

After *FIFO CONFIGURATION MODE* has been selected by setting ***FIFO_MODE*** bit of ***DSP_FIFO_CNTR_RG*** register (table 2-7) to the ***FIFO_MODE*** =0 state, DSP software must perform a series of 36 writes to ***DSP_FIFO_DATA_RG*** register in order to program new 18-bit offset values for FIFO PAE and PAF flags starting from the least significant bit of offset value for FIFO PAE flag and ending with most significant bit of offset value for FIFO PAF flag.

CAUTION

When writing to ***DSP_FIFO_DATA_RG*** register in *FIFO CONFIGURATION MODE*, only D0 data bit is valid and is used to set a series of data bits of programmed offset values for FIFO PAE and PAF flags.

New offset values for FIFO PAE and PAF flags will be set after a series of 36 writes to ***DSP_FIFO_DATA_RG*** register will be completed in *FIFO CONFIGURATION MODE*.

It is not possible for DSP software to read back programmed offset values for FIFO PAE and PAF flags.

CAUTION

It is recommended to perform reset of FIFO logic prior programming FIFO PAE and PAF flags in *FIFO CONFIGURATION MODE*.

FIFO logic can be reset by means of writing to ***DSP_FIFO_RES_RG*** register. Written data is ignored.

FIFO Data Acquisition Mode

FIFO DATA ACQUISITION MODE is selected when ***FIFO_MODE*** bit of ***DSP_FIFO_CNTR_RG*** register (table 2-7) is set to the ***FIFO_MODE*** =1 state. *FIFO DATA ACQUISITION MODE* must be used to acquire and store input ADC data stream in FIFO RAM array, and further read stored FIFO data by on-board DSP.

Input data stream and write clock for bypass FIFO in *FIFO DATA ACQUISITION MODE* come out from the outputs of the corresponding combined output data stream and clock multiplexer of ADC-SMUX (fig.2-4).

FIFO data acquisition process is activated by setting ***FIFO_DAQ_RUN*** bit of ***DSP_FIFO_CNTR_RG*** register (table 2-7) to the ***FIFO_DAQ_RUN***=1 state.

FIFO data acquisition process either terminates normally on termination flag event, or can be aborted by on-board DSP software by means of setting ***FIFO_DAQ_ABORT*** bit of ***DSP_FIFO_CNTR_RG*** register to the ***FIFO_DAQ_ABORT***=1 state. Normal termination of FIFO data acquisition process can occur on either FIFO FF flag event or FIFO PAF flag event depending upon the ***FIFO_DAQTF_SEL*** bit of ***DSP_FIFO_CNTR_RG*** register in accordance with table 2-7.

CAUTION

FIFO FF flag must be used as normal termination event for FIFO data acquisition process in case user application needs to use full FIFO depth (2^{18}=262,144) to store input data stream.

Programmable FIFO PAF flag must be used as normal termination event for FIFO data acquisition process in case user application needs to store short input data streams in FIFO and does not need to use full FIFO depth (2^{18}=262,144).

Timing diagram for FIFO data acquisition process using normal termination on FIFO PAF flag event is presented at fig. 2-9.

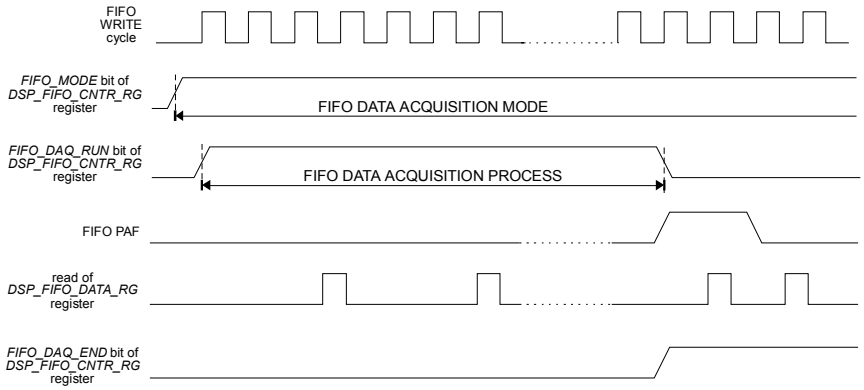


Fig.2-9. Timing diagram for FIFO data acquisition process.

After FIFO data acquisition process has been activated by setting ***FIFO_DAQ_RUN*** bit of ***DSP_FIFO_CNTR_RG*** register to the ***FIFO_DAQ_RUN***=1, each FIFO write clock increments FIFO write pointer, whereas each FIFO read, which is performed by on-board DSP software by reading

DSP_FIFO_DATA_RG register, increments FIFO read pointer and correspondingly decrements FIFO write pointer. Note, that FIFO writes are performed only during active FIFO data acquisition process, whereas FIFO data can be read by on-board DSP software anytime while FIFO data acquisition mode is selected.

CAUTION

FIFO PAF flag is synchronous to FIFO write clock during FIFO data acquisition process, and due to specifics of FIFO synchronization it will be set to active state at the 2nd FIFO write clock after reaching actual FIFO PAF generation condition.

In case it is desired to terminate FIFO data acquisition process normally at FIFO PAF event after acquiring M samples into bypass FIFO, then the offset for FIFO PAF flag must be set to (262,144-M+2) value in *FIFO CONFIGURATION MODE*..

After FIFO data acquisition process has been terminated normally, then *FIFO_DAQ_END* bit of *DSP_FIFO_CNTR_RG* register to the *FIFO_DAQ_END*=1 state. *FIFO_DAQ_END* bit will remain in the *FIFO_DAQ_END*=1 state until it will be reset by means of either setting *FIFO_DAQ_ABORT* bit of *DSP_FIFO_CNTR_RG* register to the *FIFO_DAQ_ABORT*=1 state, or by resetting FIFO logic by means of writing to *DSP_FIFO_RES_RG* register. Active state of *FIFO_DAQ_END* bit of *DSP_FIFO_CNTR_RG* register, which is set on normal termination of FIFO data acquisition process, can be also used to generate DSP external interrupts INT-0..3 and NMI (tables 2-14a and 2-14b).

In case it is required to abort currently active FIFO data acquisition process, then on-board DSP software must either set the *FIFO_DAQ_ABORT* bit of *DSP_FIFO_CNTR_RG* register to the *FIFO_DAQ_ABORT*=1state, or resetting FIFO logic by means of writing to *DSP_FIFO_RES_RG* register.

CAUTION

FIFO reset procedure resets FIFO logic along with read and write pointers, thus making stored FIFO data unavailable for read by on-board DSP software.

Instead, FIFO abort procedure via setting *FIFO_DAQ_ABORT* bit of *DSP_FIFO_CNTR_RG* register will just stop FIFO data acquisition process and freeze last value of FIFO write pointer. Stored FIFO data will remain available for normal read by on-board DSP software. After aborting, the FIFO data acquisition process can be restarted by setting *FIFO_DAQ_RUN* bit of *DSP_FIFO_CNTR_RG* register to the *FIFO_DAQ_RUN*=1 state.

2.4 Serial Peripherals

TORNADO-PX/DDC4 DCM provides a set of on-board peripherals, which are connected to the DSP on-chip McBSP-1 and McBSP-2 serial ports (fig.2-1):

- Two 12-bit 300ksps digital-to-analog converters (XDAC-1 and XDAC-2) for either gain control of external RF amplifiers or general purpose analog outputs. XDAC-1 and XDAC-2 are controlled via transmitter of DSP on-chip McBSP-1 port.
- Two on-board sampling frequency generators (PFG-1 and PFG-2) for accurate setting of virtually any sampling frequency value within the 97.65 kHz .. 65 MHz frequency range for on-board ADC-PDC and ADC-FIFO data paths. PFG-1 and PFG-2 are controlled via transmitter of DSP on-chip McBSP-1 port.
- Two external output serial links (XSL-1 and XSL-2) for digital gain control of external RF amplifiers, however they can be also used for general purpose serial data output. XSL-1 and XSL-2 are controlled via transmitter of DSP on-chip McBSP-1 port.
- 16-bit 300ksps phone DAC (PHDAC) for either audio monitoring or general purpose analog output. PHDAC is controlled via transmitter of DSP on-chip McBSP-2 port.

CAUTION

The receivers of DSP on-chip McBSP-1 and McBSP-2 ports are not used in on-board *TORNADO-PX/DDC4* environment.

DSP on-chip McBSP-1 and McBSP-2 ports configuration

DSP on-chip McBSP-1 and McBSP-2 ports have to be properly configured in order to communicate with on-board serial peripherals.

Transmitter of McBSP-1 port has to be configured to internally generated inversed frame synchronization pulse with one clock advance feature, active low output clock and 32-bit data words. Table 2-18a presents recommended setting for McBSP-1 port control registers.

CAUTION

Serial clock frequency, which is generated by McBSP-1 ports clock generator, must be less than 20 MHz in order to provide correct operation of on-board hardware.

Table 2-18a. Recommended settings for McBSP-1 port control registers.

McBSP-1 port control register	register address	contents of SPSA sub-address register (address 0038H)	recommended register setting
SPCR1	0049H	0000H	0000H
SPCR2	0049H	0001H	0041H
PCR	0049H	000EH	0A0AH
XCR1	0049H	0004H	00A0H
XCR2	0049H	0005H	0001H
SRGR1	0049H	0006H	0004H (TMS320VC5410 DSP) 0007H (TMS320VC5416 DSP)
SRGR2	0049H	0007H	2000H

Transmitter of McBSP-2 port has to be configured to internally generated inversed frame synchronization pulse with one clock advance feature, active low output clock and 16-bit data words. Table 2-18b presents recommended settings for McBSP-2 port control registers.

CAUTION

Serial clock frequency, which is generated by McBSP-2 ports clock generator, must be less than 10 MHz in order to provide correct operation of PHDAC.

Table 2-18b. Recommended settings for McBSP-2 port control registers.

McBSP-1 port control register	register address	contents of SPSA sub-address register (address 0038H)	recommended register setting
SPCR1	0035H	0000H	0000H
SPCR2	0035H	0001H	0041H
PCR	0035H	000EH	0A0AH
XCR1	0035H	0004H	0040H
XCR2	0035H	0005H	0001H
SRGR1	0035H	0006H	0009H (TMS320VC5410 DSP) 000FH (TMS320VC5416 DSP)
SRGR2	0035H	0007H	2000H

command data words for programming XDAC, PFG and XSL serial peripherals

TORNADO-PX/DDC4 DCM has been designed to use 32-bit command data words in order to program XDAC, PFG and XSL serial peripherals via DSP on-chip McBSP-1 port.

CAUTION

In order to transmit 32-bit command data words for XDAC, PFG and XSL serial peripherals over DSP on-chip McBSP-1 port, the on-board DSP software must load McBSP-1 DXR2 and DXR1 transmitter data registers.

McBSP-1 DXR2 register at address 0042H must be loaded first with the most significant 16 bits of 32-bit command data word, whereas McBSP-1 DXR1 register at address 0043H must be loaded after DXR2 register with the least significant 16 bits of 32-bit command data word.

Data transmission of 32-bit XDAC, PFG and XSL command data words over McBSP-1 port occurs after loading the DXR1 register. The McBSP-1 transmitter ready condition must be polled by on-board DSP software only prior loading the DXR2 register.

Command data word formats for programming *TORNADO-PX/DDC4* on-board XDAC, PFG and XSL serial peripherals via DSP on-chip McBSP-1 port are described below in this section.

XDAC-1 and XDAC-2 external gain control DAC

TORNADO-PX/DDC4 DCM provides two on-board 12-bit 300ksps DAC (XDAC-1 and XDAC-2) with unipolar analog outputs for either gain control of external RF amplifiers or general purpose analog outputs.

XDAC-1 and XDAC-2 digital-to-analog converters feature 12-bit data and programmable output signal scale. XDAC output signal scale is common for both XDAC-1 and XDAC-2 and can be programmed to either 2,048 VDC or 4,096 VDC value using commands below.

CAUTION

XDAC output signal scale defaults to 'UNDEFINED' on the power-on condition.

On-board DSP software must first set XDAC output scale prior writing data to XDAC-1 and/or XDAC-2. XDAC output signal scale can be set to either 2,048 VDC o 4,096 VDC using the corresponding *SET XDAC OUTPUT SIGNAL SCALE COMMAND*.

Below are the command data word formats for programming XDAC serial peripherals and XDAC output signal scale.

XDAC-1 Write Command

0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
bit-31	bit-30	Bit-29	bit-28	Bit-27	bit-26	bit-25	bit-24	bit-23	bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

1	0	0	0	DAC-11	DAC-10	DAC-9	DAC-8	DAC-7	DAC-6	DAC-5	DAC-4	DAC-3	DAC-2	DAC-1	DAC-0
bit-15	bit-14	Bit-13	bit-12	Bit-11	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XDAC-2 Write Command

0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
bit-31	bit-30	Bit-29	bit-28	Bit-27	bit-26	bit-25	bit-24	bit-23	bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

0	0	0	0	DAC-11	DAC-10	DAC-9	DAC-8	DAC-7	DAC-6	DAC-5	DAC-4	DAC-3	DAC-2	DAC-1	DAC-0
bit-15	bit-14	Bit-13	bit-12	Bit-11	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Set XDAC 2,048 V Output Signal Scale Command

0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
bit-31	bit-30	Bit-29	bit-28	Bit-27	bit-26	bit-25	bit-24	bit-23	bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1
bit-15	bit-14	Bit-13	bit-12	Bit-11	bit-10	bit-9	bit-8	bit-7	Bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Set XDAC 4,096 V Output Signal Scale Command

0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
bit-31	bit-30	Bit-29	bit-28	Bit-27	bit-26	bit-25	bit-24	bit-23	bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0
bit-15	bit-14	Bit-13	bit-12	Bit-11	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

CAUTION

XDAC-1 and XDAC-2 feature unipolar output with 12-bit linear coding, i.e. 000H value corresponds to 0 VDC output voltage, whereas FFFH value corresponds to maximum output voltage.

CAUTION

The time period between succeeding transmissions of write commands for XDAC-1 and XDAC-2 serial peripherals must be 3.3 uS or greater in order to meet settling time specification for XDAC-1 and XDAC-2 output voltage.

PFG-1 and PFG-2 sampling frequency generators

TORNADO-PX/DDC4 DCM provides two on-board programmable frequency generators (PFG-1 and PFG-2) for accurate setting of sampling frequency for on-board for on-board ADC-PDC and ADC-FIFO data paths (refer to sections “DSP environment” and “RF Signal Processing Control” earlier in this chapter). PFG-1 and

PFG-2 output frequency can be programmed to virtually any value within the 97.65 kHz .. 65 MHz frequency range.

Command data words for programming output frequency values of PFG-1 and PFG-2 sampling frequency generators comprise of 7-bit N-field (N0..N6), 7-bit M-field (M0..M6), 1-bit V-field, 2-bit R-filed (R0..R1) and 2-bit X-field (X0..X1).

PFG-1 Write Command

0	0	0	0	0	0	0	0	N0	N1	N2	N3	N4	N5	N6	M0
Bit-31	Bit-30	Bit-29	bit-28	bit-27	bit-26	bit-25	bit-24	bit-23	bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

M1	M2	M3	M4	M5	M6	V	X0	X1	R0	R1	0	1	1	0	1
Bit-15	bit-14	Bit-13	bit-12	bit-11	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

PFG-2 Write Command

0	0	1	0	0	0	0	0	N0	N1	N2	N3	N4	N5	N6	M0
Bit-31	Bit-30	Bit-29	bit-28	bit-27	bit-26	bit-25	bit-24	bit-23	bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

M1	M2	M3	M4	M5	M6	V	X0	X1	R0	R1	0	1	1	0	1
Bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

CAUTION

PFG-1 and PFG-2 write command data words feature inversed order of data bits for M, N, V, R, and X fields, which are used to program the PFG-1 and PFG-2 output frequency value, i.e. least significant bit of the corresponding filed must be transmitted first.

On-board DSP software must reverse order of data bits for M, N, V, R, and X fields, which are used to program the PFG-1 and PFG-2 output frequency value.

Output frequency value for each of the PFG-1 and PFG-2 sampling frequency generators can be programmed within the 97,65 kHz .. 65 MHz frequency range via M, N, V, R, and X fields of the PFG command as the following:

$$Fout = \frac{10MHz * N * Vv}{M * Rv * Xv * XDIV}$$

where:

Fout output frequency value (MHz) of the corresponding PFG

N is defined by the N-field of the corresponding PFG command

M is defined by the M-field of the corresponding PFG command

Vv value of V-multiplier, which defined by the V-field of the corresponding PFG command in accordance with table 2-19a

Rv value of R-divider, which defined by the R-field of the corresponding PFG command in accordance with table 2-19b

Xv value of X-divider, which defined by the X-field of the corresponding PFG command in accordance with table 2-19c

XDIV optional output divider, which can be set to either :1 or :8 value in accordance with the corresponding ***PFGx_FDIV8_EN*** bit of ***DSP_ADC_CLKSEL_RG*** register (table 2-5).

Table 2-19a. V-multiplier programming for PFG.

value of the V-field of PFG command	**value of the V-multiplier (*Vv*)**
0	X1
1	X8

Table 2-19b. R-divider programming for PFG.

value of the R-field of PFG command		**value of the R-divider (*Rv*)**
R1	***R0***	
0	*0*	:1
0	*1*	:2
1	*0*	:4
1	*1*	:8

Table 2-19c. X-divider programming for PFG.

value of the X-field of PFG command		value of the X-divider (*Xv*)
X1	***X0***	
0	*0*	:1
0	*1*	:2
1	*0*	:4
1	*1*	:8

The following restrictions are applicable for N, M and V-fields of PFG-1 and PFG-2 command data words when programming PFG-1 and PFG-2 sampling frequency generators:

$$3 \le N \le 75$$

$$3 \le M \le 50$$

$$50MHz \le \frac{10MHz * N * Vv}{M} \le 250MHz$$

CAUTION

The time period between succeeding transmissions of write commands for PFG-1 and PFG-2 sampling frequency generators must be 200 uS or greater in order to meet lock time specification for PFG-1 and PFG-2 on-chip PLL.

XSL-1 and XSL-2 external output serial links

TORNADO-PX/DDC4 DCM provides two on-board external output serial links (XSL-1 and XSL-2) for digital gain control of external RF amplifiers. XSL-1 and XSL-2 can be also used for general purpose serial data output.

Both XSL-1 and XSL-2 external output serial links feature programmable data format, programmable serial clock polarity, and programmable serial clock framing feature via *DSP_XSL_FMT_RG* register (table 2-16). These features allow to minimize digital noise for external RF gain amplifiers and to configure XSL-1 and XSL-2 to interface to virtually any external devices.

TORNADO-PX/DDC4 on-board XSL-1 and XSL-2 external serial links have been designed to interface to external hardware by means of four signals, which are available at JP2 external I/O connector (refer to Appendix A):

- XSL serial clock output (*XSL-CLK*), which is common for both XSL-1 and XSL-2 external serial links. *XSL-CLK* can be programmed by on-board DSP software and is actually the serial clock of

transmitter of the DSP on-chip McBSP-1 port. Polarity and framing feature of *XSL-CLK* output can be programmed via *XSL-CLK_POS* and *XSL-CLK_FRM* bits of *DSP_XSL_FMT_RG* register (table 2-16). For more details refer to subsection "XSL timing" later in this section.

- XSL serial data output (*XSL-DATA*), which is common for both XSL-1 and XSL-2 external serial links. Formats of data transmissions over XSL-1 and XSL-2 can be programmed separately to either 8 bits, or 16 bits, or 24 bits or 30 bits via {*XSL1-FMT1*, *XSL1-FMT0*} and {*XSL2-FMT1*, *XSL2-FMT0*} bits correspondingly of *DSP_XSL_FMT_RG* register (table 2-16). For more details refer to subsection "XSL timing" later in this section.
- XSL serial frame synchronization outputs (*XSL1-FSYNC* and *XSL2-FSYNC*), which are active low outputs and which are used to identify transmission over XSL-1 and XSL-2 correspondingly.

Below are command data words for initialization of data transmission over XSL-1 and XSL-2 external output serial links for different XSL serial data formats (8/16/24/30 data bits), which are defined via {*XSL1-FMT1*, *XSL1-FMT0*} and {*XSL2-FMT1*, *XSL2-FMT0*} bits of *DSP_XSL_FMT_RG* register for XSL-1 and XSL-2 correspondingly.

XSL-1 Write Command

(8-bit XSL data format, which corresponds to {XSL1-DF1,XSL1-DF0}={0,0} setting of DSP_XSL_FMT_RG register)

1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit-31	Bit-30	Bit-29	bit-28	bit-27	bit-26	bit-25	bit-24	bit-23	bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

0	0	0	0	0	0	0	0	XSL-7	XSL-6	XSL-5	XSL-4	XSL-3	XSL-2	XSL-1	XSL-0
Bit-15	bit-14	Bit-13	bit-12	bit-11	bit-10	bit-9	Bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XSL-1 Write Command

(16-bit XSL data format, which corresponds to {XSL1-DF1,XSL1-DF0}={0,1} setting of DSP_XSL_FMT_RG register)

1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit-31	Bit-30	Bit-29	bit-28	bit-27	bit-26	bit-25	bit-24	bit-23	bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

XSL-15	XSL-14	XSL-13	XSL-12	XSL-11	XSL-10	XSL-9	XSL-8	XSL-7	XSL-6	XSL-5	XSL-4	XSL-3	XSL-2	XSL-1	XSL-0
Bit-15	Bit-14	Bit-13	bit-12	bit-11	bit-10	bit-9	Bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XSL-1 Write Command

(24-bit XSL data format, which corresponds to {XSL1-DF1,XSL1-DF0}={1,0} setting of DSP_XSL_FMT_RG register)

1	0	0	0	0	0	0	0	XSL-23	XSL-22	XSL-21	XSL-20	XSL-19	XSL-18	XSL-17	XSL-16
Bit-31	Bit-30	Bit-29	bit-28	bit-27	bit-26	bit-25	bit-24	bit-23	Bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

XSL-15	XSL-14	XSL-13	XSL-12	XSL-11	XSL-10	XSL-9	XSL-8	XSL-7	XSL-6	XSL-5	XSL-4	XSL-3	XSL-2	XSL-1	XSL-0
Bit-15	Bit-14	Bit-13	bit-12	bit-11	bit-10	bit-9	Bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XSL-1 Write Command

(30-bit XSL data format, which corresponds to {XSL1-DF1,XSL1-DF0}={1,1} setting of DSP_XSL_FMT_RG register)

1	0	XSL-29	XSL-28	XSL-27	XSL-26	XSL-25	XSL-24	XSL-23	XSL-22	XSL-21	XSL-20	XSL-19	XSL-18	XSL-17	XSL-16
Bit-31	Bit-30	Bit-29	bit-28	bit-27	bit-26	bit-25	bit-24	bit-23	Bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

XSL-15	XSL-14	XSL-13	XSL-12	XSL-11	XSL-10	XSL-9	XSL-8	XSL-7	XSL-6	XSL-5	XSL-4	XSL-3	XSL-2	XSL-1	XSL-0
Bit-15	bit-14	Bit-13	bit-12	bit-11	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XSL-2 Write Command

(8-bit XSL data format, which corresponds to {XSL2-DF1,XSL2-DF0}={0,0} setting of DSP_XSL_FMT_RG register)

1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit-31	Bit-30	Bit-29	bit-28	bit-27	bit-26	bit-25	bit-24	bit-23	bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

0	0	0	0	0	0	0	0	XSL-7	XSL-6	XSL-5	XSL-4	XSL-3	XSL-2	XSL-1	XSL-0
Bit-15	Bit-14	Bit-13	bit-12	bit-11	bit-10	bit-9	Bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XSL-2 Write Command

(16-bit XSL data format, which corresponds to {XSL2-DF1,XSL2-DF0}={0,1} setting of DSP_XSL_FMT_RG register)

1	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*
Bit-31	Bit-30	Bit-29	bit-28	bit-27	bit-26	bit-25	bit-24	bit-23	bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

XSL-15	*XSL-14*	*XSL-13*	*XSL-12*	*XSL-11*	*XSL-10*	*XSL-9*	*XSL-8*	*XSL-7*	*XSL-6*	*XSL-5*	*XSL-4*	*XSL-3*	*XSL-2*	*XSL-1*	*XSL-0*
Bit-15	Bit-14	Bit-13	bit-12	bit-11	bit-10	bit-9	Bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XSL-2 Write Command

(24-bit XSL data format, which corresponds to {XSL2-DF1,XSL2-DF0}={1,0} setting of DSP_XSL_FMT_RG register)

1	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*XSL-23*	*XSL-22*	*XSL-21*	*XSL-20*	*XSL-19*	*XSL-18*	*XSL-17*	*XSL-16*
Bit-31	Bit-30	Bit-29	bit-28	bit-27	bit-26	bit-25	bit-24	bit-23	Bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

XSL-15	*XSL-14*	*XSL-13*	*XSL-12*	*XSL-11*	*XSL-10*	*XSL-9*	*XSL-8*	*XSL-7*	*XSL-6*	*XSL-5*	*XSL-4*	*XSL-3*	*XSL-2*	*XSL-1*	*XSL-0*
Bit-15	Bit-14	Bit-13	bit-12	bit-11	bit-10	bit-9	Bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XSL-2 Write Command

(30-bit XSL data format, which corresponds to {XSL2-DF1,XSL2-DF0}={1,1} setting of DSP_XSL_FMT_RG register)

1	*1*	*XSL-29*	*XSL-28*	*XSL-27*	*XSL-26*	*XSL-25*	*XSL-24*	*XSL-23*	*XSL-22*	*XSL-21*	*XSL-20*	*XSL-19*	*XSL-18*	*XSL-17*	*XSL-16*
Bit-31	Bit-30	Bit-29	bit-28	bit-27	bit-26	bit-25	bit-24	bit-23	Bit-22	bit-21	bit-20	bit-19	Bit-18	bit-17	Bit-16

XSL-15	*XSL-14*	*XSL-13*	*XSL-12*	*XSL-11*	*XSL-10*	*XSL-9*	*XSL-8*	*XSL-7*	*XSL-6*	*XSL-5*	*XSL-4*	*XSL-3*	*XSL-2*	*XSL-1*	*XSL-0*
Bit-15	bit-14	Bit-13	bit-12	bit-11	bit-10	bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

XSL timing and data formats

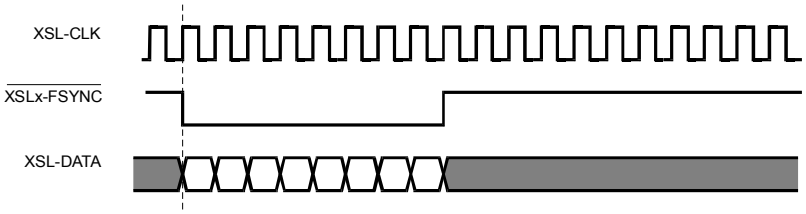
XSL-1 and XSL-2 provide active low frame synchronization outputs (*XSL1-FSYNC* and *XSL2-FSYNC*), which are used to identify transmission over XSL-1 and XSL-2 correspondingly. *XSL1-FSYNC* and *XSL2-FSYNC* outputs are set active during transmission of all data bits for XSL-1 and XSL-2 correspondingly.

Polarity of *XSL-CLK* output can be programmed to either positive or negative polarity via *XSL-CLK_POL* bit of *DSP_XSL_FMT_RG* register (table 2-16), whereas the framing feature of *XSL-CLK* output is programmed either to continuous or framed via *XSL-CLK_FRM* bit of *DSP_XSL_FMT_RG* register (refer to table 2-16 and fig.2-10).

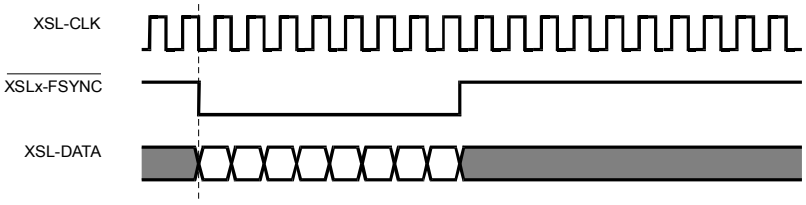
CAUTION

In case the framing feature for *XSL-CLK* is enabled, then *XSL-CLK* output defaults to the logical '0' value outside of active *XSL1-FSYNC* and *XSL2-FSYNC* frame synchronization outputs.

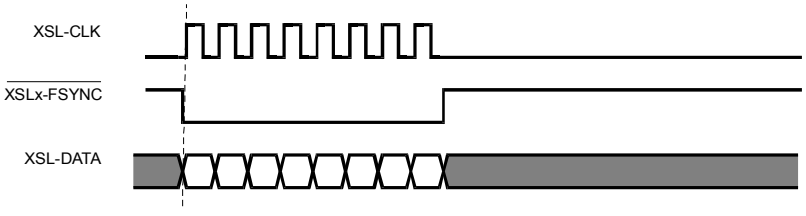
Data formats for XSL-1 and XSL-2 external output serial links (data bit length of output XSL data frame) can be configured separately for XSL-1 and XSL-2 to either 8 bits, or 16 bits, or 24 bits, or 30 bits via {*XSL1-DF1,XSL1-DF0*} and {*XSL2-DF1,XSL2-DF0*} bits correspondingly of *DSP_XSL_FMT_RG* register (table 2-16). Figure 2-11 presents XSL timing diagrams for different XSL data formats and continuous serial clock with positive polarity.



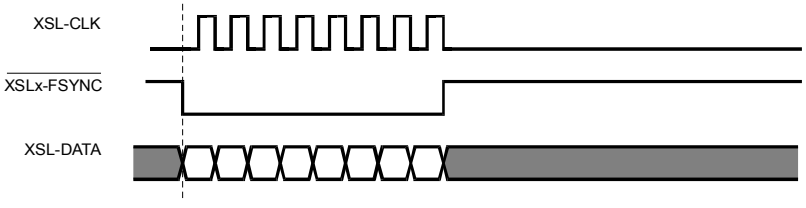
A) Continuous XSL serial clock with positive polarity
(*XSL-CLK_POL*=0, *XSL-CLK_FRM*=0, {*XSLx_DF1, XSLx_DF0*}={0,0})



B) Continuous XSL serial clock with negative polarity
(*XSL-CLK_POL*=1, *XSL-CLK_FRM*=0, {*XSLx_DF1, XSLx_DF0*}={0,0}).



C) Framed XSL serial clock with positive polarity
(*XSL-CLK_POL*=0, *XSL-CLK_FRM*=1, {*XSLx_DF1, XSLx_DF0*}={0,0}).



D) Framed XSL serial clock with negative polarity
(*XSL-CLK_POL*=1, *XSL-CLK_FRM*=1. {*XSLx_DF1, XSLx_DF0*}={0,0}).

Fig. 2-10. Polarity and framing of XSL serial clock.

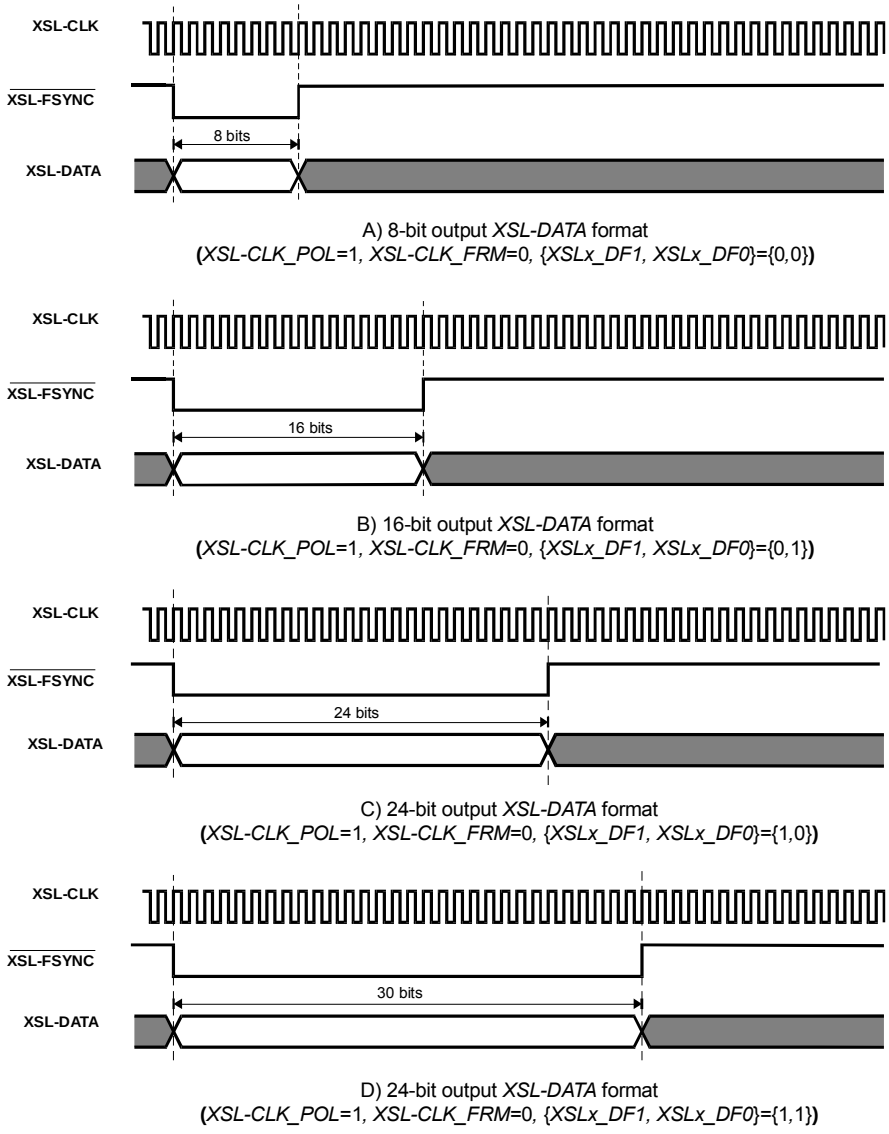


Fig. 2-11. XSL transmission for different data formats.

PHDAC phone DAC

TORNADO-PX/DDC4 DCM provides on-board 16-bit 300ksps audio quality DAC with bipolar output for connection to either external phones (PHDAC) or general purpose analog output.

PHDAC analog output can be set by transmission of 16-bit PHDAC data word via DSP on-chip McBSP-2 port. In order to transmit 16-bit data word for PHDAC via transmitter of DSP on-chip McBSP-2 port, the on-board DSP software must load McBSP-2 DXR1 transmitter data register at address 0033H.

PHDAC Write Data Word

DAC-15	*DAC-14*	*DAC-13*	*DAC-12*	*DAC-11*	*DAC-10*	*DAC-9*	*DAC-8*	*DAC-7*	*DAC-6*	*DAC-5*	*DAC-4*	*DAC-3*	*DAC-2*	*DAC-1*	*DAC-0*
bit-15	bit-14	Bit-13	bit-12	Bit-11	bit-10	Bit-9	bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

CAUTION

PHDAC feature bipolar analog output with 16-bit complement coding, i.e. 000H value corresponds to 0 VDC output voltage, whereas 7FFFH value corresponds to maximum positive output voltage and 8000H value corresponds to minimum negative output voltage

CAUTION

The time period between succeeding transmissions of 16-bit data words to PHDAC must be 3.3 uS or greater in order to meet settling time specification for PHDAC.

2.5 Host PIOX-16 Interface

Host 16-bit PIOX-16 interface of *TORNADO-PX/DDC4* DCM provides access from host *TORNADO* DSP system/controller to on-board DRPAM and DSP on-chip HPI port, and controls operation of on-board DSP via a set of control registers. On-board JP1 connector of *TORNADO-PX/DDC4* DCM (fig.A-1) is used to install into PIOX-16 site of host *TORNADO* DSP system/controller.

CAUTION

Host PIOX-16 interface of *TORNADO-PX/DDC4* DCM is enabled during host operation mode only, i.e. for *HOST/NO-BMODE*, *HOST/FLASH8-BMODE* and *HOST/HPI-BMODE* DSP bootmodes (refer to table 2-1 for more details), and is switched off during stand-alone operation mode, i.e. for *SA/NO-BMODE* and *SA/FLASH8-BMODE* DSP bootmodes.

host PIOX-16 interface address map

Host PIOX-16 interface address map for of *TORNADO-PX/DDC4* DCM comprises of control register area, DSP HPI port area, DPRAM area, and DPSEM area. Table 2-20 specifies details about host PIOX-16 interface address map.

Table 2-20. Host PIOX-16 interface address map.

address area	value on PIOX-16 reset condition	access mode	address range (in 16-bit data words)
Control Register area: *HOST_CNTR1_RG* registers (DSP reset control)	0H (DSP is in RESET state)	r/w	*BA*+0000H (bits D0..D3 only)
Control Register area: *HOST_CNTR2_RG* register (DSP bootmode control and HPI/DPRAM timeout control enable)	0H (*HOST/NO-BMODE* bootmode, DPRAM/HPI error control disabled)	r/w	*BA*+0001H (bits D0..D3 only)
Control Register area: *HOST_IE_RG* register (interrupt enable)	0H (interrupts are disabled)	r/w	*BA*+0010H (bits D0..D3 only)
Control Register area: *HOST_IS_RG* register (interrupt status)	-	r	*BA*+0011H (bits D0..D3 only)
Control Register area: *HOST_HIRQ_SEL_RG* register (PIOX-16 interrupt line selector)	0H (no PIOX-16 interrupt request)	r/w	*BA*+0012H (bits D0..D3 only)
Control Register area: *HOST_CLR_HPI_TMOUT_ERR_RG* register (clear HPI timeout error)	-	w	*BA*+0020H (written data is ignored)
Control Register area: *HOST_CLR_DPRAM_TMOUT_ERR_RG* register (clear DPRAM timeout error)	-	w	*BA*+0021H (written data is ignored)
HPI area: *HOST_HPIC_RG_LSB* register (HPIC LSB) (*refer to TMS320C54x DSP documentation for more details)*	00H	r/w	*BA*+0060H (bits D0..D7 only)
HPI area: *HOST_HPIC_RG_MSB* register (HPIC MSB) (*refer to TMS320C54x DSP documentation for more details)*	-	r/w	*BA*+0061H (bits D0..D7 only)
HPI area: *HOST_HPID_AINC_RG_LSB* register (LSB of HPI data register with address postincrement) (*refer to TMS320C54x DSP documentation for more details)*	-	r/w	*BA*+0062H (bits D0..D7 only)

HPI area: *HOST_HPID_AINC_RG_MSB* register (MSB of HPI data register with address postincrement) (*refer to TMS320C54x DSP documentation for more details)*	-	r/w	*BA*+0063H (bits D0..D7 only)
HPI area: *HOST_HPIA_RG_LSB* register (HPIA LSB) (*refer to TMS320C54x DSP documentation for more details)*	-	r/w	*BA*+0064H (bits D0..D7 only)
HPI area: *HOST_HPIA_RG_MSB* register (HPIA MSB) (*refer to TMS320C54x DSP documentation for more details)*	-	r/w	*BA*+0065H (bits D0..D7 only)
HPI area: *HOST_HPID_RG_LSB* register (LSB of HPI data register) (*refer to TMS320C54x DSP documentation for more details)*	-	r/w	*BA*+0066H (bits D0..D7 only)
HPI area: *HOST_HPID_RG_MSB* register (MSB of HPI data register) (*refer to TMS320C54x DSP documentation for more details)*	-	r/w	*BA*+0067H (bits D0..D7 only)
DPSEM area (dual-port semaphores)	-	r/w	*BA*+0070H…*BA*+0077H (bit D0 only)
DPRAM area (dual-port memory)	-	r/w	*BA*+8000H...*BA*+FFFFH
DPRAM area: *HOST_DPRAM_HM_RQ* *(Host-to-DSP interrupt request via DPRAM)*	-	r/w	*BA*+FFFFH
DPRAM area: *HOST_DPRAM_MH_RQ* *(DSP-to-Host interrupt request via DPRAM)*	-	r/w	*BA*+FFFEH

Notes: 1. Access modes: *r* - read only, *w* - write only, *r/w* - read/write.
2. '*BA*' denotes base address for host PIOX-16 interface within the address map of DSP of host *TORNADO* DSP system/controller.

CAUTION

DSP software of host *TORNADO* DSP system/controller must access different address areas of host PIOX-16 interface of *TORNADO-PX/DDC4* DCM at the PIOX-16 interface base address, which is specific for particular *TORNADO* DSP system/controller (refer to documentation for your *TORNADO* DSP system/control for more details about addressing PIOX-16 interface area).

CAUTION

When accessing Control Register area of host PIOX-16 interface from host *TORNADO* DSP system/controller, only data bits D0..D3 are valid.

When accessing HPI area of host PIOX-16 interface from host *TORNADO* DSP system/controller, only data bits D0..D7 are valid.

When accessing DPSEM area of host PIOX-16 interface from host *TORNADO* DSP system/controller, only data bit D0 is valid with bits D1..D15 being extension of D0 bit value.

When accessing DPRAM area of host PIOX-16 interface from host *TORNADO* DSP system/controller, all D0..D15 data bits are valid.

CAUTION

Reset signal for on-board PIOX-16 interface of host *TORNADO* DSP system/controller must be set to inactive state prior communication with *TORNADO-PX/DDC4* DCM.

HOST_CNTR1_RG register for DSP reset control

TORNADO-PX/DDC4 on-board DSP reset control in host operation mode is performed via *HOST_CNTR1_RG* register of host PIOX-16 interface. Note, that when accessing *HOST_CNTR1_RG* register, only data bits D0..D3 are valid.

HOST_CNTR1_RG register (r/w)

X	*0*	*0*	*0*	*M_GO (r/w, 0+)*
bits 15..4	bit-3	bit-2	bit-1	bit-0

Table 2-21 describes details about *HOST_CNTR1_RG* register bits.

Table 2-21. Register bits of *HOST_CNTR1_RG* register.

Register bits or bit fields	access mode	value on host PIOX-16 interface reset	Description
M_GO	r/w	0	Controls reset signal for on-board DSP in host operation mode. *M_GO*=0 corresponds to the RESET state of on-board DSP, i.e. active reset signal is applied to the on-board DSP. *M_GO*=1 corresponds to the RUN state of on-board DSP, i.e. no active reset signal is applied to the on-board DSP and DSP is executing application program.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

HOST_CNTR2_RG register for DSP bootmode and DPRAM/HPI timeout enable control

HOST_CNTR2_RG register of host PIOX-16 interface must be used in order to set the DSP bootmode in host operation mode (refer to section "DSP Environment" earlier in this chapter and table 2-1) and to enable timeout control for host-to-HPI and host-to-DPRAM accesses host PIOX-16 interface. Note, that when accessing *HOST_CNTR2_RG* register, only data bits D0..D3 are valid.

HOST_CNTR2_RG register (r/w)

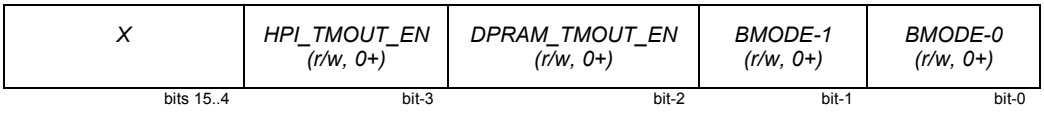


Table 2-22 describes details about *HOST_CNTR2_RG* register bits.

Table 2-22. Register bits of *HOST_CNTR2_RG* register.

register bits or bit fields	access mode	value on host PIOX-16 interface reset	Description
{*BMODE-1, BMODE-0*}	R/w	{0,0}	Defines bootmode for on-board DSP in host operation mode. Refer to table 2-1 for more details. Note, that bits {*BMODE-1, BMODE-0*} can be updated by host DSP software only during DSP is in the RESET state, i.e. when bit *M_GO* of *HOST_CNTR1_RG* register of host PIOX-16 interface is set to *M_GO*=0 state (refer to table 2-20). {*BMODE-1, BMODE-0*}={0,0} corresponds to *HOST/NO-BMODE* microprocessor (MP) start-up mode for on-board DSP without boot process. DSP reset is controlled by *M_GO* bit of *HOST_CNTR1_RG* register of host PIOX-16 interface. This mode is set as default on host PIOX-16 interface reset condition. {*BMODE-1, BMODE-0*}={0,1} corresponds to *HOST/FLASH8-BMODE* microcontroller (MC) start-up mode for on-board DSP with boot from on-board 8-bit FLASH memory. DSP reset is controlled by *M_GO* bit of *HOST_CNTR1_RG* register of host PIOX-16 interface. {*BMODE-1, BMODE-0*}={1,0} corresponds to *HOST/HPI-BMODE* microcontroller (MC) start-up mode for on-board DSP with boot via DSP on-chip HPI port. DSP reset is controlled by *M_GO* bit of *HOST_CNTR1_RG* register of host PIOX-16 interface. {*BMODE-1, BMODE-0*}={1,1} is reserved and shall not be used for definition of bootmode for on-board DSP.

DPRAM_TMOUT_EN	r/w	0	Timeout enable for host-to-DPRAM access via host PIOX-16 interface. *DPRAM_TMOUT_EN*=0 corresponds to disabled timeout control for host-to-DPRAM accesses. In case any DPRAM access collision occurs with continuous missing DPRAM ready signal, then host PIOX-16 interface access cycle will remain active until DPRAM ready signal comes active. Active host-to-DPRAM access cycle can be aborted only by applying reset signal for DSP of host *TORNADO* DSP system/controller. *DPRAM_TMOUT_EN*=0 corresponds to enabled timeout control for host-to-DPRAM access. In case any DPRAM access collision occurs with missing DPRAM ready signal, then host PIOX-16 interface access cycle will remain active either until DPRAM ready signal comes active or until timeout expires, whichever comes first, and there is no need to apply reset signal to DSP of host *TORNADO* DSP system/controller in order to terminate pending host-to-DPRAM access cycle. In case the DPRAM access timeout event will take place, then the *DPRAM_TMOUT_ERR* bit of *HOST_IS_RG* will be set and host PIOX-16 interrupt can be generated. Timeout period for host-to-DPRAM access is set to 320 ns.
HPI_TMOUT_EN	r/w	0	Timeout enable for host-to-HPI access via host PIOX-16 interface. *HPI_TMOUT_EN*=0 corresponds to disabled timeout control for host-to-HPI accesses. In case any HPI access collision occurs with continuous missing HPI ready signal (for example on-board DSP will execute IDLE 3 instruction), then host PIOX-16 interface access cycle will remain active until DSP HPI ready signal comes active. Active host-to-HPI access cycle can be aborted only by applying reset signal for DSP of host *TORNADO* DSP system/controller. *HPI_TMOUT_EN*=0 corresponds to enabled timeout control for host-to-HPI access. In case any HPI access collision occurs with missing HPI ready signal, then host PIOX-16 interface access cycle will remain active either until DSP HPI ready signal comes active or until timeout expires, whichever comes first, and there is no need to apply reset signal to DSP of host *TORNADO* DSP system/controller in order to terminate pending host-to-DPRAM access cycle. In case the DSP HPI access timeout event will take place, then the *HPI_TMOUT_ERR* bit of *HOST_IS_RG* will be set and host PIOX-16 interrupt can be generated. Timeout period for host-to-HPI access is set to 320 ns.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP bootmode in host operation mode is defined by bits {***BMODE-1, BMODE-0***} of ***HOST_CNTR2_RG*** register (refer to section “DSP Environment” earlier in this chapter and table 2-1), whereas timeout control for host-to-DPRAM and host-to-HPI access cycles is enabled via bits ***DPRAM_TMOUT_EN*** and ***HPI_TMOUT_EN*** correspondingly.

CAUTION

Note, that bits {*BMODE-1, BMODE-0*} of *HOST_CNTR1_RG* register can be updated by host DSP software only during DSP is in the RESET state, i.e. when bit *M_GO* of *HOST_CNTR1_RG* register of host PIOX-16 interface is set to *M_GO*=0 state (refer to table 2-20).

Timeout control for host-to-DPRAM and host-to-HPI access cycles of host PIOX-16 interface of *TORNADO-PX/DDC4* DCM delivers reliable and self-diagnostic operation of host DSP software of host *TORNADO* DSP system/controller. In case the timeout feature is enabled, then the pending host-to-DPRAM or host-to-HPI access cycle can be automatically terminated by on-board hardware and the corresponding either *DPRAM_TMOUT_ERR* or *HPI_TMOUT_ERR* timeout error flag will be set in case of any exception or misoperation condition within *TORNADO-PX/DDC4* on-board DSP environment.

CAUTION

DPRAM_TMOUT_ERR and *HPI_TMOUT_ERR* timeout error flags are available for software polling via *HOST_IS_RG* register of host PIOX-16 interface, and can generate interrupt request to DSP of host *TORNADO* DSP system/controller via host PIOX-16 interface in case the corresponding interrupt enable bit is set in *HOST_IE_RG* register (refer to table 2-23) and host PIOX-16 interrupt request line is selected via *HOST_HIRQ_SEL_RG* register (refer to table 2-25).

Once *DPRAM_TMOUT_ERR* or *HPI_TMOUT_ERR* flag has been set, it remains in active state until it will be cleared by host *TORNADO* DSP system/controller by means of writing to *HOST_CLR_DPRAM_TMOUT_ERR_RG* and *HOST_CLR_HPI_TMOUT_ERR_RG* registers correspondingly of host PIOX-16 interface.

Figure 2-12 demonstrates operation of timeout controller for host-to-DPRAM and host-to-HPI access cycles of host PIOX16 interface of *TORNADO-PX/DDC4* DCM.

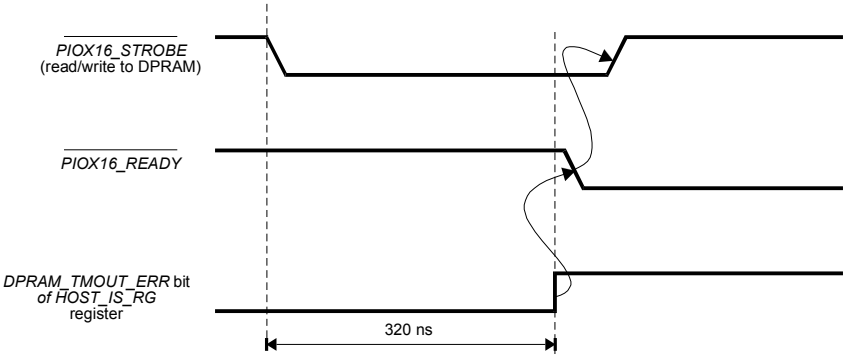


Fig.2-12a. Timeout control for host-to-DPRAM access cycle of host PIOX-16 interface.

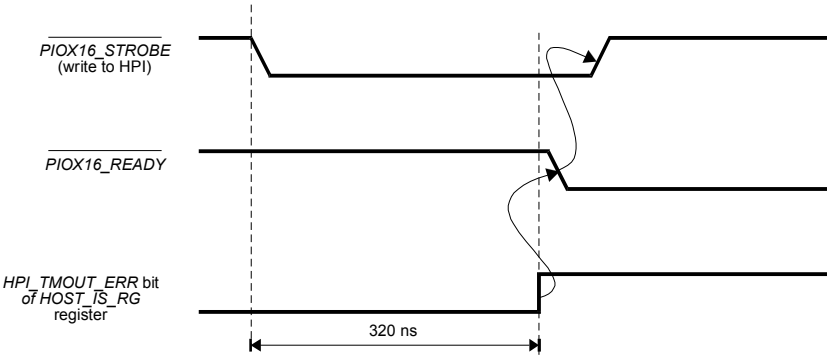


Fig.2-12b. Timeout control for host-to-HPI access cycle of host PIOX-16 interface.

HOST_CLR_DPRAM_TMOUT_ERR_RG and HOST_CLR_HPI_TMOUT_ERR_RG registers for resetting timeout errors for host-to-DPRAM and host-to-HPI accesses

HOST_CLR_DPRAM_ERR_RG and *HOST_CLR_HPI_TMOUT_ERR_RG* write-only registers of host PIOX-16 interface shall be used in order to reset *DPRAM_TMOUT_ERR* and *HPI_TMOUT_ERR* timeout error flags correspondingly. Note, that when writing to *HOST_CLR_DPRAM_ERR_RG* and *HOST_CLR_HPI_TMOUT_ERR_RG* write-only registers, written data is ignored.

HOST_CLR_DPRAM_TMOUT_ERR_RG register (w)

bits 15..4	bit-3	bit-2	bit-1	bit-0
X	x	x	X	X

HOST_CLR_HPI_TMOUT_ERR_RG register (w)

bits 15..4	bit-3	bit-2	bit-1	bit-0
X	X	x	X	X

host PIOX-16 interrupt control

Host PIOX-16 interface of *TORNADO-PX/DDC4* DCM can generate active interrupt request to DSP of host *TORNADO* DSP system/controller from the following interrupt sources:

- *TORNADO-PX/DDC4* on-board DSP writes to *DSP_DPRAM_MH_RQ* DPRAM memory location (refer to section “DSP Environment” earlier in this chapter for more details)
- *TORNADO-PX/DDC4* on-board DSP sets host request via DSP on-chip HPI port. i.e. on-board DSP sets *HINT* bit of HPIC register (refer to section “DSP Environment” earlier in this chapter and original TI TMS320C54x documentation for more details)
- timeout condition occurs for host-to-DPRAM access via host PIOX-16 interface
- timeout condition occurs for host-to-HPI access via host PIOX-16 interface.

Each of the above interrupt sources is available for software polling via *HOST_IS_RG* (table 2-24) host interrupt status register and can be enabled to generate host PIOX-16 interrupt request via *HOST_IE_RG* (table 2-23) interrupt enable register.

CAUTION

Host PIOX-16 interrupt request is generated as logical OR of enabled interrupt request sources.

TORNADO-PX/DDC4 DCM allows software selection of particular host PIOX-16 interrupt request line, which will be used to generate interrupt request to DSP of host *TORNADO* DSP system/controller via host PIOX-16 interface. Selection of particular host interrupt request line is performed via *HOST_HIRQ_SEL_RG* host interrupt line selection register (table 2-25).

HOST_IE_RG host interrupt source enable register

HOST_IE_RG register of host PIOX-16 interface must be used to set interrupt enable masks for different host PIOX-16 interrupt request sources. Note, that when accessing *HOST_IE_RG* register, only data bits D0..D3 are valid.

HOST_IE_RG register (r/w)

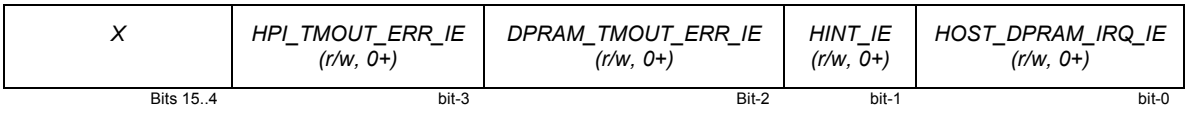


Table 2-23 describes details about *HOST_IE_RG* register bits.

Table 2-23. Register bits of *HOST_IE_RG* register.

register bits or bit fields	access mode	value on host PIOX-16 interface reset	Description
HOST_DPRAM_IRQ_IE	r/w	0	Enable mask for host PIOX-16 interrupt request on DSP write to *DSP_PRAM_MH_RQ* DPRAM address event (refer to section “DSP Environment” earlier in this chapter for more details). *HOST_DPRAM_IRQ_IE* =0 corresponds to disabled host PIOX-16 interrupt request on DSP writes to *DSP_PRAM_MH_RQ* memory address of DPRAM. *HOST_DPRAM_IRQ_IE* =1 enables host PIOX-16 interrupt request on DSP write to *DSP_PRAM_MH_RQ* memory address of DPRAM.
HINT_IE	r/w	0	Enable mask for host PIOX-16 interrupt request on active DSP-to-Host interrupt request via DSP on0chip HPI port (refer to original TI TMS320C54x documentation for more details). *HINT_IE*=0 corresponds to disabled host PIOX-16 interrupt request on DSP-to-Host interrupt request via DSP on-chip HPI port. *HINT_IE*=1 enables host PIOX-16 interrupt request on DSP-to-Host interrupt request via DSP on-chip HPI port.
DPRAM_TMOUT_ERR_IE	r/w	0	Enable mask for host PIOX-16 interrupt request on timeout condition for host-to-DPRAM access via host PIOX-16 interface. *DPRAM_TMOUT_ERR_IE*=0 corresponds to disabled host PIOX-16 interrupt request on timeout condition for host-to-DPRAM access via host PIOX-16 interface. *DPRAM_TMOUT_ERR_IE*=1 enables host PIOX-16 interrupt request on timeout condition for host-to-DPRAM access via host PIOX-16 interface.
HPI_TMOUT_ERR_IE	r/w	0	Enable mask for host PIOX-16 interrupt request on timeout condition for host-to-HPI access via host PIOX-16 interface. *HPI_TMOUT_ERR_IE*=0 corresponds to disabled host PIOX-16 interrupt request on timeout condition for host-to-HPI access via host PIOX-16 interface. *HPI_TMOUT_ERR_IE*=1 enables host PIOX-16 interrupt request on timeout condition for host-to-HPI access via host PIOX-16 interface.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

HOST_IS_RG host interrupt source status register

HOST_IS_RG read-only register of host PIOX-16 interface must be used for software polling of host interrupt request sources for host PIOX-16 interrupt request. Note, that when reading *HOST_IS_RG* register, only data bits D0..D3 are valid.

HOST_IS_RG register (r)

X	*HPI_TMOUT_ERR (r,0+)*	*DPRAM_TMOUT_ERR (r,0+)*	*HINT (r,0+)*	*HOST_DPRAM_IRQ (r)*
bits 15..4	bit-3	Bit-2	bit-1	bit-0

Table 2-24 describes details about *HOST_IS_RG* register bits.

Table 2-24. Register bits of *HOST_IS_RG* register.

Register bits or bit fields	access mode	value on host PIOX-16 interface reset	description
HOST_DPRAM_IRQ	r	-	Indicates current status of DSP-to-Host interrupt request via DPRAM (refer to section “DSP Environment” earlier in this chapter for more details). *HOST_DPRAM_IRQ*=0 corresponds to no DSP-to-Host interrupt request via DPRAM. *HOST_DPRAM_IRQ*=1 corresponds to active DSP-to-Host interrupt request via DPRAM, , which is set when on-board DSP writes to *DSP_DPRAM_MH_RQ* DPRAM location. Host PIOX-16 interface must read from *HOST_DPRAM_MH_RQ* DPRAM location order to clear *HOST_DPRAM_IRQ* flag.
HINT	r	0	Indicates current status of DSP-to-Host interrupt request via DSP on-chip HPI port (refer to original TI TMS320C54x documentation for more details). *HINT*=0 corresponds to no active DSP-to-Host interrupt request via DSP on-chip HPI port. *HINT*=1 corresponds to active DSP-to-Host interrupt request via DSP on-chip HPI port.
DPRAM_TMOUT_ERR	r	0	Indicates current status of timeout error for host-to-DPRAM access via host PIOX-16 interface. *DPRAM_TMOUT_ERR*=0 corresponds to that there was no timeout event detected for host-to-DPRAM access cycles via host PIOX-16 interface. *DPRAM_TMOUT_ERR*=1 corresponds to that there was the timeout event detected for host-to-DPRAM access cycles via host PIOX-16 interface.
HPI_TMOUT_ERR	r	0	Indicates current status of timeout error for host-to-HPI access via host PIOX-16 interface. *HPI_TMOUT_ERR*=0 corresponds to that there was no timeout event detected for host-to-HPI access via host PIOX-16 interface. *HPI_TMOUT_ERR*=1 corresponds to that there was no timeout event detected for host-to-HPI access via host PIOX-16 interface.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

HOST_HIRQ_SEL_RG host PIOX-16 interface interrupt request line selector

HOST_HIRQ_SEL_RG register of host PIOX-16 interface must be used to enable and select a particular interrupt request input of PIOX-16 interface of host *TORNADO* DSP system/controller, which will be used to set interrupt request from PIOX-16 interface of *TORNADO-PX/DDC4* DCM to host *TORNADO* DSP system/controller. Note, that when accessing *HOST_HIRQ_SEL_RG* register, only data bits D0..D3 are valid.

HOST_HIRQ_SEL_RG register (r/w)

X	*HIRQ_EN (r/w, 0+)*	*0*	*HIRQ_SEL-1 (r/w, 0+)*	*HIRQ_SEL-0 (r/w, 0+)*
Bits 15..4	bit-3	Bit-2	bit-1	bit-0

Table 2-25 describes details about *HOST_HIRQ_SEL_RG* register bits.

Table 2-25. Register bits of *HOST_HIRQ_SEL_RG* register.

register bits or bit fields	access mode	value on host PIOX-16 interface reset	description
HIRQ_EN	r/w	0	Enable mask for selection of host PIOX-16 interrupt request line. *HIRQ_EN*=0 disables selection of interrupt request line of PIOX-16 interface for setting interrupt request from host PIOX-16 interface of *TORNADO-PX/DDC4* DCM to host *TORNADO* DSP system/controller. *HIRQ_EN*=1 enables selection of interrupt request line of PIOX-16 interface for setting interrupt request from host PIOX-16 interface of *TORNADO-PX/DDC4* DCM to host *TORNADO* DSP system/controller. Selection of particular interrupt request line is performed via bits {*HIRQ-1, HIRQ-0*} of *HOST_HIRQ_SEL_RG* register.
{*HIRQ-1, HIRQ-0*}	r/w	{0,0}	This bit field defines which particular interrupt request line of PIOX-16 interface will be used to set interrupt request from host PIOX-16 interface of *TORNADO-PX/DDC4* DCM to host *TORNADO* DSP system/controller. Refer to Appendix B and your *TORNADO* DSP system/controller user's guide for more details. {*HIRQ-1, HIRQ-0*}={0,0} corresponds to the *IRQ-0* interrupt request line of PIOX-16 interface being selected to set interrupt request to host *TORNADO* DSP system/controller. {*HIRQ-1, HIRQ-0*}={0,1} corresponds to the *IRQ-1* interrupt request line of PIOX-16 interface being selected to set interrupt request to host *TORNADO* DSP system/controller. {*HIRQ-1, HIRQ-0*}={1,0} corresponds to the *IRQ-2* interrupt request line of PIOX-16 interface being selected to set interrupt request to host *TORNADO* DSP system/controller. {*HIRQ-1, HIRQ-0*}={1,1} is reserved and is not recommended for usage. No interrupt request line selected to set interrupt request to host *TORNADO* DSP system/controller.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

HPI area

HPI area of *TORNADO-PX/DDC4* host PIOX-16 interface comprises of a set of 8-bit HPI port registers for TMS320C54x DSP:

- LSB/MSB of HPI control register (HPIC)

- LSB/MSB of HPI address register (HPIA)
- LSB/MSB of HPI data register (HPID)
- LSB/MSB of HPI data register with address postincrement feature (HPID_AINC).

DSP on-chip HPI port allows access from host PIOX-16 interface of *TORNADO-PX/DDC4* DCM to DSP on-chip memory and memory-mapped registers, and allows to load DSP application code directly to DSP on0chip memory. However, since DSP on-chip HPI port is 8-bit only, access to each 16-bit data word will require two access cycle via host PIOX-16 interface and, therefore, is slower than using DPRAM area. Moreover, DSP on-chip HPI port is not good for random accesses (access to DSP on-chip memory cell, which address differs from that for the previous access and is not the next to the previously accessed address), since each random access requires four cycles in order to load address and read/write data word.

CAUTION

TORNADO-PX/DDC4 DCM has been designed with the HPI8 mode for on-board TMS320VC5410 and TMS320VC5416 DSP.

Figure 2-13 shows DSP HPI port memory map for *TORNADO-PX/DDC4* on0board TMS320VC5410 and TMS320VC5416 DSP.

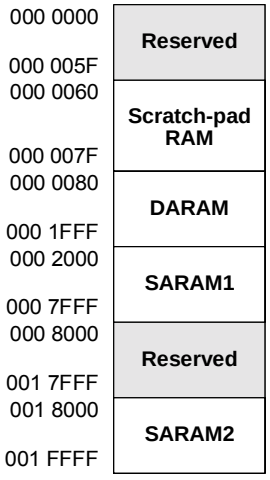


Fig.2-13a. DSP HPI port memory map for TMS320VC5410 DSP.

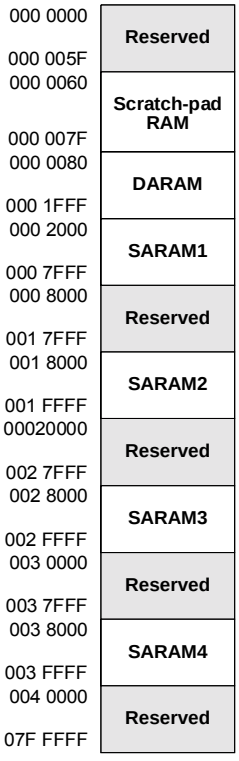


Fig.2-13b. DSP HPI port memory map for TMS320VC5416 DSP.

For more information about TMS320C54x DSP on-chip HPI port refer to original TI documentation for TMS320C54x DSP.

DPRAM area

32Kx16 DPRAM area of *TORNADO-PX/DDC4* host PIOX-16 interface (refer to table 2-20) can be used for both to store DSP program code and for communication between the on-board DSP and host DSP of host *TORNADO* DSP system/controller via host PIOX-16 interface. DPRAM can be accessed by both on-board DSP and host PIOX-16 interface.

CAUTION

Instead of communication between on-board DSP and host PIOX-16 interface via DSP on-chip HPI port (HPI area of host PIOX-16 interface address map), on-board DPRAM delivers fast random access to 16-bit memory location from host *TORNADO* DSP system/controller without need to write and store address of the memory location prior accessing the contents of this memory location.

Host-to-DPRAM access is performed 4 times faster than that via the DSP on-chip HPI port in case random DPRAM locations are being accessed, and is performed 2 times faster in case autoincremented addressing or preset DPRAM location are being accessed.

Access to DPRAM feature no arbitration delays for DSP and host PIOX-16 interface unless both on-board DSP and host PIOX-16 interface are addressing the same DPRAM memory location. In the latter case there is no arbitration preferences, and the first active accessing port will proceed without any arbitration delays, whereas the other port will be pending until the first port will finish the access cycle.

DPRAM area of host PIOX-16 interface has two specific memory locations, which are known as *HOST_DPRAM_HM_RQ* and *HOST_DPRAM_MH_RQ*. These DPRAM locations match *DSP_DPRAM_HM_RQ* and *DSP_DPRAM_MH_RQ* DPRAM locations from on-board DSP environment (refer to section "DSP Environment" earlier in this chapter). These DPRAM locations provide Host-to-DSP and DSP-to-Host interrupt generation along with standard common memory functionality. Refer to the corresponding subsection below for more details.

Generating Host-to-DSP and DSP-to-Host Interrupt Requests via DPRAM

DPRAM area of host PIOX-16 interface has two specific memory locations, which are called as *HOST_DPRAM_HM_RQ* and *HOST_DPRAM_MH_RQ* and provide Host-to-DSP and DSP-to-Host interrupt generation along with standard common memory functionality. These DPRAM locations match *DSP_DPRAM_HM_RQ* and *DSP_DPRAM_MH_RQ* memory locations from on-board DSP environment (refer to section "DSP Environment" earlier in this chapter).

HOST_DPRAM_HM_RQ and *HOST_DPRAM_MH_RQ* DSPRAM memory locations are allocated at the DPRAM addresses in accordance with table 2-20 and are the useful tool for communication between host DSP of host *TORNADO* DSP system/controller and *TORNADO-PX/DDC4* on-board DSP using interrupt request method combined with the 16-bit interrupt request code, which might be simultaneously passed via these DPRAM memory cells.

CAUTION

When host DSP of host *TORNADO* DSP system/controller writes to the *HOST_DPRAM_HM_RQ* DPRAM location via host PIOX-16 interface (refer to section "Host PIOX-16 Interface later in this chapter), then active *DSP_DPRAM_IRQ* interrupt request is generated to the DSP environment and on-board DSP can read data written by host via *DSP_DPRAM_HM_RQ* DPRAM location of on-board DSP environment. This interrupt request remains active until DSP will read contents of this DPRAM memory location. Writing to *DSP_DPRAM_HM_RQ* DPRAM location from the DSP side does not effect the state of *DSP_DPRAM_IRQ* interrupt request.

The *DSP_DPRAM_IRQ* interrupt request can generate active DSP interrupt request in case it is routed via the corresponding interrupt request selector to any of DSP external interrupt requests or DSP NMI. Refer to the corresponding subsection later in this section for more details about external DSP interrupt generation.

CAUTION

When DSP writes to the *DSP_DPRAM_MH_RQ* address, then active *HOST_DPRAM_IRQ* interrupt request is generated to host *TORNADO* DSP system/controller via host PIOX-16 interface and host *TORNADO* DSP system/controller can read data written by DSP via *HOST_DPRAM_HM_RQ* DPRAM location of host PIOX-16 interface. This interrupt request remains active until host DSP of host *TORNADO* DSP system/controller will read contents of this DPRAM memory location. Writing to *HOST_DPRAM_HM_RQ* DPRAM location from host *TORNADO* DSP system/controller side does not effect the state of *HOST_DPRAM_IRQ* interrupt request.

HOST_DPRAM_IRQ interrupt request can generate active interrupt request to host *TORNADO* DSP system/controller via host PIOX-16 interface in case it is enabled via the *HOST_IE_RG* interrupt enable register and particular host interrupt request line is selected via *HOST_HIRQ_SEL_RG* interrupt line selector register. Refer to section "Host PIOX-16 Interface" later in this chapter for more details.

DPSEM area

TORNADO-PX/DDC4 host PIOX-16 interface provides on-board dual-port hardware semaphores (DPSEM) area, which is accessible by both on-board DSP and host DSP of host *TORNADO* DSP system/controller via PIOX-16 interface.

Hardware semaphores are extremely useful tool for synchronization of access to any shared resources (DPRAM, HPI port memory locations, etc) and setting synchro-events between DSP and host PIOX-16 interface. DPSEM area comprises of eight dual-port semaphores, which appear as eight address locations within host PIOX-16

interface address map (table 2-20).. Access to DPSEM area is performed without any arbitration delays on both DSP and host PIOX-16 interface sides.

Each semaphore occupies least significant bit D0 only within 16-bit data word with bits D1..D15 being an extended copy of bit D0. Semaphore has only two valid states: '0' and '1'. The semaphore logic is active low, and the '0' state is called as 'open state' of semaphore (semaphore token), whereas the '1' state is called as 'closed state' of semaphore. Hardware semaphore logic guarantees that both ports will never get enable state (or semaphore token) simultaneously.

Table 2-4 in section "DSP Environment" earlier in this chapter provides example of sample procurement sequence for dual-port semaphores.

2.6 Emulation Tools for *TORNADO-PX/DDC4*

TORNADO-PX/DDC4 uses scan-path emulation technique for the on-board TMS320C54x DSP in order to debug on-board TMS320C54x DSP environment and software.

Compatible scan-path emulation tools include TI XDS510 or MicroLAB' *MIRAGE-510DX* universal JTAG/MPSD emulators with JTAG pod, which must connect to JP3 JTAG-IN connector on *TORNADO-PX/DDC4* mainboard.

Chapter 3. Installation and Configuration

This chapter includes instructions for installation of *TORNADO-PX/DDC4* DCM.

3.1 Installation onto *TORNADO* DSP System/Controller Mainboard

In case *TORNADO-PX/DDC4* DCM is considered to be used in host operation mode, then *TORNADO-PX/DDC4* DCM must be installed as standard PIOX-16 DCM onto host *TORNADO* DSP system/controller mainboard.

For installation of *TORNADO-PX/DDC4* DCM into PIOX-16 site of *TORNADO* DSP system/controller follow the recommendations below:

1. Switch off the power of host PC.
2. Remove *TORNADO* mainboard from PC slot.
3. Ensure that two *TORNADO* on-board spacers for mounting PIOX-16 DCM are installed into the corresponding holes on *TORNADO* mainboard (fig.3-1). If spacers are not installed, then install spacers, which are enclosed with *TORNADO-PX/DDC4* shipment package.
4. Pick-up *TORNADO-PX/DDC4* DCM from the shipment packaging and orient it parallel to *TORNADO* mainboard over PIOX-16 DCM area. Safely plug-in on-board JP1 host PIOX-16 connector of *TORNADO-PX/DDC4* DCM into the corresponding 16-bit PIOX-16 site header of host *TORNADO* mainboard (fig.3-1a). In case host *TORNADO* mainboard provides on-board 32-bit PIOX interface site, then you have to plug *TORNADO-PX/DDC4* DCM into the 16-bit PIOX-16 sub-connector of host PIOX interface site at host *TORNADO* mainboard (fig.3-1b).

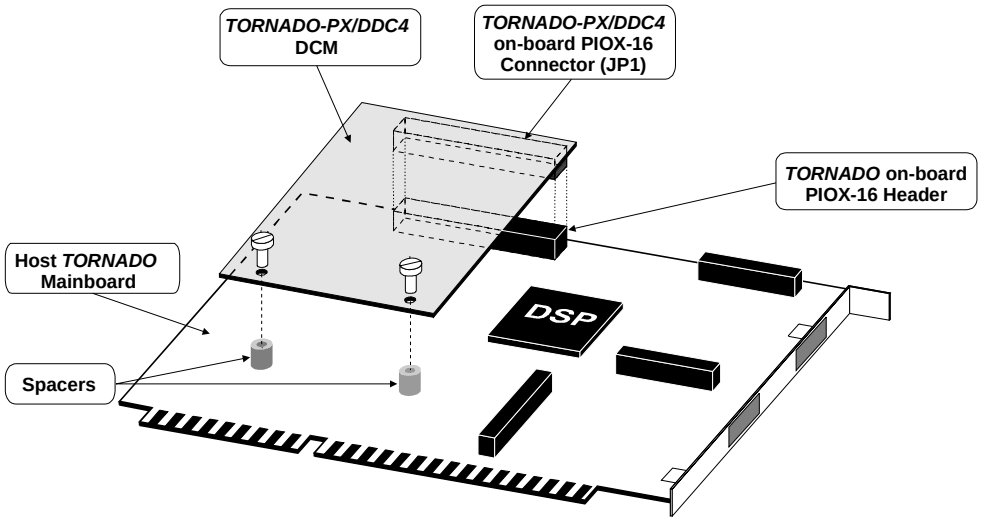


Fig. 3-1a. Installation of *TORNADO-PX/DDC4* DCM into 16-bit PIOX-16 site of host *TORNADO* DSP system.

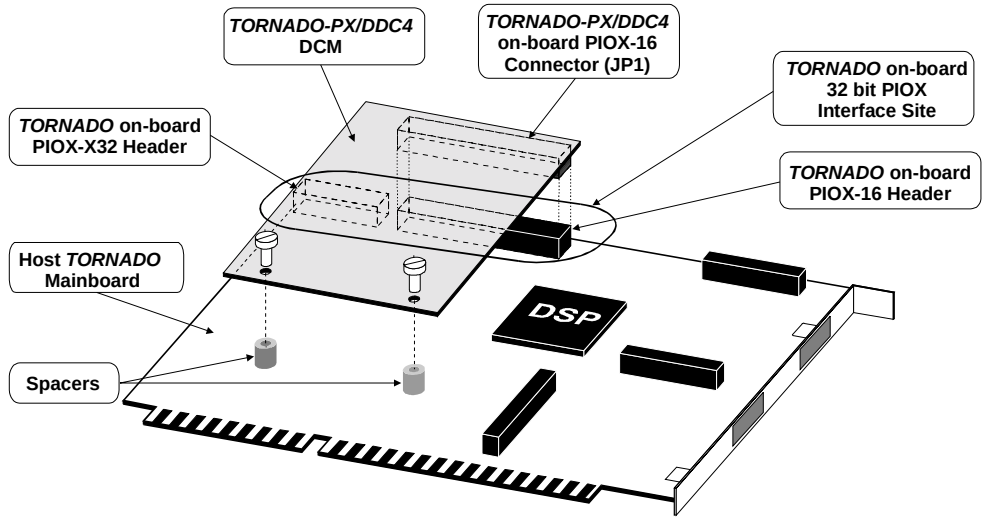


Fig. 3-1b. Installation of *TORNADO-PX/DDC4* DCM into 32-bit PIOX site of host *TORNADO* DSP system.

4. Screw in *TORNADO-PX/DDC4* DCM to the spacers at *TORNADO* mainboard.
5. Configure *TORNADO-PX/DDC4* on-board SW2 for the corresponding DSP bootmode configuration and write protection feature (refer to tables 2-1 and 2-3).
6. Connect *T/X-XIOB/DDC4* external I/O board to *TORNADO-PX/DDC4* DCM (refer to Appendix C).
7. In case *TORNADO* PC plug-in DSP system is used for installation of *TORNADO-PX/DDC4* DCM, then install *TORNADO* mainboard into PC chassis slot and screw it to the rear panel of PC.
8. In case *TORNADO* PC plug-in DSP system is used for installation of *TORNADO-PX/DDC4* DCM and in case *T/X-XIOB/DDC4* external I/O board for *TORNADO-PX/DDC4* DCM is not installed onto the rear mounting bracket of host *TORNADO* mainboard, then install and screw *T/X-XIOB/DDC4* external I/O board to the rear panel of PC.
9. Plug-in two *T/X-DDC1/C* external I/O cable sets to JP1 and JP3 external I/O connector of *T/X-XIOB/DDC4* external I/O board.
10. Connect external I/O peripherals and RF input sources to *T/X-DDC1/C* external I/O cable sets.
11. Switch on power of host PC.

3.2 Installation as Stand-alone Controller

In case *TORNADO-PX/DDC4* DCM is considered to be used in stand-alone operation mode, then *TORNADO-PX/DDC4* DCM must be installed into the custom embedded chassis compartment in accordance with the custom design.

For installation of *TORNADO-PX/DDC4* DCM as stand-alone controller into the custom embedded chassis compartment:

1. Switch off the power of embedded system.
2. Ensure that three spacers for mounting *TORNADO-PX/DDC4* are installed into the custom chassis compartment. If spacers are not installed, then install spacers, which are enclosed with *TORNADO-PX/DDC4* shipment package.

3. Pick-up *TORNADO-PX/DDC4* DCM from the shipment packaging and install it into the custom chassis compartment in accordance with custom design.
4. Screw in *TORNADO-PX/DDC4* DCM to three spacers in custom chassis compartment.
5. Install the corresponding plug into *TORNADO-PX/DDC4* on-board JP4 external link/power connector in order to apply external power to *TORNADO-PX/DDC4* DCM from the power supply of custom embedded system and to install high-speed serial link with external host or peripherals (if this is required). Note, that external power for *TORNADO-PX/DDC4* DCM can be also applied via the corresponding pins of on-board host PIOX-16 connector.
6. Configure *TORNADO-PX/DDC4* on-board SW2 for the corresponding DSP bootmode configuration and write protection feature (refer to tables 2-1 and 2-3).
7. Connect *T/X-XIOB/DDC4* external I/O board to *TORNADO-PX/DDC4* DCM (refer to Appendix C) and screw it to the custom chassis compartment.
8. Plug-in two *T/X-DDC1/C* external I/O cable sets to JP1 and JP3 external I/O connector of *T/X-XIOB/DDC4* external I/O board.
9. Connect external I/O peripherals and RF input sources to *T/X-DDC1/C* external I/O cable sets.
10. Switch on power of embedded system.

3.3 Connection to external signal I/O equipment

Connection of *TORNADO-PX/DDC4* DCM to external analog I/O equipment is performed by means of on-board JP2 and JP5/JP6 connectors (fig.A-1) and by means of optional *T/X-XIOB/DDC4* external I/O board and two *T/X-DDC1/C* external I/O cable sets (Appendix C).

CAUTION

It is highly recommended to plug-in and unplug external I/O cables into/from on-board JP2 and JP5/JP6 connectors of *TORNADO-PX/DDC4* DCM when power is switched off.

The ground signal of *TORNADO-PX/DDC4* DCM has no galvanic isolation neither from host *TORNADO* DSP system/controller, nor from the PC ground and chassis, nor from external I/O peripherals and devises.

CAUTION

When connecting external analog I/O equipment to *TORNADO-PX/DDC4* DCM you should be aware that RF-IN-1 and RF-IN-2 analog inputs and XDAC-1, XDAC-2 and PHDAC analog outputs of *TORNADO-PX/DDC4* DCM are DC coupled. If required, external DC isolation capacitors shall be used.

Appendix A. On-board Switches and Connectors.

This Appendix includes a summary description for *TORNADO-PX/DDC4* on-board switches, connectors and LED.

Board layout for *TORNADO-PX/DDC4* on-board switches, connectors and LED is presented at fig.A-1.

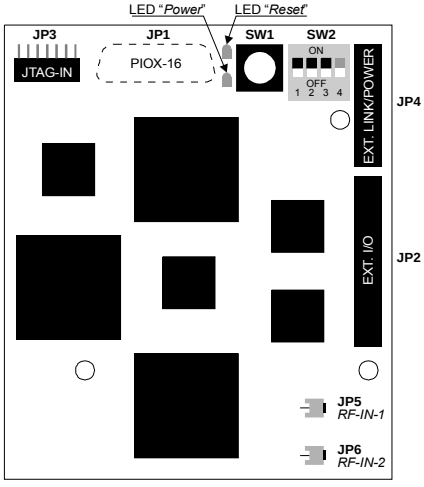


Fig.A-1. On-board switches, connectors and LED for *TORNADO-PX/DDC4* DCM.

A.1 On-board Switches

Table A-1 contains the list of on-board switches.

Table A-1. On-board switches for *TORNADO-PX/DDC4* DCM.

switch ID	switch button	switch function description	reference information
SW1		DSP reset pushbutton for DSP stand-alone operation mode.	Section 2.2
SW2	*SW2-1*	DSP host/stand-alone operation mode selector.	Section 2.2 table 2-1
	SW2-2	NO/FLASH BOOT selector for DSP stand-alone mode.	Section 2.2 table 2-1
	SW2-3	FLASH write protection control.	Section 2.2 table 2-3

A.2 On-board Connectors

Table A-2 contains the list of on-board connectors.

Table A-2. On-board connectors of *TORNADO-PX/DDC4* DCM.

connector ID	Description
JP1	Host PIOX-16 interface site male header. Pinout of JP1 host PIOX-16 connector is presented in Appendix B of this manual and in the user's guide of host *TORNADO* DSP system/controller, which is used for installation of *TORNADO-PX/DDC4* DCM.
JP2	External analog I/O connector for connection to external peripherals. Refer to the corresponding subsection below for more details.
JP3	JTAG-IN male header for connection to external TI XDS510 or MicroLAB Systems *MIRAGE-510DX* JTAG emulator. JTAG-IN connector meets TI connector specifications for connection to JTAG emulator, which must be used for debugging of on-board DSP software.
JP4	External link/power connector for DSP stand-alone operation mode. Refer to the corresponding subsection below for more details.
JP5 *JP6*	Mini-coax RF input connectors for RF channels #1 and #2 correspondingly.

pinout for JP2 external I/O connector

TORNADO-PX/DDC4 on-board JP2 external I/O connector has been designed for connection to external RS232C peripherals, for gain control of external RF amplifiers, and for connection to headphones.

Pinout of JP2 external I/O connector for *TORNADO-PX/DDC4* DCM is presented at fig.A-2, whereas the signal description is presented in table A-3.

On-board JP2 connector is 34-pin guarded 2mm straight mail header, which assumes for mating with the corresponding plug for 2mm flat ribbon cable. *TORNADO-PX/DDC4* DCM has been designed to connect external peripherals via *T/X-XIOB/DDC4* external I/O board, which connects to *TORNADO-PX/DDC4* on-board JP2 connector via 34-pin 2 mm flat cable (refer to Appendix C for more details). However, should customer application requires application specific cable for connection directly to JP2 external I/O connector at *TORNADO-PX/DDC4* DCM, then compatible plugs are available from MicroLAB Systems upon request.

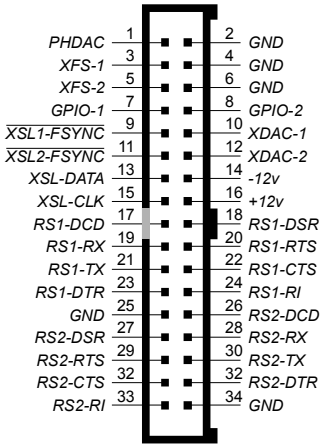


Fig. A-2. Pinout for JP2 external I/O connector of *TORNADO-PX/DDC4* DCM.

Table A-3. Signal description for JP2 external I/O connector of *TORNADO-PX/DDC4* DCM.

signal name	signal type	description	reference information
XDAC-1 *XDAC-2*	AO	Unipolar analog outputs from XDAC-1 and XDAC-2 gain control DAC for external RF amplifiers.	section 2-4
PHDAC	AO	Bipolar analog output from PHDAC phone DAC.	section 2-4
XSL-DATA *XSL-CLK* *XSL1-FSYNC* *XSL2-FSYNC*	3v/5v TTL/OUT	Serial data, serial clock and active low frame synchronization outputs correspondingly for XSL-1 and XSL-2 external serial output links.	section 2-4
GPDIO-0 *GPDIO-1*	3v/5v TTL/IO	General purpose programmable digital I/O.	section 2-2 table 2-13
RS1-TX *RS1-RX* *RS1-RTS* *RS1-CTS* *RS1-DTR* *RS1-DSR* *RS1-RI* *RS1-DCD*	RS/OUT RS/IN RS/OUT RS/IN RS/OUT RS/IN RS/IN RS/IN	RS232C I/O pins from UART-1 channel of DUART.	section 2-2

RS2-TX *RS2-RX* *RS2-RTS* *RS2-CTS* *RS2-DTR* *RS2-DSR* *RS2-RI* *RS2-DCD*	RS/OUT RS/IN RS/OUT RS/IN RS/OUT RS/IN RS/IN RS/IN	RS232C I/O pins from UART-2 channel of DUART.	section 2-2
XFS-1 *XFS-2*	3v/5v TTL/IN	External sampling frequency inputs for ADC-1 and ADC-2 sampling frequency selectors. These inputs are pulled down with 100 Ohm resistors.	section 2-2 table 2-5
+12V, -12V	-	Power supply outputs.	
GND	-	Ground.	

Notes: 1. Signal types: *AO* - analog output; *TTL/IN* - TTL compatible digital input; *TTL/OUT* - TTL compatible digital output; *TTL/IO* - TTL compatible digital input/output; *RS/IN* - RS232C compatible digital input; *RS/OUT* - RS232C compatible digital output.

pinout for JP4 external link/power connector

TORNADO-PX/DDC4 on-board JP4 external link/power connector has been designed for applying external power and reset signal during stand-alone operation, and/or for connection to external host via DSP on-chip McBSP-0 serial port.

Pinout of JP2 external I/O connector for *TORNADO-PX/DDC4* DCM is presented at fig.A-3, whereas the signal description is presented in table A-4.

On-board JP4 connector is 16-pin guarded 2mm straight mail header, which assumes for mating with the corresponding plug for 2mm flat ribbon cable. The mating 16-pin 2mm plug is enclosed as standard with *TORNADO-PX/DDC4* DCM shipment package.

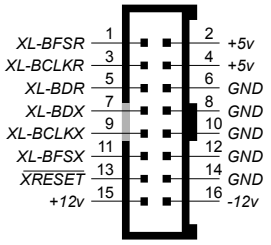


Fig. A-3. Pinout for JP4 external link/power connector of *TORNADO-PX/DDC4* DCM.

Table A-4. Signal description for JP4 external link/power connector of *TORNADO-PX/DDC4* DCM.

signal name	signal type	description	reference information
XRESET	3v/5v TTL/IN	Active low external DSP reset input for stand-alone operation. This input is pulled up via 10 kOhm resistor.	section 2-2
XL-BDR *XL-BCLKR* *XL-BFSR* *XL-BDX* *XL-BCLKX* *XL-BFSX*	3v/5v TTL/OUT TTL/IO	Receiver serial data input, receiver serial clock I/O, receiver frame synchronization I/O, transmitter serial data I/O, transmitter serial clock I/O, transmitter frame synchronization I/O for DSP on0chip McBSP-0 serial port. These pins shall be used as high-speed external link port for communication with compatible external host computers or peripherals. For more information about TMS320C54xx DSP on0chip McBSP port operation refer to the corresponding original TI documentation for TMS320C5000 DSP.	section 2-2
+5v, +12V, -12V	-	External power supply inputs.	
GND	-	Ground.	

Notes: 1. Signal types: *TTL/IN* - TTL compatible digital input; *TTL/OUT* - TTL compatible digital output;*TTL/IO* - TTL compatible digital input/output.

A.3 On-board LED

On-board LED for *TORNADO-PX/DDC4* DCM are presented in table A-5.

Table A-5. On-board LED for *TORNADO-PX/DDC4* DCM.

LED	LED function description
LED1	DSP reset is active (RED).
LED2	DSP power is applied (GREEN).

Appendix B. PIOX-16 Interface Site

This appendix contains information about *TORNADO* PIOX-16 interface site specifications. This description is general to all *TORNADO* DSP systems/controllers, whereas different *TORNADO* boards with different DSP platforms may differ in the number of interrupts requests via PIOX-16 interface and in timer/IO pin specifications. Refer to your particular *TORNADO* user's guide for more details.

B.1 General Description

TORNADO architecture allows expansion of the on-board DSP I/O resources via on-board 16-bit parallel I/O expansion interface site (PIOX-16) (fig.B-1), which is designed to carry compatible DCM (DCM).

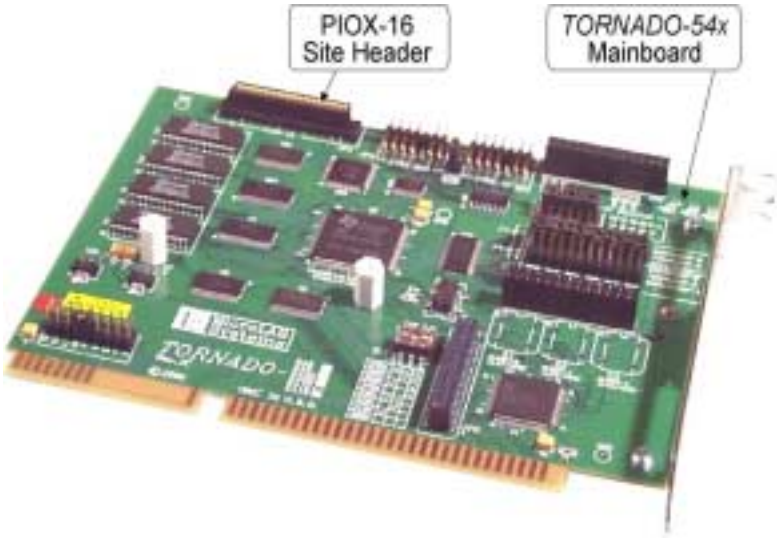


Fig.B-1. PIOX-16 site at *TORNADO-54x* board.

Some *TORNADO* boards (typically 32-bit *TORNADO* DSP systems for PC) provide 16-bit PIOX-16 site as a subset of on-board 32-bit PIOX interface site, whereas other *TORNADO* boards (typically *TORNADO* stand-alone DSP controllers and 16-bit *TORNADO* DSP systems for PC) provide PIOX-16 site only. Refer to your host *TORNADO* board user's guide for information about particular PIOX or PIOX-16 interface site installed.

Figure B-2 demonstrates installation of PIOX-16 DCM into PIOX-16 site of host *TORNADO* DSP system/controller.

Fig.B-2. TORNADO-54x board with PIOX-16 DCM installed.

B.2 PIOX-16 Interface Site Connector and Signals

TORNADO PIOX-16 interface site comprises of signals for SIO-0 and SIO-1 logical serial ports, DSP on-chip TM/XIO-0/1 timers/IO pins, three DSP interrupts, PIOX-16 reset control, and power ±5V/±12V power supplies.

PIOX-16 interface appears as the 64Kx16 sub-area of DSP external memory or I/O resources. PIOX-16 features 16-bit data transfer cycles.

PIOX-16 connector and signal description

PIOX-16 connector is a high-density DDK 50-pin DHB-series dual-row female connector with 0.05" pin pitch. Compatible PIOX-16 plugs for customer designed DCM are available upon request from MicroLAB Systems.

PIOX-16 connector pinout is presented at fig B-3, whereas signal description for PIOX-16 connector is presented in table B-1.

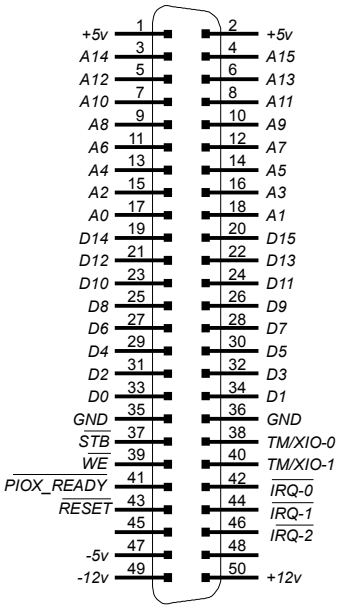


Fig.B-3. PIOX-16 connector pinout (top view).

Table B-1. PIOX-16 signal description.

Signal name	signal type	description
Address and Data Bus		
A0..A15	O	DSP address bus.
D0..D15	I/O	DSP data bus.
Data Transfer Control		
$\overline{STB}$	O	Active low PIOX-16 data transfer strobe.
$\overline{WE}$	O	Active low PIOX-16 write enable signal.
$\overline{PIOX\_READY}$	I	Active low PIOX-16 data ready acknowledge signal. This signal is generated by PIOX-16 DCM in order to complete transmission cycle over PIOX-16 interface. This input has pull-up resistor.

DSP Timers, Reset and Interrupt Requests		
TM/XIO-0 *TM/XIO-1*	I/O/Z	These signals are typically connected to the DSP on-chip TIMER-0 and TIMER-1 I/O pins and can be software configured by DSP as either timer or I/O pin. However, in some *TORNADO* boards (for example *TORNADO-54x* board) these signals can be controlled by on-board I/O controller.
$\overline{RESET}$	O	Active low PIOX-16 reset signal. Some *TORNADO* boards (for example *TORNADO-3x* boards) wires this signal directly from the DSP reset signal, and PIOX-16 plugged-in DCM reset is asserted simultaneously with *TORNADO* on-board DSP reset. However some *TORNADO* boards (for example *TORNADO-54x/6x* etc. boards) feature dedicated PIOX-16 site reset signal, which is controlled by *TORNADO* on-board DSP for better synchronization between the DSP software and PIOX-16 DCM operation.
$\overline{IRQ-0}$ $\overline{IRQ-1}$ $\overline{IRQ-2}$	I	Active low external interrupt request lines for *TORNADO* on-board DSP. These lines are pulled up.
Power Supplies		
GND		Ground.
+5v		+5v power (from ISA-bus).
+12v		+12v power (from ISA-bus).
-5v		-5v power (from ISA-bus).
-12v		-12v power (from ISA-bus).

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.

PIOX-16 site signal levels

Signal levels for PIOX-16 interface signals correspond to that for the CMOS/TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

CAUTION

Some *TORNADO* boards (*TORNADO-30/31/32L/542L*) provide PIOX-16 interface signal levels compatible with that for CMOS/TTL only, whereas other *TORNADO* boards (*TORNADO-33/54xx/6x/E6x/P6x/E3x/E6x*) provide PIOX-16 interface signal levels universal for both 3V TLL and standard TTL. Refer to documentation for your particular *TORNADO* board for information about PIOX-16 interface signal levels.

timing diagram for PIOX-16 data transmission cycle

Figure B-4 presents timing diagram for typical PIOX-16 data transmission cycle for *TORNADO-54x* DSP system. This data transfer timing is known as the industry standard MOTOROLA mode and assumes usage of data strobe signal and write enable signal.

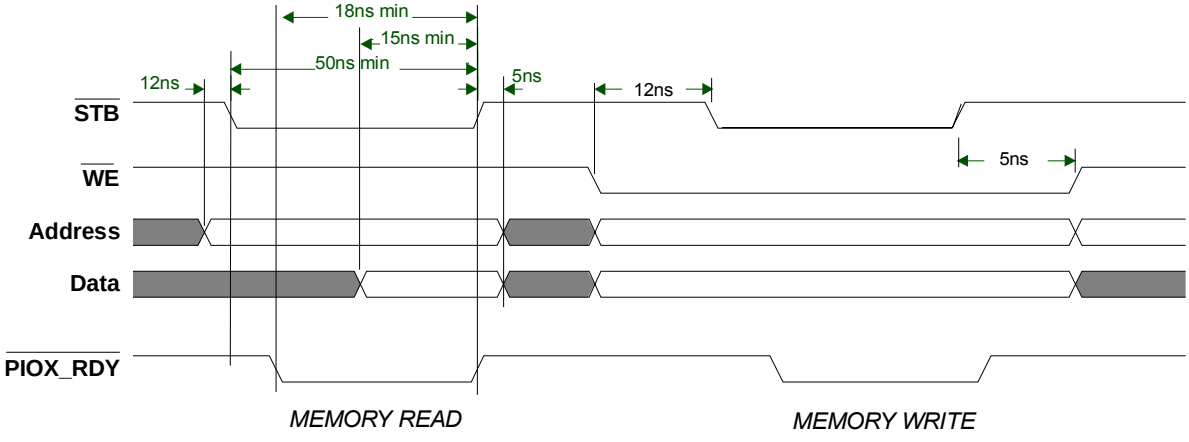


Fig.B-4. Timing diagram of PIOX-16 data transfer for *TORNADO-54x*.

Other *TORNADO* DSP systems/controllers (*TORNADO-3x/6x/P3x/P6x/E3x/E6x*, etc) provide similar timing for PIOX-16 data transmission cycles with the only differences applied to specific timing parameters. Refer to documentation for your particular *TORNADO* board for information about PIOX-16 timing specifications.

B.3 Physical Dimensions for PIOX-16 DCM

Physical dimensions for PIOX-16 DCM are presented at fig.B-5. This information is intended for those customers, who need to design custom PIOX-16 DCM.

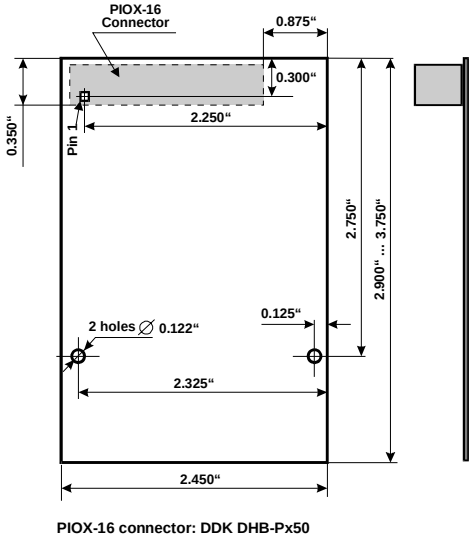


Fig.B-5. Physical dimensions for PIOX-16 DCM.

Appendix C. External Cable Sets for *TORNADO-PX/DDC4*

This appendix contains information about external cable sets for *TORNADO-PX/DDC4* DCM, which include *T/X-XIOB/DDC4* external I/O board and *T/X-DDC1/C* external I/O cable set. Note, that *T/X-DDC1/C* external I/O cable set can be also used with *T/SDAS-DDC1* single-channel DRR SIOX DCM for *TORNADO* DSP systems/controllers/coprocessors.

C.1 Connection of external I/O peripherals and devices to *TORNADO-PX/DDC4* DCM

TORNADO-PX/DDC4 DCM provides on-board JP2 external I/O connector and JP5/JP6 mini-coax RF-IN connectors (refer Appendix A) for connection to external peripherals, devices and RF signal sources.

External peripherals, devices and RF sources can either directly connect to *TORNADO-PX/DDC4* on-board JP2 and JP5/JP6 connectors, or, for more convenience, can connect by means of optional *T/X-XIOB/DDC4* external I/O board and two *T/X-DDC1/C* external I/O cable sets (fig.C-1), which come standard with *TORNADO-PX/DDC4* DCM shipment package and are used for connection to external signal sources and peripherals using industry standard end connectors.

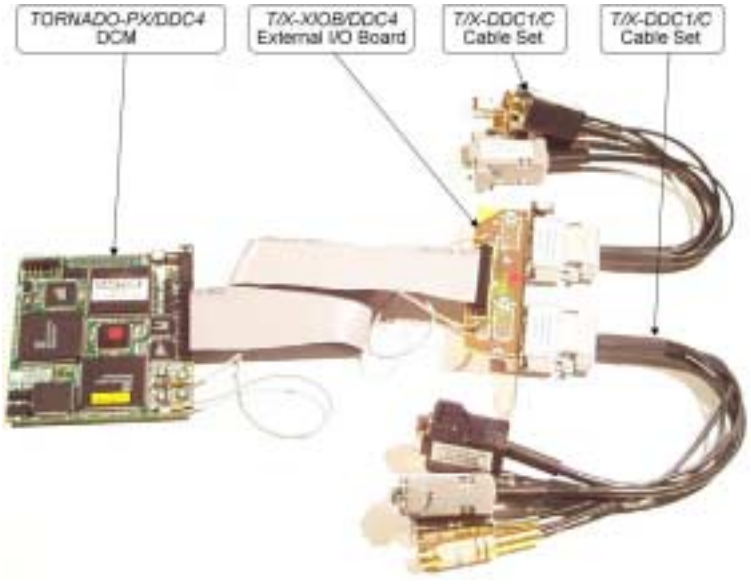


Fig. C-1. TORNADO-PX/DDC4 DCM with *T/X-XIOX/DDC4* external I/O board and two *T/X-DDC1/C* external I/O cable sets.

Optional *T/X-XIOB/DDC4* external I/O board can be installed at the rear panel of PC chassis and converts JP2 and JP5/JP6 *TORNADO-PX/DDC4* on-board connectors into two remote single-channel external I/O

connectors, which are compatible with that for *T/SDAS-DDC1* DCM and which allow connection to external RS232C compatible devices, phones, RF amplifiers, and other devices.

T/X-DDC1/C external I/O cable sets provides industry standard connectors for connection to external I/O peripherals, devices and RF sources.

This appendix contains description for *T/X-XIOB/DDC4* external I/O board and *T/X-DDC1/C* external I/O cable set.

C.2 *T/X-XIOB/DDC4* External I/O Board

This section contains description for *T/X-XIOB/DDC4* external I/O board (fig.C-2), which comes standard with *TORNADO-PX/DDC4* DCM and is used for connection to external signal sources and peripherals using industry standard end connectors via two *T/X-DDC1/C* external I/O cable sets for *T/SDAS-DDC1* DCM.

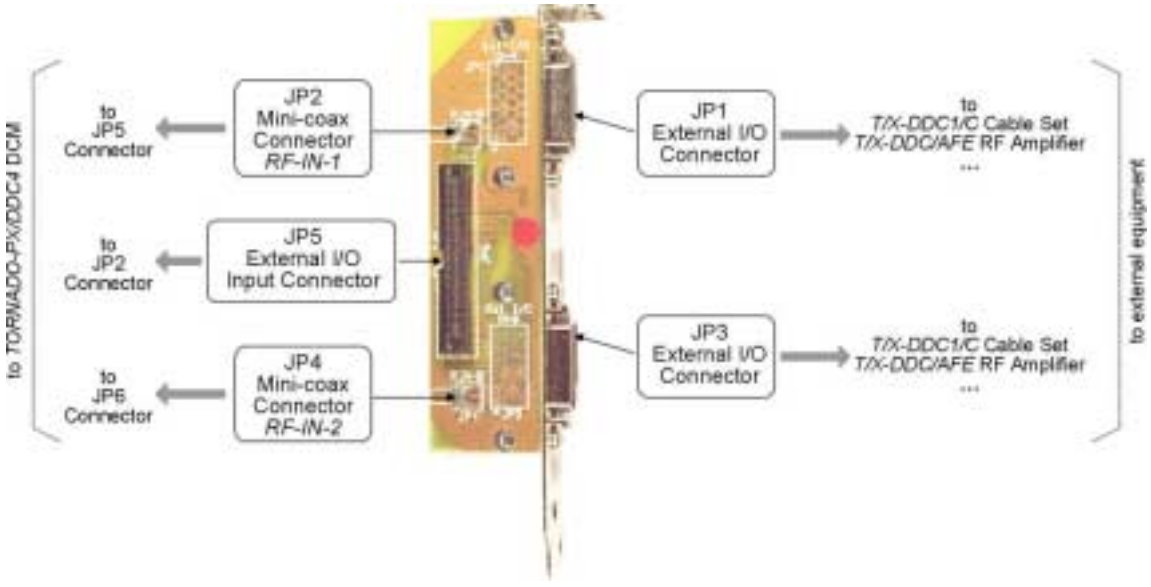


Fig. C-2. T/X-XIOB/DDC4 external I/O board.

installation

T/X-XIOB/DDC4 external I/O board either installs in a separate slot at the rear panel of PC chassis, or can be installed directly onto the rear mounting bracket of *TORNADO* PC plug-in DSP systems in order to save space inside PC chassis compartment.

schematic diagram for T/X-XIOB/DDC4 external I/O connector board

T/X-XIOB/DDC4 external I/O board comprises of the following on-board connectors:

- Input JP2 and JP4 mini-coax connectors, which shall connect to *TORNADO-PX/DDC4* on-board JP5 and JP6 RF input mini-coax connectors correspondingly via 12" miniature RF coaxial cables.

- Input JP5 guarded 2mm 34-pin straight male header, which must connect to *TORNADO-PX/DDC4* on-board JP2 external I/O connector via 12" 2mm flat ribbon cable.
- Output JP1 and JP3 external I/O connectors, which are compatible with that for *T/SDAS-DDC1* DCM and which allow connection to external RS232C compatible devices, phones, RF amplifiers, and other devices via *T/SDAS-DDC1/C* external I/O cable sets. *T/X-XIOB/DDC4* on-board JP1 and JP3 connectors are 26-pin half pitch DHA-RA26 series receptacles from Fujikura-DDK Ltd. In case customer needs to design his own application specific cable for connection to JP1/JP3 connectors of *TORNADO-PX/DDC4* DCM, then compatible plugs for JP1/JP3 connectors are available from MicroLAB Systems upon request.

Fig.C-3 shows generic schematic diagram of *T/X-XIOB/DDC4* external I/O board for *TORNADO-PX/DDC4* DCM. Signals description is provided in table A-3 for *TORNADO-PX/DDC4* on-board JP2 external I/O connector.

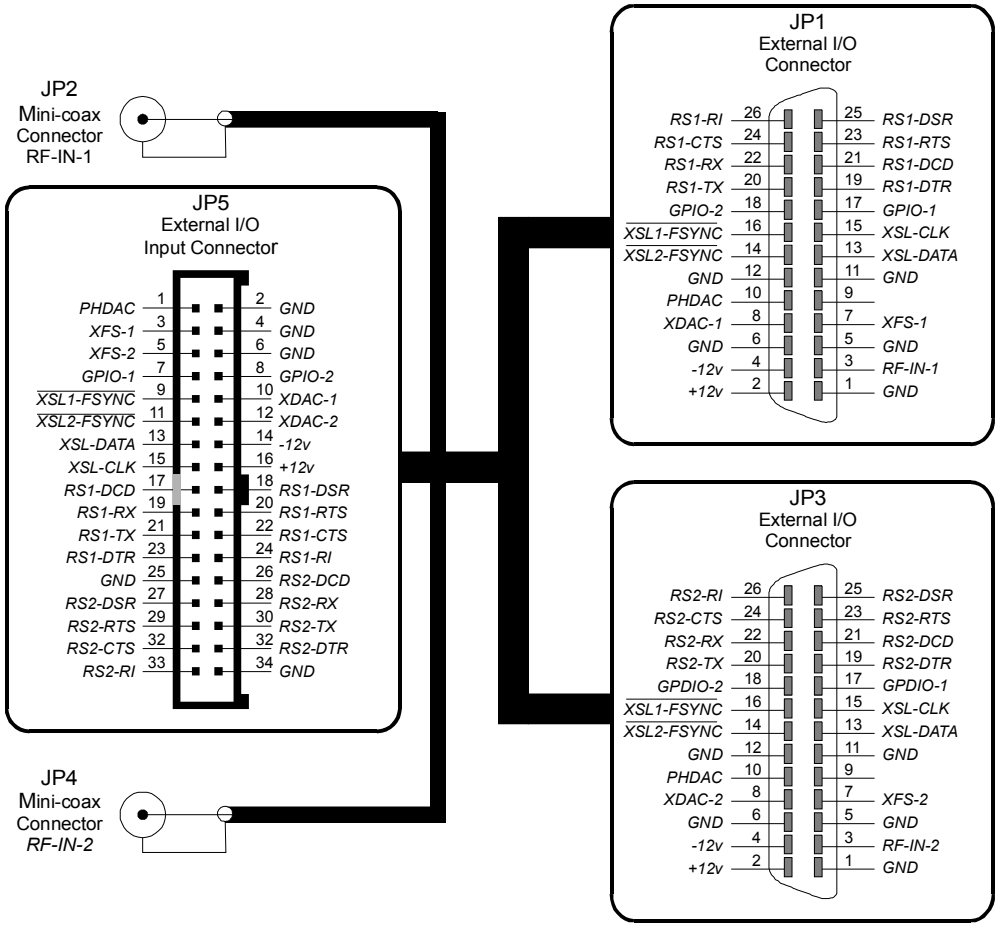


Fig.C-3. Schematic diagram of *T/X-XIOB/DDC4* external I/O board.

C.3 *T/X-DDC1/C* External I/O Cable Set

This section contains description for *T/X-DDC1/C* cable set (fig.C-4), which comes standard with *TORNADO-PX/DDC4* and *T/SDAS-DDC1* DCM and is used for connection to external signal sources and peripherals using industry standard end connectors.

Fig. C-4. T/X-DDC1/C external I/O cable set.

T/X-DDC1/C external I/O cable set for *TORNADO-PX/DDC4* and *T/SDAS-DDC1* DCM plugs either into the JP2 connector at *T/SDAS-DDC1* DCM or into the JP1/JP3 connectors at *T/X-XIOB/DDC4* external I/O board for *TORNADO-PX/DDC4* DCM (refer to fig.C-3 and section "*T/X-XIOB/DDC4* external I/O board" earlier in this appendix).

schematic diagram for T/X-DDC1/C external I/O cable set

T/X-DDC1/C external I/O cable set splits I/O signals from *T/X-XIOB/DDC4* external I/O board or *T/SDAS-DDC1* DCM into several function groups via industry-standard end-user connectors in order to simplify connection to external I/O equipment.

T/X-DDC1/C cable set comprises of the following end-user connectors:

- industry standard RF-IN BNC coax connector for RF analog signal input
- RCA jack at XDAC analog output of *T/X-XIOB/DDC4* external I/O board for *TORNADO-PX/DDC4* DCM (or XDAC-1 analog output for *T/SDAS-DDC1* DCM) for external gain control, phones, and general purpose analog output (recommended usage is to connect to external RF amplifier for gain control)
- 3.5mm mini jack at the PHDAC analog output of *T/X-XIOB/DDC4* external I/O board for *TORNADO-PX/DDC4* DCM (or XDAC-2 analog output for *T/SDAS-DDC1* DCM) for either connection to external phones, or gain control of external RF amplifier, or general purpose analog output (recommended usage is connect to external phones)
- D-Sub DB-9 male 9-pins connector for RS232C interface, which meets the industry-standard pinout for PC COM ports
- high-density D-Sub DBH-15 female 15-pins connector (compatible with connectors for PC VGA monitors) for auxiliary signal I/O and power output.

Fig.C-5 shows generic schematic diagram of ***T/X-DDC1/C*** cable. Signal description is provided in table A-3 for JP2 external I/O connector of ***TORNADO-PX/DDC4*** DCM.

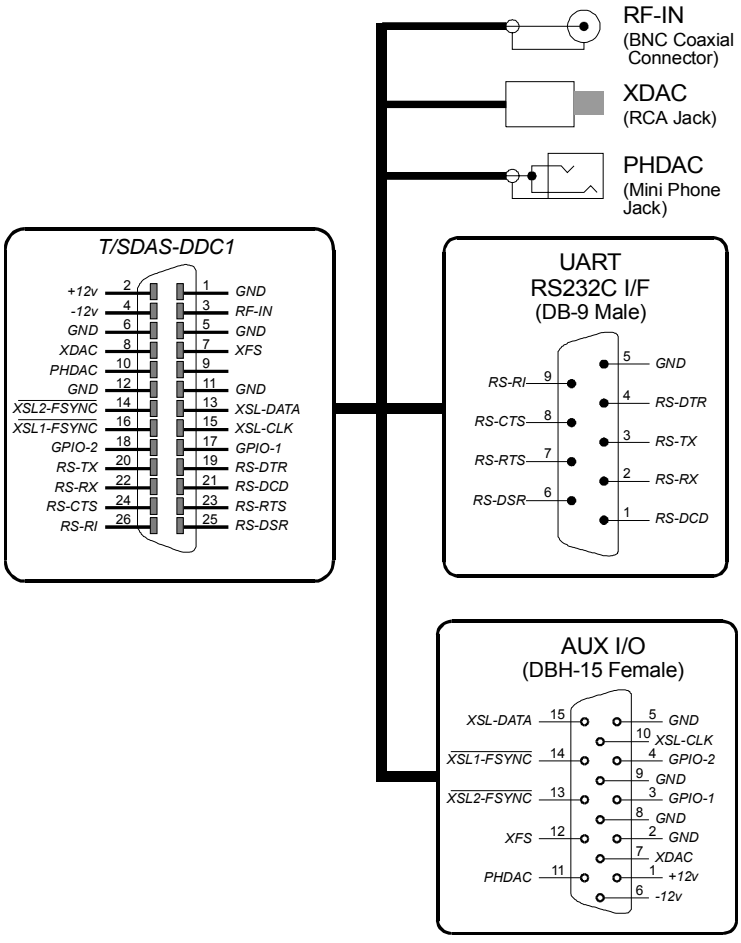


Fig.C-5. Schematic diagram of *T/X-DDC1/C* cable.

Appendix D. FLASH Memory Programming

This appendix contains detail information about programming procedure for *TORNADO-PX/DDC4* on-board FLASH memory.

CAUTION

FLASH memory programming routines for *TORNADO-PX/DDC4* on-board DSP environment are supplied as a standard part of on-board DSP utility software with *TORNADO-PX/DDC4* DCM.

Information in this appendix is provided for advanced users only, who need to design their own code for programming *TORNADO-PX/DDC4* on-board FLASH memory.

D.1 Accessing FLASH Memory at *TORNADO-PX/DDC4*

TORNADO-PX/DDC4 DCM provides on-board 128Kx8 in-system programmable FLASH memory, which can be used as boot source during *SA/FLASH8-BMODE* or *HOST/FLASH8-BMODE* DSP bootmodes (refer to section "DSP Environment" in chapter 2 and table 2-1), and/or to store general purpose non-volatile data.

FLASH memory addressing

TORNADO-PX/DDC4 on-board 128Kx8 FLASH memory is allocated to DSP external data memory area (refer to section "DSP Environment" and table 2-2).

FLASH memory becomes available for read/write by on-board DSP software inside DSP external data memory area in case the *DROM* bit of DSP on-chip PMST register is set to the *DROM*=0 state (refer to original TI documentation for TMS320C5000 DSP), and in case the *XDMEM_SEL* bit of *DSP_XDMP_RG* register is set to the *XDMEM_SEL*=1 state (refer to table 2-10).

128Kx8 FLASH memory space is splitted into 32Kx8 FLASH memory pages in order to meet external data memory addressing requirement for TMS320C54x DSP. FLASH memory page is selected by the {*FPAGE-1*, *FPAGE-0*} bits of *DSP_XDMP_RG* register (refer to table 2-10).

CAUTION

FLASH memory description below is presented with assumption that 128K linear FLASH memory address space is not splitted into overlapped FLASH memory pages as it is done in *TORNADO-PX/DDC4* DCM.

User software must perform corresponding processing of linear FLASH memory address in order to convert it to pages in accordance with *TORNADO-PX/DDC4* DCM architecture.

FLASH memory write protection

TORNADO-PX/DDC4 on-board hardware allows to inhibit writes to on-board FLASH memory in order to provide safety and integrity of FLASH memory contents after programming.

FLASH memory write protection is controlled by on-board SW2-3 switch (refer to fig.A-1) in accordance with table 2-3 (refer to section "DSP Environment" for more details).

D.2 FLASH Chip Description

This section contains detail description for *TORNADO-PX/DDC4* on-board FLASH memory.

Command Definitions

When FLASH chip is in the READ mode, then any write to FLASH is interpreted as write to FLASH command register until device will be returned back to READ mode using READ command.

Writing specific address and data commands or sequences into the command register initiates device operations. Table D-1 defines the valid register command sequences.

CAUTION

Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

Table D-1. FLASH Command Definitions

command sequence (note 1)	**cycles**	**bus cycles** (notes 2-4)											
		First		**Second**		**Third**		**Fourth**		**fifth**		**sixth**	
		addr	**data**	**addr**	**data**	**addr**	**data**	**addr**	**data**	**addr**	**data**	**addr**	**data**
Read (note 5)	1	RA	RD										
Reset (note 6)	1	XXX	F0										
Byte program	4	555	AA	2AA	55	555	A0	PA	PD				
Unlock bypass	3	555	AA	2AA	55	555	20						
Unlock Bypass Program (note 9)	2	XXX	A0	PA	PD								
Unlock Bypass Reset (note 10)	2	XXX	90	XXX	00								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	10
Erase Suspend (note 11)	1	XXX	B0										
Erase Resume (note 12)	1	XXX	30										
Autoselect Mode (note 7)													
Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
Device ID	4	555	AA	2AA	55	555	90	X01	6E				
Sector protect verify (note 8)	4	555	AA	2AA	55	555	90	SA X02	00				
									01				

Legend:

X Don't care
RA Address of the memory location to be read.
RD Data read from location *RA* during read operation.
PA Address of the memory location to be programmed.
PD Data to be programmed at location *PA*.
SA Address of the sector to be erased or verified. Address bits A16–A14 uniquely select any sector.

Notes:
1. See Table 1 for descriptions of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operations.
4. Address bits A16–A11 are don't care for unlock and command cycles, unless SA or PA required.
5. No unlock or command cycles required when device is in read mode.
6. The Reset command is required to return to the read mode when the device is in the autoselect mode or if DQ5 goes high.
7. The fourth cycle of the autoselect command sequence is a read cycle.
8. The data is 00h for an unprotected sector and 01h for a protected sector. The complete bus address in the fourth cycle is composed of the sector address (A16–A14), A1 = 1, and A0 = 0.
9. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
10. The Unlock Bypass Reset command is required to return to reading array data when the device is in the Unlock Bypass mode.
11. The system may read and program functions in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
12. The Erase Resume command is valid only during the Erase Suspend mode.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more information on this mode.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" section, next.

See also "Requirements for Reading Array Data" in the "Device Bus Operations" section for more information. The Read Operations table provides the read parameters.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table D-1 shows the address and data requirements.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table D-2 for the valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Table D-2. Uniform Sector Address Table.

sector	A16	A15	A14	address range
SA0	0	0	0	00000H-03FFFH
SA1	0	0	1	04000H-07FFFH
SA2	0	1	0	08000H-0BFFFH
SA3	0	1	1	0C000H-0FFFFH
SA4	1	0	0	10000H-13FFFH
SA5	1	0	1	14000H-17FFFH
SA6	1	1	0	18000H-1BFFFH
SA7	1	1	1	1C000H-1FFFFH

Byte Program Command Sequence

The device programs one byte of data for each program operation. The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. Table D-1 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. See “Write Operation Status” for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries.

CAUTION

A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set DQ5 to "1," or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table D-1 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't cares for both cycles. The device then returns to reading array data.

Figure D-1 illustrates the algorithm for the program operation.

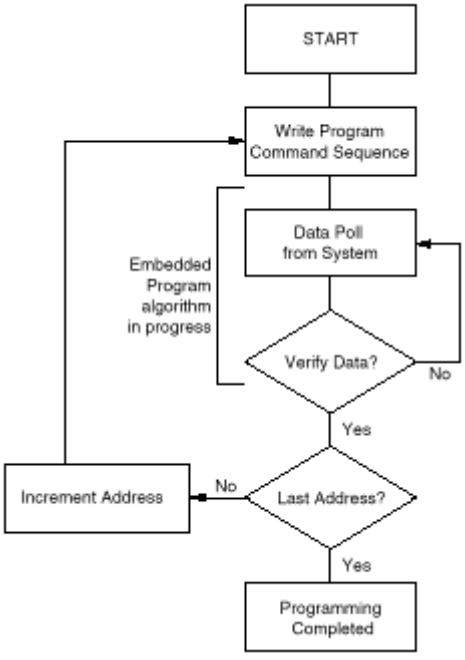


Fig.D-1. Program Operation.

Note: 1. See Table D-1 for program command sequence.

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table D-1 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See “Write Operation Status” for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure D-2 illustrates the algorithm for the erase operation.

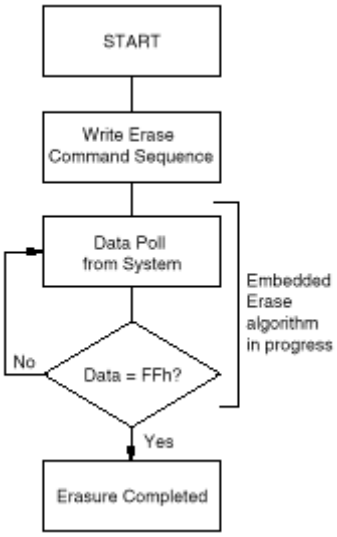


Fig.D-2. Erase Operation.

Notes:
1. See Table D-1 for erase command sequence.
2. See "DQ3: Sector Erase Timer" for more information.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. Table D-1 shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 µs, the system need not monitor DQ3.

CAUTION

Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the "DQ3: Sector Erase Timer" section.) The time-out begins from the rising edge of the final WE# pulse in the command sequence. Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. (Refer to "Write Operation Status" for information on these status bits.)

Figure D-2 illustrates the algorithm for the erase operation.

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are "don't-cares" when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See "Write Operation Status" for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See "Write Operation Status" for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

The system must write the Erase Resume command (address bits are "don't care") to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table D-3 and the following subsections describe the functions of these bits. DQ7, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Table D-3. Write Operation Status.

operation		DQ7 (note 2)	DQ6	DQ5 (note 1)	DQ3	DQ2 (note 2)
Standard mode	Embedded Program Algorithm	DQ7	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle
Erase Suspend mode	Reading with Erase Suspended Sector	1	No Toggle	0	N/A	No toggle
	Reading with Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Erase-Suspend-Program	DQ7	Toggle	0	N/A	N/A

Notes:
1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "DQ5: Exceeded Timing Limits" for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1"; prior to this, the device outputs the "complement," or "0." The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the following read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. Table D-3 shows the outputs for Data# Polling on DQ7. Figure D-3 shows the Data# Polling algorithm.

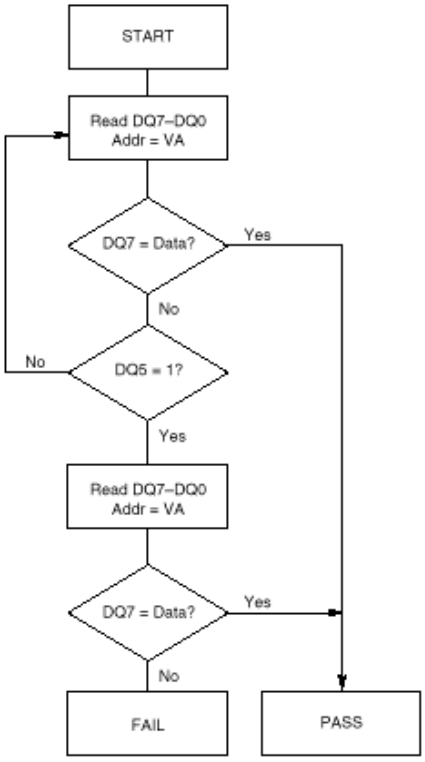


Fig.D-3. Data# Polling Algorithm.

Notes:
1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
2. DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle (The system may use either OE# or CE# to control the read cycles). When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to deter-mine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table D-3 shows the outputs for Toggle Bit I on DQ6. Figure D-4 shows the toggle bit algorithm in flowchart form, and the section "Reading Toggle Bits DQ6/DQ2" explains the algorithm. See also the subsection on DQ2: Toggle Bit II.

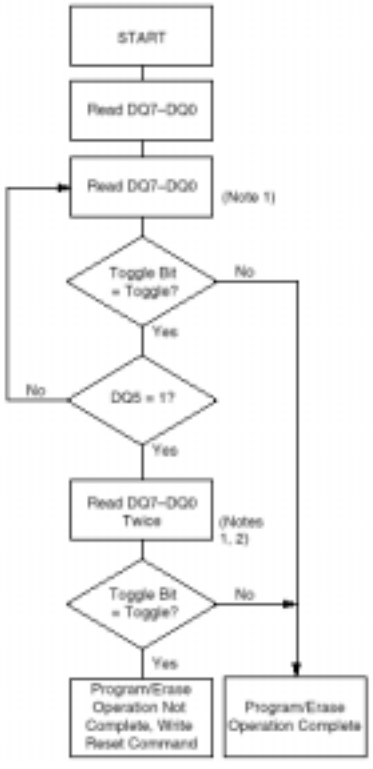


Fig.D-4. Toggle Polling Algorithm.

Notes: 1. Read toggle bit twice to determine whether or not it is toggling. See text.
2 . Recheck toggle bit because it may stop toggling as DQ5 changes to “1”. See text.

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for era-sure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for era-sure. Thus, both status bits are required for sector and mode information. Refer to Table D-3 to compare outputs for DQ2 and DQ6.

Figure D-4 shows the toggle bit algorithm in flowchart form, and the section “Reading Toggle Bits DQ6/DQ2” explains the algorithm. See also the DQ6: Toggle Bit I subsection.

Reading Toggle Bits DQ6/DQ2

Refer to Figure D-4 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure D-4).

Table D-3 shows the outputs for Toggle Bit I on DQ6. Figure D-4 shows the toggle bit algorithm. See also the subsection on DQ2: Toggle Bit II.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.”

CAUTION

Only an erase operation can change a "0" back to a "1." Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a "1." Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from "0" to "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the "Sector Erase Command Sequence" section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is "1", the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table D-3 shows the outputs for DQ3.

Appendix E. Glossary of Terms.

This Glossary contains definition for terms and other synchronism used along in this databook.

A

ADC-1/2
On-board analog-to-digital converters. Refer to section 2.3 for more details.

ADC-SMUX
On-board ADC output data stream mutiplexer. Refer to sections 2.1 and 2.3 for more details.

ADC Overflow
Overflow condition for ADC output data, which is detected by on-board ADC overflow controller. *ADC1_OVF*, *ADC2_OVF* and *ADC12_OVF* flags, which indicate corresponding ADC overflow event, are available via *DSP_ADC_FIFO_STAT_RG* register. Refer to sections 2.2 and 2.3 for more details.

B

Bootmode
DSP start-up bootmode, which is defined by on-board SW2 switch and by bits {*BMODE-1, BMODE-0*} of *HOST_CNTR2_RG* register. Refer to sections 2.2 and 2.5 for more details.

Bypass FIFO
Same as FIFO.

C

D

DAC
Digital-to-analog converter. Refer to sections 2.2 and 2.4 for more details.

DCM
Daughter-card module. *TORNADO-PX/DDC4* is DCM, which plugs into PIOX-16 interface site of host *TORNADO* DSP system/controller.

DDC

Digital down converter. Same as PDC.

DPRAM

On-board dual-port memory, which is available for access from both on-board DSP and host PIOX-16 interface. Refer to section 2.2 for more details.

DPSEM

On-board dual-port semaphores memory area, which is available for access from both on-board DSP and host PIOX-16 interface. Refer to section 2.2 for more details.

DSP

On-board TI TMS320VC5410 or TMS320VC5416 Digital Signal Processor, which is used for system control and communication with host *TORNADO* DSP system/controller. Refer to sections 2.1, 2.2 and 2.3 or more details.

DSP_ADC_CLKSEL_RG

Register inside DSP environment, which is used to select sampling frequency source for on-board ADC. Refer to sections 2.2 and 2.3 for more details.

DSP_ADC_FIFO_STAT_RG

Read-only register inside DSP environment, which is used to read status of ADC overflow flags and FIFO flags. Refer to sections 2.2 and 2.3 for more details.

DSP_AUX_IRQ_STAT_RG

Read-only register inside DSP environment, which is used to read status of auxiliary interrupt request inputs. Refer to section 2.2 for more details.

DSP_CLR_ADC_OVF_RG

Write-only register inside DSP environment, which is used to clear ADC overflow flags. Refer to sections 2.2 and 2.3 for more details.

DSP_DPRAM_HM_RQ

Dual-port memory location inside DSP environment, which is used to generate interrupt from host PIOX-16 interface to on-board DSP. Refer to section 2.2 for more details.

DSP_DPRAM_MH_RQ

Dual-port memory location inside DSP environment, which is used to generate interrupt from on-board DSP to host PIOX-16 interface. Refer to section 2.2 for more details.

DSP_FIFO_DATA_RG

FIFO data read register inside DSP environment, which is used to read FIFO data and to program FIFO flags read FIFO output data. Refer to sections 2.2 and 2.3 for more details.

DSP_FIFO_CNTR_RG

FIFO control register inside DSP environment, which is used to set FIFO operation mode and to start/abort FIFO data acquisition process. Refer to sections 2.2 and 2.3 for more details.

DSP_FIFO_RES_RG

Write-only register inside DSP environment, which is used to reset FIFO flags. Refer to sections 2.2 and 2.3 for more details.

DSP_GPIO_DIR_RG, DSP_GPIO_DATA_RG
Registers inside DSP environment, which are used to set direction and read/write data to the *GPIO-0/1* digital I/O pins of JP2 external I/O register. Refer to section 2.2 for more details.

DSP_MIRQ0_SEL_RG.. DSP_MIRQ3_SEL_RG, DSP_MNMI_SEL_RG
Registers inside DSP environment, which are used to select interrupt signal source for DSP external interrupts. Refer to section 2.2 for more details.

DSP_PDC_FIFO_ISEL_RG
Register inside DSP environment, which is used to select real-time input data stream for PDC and FIFO. Refer to sections 2.2 and 2.3 for more details.

DSP_PDCx_AOUT0_RG..DSP_PDCx_AOUT7_RG,
DSP_PDCx_BOUT0_RG..DSP_PDCx_BOUT7_RG
HSP50214 PDC on-chip registers, which are used to real real-time PDC output data. Refer to sections 2.2 and 2.3 for more details.

DSP_PDCx_HDL0_RG, DSP_PDCx_HDL1_RG,
DSP_PDCx_HDL2_RG, DSP_PDCx_HDL3_RG,
DSP_PDCx_WRADDR_RG, DSP_PDCx_RDADDR_RG,
HSP50214 PDC on-chip registers, which are used to configure PDC and to read PDC status information. Refer to sections 2.2 and 2.3 for more details.

DSP_PDC_STAT_RG
Read-only register inside DSP environment, which is used to read PDC status information. Refer to sections 2.2 and 2.3 for more details.

DSP_SYS_STAT_RG
Read-only register inside DSP environment, which is used to read DSP start-up bootmode information. Refer to section 2.2 for more details.

DSP_WDT_EN_RG
Register inside DSP environment, which is used to enable WDT feature during DSP stand-alone operation mode. Refer to section 2.2 for more details.

DSP_WDT_RES_RG
Write-only register inside DSP environment, which is used to reset WDT. Refer to section 2.2 for more details.

DSP_XDMP_RG
Register inside DSP environment, which is used to select either DPRAM or FLASH memory to be mapped into DSP external memory area, and to select FLASH memory page addressed.. Refer to section 2.2 for more details.

DSP_XSL_FMT_RG

Register inside DSP environment, which is used to set data format, clock polarity and clock framing feature for XSL-1/2 external output serial links. Refer to sections 2.2 and 2.4 for more details.

DUART

On-board PC16552D Dual-channel Universal Asynchronous Receiver-Transmitter. *TORNADO-PX/DDC4* DCM provides two on-board UART channels (UART-1 and UART-2 as the part of DUART) with RS232C interface for communication with external RF tuners and general purpose peripherals. Each UART channel is hardware compatible with PC COM port controller. Refer to section 2.2 for more details.

E

F

FIFO

On-board high density First-In-First-Output device, which is used to store ADC output data for general purpose and spectral analysis. Refer to sections 2.1, 2.2 and 2.3 for more details.

FLASH

On-board non-volatile FLASH memory, which can be used to store DSP boot code and non-volatile data. Refer to section 2.2 and Appendix D for more details.

G

GPIO-0/1

General purpose digital I/O bits, which can be used for control of external peripherals. *GPIO-0/1* are controlled via *DSP_GPIO_DIR_RG* and *DSP_GPIO_DATA_RG* registers. Refer to section 2.2 for more details.

H

Host PIOX-16 interface

TORNADO-PX/DDC4 on-board host PIOX-16 interface, which is used to install onto host *TORNADO* DSP system/controller and for communication with host DSP. Refer to section 2.5 and Appendix B for more details.

HOST/NO-BMODE, HOST/FLASH8-BMODE, HOST/HPI-BMODE

DSP start-up bootmodes for host operation mode. Refer to section 2.2 for more details.

HOST_CLR_DPRAM_TMOUT_ERR_RG

Write-only register inside host PIOX-16 interface environment, which is used to clear timeout error flag for host-to-DPRAM access. Refer to section 2.5 for more details.

HOST_CLR_HPI_TMOUT_ERR_RG
Write-only register inside host PIOX-16 interface environment, which is used to clear timeout error flag for host-to-HPI access. Refer to section 2.5 for more details.

HOST_CNTR1_RG
Register inside host PIOX-16 interface environment, which is used to control DSP reset signal during host operation mode for *TORNADO-PX/DDC4* DCM. Refer to section 2.5 for more details.

HOST_CNTR2_RG
Register inside host PIOX-16 interface environment, which is used to set DSP bootmode during host operation mode for *TORNADO-PX/DDC4* DCM and to enable timeout control for host-to-DPRAM and host-to-HPI access. Refer to section 2.5 for more details.

HOST_DPRAM_HM_RQ
Dual-port memory location inside host PIOX-16 interface environment, which is used to generate interrupt from host PIOX-16 interface to on-board DSP. Refer to section 2.5 for more details.

HOST_DPRAM_MH_RQ
Dual-port memory location inside host PIOX-16 interface environment, which is used to generate interrupt from on-board DSP to host PIOX-16 interface. Refer to section 2.5 for more details.

HOST_HIRQ_SEL_RG
Register inside host PIOX-16 interface environment, which is used to enable and select particular interrupt request line of host PIOX-16 interface in order to set interrupt request from *TORNADO-PX/DDC4* DCM to host *TORNADO* DSP system/controller. Refer to section 2.5 for more details.

HOST_HPIC_RG_LSB, HOST_HPIC_RG_MSB,
HOST_HPIA_RG_LSB, HOST_HPIA_RG_MSB,
HOST_HPID_RG_LSB, HOST_HPID_RG_MSB,
HOST_HPID_AINC_RG_LSB, HOST_HPID_AINC_RG_MSB,
DSP on-chip HPI port registers, which are mapped to host PIOX-16 interface environment for host-to-HPI access. Refer to section 2.5 for more details.

HOST_IE_RG
Register inside host PIOX-16 interface environment, which is used to set enable masks for interrupt request sources. Refer to section 2.5 for more details.

HOST_IS_RG
Read-only register inside host PIOX-16 interface environment, which is used to read interrupt request source status information. Refer to section 2.5 for more details.

HPI
TMS320C54x DSP on-chip 8-bit host port interface, which is used to access DSP on-chip memory and registers from host PIOX-16 interface environment. Refer to section 2.6 for more details.

I

IRQ-0, IRQ-1, IRQ-2,

Host PIOX-16 interface interrupt request inputs, which are used to send interrupt request to host DSP of host *TORNADO* DSP system/controller from *TORNADO-PX/DDC4* DCM. Refer to section 2.5 and Appendix B for more details.

J

JTAG

Joint Test Action Group interface, which is a part of the TMS320C2xx/VC33/C4x/C5x/ C54x/C6x/C8x DSP on-chip hardware and is used for debugging DSP hardware/software for *TORNADO-PX/DDC4* DCM using external JTAG emulators (TI XDS510 and MicroLAB' *MIRAGE-510DX, UECMX*). Refer to section 2.6 for more details.

JTAG-IN

On-board input connector, which is used for connection to external JTAG emulator. Refer to section 2.6 and Appendix A for more details.

K

L

LED

Light emitting diode indicator. Refer to Appendix A for more details.

M

McBSP

TMS320C54x DSP on-chip serial ports. Refer to sections 2.2 and 2.4 for more details.

N

O

P

PDC

On-board Intersil HSP50214 programmable down converters. Refer to sections 2.2 and 2.3 for more details.

PFG-1/2

On-board programmable sampling frequency generators, which can be used to set sampling frequency for on-board ADC-PDC and ADC-FIFO RF signal processing paths. Refer to sections 2.2, 2.3 and 2.4 for more details.

PHDAC

On-board audio quality digital-to-analog converter, which is used either for connection to external phones or for general purpose analog output.. Refer to sections 2.2 and 2.4 for more details.

PIOX

32-bit Parallel I/O eXpansion interface site for compatible daughter-card modules (DCM) at *TORNADO* PC plug-in DSP systems. PIOX comprises of 16-bit PIOX-16 interface site and PIOX-X32 32-bit extension interface site. Refer to sections 2.6 and 3.1, and Appendix B for more details.

PIOX-16

16-bit Parallel I/O eXpansion interface site for compatible daughter-card modules (DCM) at *TORNADO* PC plug-in DSP systems and controllers. *TORNADO-PX/DDC4* DCM plugs into PIOX-16 interface site on host *TORNADO* DSP system/controller. Refer to sections 2.6 and 3.1, and Appendix B for more details.

Pod

Electronic device, which connects external JTAG emulator with *TORNADO-PX/DDC4* on-board JTAG-IN connector for uploading and debugging on-board DSP software.

Q

R

S

SA/NO-BMODE, SA/FLASH8-BMODE

DSP start-up bootmodes for stand-alone operation mode. Refer to section 2.2 for more details.

T

U

UART

Universal Asynchronous Receiver-Transmitter. *TORNADO-PX/DDC4* DCM provides two on-board UART channels (UART-1 and UART-2 as the part of DUART) with RS232C interface for communication with external RF tuners and general purpose peripherals. Each UART channel is hardware compatible with PC COM port controller. Refer to section 2.2 for more details.

V

W

WDT

On-board watch-dog timer, which can be used to restart on-board DSP in case of either idle or mis-operation condition for on-board DSP software. WDT can be used in case *TORNADO-PX/DDC4* DCM is running in stand-alone mode. WDT is controlled via *DSP_WDT_EN_RG* and *DSP_WDT_RES_RG* registers. Refer to section 2.2 for more details.

X

XDAC-1/2

On-board general purpose digital-to-analog converters, which can be used for gain control of external RF amplifiers or for general purpose analog output. Refer to sections 2.2 and 2.4 for more details.

XSL-1/2

On-board external output serial links, which can be used for digital gain control of external RF amplifiers or for general purpose serial output. Refer to sections 2.2 and 2.4 for more details.

Y

Z