TORNADO-PX/DDC4 rev.1B

Quad Channel Digital Radio Receiver PIOX-16 Coprocessor/Controller
for *TORNADO* DSP Systems/Controllers

Addendum to
TORNADO-PX/DDC4 rev.1A
User's Guide

covers:
TORNADO-PX/DDC4 rev.1A-2, rev.1B

About this Document

This document contains addendum to *TORNADO-PX/DDC4 rev.1A User's Guide* in order to describe updates, which have been done in *TORNADO-PX/DDC4 rev.1A-2*. and *rev.1B*.

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1. Revision History

TORNADO-PX/DDC4 rev.1A-2 and *rev.1B* are upward compatible hardware updates for *TORNADO-PX/DDC4 rev.1A* and are shipping since March'2001 (rev.1A) and since June-2003 (rev.1B). Revision 1A-2 hardware update has been introduced as an intermediate upgrade for further compatibility with upcoming *TORNADO-PX/DDC4 rev.1B*, whereas *TORNADO-PX/DDC4 rev.1B* board is a redesigned boar with several new features.

CAUTION

TORNADO-PX/DDC4 rev.1A-2 board is manufactured using *TORNADO-PX/DDC4 rev.1A* PCB (printed circuit board).

TORNADO-PX/DDC4 rev.1A-2 board can be recognized by means of attached label with 'FPGA rev.1A-2' text on it.

TORNADO-PX/DDC4 rev.1B board is a redesigned *TORNADO-PX/DDC4 rev.1A* board with several new features available.

All software, which has been designed for *TORNADO-PX/DDC4 rev.1A* board, will run without any modifications at *TORNADO-PX/DDC4 rev.1A-2* board. For *TORNADO-PX/DDC4 rev.1B* board, only (if any) re-compilation of DSP software for *TORNADO-PX/DDC4 rev.1A* board is required using new provided header file due to a higher capacity on-board FLASH memory used.

Vise-versa, software, which has been designed for *TORNADO-PX/DDC4 rev.1A-2*, will run at *TORNADO-PX/DDC4 rev.1A-2* board without almost any modifications (if any), however this requires clear understanding of all update details, which are described below. Similar, software, which has been designed for *TORNADO-PX/DDC4 rev.1B*, will run at *TORNADO-PX/DDC4 rev.1A-2* without almost any modifications (if any), however this requires clear understanding of all update details, which are described below.

2. What's new in *TORNADO-PX/DDC4 rev.1A-2 board*

The following is a detail list of hardware updates for *TORNADO-PX/DDC4 rev.1A-2* board against previous *TORNADO-PX/DDC4 rev.1A* board release:

- *DSP_SYS_STAT_RG* read-only register (address 00EEH@I/O) has been modified to include *DSP_ID* bit, which allows to identify installed TMS320C54x DSP chip type (either TMS320VC5410 or TMS320VC5416) via DSP software. Since TMS320VC5410 and TMS320VC5416 feature significantly different internal DSP clock frequency (100MHz for TMS320VC5410 and 160MHz for TMS320VC5416), then *DSP_ID* bit allows DSP software to automatically configure DSP on-chip registers SWWSR, SWCR, BSCR and CLKMD registers, which control timing of the DSP expansion bus, as well as to automatically configure other DSP operation registers, which are sensitive to DSP clock frequency (DSP on-chip timer, etc).
- *DSP_XDMP_RG* register (address 00EEH@I/O) has been modified to include bits *FPAGE-2* and *FPAGE-3* bits, which allow to address 4Mbit (512Kx8) FLASH memory instead of currently available

1Mbit (128Kx8) FLASH memory. However, *TORNADO-PX/DDC4 rev.1A-2* is still shipped with 1Mbit FLASH memory only, so this feature has been introduced for compatibility with upcoming *TORNADO-PX/DDC4 rev.1B* release, and bits {*FPAGE-2, FPAGE-3*} of *DSP_XDMP_RG* register shall be actually ignored for *TORNADO-PX/DDC4 rev.1A-2*.

3.　　　 What's new in *TORNADO-PX/DDC4 rev.1B board*

The following is a detail list of hardware updates for *TORNADO-PX/DDC4 rev.1B* board against previous *TORNADO-PX/DDC4 rev.1A-2* board release:

- *TORNADO-PX/DDC4 rev.1B* board is shipping with TMS320C5416 DSP only.
- *TORNADO-PX/DDC4 rev.1B* board can be shipped with either input RF operational amplifiers, or with input RF transformers. Input RF transformers provides better distortions, however features 100kHz..200MHz signal pass bandwidth, whereas RF operational amplifiers can provide as low signal pass frequency as 1kHz. This allows to adopt on-board hardware for different input signal requirements.
- *TORNADO-PX/DDC4 rev.1B* board features improved high-frequency SNR and THD parameters this allowing to perform processing of smaller RF signals.
- *TORNADO-PX/DDC4 rev.1B* board can be shipped with either 10MHz ±50ppm on-board PFG reference clock generator (the same as for *TORNADO-PX/DDC4 rev.1A* and *rev.1A-2* boards), or with high-stable 19.68MHz ±50ppm on-board PFG reference clock generator, which is a typical selection for cellular telephony applications. In order *TORNADO-PX/DDC4* on-board DSP software could correctly configure on-board PFG generators, the frequency ID code for on-board PFG reference clock is available via the corresponding bit of *DSP_SYS_STAT_RG* read-only register. Updated *DDC4_DSP.H* and *DDC4_DX.H* header files for *TORNADO-PX/DDC4* on-board TMS320C54xx DSP environment automatically takes care of the PFG reference clock frequency ID.
- *TORNADO-PX/DDC4 rev.1B* board features reduced power consumption from +12v and –12v power supplies (maximum 80mA per each of power supply), however power consumption at +5v power supply has been increased by 360mA to the total of 1.8A maximum.
- *DSP_SYS_STAT_RG* read-only register (address 00EEH@I/O) has been modified to include *REV_ID* and *PFG_REF_CLK_FREQ_ID* bits, which allow DSP software to identify board revision for automatic detection of on-board FLASH memory capacity (refer to the corresponding item below) and to identify PFG reference clock frequency ID.
- *DSP_XDMP_RG* register (address 00EEH@I/O) has the same format as for *TORNADO-PX/DDC4 rev.1A-2* board with bits *FPAGE-2* and *FPAGE-3* bits, which allow to address 4Mbit (512Kx8) FLASH memory. However, instead of 1Mbit (128Kx8) FLASH memory, which ahs been installed onto *TORNADO-PX/DDC4 rev.1A-2* and *rev.1A* boards, *TORNADO-PX/DDC4 rev.1B* board is shipped with 4Mbit (512Kx8) FLASH memory thus delivering 4x times more on-board FLASH capacity. *TORNADO-PX/DDC4 rev.1B* on-board 4Mbit (512Kx8) FLASH memory is absolutely identically in terms of control to the former 1Mbit (128Kx8) FLASH memory, except for the sector length, which is 64kbytes for 4Mbit FLASH memory instead of 16kbytes for 1Mbi FLASH memory. Updated *DDC4_DSP.H* and *DDC4_DX.H* header files for *TORNADO-PX/DDC4* on-board TMS320C54xx DSP environment automatically takes care of the board revision ID and performs correct selection of FLASH memory sector length.

3.   Updated *DSP_SYS_STAT_RG* register

Below is the data format for updated *DSP_SYS_STAT_RG* register, which is available for read-only and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area. New introduced bits are shown in bold. Table [2-11] provides details about *DSP_SYS_STAT_RG* register bits.

DSP_SYS_STAT_RG register (r)

X	DSP_ID (r)	0	REV_ID (r)	PFG_REF_CLK_FREQ_ID (r)	0	SA_MODE (r)	BMODE-1 (r)	BMODE-0 (r)
bit-15...bit-8	Bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table [2-11]. Register bits of *DSP_SYS_STAT_RG* register.

register bits	access mode	Description
SA_MODE	R	Returns the DSP start up operation mode. *SA_MODE* bit does not change during DSP running until DSP reset signal will be applied. *SA_MODE* =0 corresponds to the on-board DSP running under the control of host PIOX-16 interface (*HOST/NO-BMODE*, *HOST/FLASH8-BMODE* and *HOST/HPI-BMODE* bootmodes in accordance with table 2-1). *SA_MODE* =1 corresponds to the on-board DSP running in stand-alone mode (*SA/NO-BMODE* and *SA/FLASH-BMODE* bootmodes in accordance with table 2-1).
{*BMODE-1, BMODE-0*}	R	Returns DSP boot mode. *BMODE-1/0* bits do not change during DSP running until DSP reset signal will be applied. {*BMODE-1, BMODE-0*} ={0,0} corresponds to the microprocessor start-up modes without boot process (*SA/NO-BMODE* and *HOST/NO-BMODE* bootmodes in accordance with table 2-1). {*BMODE-1, BMODE-0*} ={0,1} corresponds to the microcontroller start-up modes with boot from 8-bit FLASH memory (*SA/FLASH8-BMODE* and *HOST/FLASH8-BMODE* bootmodes in accordance with table 2-1). {*BMODE-1, BMODE-0*} ={0,1} corresponds to the microcontroller start-up modes with boot via HPI port (*HOST/HPI-BMODE* bootmodes in accordance with table 2-1). {*BMODE-1, BMODE-0*} ={1,1} is reserved and should not be read.
DSP_ID	R	Returns DSP ID code. This add to *DSP_SYS_STAT_RG* register is available since *TORNADO-PX/DDC4* rev.1A-2 board. *DSP_ID* =0 corresponds to installed on-board TMS320VC5410 DSP with 100 MHz DSP clock frequency. *DSP_ID* =1 corresponds to installed on-board TMS320VC5416 DSP with 160 MHz DSP clock frequency.

REV_ID	R	Returns board revision ID code. This add to *DSP_SYS_STAT_RG* register is available since *TORNADO-PX/DDC4* rev.1B board. *REV_ID* =0 corresponds to *TORNADO-PX/DDC4 rev.1A* and *rev.1A-2* boards. *REV_ID* =1 corresponds to *TORNADO-PX/DDC4 rev.1B* board.
PFG_REF_CLK_FREQ_ID	R	Returns frequency ID for on-board revision PFG reference clock generator. This add to *DSP_SYS_STAT_RG* register is available since *TORNADO-PX/DDC4* rev.1B board. *PFG_REF_CLK_FREQ_ID* =0 corresponds to on-board 10MHz ±50ppm PFG reference clock generator installed, which was standard for *TORNADO-PX/DDC4 rev.1A* and *rev.1A-2* boards and is also a factory default for *TORNADO-PX/DDC4 rev.1B* board. *PFG_REF_CLK_FREQ_ID* =1 corresponds to on-board high-stable 19.68MHz ±2ppm PFG reference clock generator installed, which is available as an option for *TORNADO-PX/DDC4 rev.1B* boards only.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

4.   Updated *DSP_XDMP_RG* register for selection of accessed external data memory

Below is the data format for updated *DSP_XDMP_RG* register, which is available for read/write and is allocated to the least significant byte of DSP 16-bit data word within the DSP I/O area. New introduced bits are shown in bold. Table [2-10] provides details about *DSP_XDMP_RG* register bits.

DSP_XDMP_RG Register (r/w)

X	XDMEM_SEL (r/w)	0	0	0	**FPAGE-3** **(r/w, 0+)**	**FPAGE-2** **(r/w, 0+)**	FPAGE-1 (r/w, 0+)	FPAGE-0 (r/w, 0+)
bits 15..8	bit-7	Bit-6	bit-5	bit-4	bit-3	Bit-2	bit-1	bit-0

Table [2-10]. Register bits of *DSP_XDMP_RG* register.

register bits	access mode	value on DSP reset	Description
XDMEM_SEL	r/w	0 (for *SA/NO-BMODE HOST/NO-BMODE HOST/HPI-BMODE* bootmodes) 1 (for *SA/FLASH8-BMODE HOST/FLASH8-BMODE* bootmodes)	Defines the memory (DPRAM or FLASH), which is mapped to the [8000H..FFFFH] external data memory address space of on-board TMS320C54x DSP in case bit DROM of DSP on-chip PMST register is set to the DROM=0 state. *XDMEM_SEL* =0 corresponds to DPRAM memory is mapped to the DSP external data memory area. *XDMEM_SEL* =1 corresponds to FLASH memory is mapped to the DSP external data memory area.
FPAGE-0, FPAGE-1, **FPAGE-2, FPAGE-3**	r/w	{0,0,0,0}	Select particular 32K page of 512Kx8 FLASH memory, which is mapped to the [8000H..FFFFH] external data memory address space of on-board TMS320C54x DSP in case bit *XDMEM_SEL* of *DSP_XDMP_RG* register is set to the XDMEM_SEL=1 state and DROM of DSP on-chip PMST register is set to the DROM=0 state. Bits FPAGE-2 and FPAGE-3 have been added since *TORNADO-PX/DDC4 rev.1A-2* board revision. *TORNADO-PX/DDC4 rev.1A-2* board is still shipped with 1Mbit (128Kx8) FLASH memory only (FLASH sector length is 16kbytes), so bits {*FPAGE-2, FPAGE-3*} of *DSP_XDMP_RG* register shall be actually ignored for *TORNADO-PX/DDC4 rev.1A-2*. *TORNADO-PX/DDC4 rev.1B* board is shipped with 4Mbit (512Kx8) FLASH memory (FLASH sector length is 64kbytes), so bits {*FPAGE-2, FPAGE-3*} of *DSP_XDMP_RG* register shall be used for *TORNADO-PX/DDC4 rev.1B* boards.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

CAUTION

DSP_XDMP_RG register defaults to the DPRAM memory selected as external data memory for on-board DSP on the DSP reset condition in case DSP starts in either *SA/NO-BMODE*, or *HOST/NO-BMODE*, or *HOST/HPI-BMODE* bootmode.

DSP_XDMP_RG register defaults to the FLASH memory page #0 selected as external data memory for on-board DSP on the on the DSP reset condition in case DSP starts in either *SA/FLASH8-BMODE* or *HOST/FLASH8-BMODE* bootmode.