

TORNADO-PX64xxQ

23 BIPS Quad TMS320C64xx 32-bit Fixed-point DSP Coprocessor DCM
with Universal Host PIOX-16/PIOX-32 Interface
for *TORNADO* DSP Systems/Controllers

User's Guide

covers:
TORNADO-PX6414Q/PX6415Q/PX6416Q rev.1A

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About this Document

This user's guide contains technical description for *TORNADO-PX64xxQ* quad TMS320C6414/C6415/C6416 DSP coprocessor daughter-card module (DCM) for parallel I/O expansion (PIOX) DCM site of host *TORNADO* DSP systems/controllers.

This document does not include detail description neither for the on-board components nor for the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C6x Peripheral Reference Guide.*** Texas Instruments Inc, SPRU190D, USA, 2001.
2. ***TMS320C6x CPU and Instruction Set Reference Guide.*** Texas Instruments Inc, SPRU189F, USA, 2000.
3. ***TMS320C6x Programmer's Guide.*** Texas Instruments Inc, SPRU198D, USA, 2000.
4. ***TMS320C6x Optimizing C Compiler User's Guide.*** Texas Instruments Inc, SPRU187I, USA, 2001.
5. ***TMS320C6x Assembly Language Tools User's Guide.*** Texas Instruments Inc, SPRU186I, USA, 2001.

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Chapter 1. Introduction

This chapter contains general description for ultra-high performance *TORNADO-PX64xxQ* quad TMS320C64xx 32-bit fixed-point DSP coprocessor DCM with universal host PIOX-16/PIOX-32 interface for *TORNADO* DSP systems and controllers.

TORNADO-PX64xxQ product line comprises of *TORNADO-PX6414Q*, *TORNADO-PX6415Q* and *TORNADO-PX6416Q* DSP coprocessor PIOX DCM, which are designed to accommodate four 32-bit fixed-point TMS320C6414, TMS320C6415 and TMS320C6416 DSP correspondingly from Texas Instruments Inc. (TI).

CAUTION

The particular DSP installed specifies the final name of *TORNADO-PX64xxQ* DSP coprocessor DCM, i.e. *TORNADO-PX6414Q* (with four TMS320C6414 DSP), or *TORNADO-PX6415Q* (with four TMS320C6415 DSP), or *TORNADO-PX6416Q* (with for TMS320C6416 DSP).

CAUTION

‘*TORNADO-PX64xxQ*’ notation denotes that the supplied information is applicable to all *TORNADO-P64xxQ* DSP coprocessor DCM.

Should information be a product specific, then the name of the corresponding product (*TORNADO-PX6414Q*, or *TORNADO-PX6415Q*, or *TORNADO-PX6416Q*) will be highlighted.

1.1 General Information

TORNADO-PX64xxQ is quad TMS320C64xx DSP coprocessor PIOX (parallel I/O expansion) DCM for host *TORNADO* PC plug-in DSP systems and *TORNADO-E* stand-alone DSP controllers from MicroLAB Systems Ltd.

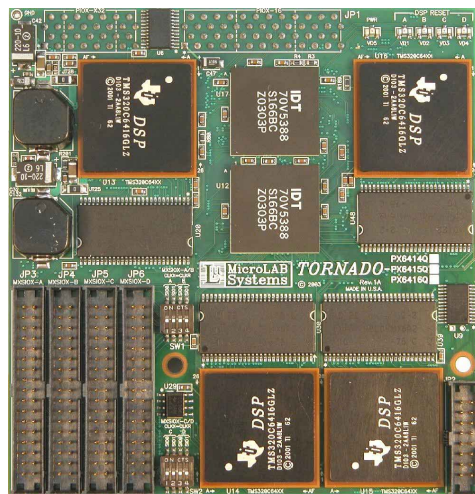


Fig. 1-1. TORNADO-PX64xxQ quad TMS320C64xx DSP coprocessor DCM.

Installation onto TORNADO DSP System/Controller

TORNADO-PX64xxQ quad TMS320C64xx DSP coprocessor DCM plugs either into 32-bit PIOX-32 (parallel I/O expansion) or 16-bit PIOX-16 DCM interface site of host TORNADO PC plug-in DSP systems (fig.1-2a) and host TORNADO-E stand-alone DSP controllers (fig.1-2b) from MicroLAB Systems Ltd.



Fig. 1-2a. TORNADO-PX64xxQ DCM installed into 32-bit PIOX-32 DCM site of host TORNADO-P6416 PCI-bus plug-in DSP system.

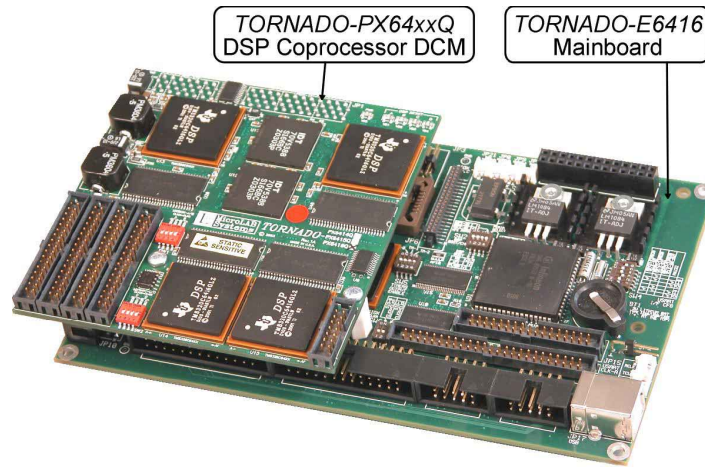


Fig. 1-2b. *TORNADO-PX64xxQ* DCM installed into 16-bit PIOX-16 DCM site of host *TORNADO-E6416* stand-alone DSP controller.

Overview

TORNADO-PX64xxQ DSP coprocessor DCM provides four on-board 32-bit fixed-point TMS320C6414/C6415/C6416 DSP from TI.

Each of on-board TMS320C64xx DSP runs at either 600 MHz (*TORNADO-PX64xxQ/600*) or 720 MHz (*TORNADO-PX64xxQ/720*) and provides up to 4800 MIPS or 5760 MIPS peak DSP performance correspondingly for the total of 19.2 BIPS or 23.040 BIPS.

Each of on-board TMS320C64xx DSP features 1 Mbyte on-chip RAM for program/data/cache, three McBSP serial ports, 64 DMA channels, three timers, and either 4Mx32 or 16Mx32 external synchronous dynamic RAM (SDRAM).

On-board DSP-to-DSP communication can be performed either via 32Kx32 or 64Kx32 shared static RAM (SSRAM), which is shared between all on-board DSP, or DSP on-chip McBSP ports (serial links), or via mutual interrupt requests.

Host PIOX interface provides access to HPI port of each on-board TMS320C64xx DSP, and contains a set of control registers for DSP reset, host interrupt selection, and for error processing.

External I/O

TORNADO-PX64xxQ DSP coprocessor DCM provides on-board four MXSIOX (mini serial I/O expansion) interface connectors for optional connection of external SIOX rev.B (serial I/O expansion) DCM for real-time analog/digital I/O DCM (one SIOX rev.B DCM per each DSP), or for board-to-board communication between multiple *TORNADO-PX64xxQ* DSP coprocessor DCM or compatible devices in multi-board multi-DSP systems.

This feature allows to use *TORNADO-PX64xxQ* DSP coprocessor DCM either as application specific I/O DSP coprocessor (depending upon the type of connected SIOX rev.B DCM) in order to unload host *TORNADO* DSP

system/controller from real-time I/O operations, or to expand DSP coprocessor DCM network via board-to-board links.

Up to four external *T/SU-X1*, *T/SU-X2* or *T/SU-X3* SIOX rev.B mini-extendors can be connected to *TORNADO-PX64xxQ* on-board MXSIOX interface connectors for real-time analog/digital I/O via external SIOX rev.B DCM as shown at figure 1-3a.

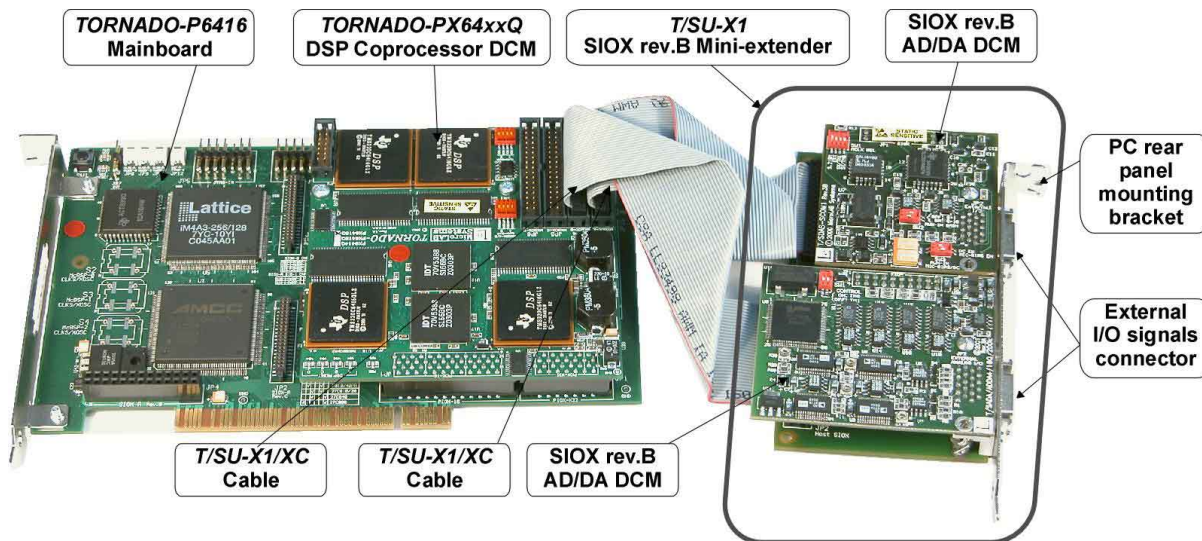


Fig. 1-3a. *TORNADO-PX6416* DSP system with *TORNADO-PX64xxQ* DSP coprocessor DCM with two optional *T/SU-X1* SIOX rev.B mini-extendors and two SIOX rev.B AD/DA DCM used for external analog signal I/O.

Up to four external *T/X-XSLC1* serial link converters can be connected to *TORNADO-PX64xxQ* on-board MXSIOX interface connectors for board-to-board communication between several *TORNADO-PX64xxQ* DSP coprocessor DCM or compatible serial link devices (for example *TORNADO-PX/DDC4G* 105 MHz quad digital radio receiver coprocessor DCM) as shown at figure 1-3b.

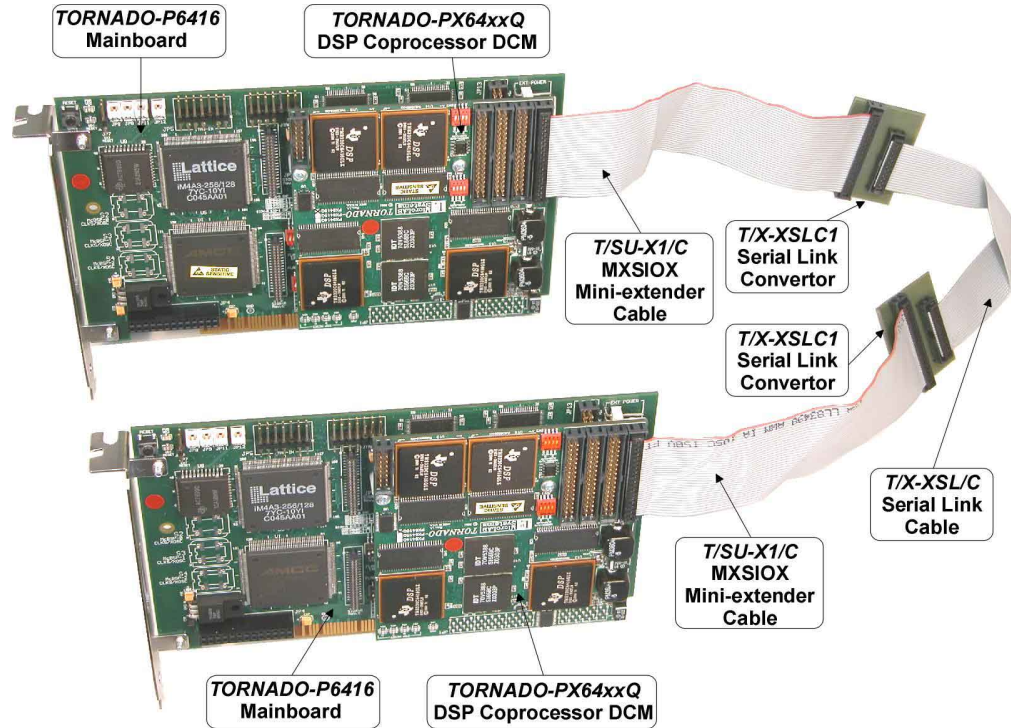


Fig. 1-3b. Two **TORNADO-PX6416** DSP systems with **TORNADO-PX64xxQ** DSP coprocessor DCM installed using optional **T/X-XSLC1** serial link converters for board-to-board communication.

Optional external **T/SU-X1**, **T/SU-X2** and **T/SU-X3** SIOX rev.B mini-extendors and **T/X-XSLC1** serial link converter connect directly to **TORNADO-PX64xxQ** DSP coprocessor DCM via on-board dedicated connectors and **T/SU-X1/XC** extender cable, and can install either at the rear-panel of host PC chassis or into custom chassis.

Applications

TORNADO-PX64xxQ DSP coprocessor DCM has been designed for general purpose multi-DSP and multi-board applications with optional real-time analog/digital I/O, on-board DSP-to-DSP communication, and for external board-to-board communication. Application areas include multi-channel speech/fax/modem signal processing, multi-channel digital radio, multi-channel IP telephony, etc applications, which require multi-channel DSP with optional real-time I/O.

1.2 Technical Specification

The following are technical specifications for **TORNADO-PX64xxQ** DSP coprocessor DCM for **TORNADO** DSP systems/controllers.

<i><u>Parameter description</u></i>	<i><u>parameter value</u></i>
<i>DSP</i>	
DSP type	TMS320C6414 (<i>TORNADO-PX6414Q</i>) TMS320C6415 (<i>TORNADO-PX6415Q</i>) TMS320C6416 (<i>TORNADO-PX6416Q</i>) from Texas Instruments Inc
DSP clock frequency	600 MHz (<i>TORNADO-PX64xxQ/600</i>) 720 MHz (<i>TORNADO-PX64xxQ/720</i>)
number of on-board DSP	4
<i>On-board memory</i>	
Synchronous shared static RAM (SSRAM)	0K/32K/64Kx32 (0ws synchronous quad-port static RAM)
Synchronous dynamic RAM (SDRAM) per DSP	0M/4M/16Mx32 0ws SDRAM
<i>DSP-to-DSP communication</i>	
Maximum serial data rate for on-board DSP-to-DSP communication via serial links	75 Mbit/s (600 MHz TMS320C64xx DSP) 60 Mbit/s (720 MHz TMS320C64xx DSP)
Maximum serial data rate for external board-to-board communication via serial links and real-time I/O via external SIOX rev.B DCM	50 Mbit/s (600 MHz TMS320C64xx DSP) 45 Mbit/s (720 MHz TMS320C64xx DSP)
<i>On-board MXSIOX interface connectors for external SIOX rev.B DCM options and board-to-board communication</i>	
support for external SIOX rev.B DCM	via <i>T/SU-X1</i> , <i>T/SU-X2</i> , and <i>T/SU-X3</i> SIOX rev.B mini-extendors
support for board-to-board communication	via <i>T/X-XSLC1</i> serial link converters
number of on-board MXSIOX interface connectors for connection to external <i>T/SU-X1</i> , <i>T/SU-X2</i> , <i>T/SU-X3</i> external SIOX rev.B mini-extendors and/or <i>T/X-XSLC1</i> external serial link converters	4 (one MXSIOX connector per each DSP)
maximum recommended CLKX/CLKR frequency (for 0.25m long SIOX rev.B mini-extender cable)	50 MHz
<i>Host PIOX Interface</i>	
supported PIOX data format modes	32-bit PIOX-32 16-bit PIOX-16 (auto detected with software selection)
supported TMS320C64xx HPI data format modes	16/32-bit (software selected)

software configured PIOX interrupt request inputs	IRQ-0, IRQ-1, IRQ-2, IRQ-3
I/O ports	8-bit control registers (32) 16/32-bit DSP HPI ports (32)
access time	< 20 ns (control registers access) < 40ns..160ns (typ HPI access)
TMS320C64xx DSP HPI port access timeout	2.5us (software enabled)
<i>physical and power:</i>	
Dimensions	3.60" x 3.75" (91.4 x 95.3 mm)
Power supplies required	+5v for operation of on-board hardware ±12v/-5v are routed to on-board MXSIOX interface connectors
power consumption via host PIOX interface (without external optional SIOX rev.B DCM)	+5v @ 1.8 A (typ) ±12v/-5v are routed to MXSIOX connectors
external operating temperature	0°C .. +60°C

Chapter 2. System Architecture and Construction

This chapter contains detail description for architecture and construction of *TORNADO-PX64xxQ* DSP coprocessor DCM for *TORNADO* DSP systems/controllers.

2.1 System Architecture

System architecture and construction for *TORNADO-PX64xxQ* DSP coprocessor DCM are presented at fig.2-1 and fig.2-2 correspondingly.

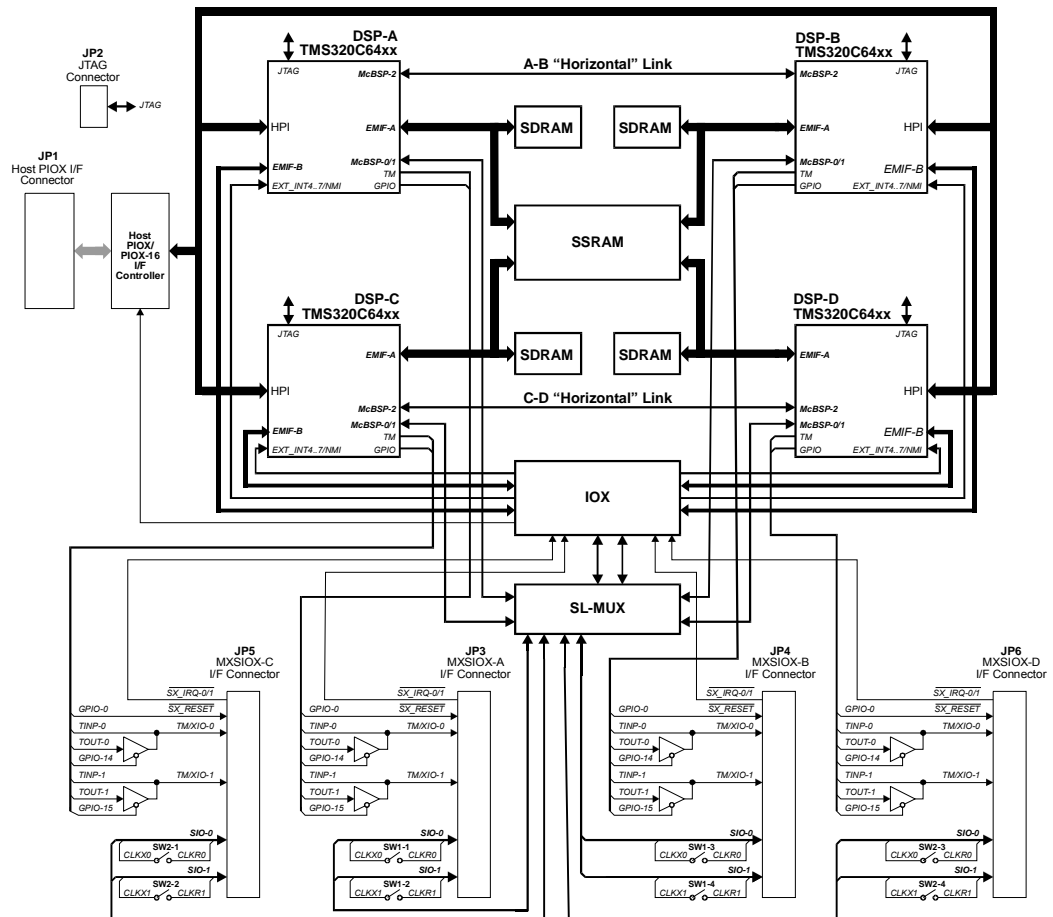


Fig.2-1. Block diagram of *TORNADO-PX64xxQ* DSP Coprocessor DCM.

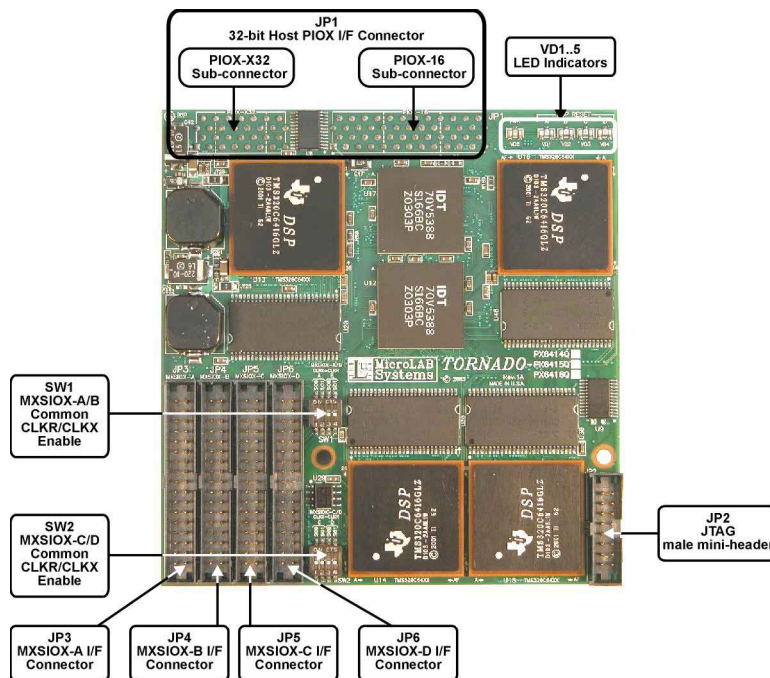


Fig.2-2. Construction of *TORNADO-PX64xxQ* DSP Coprocessor DCM.

TORNADO-PX64xxQ DSP coprocessor DCM installs as PIOX or PIOX-16 DCM onto host *TORNADO* DSP system/controller mainboard and comprises of the following components:

- four 32-bit fixed-point TMS320C64xx DSP with up to 720 MHz DSP clock frequency providing up to 5760 MIPS peak DSP peak performance
- up to 16Mx32 (64 Mbytes) local synchronous dynamic RAM (SDRAM) memory for each DSP, which are connected to EMIF-A interface of the corresponding DSP and can be used to store large local data arrays
- up to 64Kx32 (256 kbytes) synchronous shared static RAM (SSRAM) available for all DSP, which , which is connected to EMIF-A interface of each DSP and can be used for high-speed data exchange between DSP
- MXSIOX-A..B interface connectors (JP3..JP6) for connection to optional external *T/SU-X1*, *T/SU-X2* or *T/SU-X3* SIOX rev.B mini-extendors, which can be used either to install SIOX rev.B DCM for analog/digital I/O, and/or for connection to optional external *T/X-XSLC1* serial link converters for board-to-board communication for multi-board multi-DSP system expansion
- common CLKX/CLKR serial clock enable switches (SW1..SW4) for MXSIOX-A..B interface connectors
- 'A-to-B' and 'C-to-D' DSP-to-DSP 'horizontal' serial links, which are provided via TMS320C64xx DSP on-chip McBSP-2 serial ports
- DSP-to-DSP serial links multiplexer (SL-MUX), which is used to enable/disable 'vertical' and 'diagonal' serial links for on-board DSP-to-DSP communication and to alternatively disable/enable SIO-1 and SIO-0 serial ports of on-board MXSIOX-A..D interface connectors
- DSP I/O expansion (IOX) controller

- JTAG connector (JP2) for connection to external JTAG emulator
- host PIOX interface header (JP1) for installation onto host *TORNADO* DSP systems/controllers and host PIOX interface controller.

DSP pool

TORNADO-PX64xxQ on-board DSP pool comprises of four state of the art 32-bit fixed-point TI TMS320C6414 (*TORNADO-PX6414Q*), TMS320C6415 (*TORNADO-PX6415Q*), or TMS320C6416 (*TORNADO-PX6416Q*) DSP, which are on-board numbered as DSP-A..D and are organized as 2x2 DSP pool. Each DSP runs at 600 MHz (*TORNADO-PX64xxQ/600*) or 720 MHz (*TORNADO-PX64xxQ/720*) internal DSP clock frequency thus delivering summary on-board 19,200 MIPS and 23,040 MIPS peak DSP performance correspondingly.

TI TMS320C64xx DSP feature VelociTI very-long instruction word (VLIW) on-chip architecture, 1 Mbyte on-chip RAM for program and data, 64 EDMA channels, three McBSP serial ports, three timers, and hardware Viterbi and Turbo decoders (TMS320C6416 DSP only).

Data transfer between host *TORNADO* DSP system/controller and DSP environment (DSP on-chip memory, SDRAM, SSRAM, etc) for each on-board TMS320C64xx DSP as well as upload of DSP start-up code are performed via host PIOX interface using DSP on-chip HPI port either in 16-bit or 32-bit HPI data format mode.

For more details about TMS320C64xx DSP refer to the corresponding original TI documentation and to section [“TMS320C64xx DSP Environment”](#) later in this chapter.

On-board synchronous dynamic RAM (SDRAM) memory

TORNADO-PX64xxQ DSP coprocessor DCM provides either 4Mx32 or 16Mx32 on-board local SDRAM for each TMS320C64xx DSP for local large real-time data arrays. Local SDRAM is connected to the EMIF-A external memory interface of each TMS320C64xx DSP.

For more details about SDRAM memory refer to section [“TMS320C64xx DSP Environment”](#) later in this chapter.

On-board DSP-to-DSP communication paths

TORNADO-PX64xxQ DSP coprocessor DCM provides several flexible on-board DSP-to-DSP communication paths, which have been designed to meet different multi-DSP user applications:

- DSP-to-DSP communication via either 32Kx32 or 64Kx32 on-board shared static RAM (SSRAM), which is shared by all on-board TMS320C64xx DSP. SSRAM is a ideal solution for high-speed data exchange via shared variables and data arrays. SSRAM is typically used for DSP-to-DSP synchronization and transfer of small real-time data arrays. SSRAM appears as a high-speed synchronous quad-port static RAM (QPRAM) connected to EMIF-A external memory interface of each TMS320C64xx DSP. SSRAM supports generation of *ORed interrupt requests via shared SSRAM* to each on-board DSP along with message pass via dedicated SSRAM memory locations. For more details about DSP-to-DSP communication via SSRAM memory refer to section [“TMS320C64xx DSP Environment”](#) later in this chapter.
- DSP-to-DSP communication via ‘horizontal’, ‘vertical’ and ‘diagonal’ serial links, which are actually TMS320C64xx DSP on-chip McBSP-0/1/2 serial ports routed via on-board serial link multiplexer (SL-MUX). Serial links are typically used for stream-line data bulk real-time data transfers under the control of TMS320C64xx DSP on-chip EDMA controllers. ‘Vertical’ and ‘diagonal’ serial links for

each DSP can be enabled/disabled by host *TORNADO* DSP software and, once disabled, can be routed out to on-board MXSIOX edge connectors for external analog I/O and/or for board-to-board communication. For more details about DSP-to-DSP communication via 'horizontal', 'vertical' and 'diagonal' serial links refer to section [“TMS320C64xx DSP Environment”](#) later in this chapter.

- DSP-to-DSP communication via 'horizontal', 'vertical' and 'diagonal' *interrupt requests*, which are available for each DSP and correspond to generation of interrupt request to the 'horizontal', 'vertical' and 'diagonal' DSP neighbour node. 'Horizontal', 'vertical' and 'diagonal' interrupt requests are typically used to set DSP-to-DSP ready or attention events without any data message passing. 'Horizontal', 'vertical' and 'diagonal' interrupt requests are used to generate node-to-node interrupt requests with the sender DSP node being exactly identified by the recipient DSP node. For more details about DSP-to-DSP communication via 'horizontal', 'vertical', 'diagonal' and 'DSP broadcast' DSP-to-DSP interrupt requests refer to section [“TMS320C64xx DSP Environment”](#) later in this chapter.
- DSP-to-DSP communication via *ORed interrupt requests via shared SSRAM*, which are typically used to set attention event to particular DSP along with data message passing. ORed interrupt requests via SSRAM can be generated to any particular on-board DSP as the logical OR of interrupt requests from all DSP neighbours of this DSP. The recipient DSP node will be generally unable to identify the sender DSP node. For more details about generation of interrupt requests via SSRAM memory refer to section [“TMS320C64xx DSP Environment”](#) later in this chapter.

For more details about different DSP-to-DSP communication paths refer to section [“TMS320C64xx DSP Environment”](#) later in this chapter.

External analog/digital I/O via optional SIOX rev.B DCM

TORNADO-PX64xxQ DSP coprocessor DCM provides on-board MXSIOX-A..D interface connectors (JP3..6) for optional connection of up to four external *T/SU-X1*, *T/SU-X2* or *T/SU-X3* SIOX rev.B mini-extendors (one mini-extender per each DSP node).

Each external *T/SU-X1*, *T/SU-X2* and *T/SU-X3* SIOX rev.B mini-extender can carry one or two SIOX rev.B DCM. This allows to add AD/DA/DIO and application specific I/O front-end feature to each TMS320C64xx DSP core and to convert *TORNADO-PX64xxQ* DSP coprocessor DCM into universal DSP and application specific I/O coprocessor.

A variety of SIOX rev.B DCM include speech/fax/modem AD/DA DCM, telecom interfaces, audio AD/DA, DAT interface, multi-channel instrumentation AD/DA/DIO DCM, application specific I/O coprocessors, and many more.

SIOX rev.B sites of *T/SU-X1*, *T/SU-X2* or *T/SU-X3* SIOX rev.B mini-extendors comprise of signals for two serial ports (SIO-0 and SIO-1), two timer/IO lines, two external interrupt request inputs, reset control, and power supplies.

SIO-0 and SIO-1 serial ports of each MXSIOX interface connector are routed to McBSP-0 and McBSP-1 serial ports of the corresponding TMS320C64xx DSP in case the corresponding 'diagonal' and 'vertical' serial links are disabled for the corresponding DSP.

For more details about support for external SIOX rev.B DCM sites refer to section [“Serial I/O Expansion Interface \(MXSIOX\)”](#) later in this chapter, and [Appendix 'C'](#) later in this manual.

Board-to-board communication via MXSIOX interface connectors

Along with connection to optional external *T/SU-X1*, *T/SU-X2* or *T/SU-X3* SIOX rev.B mini-extendors for analog/digital I/O expansion via external SIOX rev.B DCM, on-board MXSIOX-A..D interface connectors of *TORNADO-PX64xxQ* DSP coprocessor DCM can be also used for board-to-board communication via serial links in multi-board multi-DSP systems. Board-to-board communication via serial links is available via *T/X-XSLC1* serial link converters, which connect directly to *TORNADO-PX64xxQ* on-board MXSIOX connector.

For more details about board-to-board communication via optional external *T/X-XSLC1* serial link converters refer to section [“TMS320C64xx DSP environment”](#) and [Appendix ‘C’](#) later in this manual.

DSP I/O expansion controller (IOX)

TORNADO-PX64xxQ DSP coprocessor DCM provides DSP I/O expansion controller (IOX), which comprises of a set of external local I/O ports for each on-board DSP used for DSP environment control and DSP-to-DSP interrupt request generation. DSP IOX controller is connected to EMIF-B external memory interface of each on-board DSP.

For more details about DSP IOX control registers refer to section [“TMS320C64xx DSP Environment”](#) later in this chapter.

DSP external interrupts

TORNADO-PX64xxQ DSP coprocessor DCM provides multi-source software configured four TMS320C64xx DSP EXT_INT4..7 external interrupts and NMI for each of on-board DSP. Available interrupt sources comprise of DSP-to-DSP ‘horizontal’, ‘vertical’ and ‘diagonal’ interrupt requests, ‘host broadcast’ interrupt request, corresponding interrupt request from SSRAM, and two external interrupt requests from the corresponding MXSIOX interface connector. Selection of particular interrupt source for each of four DSP external interrupts and NMI for each on-board DSP is performed by means of the corresponding interrupt selector registers, which are the part of the DSP IOX controller.

Host PIOX interface and controller

TORNADO-PX64xxQ DSP coprocessor DCM allows installation into both 32-bit PIOX-32 and 16-bit PIOX-16 I/O expansion site of host *TORNADO* DSP system/controller.

Host PIOX interface controller comprises of a set of control and status registers for DSP reset control, host PIOX interrupt control, error processing and for access to HPI port of each on-board TMS320C64xx DSP.

On-board logic automatically detects the type of host PIOX interface (JP1 connector) and allows software selection between 32-bit and 16-bit data formats for access to DSP on-chip HPI ports in case host 32-bit PIOX-32 interface is detected.

For more details about host PIOX interface and controller refer to section [“Host PIOX Interface”](#) later in this chapter and to [Appendix ‘B’](#) later in this manual.

DSP reset control and LED indicators

Individual reset signals for each on-board TMS320C64xx DSP can be set by host *TORNADO* DSP software via the corresponding control registers of host PIOX interface controller of *TORNADO-PX64xxQ* DSP coprocessor DCM.

For user convenience, on-board LED indicators (VD1..VD5) are used in order to display current state of DSP reset signal and of host power.

Debugging of TMS320C64xx DSP software

On-board TMS320C64xx DSP software for *TORNADO-PX64xxQ* DSP coprocessor DCM can be developed and debugged using either TI XDS or MicroLAB Systems *MIRAGE* JTAG scan-path emulators via on-board JTAG connector (JP2) and TI C6000 Code Composer Studio tools.

For more details about debugging TMS320C64xx DSP software for *TORNADO-PX64xxQ* DSP coprocessor DCM refer to section [“Emulation Tools for TORNADO-PX64xxQ DSP Coprocessor DCM”](#) later in this chapter.

2.2 TMS320C64xx DSP Environment

TORNADO-PX64xxQ on-board DSP environment comprises of four state of the art 32-bit fixed-point TI TMS320C6414 (*TORNADO-PX6414Q*), TMS320C6415 (*TORNADO-PX6415Q*), or TMS320C6416 (*TORNADO-PX6416Q*) DSP.

TORNADO-PX64xxQ on-board DSP pool can be used for general purpose multi-channel DSP applications, for communication with host *TORNADO* DSP system/controller, for communication with optional external SIOX rev.B AD/DA/DIODECM for real-time analog/digital I/O and for board-to-board communication with external compatible DSP boards via serial links.

TMS320C64xx DSP pool

TORNADO-PX64xxQ on-board TI TMS320C64xx DSP feature VelociTI very-long instruction word (VLIW) on-chip architecture, 1 Mbyte on-chip RAM for program and data, 64 EDMA channels, three McBSP serial ports, three timers, and hardware Viterbi and Turbo decoders (TMS320C6416 DSP only).

Each DSP runs at either 600 MHz (*TORNADO-PX64xxQ/600*) or 720 MHz (*TORNADO-PX64xxQ/720*) internal DSP clock frequency thus delivering summary on-board DSP performance 19,200 MIPS and 23,040 MIPS correspondingly. EMIF-A/B bus clock for each TMS320C64xx DSP is either 100 MHz for 600 MHz DSP grade, or 120 MHz for 720 MHz DSP grade.

CAUTION

This manual does not contain description and programming details
for on-board TI TMS320C64xx DSP.

For more information refer to original TI TMS320C64xx datasheet and user's guides for
TMS320C64xx DSP, which are supplied in either paper or electronic form together with this
manual.

TORNADO-PX64xxQ on-board TI TMS320C64xx DSP are organized as 2x2 DSP pool and are on-board numbered as DSP-A..D (refer to fig.2-1) and have unique associated DSP node ID for each on-board DSP. Each of on-board TMS320C64xx DSP has its 'corresponding 'horizontal', 'vertical' and 'diagonal' DSP neighbours

and can communicate with them via on-board SSRAM, DSP-to-DSP serial links and DSP-to-DSP interrupt requests. For more details about DSP-to-DSP communication refer to subsection [“Summary of DSP-to-DSP communication”](#) below.

TORNADO-PX64xxQ on-board DSP software and host *TORNADO* DSP software can read the speed grade ID for on-board TMS320C64xx DSP via [DSP_REV_ID_RG](#) IOX control register and [HOST_DEV_ID_RG](#) host interface control register correspondingly in order to perform run-time configuration of the corresponding environments.

TMS320C64xx DSP endian mode

TORNADO-PX64xxQ DSP coprocessor DCM supports little endian mode only for all on-board TMS320C64xx DSP.

TMS320C64xx DSP memory map

All *TORNADO-PX64xxQ* on-board TMS320C64xx DSP feature identical memory map, which comprises of the following valid DSP memory areas:

- TMS320C64xx DSP on-chip memory and control registers areas in accordance with TMS320C64xx DSP on-chip memory map (refer to original TI documentation for TMS320C64xx DSP for more details)
- EMIF-A CE-0 area, which is used to control shared 32-bit SSRAM memory bank
- EMIF-A CE-2 area, which is used to control local 32-bit SDRAM memory bank
- EMIF-B CE-0 area, which is used to controls local 4-bit IOX control registers.

CAUTION

Unlisted DSP memory areas are reserved and shall not be accessed from TMS320C64xx DSP software.

CAUTION

TMS320C64xx DSP address space for *TORNADO-PX64xxQ* DSP coprocessor DCM is the address space for 8-bit (byte) data words.

16-bit data words are allocated on the x2 address boundaries.

32-bit data words are allocated on x4 address boundaries.

Detail memory map for *TORNADO-PX64xxQ* on-board TMS320C64xx DSP is presented in table 2-1.

Table 2-1. Memory map for TMS320C64xx DSP of *TORNADO-PX64xxQ* DSP coprocessor.

memory area of TMS320C64xx DSP	DSP address range (in bytes)	valid data bits	value at DSP RESET	access mode	wait states (EMIF bus clock cycles)	EMIF CE area and mode
On-board (DSP off-chip) memories						
SSRAM	80000000H ..8001FFFFH (32Kx32) 80000000H ..803FFFFFH (64Kx32)	D0..D31	-	r/w	0ws	EMIF-A CE-0 32-bit SBSRAM mode
SSRAM: SSRAM DSPA_RQ SSRAM location (DSP-B/C/D to DSP-A interrupt request via SSRAM)	8001FFFCH (32Kx32) 8003FFFCH (64Kx32)	D0..D31	-	r/w	0ws	
SSRAM: SSRAM DSPB_RQ SSRAM location (DSP-A/C/D to DSP-B interrupt request via SSRAM)	8001FFF8H (32Kx32) 8003FFF8H (64Kx32)	D0..D31	-	r/w	0ws	
SSRAM: SSRAM DSPC_RQ SSRAM location (DSP-A/B/D to DSP-C interrupt request via SSRAM)	8001FFF4H (32Kx32) 8003FFF4H (64Kx32)	D0..D31	-	r/w	0ws	
SSRAM: SSRAM DSPD_RQ SSRAM location (DSP-A/B/C to DSP-D interrupt request via SSRAM)	8001FFF0H (32Kx32) 8003FFF0H (64Kx32)	D0..D31	-	r/w	0ws	
SDRAM	A0000000H ..A0FFFFFFH (4Mx32) A0000000H ..A3FFFFFFH (16Mx32)	D0..D31	-	r/w	0ws	EMIF-A CE-2 32-bit SDRAM mode

IOX control registers						
IOX area: <u>DSP_EXT_INT4_SEL_RG</u> register (DSP_EXT_INT4 source selector)	60000000H	D0..D3 @W16	0H	r/w	AWS	EMIF-B CE-0 16-bit ASYNC mode
IOX area: <u>DSP_EXT_INT5_SEL_RG</u> register (DSP_EXT_INT5 source selector)	60000002H	D0..D3 @W16	0H	r/w	AWS	
IOX area: <u>DSP_EXT_INT6_SEL_RG</u> register (DSP_EXT_INT6 source selector)	60000004H	D0..D3 @W16	0H	r/w	AWS	
IOX area: <u>DSP_EXT_INT7_SEL_RG</u> register (DSP_EXT_INT7source selector)	60000006H	D0..D3 @W16	0H	r/w	AWS	
IOX area: <u>DSP_NMI_SEL_RG</u> register (DSP NMI source selector)	60000008H	D0..D3 @W16	0H	r/w	AWS	
IOX area: <u>DSP_DEV_ID_RG</u> register (device ID)	6000000aH	D0..D3 @W16	-	R	AWS	
IOX area: <u>DSP_REV_ID_RG</u> register (revision ID)	6000000cH	D0..D3 @W16	-	R	AWS	
IOX area: <u>DSP_SYS_STAT_RG</u> register (system information)	6000000eH	D0..D3 @W16	-	R	AWS	
IOX area: <u>DSP_NODE_ID_RG</u> register (DSP node ID)	60000010H	D0..D3 @W16	-	R	AWS	
IOX area: <u>DSP_XMEM_LEN_ID_RG</u> register (DSP external memory configuration)	60000012H	D0..D3 @W16	-	R	AWS	

IOX area: <u>DSP BROADCAST RQ RG</u> register (broadcast request generation to all other DSP)	60000018H	Write data is ignored @W16	-	W	AWS	
IOX area: <u>DSP HORIZ RQ RG</u> register (request generation to the 'horizontal' DSP neighbour node)	6000001aH	Write data is ignored @W16	-	W	AWS	
IOX area: <u>DSP VERT RQ RG</u> register (request generation to the 'vertical' DSP neighbour node)	6000001cH	Write data is ignored @W16	-	W	AWS	
IOX area: <u>DSP DIAG RQ RG</u> register (request generation to the 'diagonal' DSP neighbour node)	6000001eH	Write data is ignored @W16	-	W	AWS	
<i>DSP on-chip memory and peripheral registers</i>						
TMS320C64xx DSP on-chip RAM (refer to original TI documentation for more details)	00000000H ..000FFFFFH	D0..D31	-	r/w	-	-
TMS320C64xx DSP on-chip peripheral registers (refer to original TI documentation for more details)	01800000H ..02000033H	D0..D31	-	r/w	-	-

- Notes:
1. IOX area denotes on-board I/O expansion controller.
 2. 'AWS' denotes number of software programmed wait states for accessing asynchronous EMIF-B CE-0 area, which is the sum of read/write strobe wait states, read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
 3. @W16 denotes that the address step for consecutive data words of this area corresponds to 16-bit data words. Refer to the corresponding subsection below for more details.
 4. Other DSP memory and I/O areas are reserved. Do not access these DSP address areas.
 5. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

TMS320C64xx DSP reset control

Individual reset signals for each *TORNADO-PX64xxQ* on-board TMS320C64xx DSP are controlled by host *TORNADO* DSP software via *DSPA_RESET...DSPD_RESET* bits of [HOST_CNTR1_RG](#) host interface control register of host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM (refer to [table 2-16](#) and section "[Host PIOX Interface](#)" later in this chapter for more details).

On-board LED indicators (VD1..VD4) are provided for visual indication of current state for the reset signals for each of on-board *TORNADO-PX64xxQ* DSP.

TMS320C64xx DSP bootmode configuration

TORNADO-PX64xxQ DSP coprocessor allows to configure on-board TMS320C64xx DSP to start either without bootmode or boot via DSP on-chip HPI port in order to meet requirements of different applications.

TORNADO-PX64xxQ DSP coprocessor DCM allows to configure identical or individual DSP bootmodes for each of on-board TMS320C64xx DSP by host **TORNADO** DSP software via **DSP_BMODE_CNTR** bit of **HOST_CNTR2_RG** host interface control register of host PIOX interface in accordance with [table 2-2](#) below (refer to [table 2-17](#) and section “Host PIOX Interface” later in this chapter for more details).

CAUTION

DSP_BMODE_CNTR bit of **HOST_CNTR2_RG** register of host PIOX interface are used to set DSP bootmode for particular DSP(s) only during release of these DSP(s) from the reset state, i.e. when the corresponding **DSPA_RESET..DSPD_RESET** bits of **HOST_CNTR1_RG** host interface control register perform transition from the ‘0’ to the ‘1’ state (refer to [table 2-16](#) and section “Host PIOX Interface” later in this chapter for more details).

After the reset signal(s) for particular DSP(s) will be released via bits **DSPA_RESET..DSPD_RESET** of **HOST_CNTR1_RG** host interface control register of host PIOX interface, then these DSP(s) will start execution in accordance with selected DSP bootmode, which is fixed and not anymore effected by bit **DSP_BMODE_CNTR** of **HOST_CNTR2_RG** host interface control register (refer to [table 2-17](#) and section “Host PIOX Interface” later in this chapter for more details).

The DSP bootmode status for all on-board DSP, which have been releases from the reset state, are available for host **TORNADO** DSP software via bits **DSP-A_BMODE_STAT..DSP-D_BMODE_STAT** of **HOST_DSP_CNF_STAT_RG** host interface control register (refer to [table 2-17](#) and section “Host PIOX Interface” later in this chapter for more details), and is available for DSP software of each on-board TMS320C64xx DSP via **DSP_BMODE** bit of **DSP_SYS_STAT_RG** IOX control register (refer to [table 2-4](#)).

Table 2-2. TMS320C64xx DSP bootmode configurations for **TORNADO-PX64xxQ** on-board DSP.

TMS320C64xx DSP Bootmode	Description	DSP_BMODE_CNTR bit of HOST_CNTR2_RG register	DSPA_RESET..DSPD_RESET bits of HOST_CNTR1_RG register
NO BOOT	No DSP boot process.	0	0→1
HPI BOOT	DSP boot via HPI port.	1	0→1

Note: 1. '0→1' denotes transition from the '0' state to the '1' state for the corresponding bit.
2. Highlighted configuration corresponds to host PIOX reset condition.

In case *TORNADO-PX64xxQ* on-board TMS320C64xx DSP is configured to start in '*NO BOOT*' mode, then it will start execution from DSP on-chip memory address 0x00000000 immediately after release of the reset signal for this DSP. '*NO BOOT*' DSP bootmode is typically selected during debugging of DSP software via JTAG emulator and in case DSP execution code has been already uploaded into DSP on-chip memory.

In case '*HPI BOOT*' DSP bootmode is selected, then TMS320C64xx DSP kernel is held in the reset state after release of DSP reset signal while the remainder of the DSP devices is functional, including DSP on-chip HPI port and EMIF-A/B external memory interfaces. In '*HPI BOOT*' DSP bootmode, host *TORNADO* DSP software can access all DSP memory areas including DSP on-chip and off-chip memories and peripherals in order to upload code/data into DSP environment.

CAUTION

Accessing DSP off-chip memories (SSRAM, SDRAM) and IOX control registers during '*HPI BOOT*' DSP bootmode requires that host *TORNADO* DSP software must correctly configure all DSP on-chip EMIF-A/B control registers via DSP HPI port in accordance with [table 2-3](#) prior accessing external DSP memories.

TMS320C64xx DSP on-chip EMIF-A/B control registers can be configured by host *TORNADO* DSP application software using supplied *TORNADO-PX64xxQ* host DSP control utilities (refer to [Appendix 'D'](#) of this manual for more details).

In '*HPI BOOT*' DSP bootmode, TMS320C64xx DSP kernel will be released from the reset state and will start program execution from memory location at address 0x00000000H as soon as host *TORNADO* DSP software will set *DSPINT* bit of DSP on-chip *HPIC* register for this DSP (the corresponding *HOST_HPI32_DSPx_HPIC_RG*, or *HOST_HPI16_DSPx_HPIC_LSW_RG* and *HOST_HPI32_DSPx_HPIC_MSW_RG* registers of *TORNADO-PX64xxQ* host PIOX interface, refer to [table 2-15](#) and section '[Host PIOX Interface](#)' later in this chapter for more details). Note, that '*HPI BOOT*' DSP bootmode is the only way to upload DSP execution code from host *TORNADO* DSP software via host PIOX interface into on-board TMS320C64xx DSP environments.

For more details and TMS320C64xx DSP bootmodes refer to original TI documentation for TMS320C6xxx DSP, which is included in either paper or electronic form along with this manual.

Setting EMIF-A/B control registers for TMS320C64xx DSP

In order to provide correct operation of *TORNADO-PX64xxQ* on-board SSRAM, SDRAM and IOX control registers, which are all external to on-board TMS320C64xx DSP, DSP application software shall correctly set TMS320C64xx DSP on-chip EMIF-A/B control registers in accordance with table 2-3 for each of on-board TMS320C64xx DSP prior accessing external memories and IOX control registers.

CAUTION

TMS320C64xx DSP on-chip EMIF-A/B control registers shall be configured upon the on-board SDRAM capacity and DSP clock frequency.

TMS320C64xx DSP on-chip EMIF-A/B control registers can be configured by on-board TMS320C64xx DSP application software using supplied *TORNADO-PX64xxQ* DSP control utilities (refer to [Appendix 'D'](#) of this manual for more details).

Table 2-3. Recommended settings for EMIF-A/B control registers of TMS320C64xx DSP for TORNADO-PX64xxQ DSP coprocessor.

TMS320C64xx DSP on-chip EMIF control register	EMIF area mode	value
<i>TMS320C64xx EMIF-A Control Registers</i>		
<i>EMIF-A Global Control Register (EMIFA_GBLCTL)</i>	-	0x0001207c
<i>EMIF-A CE-0 Space Control Register (EMIFA_CE0CTL)</i> <i>(area controls 32-bit SSRAM)</i>	32-bit SBSRAM	0x00000040
<i>EMIF-A CE-0 Space Secondary Control Register (EMIFA_CE0SEC)</i>		0x00000002
<i>EMIF-A CE-1 Space Control Register (EMIFA_CE1CTL)</i> <i>(area is reserved)</i>	8-bit ASYNC (reserved)	0xffffffff03 (DSP reset default)
<i>EMIF-A CE-1 Space Secondary Control Register (EMIFA_CE1SEC)</i>		x
<i>EMIF-A CE-2 Space Control Register (EMIFA_CE2CTL)</i> <i>(area controls 32-bit SDRAM)</i>	32-bit SDRAM	0x00000030
<i>EMIF-A CE-2 Space Secondary Control Register (EMIFA_CE2SEC)</i>		x
<i>EMIF-A CE-3 Space Control Register (EMIFA_CE3CTL)</i> <i>(area is reserved)</i>	8-bit ASYNC (reserved)	0xffffffff03 (DSP reset default)

<i>EMIF-A CE-3 Space Secondary Control Register (EMIFA_CE3SEC)</i>		x
<i>EMIF-A SDRAM Control Register (EMIFA_SDCTL)</i>	-	0x57115000 (SDRAM 4Mx32, DSP clock 600 MHz) 0x63115000 (SDRAM 16Mx32, DSP clock 600 MHz) 0x57117000 (SDRAM 4Mx32, DSP clock 720 MHz) 0x63117000 (SDRAM 16Mx32, DSP clock 720 MHz)
<i>EMIFA SDRAM Extension Register (EMIFA_SDEXT)</i>	-	0x00014d29 (DSP clock 600 MHz) 0x00014d3b (DSP clock 720 MHz)
<i>EMIFA SDRAM Timing Register (EMIFA_SDTIM)</i>	-	1562 (SDRAM 4Mx32, DSP clock 600 MHz) 781 (SDRAM 16Mx32, DSP clock 600 MHz) 1875 (SDRAM 4Mx32, DSP clock 720 MHz) 937 (SDRAM 16Mx32, DSP clock 720 MHz)
TMS320C64xx EMIF-B Control Registers		
<i>EMIF-B Global Control Register (EMIFB_GBLCTL)</i>	-	0x0001207c
<i>EMIF-B CE-0 Space Control Register (EMIFB_CE0CTL)</i> (area controls IOX control registers)	16-bit ASYNC	0x10914211 r/w strobe: 2 clk r/w setup: 1 clk r/w hold: 1 clk
<i>EMIF-B CE-0 Space Secondary Control Register (EMIFB_CE0SEC)</i>		x
<i>EMIF-B CE-1 Space Control Register (EMIFB_CE1CTL)</i> (area is reserved)	8-bit ASYNC (reserved)	0xfffff03
<i>EMIF-B CE-1 Space Secondary Control Register (EMIFB_CE1SEC)</i>		x

EMIF-B CE-2 Space Control Register (EMIFB_CE2CTL) (area is reserved)	8-bit ASYNC (reserved)	0xffffffff03
EMIF-B CE-2 Space Secondary Control Register (EMIFB_CE2SEC)		x
EMIF-B CE-3 Space Control Register (EMIFB_CE3CTL) (area is reserved)	8-bit ASYNC (reserved)	0xffffffff03
EMIF-B CE-3 Space Secondary Control Register (EMIFB_CE3SEC)		x
EMIF-B SDRAM Control Register (EMIFB_SDCTL)	-	x
EMIFB SDRAM Extension Register (EMIFB_SDEXT)	-	x
EMIFB SDRAM Timing Register (EMIFB_SDTIM)	-	x

- Notes:
1. EMIF-A/B control registers settings are provided for *TORNADO-PX64xxQ* DSP coprocessor configurations with 4M/16Mx32 SDRAM and DSP clock frequency 600 MHz and 720 MHz.
 2. 'X' denote don't care value.

CAUTION

EMIF-A/B clock for *TORNADO-PX64xxQ* on-board TMS320C64xx DSP is set to 1/6-th of DSP clock and is equal to 100 MHz for 600 MHz TMS320C64xx DSP grade and to 120 MHz for 720 MHz TMS320C64xx DSP grade.

For more details about TMS320C64xx DSP EMIF-A/B control registers refer to original documentation for TI TMS320C6xxx DSP, which is included in either paper or electronic form along with this manual.

On-board synchronous dynamic RAM (SDRAM) memory

TORNADO-PX64xxQ DSP coprocessor DCM provides either 4Mx32 or 16Mx32 on-board local SDRAM for each TMS320C64xx DSP for local large real-time data arrays.

Local SDRAM for each DSP is connected to EMIF-A external memory interface of each TMS320C64xx DSP and runs at 100 MHz (*TORNADO-PX64xxQ/600*) or 120 MHz (*TORNADO-PX64xxQ/720*) EMIF-A bus clock.

CAUTION

SDRAM memory contents can be corrupted in case the corresponding TMS320C64xx DSP is held in the RESET state.

TORNADO-PX64xxQ on-board DSP software and host *TORNADO* DSP software can read the SDRAM length ID via [DSP_XMEM_LEN_ID_RG](#) IOX control register and [HOST_DSP_XMEM_LEN_ID_RG](#) host interface control register correspondingly in order to perform run-time configuration of the corresponding environments.

On-board shared static RAM (SSRAM) memory for high-speed DSP-to-DSP communication

TORNADO-PX64xxQ DSP coprocessor DCM provides either 32Kx32 or 64Kx32 on-board shared static RAM (SSRAM), which is shared by all on-board TMS320C64xx DSP.

CAUTION

SSRAM memory can be used for high-speed data exchange between on-board DSP using shared variables and small real-time data arrays.

SSRAM appears as a high-speed synchronous quad-port static RAM (QPRAM). SSRAM is connected to EMIF-A external memory interface of each TMS320C64xx DSP and runs at 100 MHz (*TORNADO-PX64xxQ/600*) or 120 MHz (*TORNADO-PX64xxQ/720*) EMIF-A bus clock.

CAUTION

SSRAM memory contents is not modified in case the corresponding TMS320C64xx DSP is held in the RESET state.

There is no access arbitration to SSRAM from all on-board TMS320C64xx DSP, i.e. any number of on-board DSP can simultaneously read/write to SSRAM memory locations.

CAUTION

There is no SSRAM consistency conflict if several *TORNADO-PX64xxQ* on-board TMS320C64xx DSP are accessing different SSRAM memory locations (either simultaneously or at different time instants).

There is no SSRAM consistency conflict if several *TORNADO-PX64xxQ* on-board TMS320C64xx DSP are reading from the same SSRAM memory location (either simultaneously or at different time instants).

CAUTION

There might be the SSRAM consistency conflict if several *TORNADO-PX64xxQ* on-board TMS320C64xx DSP are simultaneously writing to the same SSRAM memory location.

SSRAM allocated software semaphores shall be used to protect critical shared SSRAM data from corruption and to exclude simultaneous access to specific SSRAM memory locations from several on-board DSP.

SSRAM also allows generation of *ORed interrupt requests via shared SSRAM* along with message pass to each DSP via dedicated SSRAM memory locations.

TORNADO-PX64xxQ on-board DSP software and host *TORNADO* DSP software can read the SSRAM length ID via [DSP_XMEM_LEN_ID_RG](#) IOX control register and [HOST_DSP_XMEM_LEN_ID_RG](#) host interface control register correspondingly in order to perform run-time configuration of the corresponding environments.

DSP IOX control registers area

Each TMS320C64xx DSP environment of *TORNADO-PX64xxQ* DSP coprocessor DCM includes its own I/O expansion (IOX) registers area, which comprises of a set of control registers and is used to control on-board DSP-to-DSP communication and external DSP environment for the corresponding TMS320C64xx DSP.

DSP IOX control registers area for each on-board TMS320C64xx DSP is mapped into 16-bit asynchronous EMIF-B CE-0 area of the corresponding DSP (refer to table 2-1). Data formats for DSP IOX control registers are presented below in this section.

DSP IOX control registers area includes the following registers:

- read-only [DSP_SYS_STAT_RG](#) IOX control register (system status)
- read-only [DSP_NODE_ID_RG](#) IOX control register (node ID)
- read-only [DSP_DEV_ID_RG](#) IOX control register (device ID)
- read-only [DSP_REV_ID_RG](#) IOX control register (revision ID)
- read-only [DSP_XMEM_LEN_ID_RG](#) IOX control register (external DSP memory length ID)
- [DSP_NMI_SEL_RG](#) IOX control register (DSP NMI non-maskable interrupt source selector)

- [DSP_EXT_INT4_SEL_RG..DSP_EXT_INT7_SEL_RG](#) IOX control registers (DSP EXT_INT4..7 external interrupt source selector)
- write-only [DSP_HORIZ_RQ_RG](#), [DSP_VERT_RQ_RG](#) and [DSP_DIAG_RQ_RG](#) IOX control registers (generates interrupt request to ‘horizontal’, ‘vertical’ and ‘diagonal’ DSP neighbour nodes correspondingly)
- write-only [DSP_BROADCAST_RQ_RG](#) IOX control register (generates interrupt request to all ‘horizontal’, ‘vertical’ and ‘diagonal’ DSP neighbour nodes simultaneously).

CAUTION

DSP IOX control registers for *TORNADO-PX64xxQ* DSP coprocessor DCM are mapped to 16-bit asynchronous EMIF-B CE-0 external TMS320C64xx DSP memory space and shall be accessed either as 8-bit, or 16-bit datawords with datawords address increment ‘+2’.

CAUTION

DSP IOX control registers occupy D0..D3 bits of 16-bit DSP datawords with D4..D15 bits being ignored during write operations and return undefined data during read operations.

DSP_SYS_STAT_RG IOX control register

Read-only *DSP_SYS_STAT_RG* IOX control register must be used by DSP software in order to get DSP bootmode configuration, current HPI port data format, and enable status for ‘vertical’ and ‘diagonal’ DSP-to-DSP serial links for the corresponding TMS320C64xx DSP of *TORNADO-PX64xxQ* DSP coprocessor DCM.

DSP_SYS_STAT_RG IOX control register(r)

x	DIAG_LINK_EN (r)	VERT_LINK_EN (r)	HPI_FMT (r)	DSP_BMODE (r)
bit-15...bit-8	bit-3	bit-2	bit-1	bit-0

Table 2-4 provides details about *DSP_SYS_STAT_RG* IOX control register bits.

Table 2-4. Register bits of *DSP_SYS_STAT_RG* IOX control register.

register bits	access mode	value on DSP reset	Description
<i>DSP_BMODE</i>	r	-	<p>Returns DSP bootmode with which this DSP has started code execution. DSP bootmode is set by host <i>TORNADO</i> DSP software via <i>DSP_BMODE_CNTR</i> bit of <i>HOST_CNTR2_RG</i> host interface control register of host PIOX interface. Refer to table 2-2 and to subsection “TMS320C64xx DSP bootmode configuration” earlier in this section for more details how to set DSP bootmode for <i>TORNADO-PX64xxQ</i> DSP coprocessor.</p> <p><i>DSP_BMODE</i> =0 denotes that DSP has started in ‘NO BOOT’ bootmode.</p> <p><i>DSP_BMODE</i> =1 denotes that DSP has been booted in ‘HPI BOOT’ bootmode.</p>
<i>HPI_FMT</i>	r	-	<p>Returns DSP on-chip HPI port data format with which this DSP has started code execution. HPI port data format is set by host <i>TORNADO</i> DSP software via <i>DSP_HPI_FMT_CNTR</i> bit of <i>HOST_CNTR2_RG</i> host control register of host PIOX interface. Refer to section “Host PIOX Interface” for more details how to set DSP on-chip HPI port data format for <i>TORNADO-PX64xxQ</i> DSP coprocessor.</p> <p><i>HPI_FMT</i> =0 denotes that DSP on-chip HPI port has been configured in 16-bit HPI16 data format mode.</p> <p><i>HPI_FMT</i> =1 denotes that DSP on-chip HPI port has been configured in 32-bit HPI32 data format mode (available for <i>TORNADO</i> PC plug-in DSP systems with 32-bit PIOX-32 interface only).</p>
<i>VERT_LINK_EN</i>	r	-	<p>Returns enable status for ‘vertical’ serial link via DSP on-chip McBSP-1 serial port to the ‘vertical’ DSP neighbour node for this particular DSP and the corresponding ‘vertical’ DSP neighbour node. Enable control for DSP-A to DSP-C and DSP-B to DSP-D ‘vertical’ serial links are set by host <i>TORNADO</i> DSP software independently via <i>DSP-AC_VERT_LINK_EN</i> and <i>DSP-BD_VERT_LINK_EN</i> bits correspondingly of <i>HOST_DSP_LINK_CNF_RG</i> host interface control register of host PIOX interface. Refer to subsection “DSP-to-DSP communication via ‘horizontal’, ‘vertical’ and ‘diagonal’ serial links” later in this section and to section “Host PIOX Interface” later in this chapter for more details about on-board DSP-to-DSP serial links and how to set enable control for on-board DSP-to-DSP ‘vertical’ serial links for <i>TORNADO-PX64xxQ</i> DSP coprocessor.</p> <p><i>VERT_LINK_EN</i> =0 denotes that ‘vertical’ serial link for this on-board DSP node and its ‘vertical’ DSP neighbour node is disabled and DSP on-chip McBSP-1 serial ports for these DSP nodes are routed out to SIO-1 serial port of the corresponding on-board MXSIOX interface connectors.</p> <p><i>VERT_LINK_EN</i> =1 denotes that ‘vertical’ serial link via DSP on-chip McBSP-1 serial ports for this on-board DSP node and its ‘vertical’ DSP neighbour node is enabled and SIO-1 serial ports of the corresponding on-board MXSIOX interface connectors are disabled.</p>

<i>DIAG_LINK_EN</i>	r	-	<p>Returns enable status for 'diagonal' serial link via DSP on-chip McBSP-0 serial port to the 'diagonal' DSP neighbour node for this particular DSP and corresponding 'diagonal' DSP neighbour node. Enable control for DSP-A to DSP-D and DSP-B to DSP-C 'diagonal' serial links are set by host <i>TORNADO</i> DSP software independently via <i>DSP_AD_DIAG_LINK_EN</i> and <i>DSP_BC_DIAG_LINK_EN</i> bits correspondingly of HOST_DSP_LINK_CNF_RG host interface control register of host PIOX interface. Refer to subsection "DSP-to-DSP communication via 'horizontal', 'vertical' and 'diagonal' serial links" later in this section and to section "Host PIOX Interface" later in this chapter for more details about on-board DSP-to-DSP serial links and how to set enable control for on-board DSP-to-DSP 'diagonal' serial links for <i>TORNADO-PX64xxQ</i> DSP coprocessor.</p> <p><i>DIAG_LINK_EN</i> =0 denotes that 'diagonal' serial link for this on-board DSP node and its 'diagonal' DSP neighbour node is disabled and DSP on-chip McBSP-0 serial ports for these DSP nodes are routed out to SIO-0 serial port of the corresponding on-board MXSIOX interface connectors.</p> <p><i>DIAG_LINK_EN</i> =1 denotes that 'diagonal' serial link via DSP on-chip McBSP-0 serial ports for this on-board DSP node and its 'diagonal' DSP neighbour node is enabled and SIO-0 serial ports of the corresponding on-board MXSIOX interface connectors are disabled.</p>
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- Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
 2. Highlighted configurations correspond to default settings on DSP reset condition.

DSP_NODE_ID_RG IOX control register

Read-only *DSP_NODE_ID_RG* IOX control register must be used by DSP software in order to identify particular DSP node where the software is running. Each *TORNADO-PX64xxQ* on-board DSP has its unique node ID, which corresponds to on-board DSP numbering.

DSP node self-identification via DSP software is an ultimate requirement for multiprocessor systems. Typically, all DSP in multiprocessor DSP systems (as it is in *TORNADO-PX64xxQ* DSP coprocessor DCM) are executing the same software code with multiple conditional branching upon the DSP node ID and need to know whether particular DSP is either 'master' or 'slave' for DSP-to-DSP communication, which one of 'horizontal', 'vertical' or 'diagonal' serial links or interrupt requests to use in order to communicate with particular DSP, what is the SSRAM address in order to pass message and set ORed interrupt request via SSRAM to particular on-board DSP, whether 'vertical' and/or 'diagonal' serial links are used for real-time analog/digital I/O via external SIOX rev.B DCM or for board-to-board communication, etc.

DSP_NODE_ID_RG IOX control register(r)

X	0	0	<i>DSP_NODE_ID-1</i> (r)	<i>DSP_NODE_ID-0</i> (r)
bit-15...bit-8	bit-3	bit-2	bit-1	bit-0

Table 2-5 provides details about *DSP_NODE_ID_RG* IOX control register bits.

Table 2-5. Register bits of *DSP_NODE_ID_RG* IOX control register.

register bits	access mode	value on DSP reset	Description
{ <i>DSP_NODE_ID</i> -1..0}	r	-	Returns unique DSP node ID for each on-board DSP of <i>TORNADO-PX64xxQ</i> DSP coprocessor. { <i>DSP_NODE_ID</i> -1..0} = [0,0] corresponds to on-board DSP-A. { <i>DSP_NODE_ID</i> -1..0} = [0,1] corresponds to on-board DSP-B. { <i>DSP_NODE_ID</i> -1..0} = [1,0] corresponds to on-board DSP-C. { <i>DSP_NODE_ID</i> -1..0} = [1,1] corresponds to on-board DSP-D.

Note:

- 1. Access modes: r/w – read/write; r – read-only; w – write only.
- 2. Highlighted configurations correspond to default settings on DSP reset condition.

***DSP_DEV_ID_RG* IOX control register**

Read-only *DSP_DEV_ID_RG* IOX control register must be used by DSP software in order to identify particular *TORNADO-PX64xxQ* board type, i.e. either of *TORNADO-PX6414Q*, or *TORNADO-PX6415Q*, or *TORNADO-PX6416Q* , which is actually defined by the TMS320C64xx DSP type installed.

DSP_DEV_ID_RG IOX control register(r)

X	0	0	<i>DEV_ID</i> -1 (r)	<i>DEV_ID</i> -0 (r)
Bit-15...bit-8	bit-3	bit-2	bit-1	bit-0

Table 2-6 provides details about *DSP_DEV_ID_RG* IOX control register bits.

Table 2-6. Register bits of *DSP_DEV_ID_RG* IOX control register.

register bits	access mode	value on DSP reset	Description
{ <i>DEV_ID-1..0</i> }	r	-	<p>Returns unique device ID for each available type of <i>TORNADO-PX64xxQ</i> DSP coprocessor boards.</p> <p>{<i>DEV_ID-1..0</i>} = [0,0] corresponds to <i>TORNADO-PX6414Q</i> DSP coprocessor board with TMS320C6414 DSP.</p> <p>{<i>DEV_ID-1..0</i>} = [0,1] corresponds to <i>TORNADO-PX6415Q</i> DSP coprocessor board with TMS320C6415 DSP.</p> <p>{<i>DEV_ID-1..0</i>} = [1,0] corresponds to <i>TORNADO-PX6416Q</i> DSP coprocessor board with TMS320C6416 DSP.</p> <p>{<i>DEV_ID-1..0</i>} = [1,1] is reserved for future expansion <i>TORNADO-PX6414Q</i> DSP coprocessor product line and never reads via <i>DSP_DEV_ID_RG</i> IOX control register.</p>

Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

Read-only data returned by *DSP_DEV_ID_RG* IOX control register of the DSP environment is also available via bits D0..D3 of [HOST_DEV_ID_RG](#) host interface control register (refer to [table 2-20](#) and section “[Host PIOX Interface](#)” for more details).

***DSP_REV_ID_RG* IOX control register**

Read-only *DSP_REV_ID_RG* IOX control register must be used by DSP software in order to identify particular firmware revision of *TORNADO-PX64xxQ* board and DSP clock frequency (speed) for on-board TMS320C64xx DSP.

Board revision ID is important for future expansion of on-board firmware in order to correctly configure on-board resources upon the board revision, whereas DSP clock frequency information must be used in order to properly configure TMS320C64xx DSP EMIF control registers (refer to [table 2-3](#) for more details) for accessing DSP external memories and peripherals.

***DSP_REV_ID_RG* IOX control register(r)**

X	<i>DSP_SPEED_ID-1</i> (r)	<i>DSP_SPEED_ID-0</i> (r)	<i>REV_ID-1</i> (r)	<i>REV_ID-0</i> (r)
bit-15...bit-8	bit-3	bit-2	bit-1	bit-0

Table 2-7 provides details about *DSP_REV_ID_RG* IOX control register bits.

Table 2-7. Register bits of *DSP_REV_ID_RG* IOX control register.

register bits	access mode	value on DSP reset	Description
{ <i>REV_ID-1..0</i> }	r	-	<p>Returns unique revision ID for each available firmware revision of <i>TORNADO-PX64xxQ</i> DSP coprocessor boards.</p> <p>{<i>REV_ID-1..0</i>} = [0,0] is reserved.</p> <p>{<i>REV_ID-1..0</i>} = [0,1] corresponds to firmware revision 1 of <i>TORNADO-PX64xxQ</i> DSP coprocessor board. So far, this is the only available firmware revision for <i>TORNADO-PX64xxQ</i> DSP coprocessor boards.</p> <p>{<i>REV_ID-1..0</i>} = [1,0] is reserved.</p> <p>{<i>REV_ID-1..0</i>} = [1,1] is reserved.</p>
{ <i>DSP_SPEED_ID-1..0</i> }	r	-	<p>Returns unique ID for DSP clock frequency (speed) grade of <i>TORNADO-PX64xxQ</i> on-board TMS320C64xx DSP.</p> <p>{<i>DSP_SPEED_ID-1..0</i>} = [0,0] corresponds to 600 MHz frequency grade for on-board TMS320C64xx DSP.</p> <p>{<i>DSP_SPEED_ID-1..0</i>} = [0,1] corresponds to 720 MHz frequency grade for on-board TMS320C64xx DSP.</p> <p>{<i>DSP_SPEED_ID-1..0</i>} = [1,0] is reserved.</p> <p>{<i>DSP_SPEED_ID-1..0</i>} = [1,1] is reserved.</p>

- Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
 2. Highlighted configurations correspond to default settings on DSP reset condition.

Read-only data returned by *DSP_REV_ID_RG* IOX control register of the DSP environment is also available via bits D4..D7 of [HOST_DEV_ID_RG](#) host interface control register (refer to [table 2-20](#) and section [“Host PIOX Interface”](#) for more details).

***DSP_XMEM_LEN_ID_RG* IOX control register**

Read-only *DSP_XMEM_LEN_ID_RG* IOX control register must be used by DSP software in order to identify capacity of on-board DSP external SSRAM and SDRAM memories of *TORNADO-PX64xxQ* DSP coprocessor.

TORNADO-PX64xxQ on-board DSP software must know SSRAM memory capacity in order to adjust length of data arrays allocated in SSRAM and in order to correctly address four specific SSRAM memory locations, which are used to generate ORed interrupt request to particular DSP (*SSRAM_DSPA_RQ*, *SSRAM_DSPB_RQ*, *SSRAM_DSPC_RQ* and *SSRAM_DSPD_RQ* SSRAM memory locations in [table 2-1](#)).

TORNADO-PX64xxQ on-board DSP software must also know SDRAM memory capacity in order to adjust length of data arrays allocated in SDRAM and in order to correctly configure TMS320C64xx DSP EMIF-A SDRAM control registers (refer to [table 2-3](#) for more details).

DSP_XMEM_LEN_ID_RG IOX control register(r)

X	SDRAM_LEN_ID-1 (r)	SDRAM_LEN_ID-0 (r)	SSRAM_LEN_ID-1 (r)	SSRAM_LEN_ID-0 (r)
bit-15...bit-8	bit-3	bit-2	bit-1	bit-0

Table 2-8 provides details about *DSP_XMEM_LEN_ID_RG* IOX control register bits.

Table 2-8. Register bits of *DSP_XMEM_LEN_ID_RG* IOX control register.

register bits	access mode	value on DSP reset	Description
{SSRAM_LEN_ID-1..0}	r	-	<p>Returns unique ID for SSRAM memory capacity installed onto <i>TORNADO-PX64xxQ</i> DSP coprocessor board.</p> <p>{SSRAM_LEN_ID-1..0} = [0,0] denotes that SSRAM memory is not installed.</p> <p>{SSRAM_LEN_ID-1..0} = [0,1] denotes that on-board SSRAM memory capacity is 32Kx32 (128 kbytes).</p> <p>{SSRAM_LEN_ID-1..0} = [1,0] denotes that on-board SSRAM memory is 64Kx32 (256 kbytes).</p> <p>{SSRAM_LEN_ID-1..0} = [1,1] is reserved.</p>
{SDRAM_LEN_ID-1..0}	r	-	<p>Returns unique ID for SDRAM memory capacity installed onto <i>TORNADO-PX64xxQ</i> DSP coprocessor board.</p> <p>{SDRAM_LEN_ID-1..0} = [0,0] denotes that SDRAM memory is not installed.</p> <p>{SDRAM_LEN_ID-1..0} = [0,1] denotes that on-board SDRAM memory capacity is 4Mx32 (16 Mbytes).</p> <p>{SDRAM_LEN_ID-1..0} = [1,0] denotes that on-board SSRAM memory is 16Mx32 (64 Mbytes).</p> <p>{SDRAM_LEN_ID-1..0} = [1,1] is reserved.</p>

- Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
 2. Highlighted configurations correspond to default settings on DSP reset condition.

Read-only data returned by *DSP_XMEM_LEN_ID_RG* IOX control register of the DSP environment is also available via bits D0..D3 of [HOST DSP XMEM LEN ID RG](#) host interface control register (refer to [table 2-21](#) and section [“Host PIOX Interface”](#) for more details).

DSP_EXT_INT4_SEL_RG IOX control register (r/w)
DSP_EXT_INT5_SEL_RG IOX control register (r/w)
DSP_EXT_INT6_SEL_RG IOX control register (r/w)
DSP_EXT_INT7_SEL_RG IOX control register (r/w)
DSP_NMI_SEL_RG IOX control register (r/w)

X	0	INT_SEL-2 (r)	INT_SEL-1 (r)	INT_SEL-0 (r)
bit-15...bit-8	bit-3	bit-2	bit-1	bit-0

Each DSP external interrupt selector register of *TORNADO-PX64xxQ* DSP coprocessor DCM allows selection from seven different interrupt sources via *DSP_EXT_INT4_SEL_RG*.. *DSP_EXT_INT7_SEL_RG* and *DSP_NMI_SEL_RG* IOX control registers in accordance with table 2-9. All DSP external interrupt selector registers default to the 0H state on DSP reset condition, which corresponds to disabled interrupt request.

Table 2-9. Interrupt sources for DSP external interrupt selectors.

{INT_SEL-2..INT_SEL-0} bits of <i>DSP_EXT_INT4_SEL_RG</i> <i>DSP_EXT_INT5_SEL_RG</i> <i>DSP_EXT_INT6_SEL_RG</i> <i>DSP_EXT_INT7_SEL_RG</i> <i>DSP_NMI_SEL_RG</i> <i>DSP External Interrupt Source Selector IOX control registers</i>			DSP Interrupt source
INT_SEL-2 bit	INT_SEL-1 bit	INT_SEL-0 bit	
0	0	0	Interrupt is disabled. This is default value on DSP reset condition.
0	0	1	ORed interrupt request via SSRAM, which occurs when any of DSP neighbour nodes for this particular DSP node will write to the corresponding SSRAM memory location (<i>SSRAM_DSPA_RQ</i> .. <i>SSRAM_DSPD_RQ</i>) in accordance with table 2-1 . Interrupt request will be cleared after this particular DSP node will read the corresponding SSRAM memory location.
0	1	0	External <i>SX_IRQ-0</i> interrupt request from the corresponding MXSIOX interface connector.
0	1	1	External <i>SX_IRQ-1</i> interrupt request from the corresponding MXSIOX interface connector.
1	0	0	'Horizontal' interrupt request from the 'horizontal' DSP neighbour node, i.e. when 'horizontal' DSP neighbour node writes to <i>DSP_HORIZ_RQ_RG</i> IOX control register.
1	0	1	'Vertical' interrupt request from the 'vertical' DSP neighbour node, i.e. when 'vertical' DSP neighbour node writes to <i>DSP_VERT_RQ_RG</i> IOX control register.

1	1	0	'Diagonal' interrupt request from the 'diagonal' DSP neighbour node, i.e. when 'diagonal' DSP neighbour node writes to <i>DSP_DIAG_RQ_RG</i> IOX control register.
1	1	1	'Host broadcast' interrupt request from host <i>TORNADO</i> DSP software, i.e. when host DSP software writes to <i>HOST_BROADCAST_RQ_RG</i> host PIOX interface register. This interrupt request from host is broadcasted to all <i>TORNADO-PX64xxQ</i> on-board DSP nodes.

Note: 1. Highlighted configurations correspond to default settings on DSP reset condition.

CAUTION

TMS320C64xx DSP on-chip *EXTERNAL INTERRUPT POLARITY* register (@0x019C0008) for each of on-board TMS320C64xx DSP of *TORNADO-PX64xxQ* DSP coprocessor must be set to the 0x00000000 value, that corresponds to active low-to-high interrupt transitions.

As the default state on DSP reset conditions, TMS320C64xx DSP on-chip TMS320C64xx DSP on-chip high/low interrupt multiplexer registers (@0x019C0000 and @0x019C0004) map DSP external EXT_INT4..7 interrupt requests to DSP on-chip #4..7 interrupt requests/priorities correspondingly. However, if default DSP on-chip interrupt selection priority is not satisfactory, then TMS320C64xx DSP on-chip high/low interrupt multiplexer registers (@0x019C0000 and @0x019C0004) can be also used to select particular DSP on-chip interrupt request input/priority, which will be used to interrupt the DSP core on EXT_INT4..7 interrupt request events.

CAUTION

For more information about how to configure TMS320C64xx DSP on-chip high/low interrupt multiplexer registers refer to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

DSP_HORIZ_RQ_RG, DSP_VERT_RQ_RG, DSP_DIAG_RQ_RG and DSP_BROADCAST_RQ_RG IOX control registers for generation interrupt requests to DSP neighbour nodes

Each of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP node can generate DSP-to-DSP interrupt request either to any of its 'horizontal', 'vertical' and 'diagonal' DSP neighbour nodes individually or to all DSP these neighbour nodes simultaneously.

Individual DSP-to-DSP interrupt requests to 'horizontal', 'vertical' and 'diagonal' DSP neighbour nodes are generated via *DSP_HORIZ_RQ_RG*, *DSP_VERT_RQ_RG*, and *DSP_DIAG_RQ_RG* IOX control registers correspondingly, whereas broadcast interrupt requests to all DSP neighbour nodes correspondingly can be generated via *DSP_BROADCAST_RQ_RG* IOX control register.

CAUTION

Data written to *DSP_HORIZ_RQ_RG*, *DSP_VERT_RQ_RG*, *DSP_DIAG_RQ_RG* and *DSP_BROADCAST_RQ_RG* IOX control registers is ignored.

DSP_HORIZ_RQ_RG IOX control register (w)
DSP_DIAG_RQ_RG IOX control register (w)
DSP_VERT_RQ_RG IOX control register (w)
DSP_BROADCAST_RQ_RG IOX control register (w)

X	x	x	x	x
bit-15...bit-8	bit-3	bit-2	bit-1	bit-0

Summary of DSP-to-DSP communication paths

TORNADO-PX64xxQ DSP coprocessor DCM provides several flexible on-board DSP-to-DSP communication paths, which have been designed to meet different multi-DSP user applications (fig.2-4):

- DSP-to-DSP communication via shared static RAM (SSRAM) for high-speed data exchange via shared variables and data arrays. SSRAM is typically used for DSP-to-DSP synchronization and transfer of small amount of real-time data. Refer to subsection [“On-board static RAM \(SSRAM\) memory for high-speed DSP-to-DSP communication”](#) for more details about TORNADO-PX64xxQ on-board SSRAM.
- DSP-to-DSP communication via ‘horizontal’, ‘vertical’ and ‘diagonal’ serial links (fig.2-4a), which are actually TMS320C64xx DSP on-chip McBSP-0/1/2 serial ports. Serial links are typically used for stream-line data bulk real-time data transfers under the control of TMS320C64xx DSP on-chip EDMA controllers. ‘Vertical’ and ‘diagonal’ serial links for each DSP can be routed out to on-board MXSIOX edge connectors for external analog I/O and/or for board-to-board communication. Refer to subsection [“DSP-to-DSP communication via ‘horizontal’, ‘vertical’ and ‘diagonal’ serial links”](#) later in this section for more details about DSP-to-DSP communication via on-board DSP-to-DSP serial links.
- DSP-to-DSP communication via ‘horizontal’, ‘vertical’ and ‘diagonal’ interrupt requests (fig.2-4b), which are typically used to set DSP-to-DSP ready or attention events without any data message passing. ‘Horizontal’, ‘vertical’ and ‘diagonal’ interrupt requests are used to generate node-to-node interrupt requests with the sender DSP node being exactly identified by the recipient DSP node. Refer to subsection [“DSP-to-DSP communication via ‘horizontal’, ‘vertical’ and ‘diagonal’ interrupt requests”](#) later in this section for more details about DSP-to-DSP communication via on-board DSP-to-DSP interrupt requests.
- DSP-to-DSP communication via ORed interrupt requests via shared SSRAM (fig.2-4c), which are typically used to set attention event to particular DSP along with data message passing. ORed interrupt requests via SSRAM can be generated to any particular on-board DSP as the logical OR of interrupt requests from all DSP neighbours of this DSP. The recipient DSP node will be generally unable to identify the sender DSP node (refer to subsection [“DSP-to-DSP communication via ORed interrupt requests via SSRAM”](#) later in this section for more details).

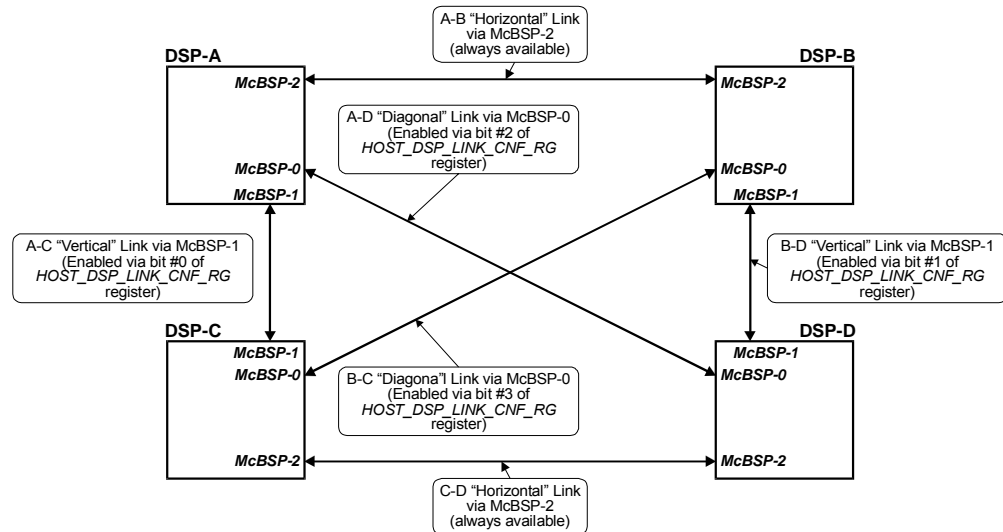


Fig.2-4a. On-board DSP-to-DSP communication topology via serial links for *TORNADO-PX64xxQ* DSP Coprocessor DCM.

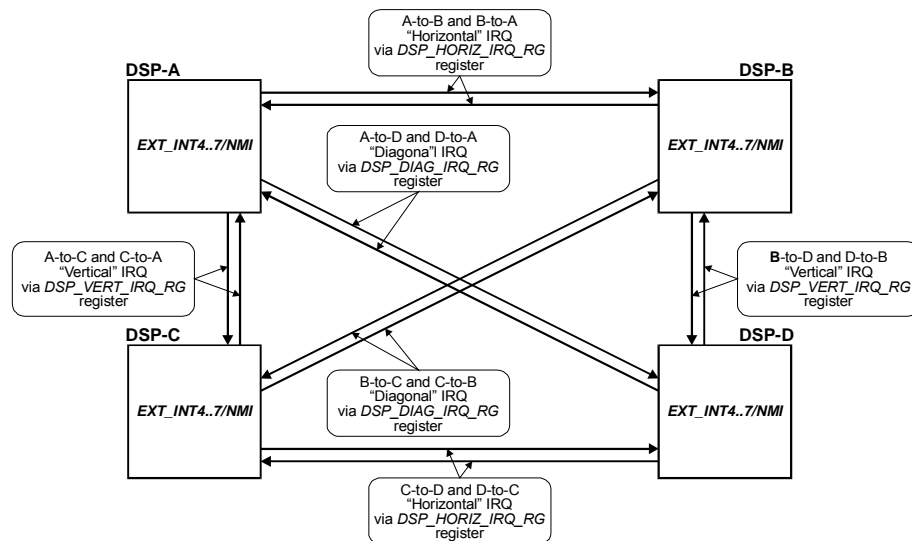


Fig.2-4b. On-board DSP-to-DSP communication topology via DSP-to-DSP interrupt requests for *TORNADO-PX64xxQ* DSP Coprocessor DCM.

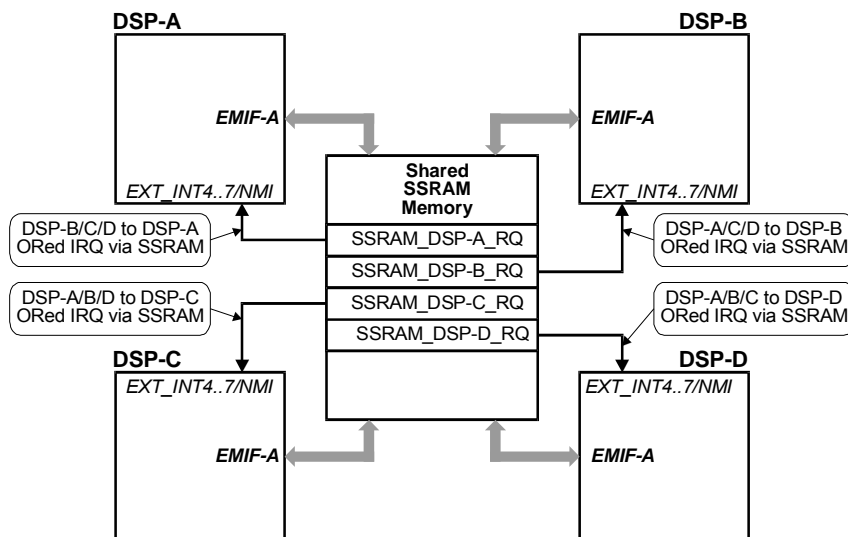


Fig.2-4c. On-board DSP-to-DSP communication topology via SSRAM DSP-to-DSP interrupt requests for *TORNADO-PX64xxQ* DSP Coprocessor DCM.

DSP-to-DSP communication via 'horizontal', 'vertical' and 'diagonal' serial links

TORNADO-PX64xxQ DSP coprocessor DCM supports DSP-to-DSP communication via bidirectional serial links, which appear as TMS320C64xx on-chip McBSP serial ports connected between on-board DSP in accordance with [fig.2-4a](#).

CAUTION

'Horizontal', 'vertical' and 'diagonal' bidirectional serial links shall be used for DSP-to-DSP streamline data transfers using TMS320C64xx DSP on-chip EDMA controllers.

All of 'horizontal', 'vertical' and 'diagonal' bidirectional serial links of *TORNADO-PX64xxQ* DSP coprocessor DCM are implemented by direct connection of McBSP serial port receiver signals of each of two involved DSP nodes to the McBSP serial port transmitter signals of opposite DSP nodes in accordance with [fig.2-5](#).

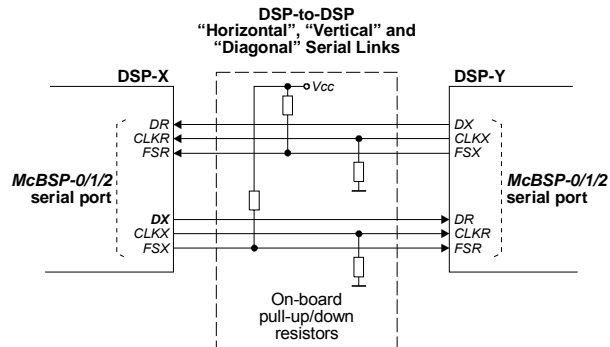


Fig.2-5. Block-diagram for bidirectional serial links connection for on-board DSP-to-DSP communication at *TORNADO-PX64xxQ* DSP Coprocessor DCM.

CAUTION

FSX and FSR signals of involved McBSP serial ports for on-board 'horizontal', 'vertical' and 'diagonal' bidirectional serial links of *TORNADO-PX64xxQ* DSP coprocessor DCM are provided with on-board pull-up resistors and shall be configured as active low via TMS320C64xx DSP software in order to exclude false transmissions during McBSP port software configuration procedure and to increase noise immunity.

CLKX and CLKR signals of involved McBSP serial ports for on-board 'horizontal', 'vertical' and 'diagonal' bidirectional serial links of *TORNADO-PX64xxQ* DSP coprocessor DCM are provided with on-board pulled-down resistors and shall be configured as active high via TMS320C64xx DSP software.

CAUTION

Maximum serial link data transfer speed for on-board DSP-to-DSP communication over 'horizontal', 'vertical' and 'diagonal' serial links must not exceed 75 Mbit/s.

Except for the above maximum serial link data transfer speed requirement and FSX/FSR and CLX/CLKR signal polarity requirement, it is up to the user DSP software application how to configure McBSP serial ports (number of data frames, data frame length and data word length, etc) for usage as on-board DSP-to-DSP serial links in order to best meet customer application. However, it is recommended that the McBSP serial ports of both involved DSP nodes shall be configured as the following for usage as the serial link of *TORNADO-PX64xxQ* DSP coprocessor DCM:

- FSR is configured as active low input
- CLKR is configured as active high input

- DR is configured as active high input
- FSX is configured as active low output, which is either generated on the DXR-to-XSR register load condition (recommended) or is generated by frame sync generator upon the customer application
- CLKX is configured as active high output generated by sample rate generator, which is recommended to be configured to 75 MHz output sample data rate for 600 MHz TMS320C64xx DSP clock frequency grade and to 60 MHz output sample data rate for 720 MHz TMS320C64xx DSP clock frequency grade
- DX is configured as active high output
- one data frame with one 32-bit data word is used.

CAUTION

It is recommended, that TMS320C64xx DSP software utility functions (refer to [Appendix 'D'](#) of this manual for more details) are used to configure DSP on-chip McBSP serial ports for DSP-to-DSP communication over 'horizontal', 'vertical' and 'diagonal' serial links.

'Horizontal' bidirectional serial links are always enabled between on-board 'horizontal' DSP neighbour nodes (DSP-A and DSP-B, and DSP-C and DSP-D correspondingly) and are provided via DSP on-chip McBSP-2 serial ports of involved DSP nodes.

'Vertical' serial links are optional links between on-board 'vertical' DSP neighbour nodes (DSP-A and DSP-C, and DSP-B and DSP-D correspondingly) and are provided via DSP on-chip McBSP-1 serial ports of involved DSP nodes. Each of two on-board 'vertical' serial links is individually enabled via host DSP software of host *TORNADO* DSP system/controller via *DSP-AC_LINK_EN* and *DSP-AC_LINK_EN* bits of *HOST_DSP_LINK_CNF_RG* host interface control register of host PIOX interface (refer to [table 2-19](#) and section ["Host PIOX Interface"](#) later in this chapter for more details). Tables 2-10a and 2-10b provides details about enable control for on-board DSP-to-DSP 'vertical' serial links.

Table 2-10a. Enable control for DSP-A to DSP-C 'vertical' serial link.

<i>DSP-AC_LINK_EN</i> bit of <i>HOST_DSP_LINK_CNF_RG</i> register	Description
<i>0</i>	DSP-A to DSP-C 'vertical' serial link is disabled. McBSP-1 serial ports of DSP-A and DSP-C are routed out to the SIO-1 serial ports of on-board MXSIOX-A (JP3) and MXSIOX-C (JP5) connectors correspondingly for external analog/digital I/O and/or board-to-board communication. Refer to section "Serial I/O Expansion Interface (MXSIOX)" later in this chapter for more details.
<i>1</i>	DSP-A to DSP-C 'vertical' serial link is enabled via McBSP-1 serial ports of DSP-A and DSP-C. SIO-1 serial ports of on-board MXSIOX-A (JP3) and MXSIOX-C (JP5) connectors are disabled.

Note: 1. Highlighted configuration corresponds to default host PIOX reset condition.

Table 2-10b. Enable control for DSP-B to DSP-D ‘vertical’ serial link.

DSP-BD_LINK_EN bit of HOST_DSP_LINK_CNF_RG register	Description
0	DSP-B to DSP-D ‘vertical’ serial link is disabled. McBSP-1 serial ports of DSP-B and DSP-D are routed out to the SIO-1 serial ports of on-board MXSIOX-B (JP4) and MXSIOX-D (JP6) connectors correspondingly for external analog/digital I/O and/or board-to-board communication. Refer to section “Serial I/Q Expansion Interface (MXSIOX)” later in this chapter for more details.
1	DSP-B to DSP-D ‘vertical’ serial link is enabled via McBSP-1 serial ports of DSP-B and DSP-D. SIO-1 serial ports of on-board MXSIOX-B (JP4) and MXSIOX-D (JP6) connectors are disabled.

Note: 1. Highlighted configuration corresponds to default host PIOX reset condition.

In case ‘vertical’ serial link is disabled, then McBSP-1 serial port of involved DSP ‘vertical’ neighbour nodes are routed out to the SIO-1 serial ports of corresponding MXSIOX interface connectors.

‘Diagonal’ serial links are optional links between on-board ‘vertical’ DSP neighbour nodes (DSP-A and DSP-D, and DSP-B and DSP-C correspondingly) and are provided via DSP on-chip McBSP-0 serial ports of involved DSP nodes. Each of two on-board ‘diagonal’ serial links is individually enabled via host DSP software of host *TORNADO* DSP system/controller via *DSP-AD_LINK_EN* and *DSP-BC_LINK_EN* bits of [HOST_DSP_LINK_CNF_RG](#) host interface control register of host PIOX interface (refer to [table 2-19](#) and section [“Host PIOX Interface”](#) later in this chapter for more details). Tables 2-11a and 2-11b provides details about enable control for on-board DSP-to-DSP ‘diagonal’ serial links.

Table 2-11a. Enable control for DSP-A to DSP-D ‘diagonal’ serial link.

DSP-AD_LINK_EN bit of HOST_DSP_LINK_CNF_RG register	Description
0	DSP-A to DSP-D ‘diagonal’ serial link is disabled. McBSP-0 serial ports of DSP-A and DSP-D are routed out to the SIO-0 serial ports of on-board MXSIOX-A (JP3) and MXSIOX-D (JP6) connectors correspondingly for external analog/digital I/O and/or board-to-board communication. Refer to section “Serial I/Q Expansion Interface (MXSIOX)” later in this chapter for more details.
1	DSP-A to DSP-D ‘diagonal’ link is enabled via McBSP-0 serial ports of DSP-A and DSP-D. SIO-0 serial ports of on-board MXSIOX-A (JP3) and MXSIOX-D (JP6) connectors are disabled.

Note: 1. Highlighted configuration corresponds to default host PIOX reset condition.

Table 2-11b. Enable control for DSP-B to DSP-C 'diagonal' serial link.

DSP-BC_LINK_EN bit of HOST_DSP_LINK_CNF_RG register	Description
0	DSP-B to DSP-C 'diagonal' serial link is disabled. McBSP-0 serial ports of DSP-B and DSP-C are routed out to the SIO-0 serial ports of on-board MXSIOX-B (JP4) and MXSIOX-C (JP5) connectors correspondingly for external analog/digital I/O and/or board-to-board communication. Refer to section "Serial I/O Expansion Interface (MXSIOX)" later in this chapter for more details.
1	DSP-B to DSP-C 'diagonal' link is enabled via McBSP-0 serial ports of DSP-B and DSP-C. SIO-0 serial ports of on-board MXSIOX-B (JP4) and MXSIOX-C (JP5) connectors are disabled.

Note: 1. Highlighted configuration corresponds to default host PIOX reset condition.

In case 'diagonal' serial link is disabled, then McBSP-0 serial port of involved DSP 'diagonal' neighbour nodes are routed out to the SIO-0 serial ports of corresponding MXSIOX interface connectors.

DSP-to-DSP communication via 'horizontal', 'vertical' and 'diagonal' interrupt requests

TORNADO-PX64xxQ DSP coprocessor DCM supports DSP-to-DSP communication via DSP-to-DSP interrupt requests as the following ([fig.2-4b](#)):

- 'horizontal' interrupt requests can be generated between on-board 'horizontal' DSP neighbour nodes (as DSP-A to DSP-B, and DSP-C to DSP-D) when writing to **DSP_HORIZ_RQ_RG** IOX control register (written data is ignored) as it is described in the corresponding subsection earlier
- 'vertical' interrupt requests can be generated between on-board 'vertical' DSP neighbour nodes (as DSP-A to DSP-C, and DSP-B to DSP-D) when writing to **DSP_VERT_RQ_RG** IOX control register (written data is ignored) as it is described in the corresponding subsection earlier
- 'diagonal' interrupt requests can be generated between on-board 'diagonal' DSP neighbour nodes (as DSP-A to DSP-D, and DSP-B to DSP-C) when writing to **DSP_DIAG_RQ_RG** IOX control register (written data is ignored) as it is described in the corresponding subsection earlier
- 'DSP broadcast' interrupt requests can be generated by each DSP as simultaneous interrupt request to all its DSP neighbour nodes simultaneously when writing to **DSP_BROADCAST_RQ_RG** IOX control register (written data is ignored) as it is described in the corresponding subsection earlier.

CAUTION

‘Horizontal’, ‘vertical’, ‘diagonal’ and ‘broadcast’ DSP-to-DSP interrupt requests do not transfer data between DSP nodes and shall be used to set an interrupt events only.

‘Horizontal’, ‘vertical’ and ‘diagonal’ interrupt requests are used to generate node-to-node interrupt requests with the sender DSP node being exactly identified by the recipient DSP node.

In order the recipient DSP node could receive either of ‘horizontal’, ‘vertical’, ‘diagonal’ interrupt request from the corresponding DSP neighbour node, then any (or several) of [DSP_EXT_INT4_SEL_RG](#), [DSP_EXT_INT5_SEL_RG](#), [DSP_EXT_INT6_SEL_RG](#), [DSP_EXT_INT7_SEL_RG](#), or [DSP_NMI_SEL_RG](#) IOX control registers shall be configured to the corresponding ‘horizontal’, ‘vertical’, ‘diagonal’ interrupt request source in accordance with [table 2-9](#) earlier in this section.

DSP-to-DSP communication via ORed interrupt requests via SSRAM

TORNADO-PX64xxQ DSP coprocessor DCM also offers DSP-to-DSP communication via DSP-to-DSP communication via *ORed interrupt requests via shared SSRAM* ([fig.2-4c](#)), which are most commonly used to set attention event to particular DSP along with data message passing.

ORed interrupt requests via SSRAM can be generated to any particular on-board DSP as the logical OR of interrupt requests from all DSP neighbours of this DSP.

CAUTION

ORed interrupt requests via SSRAM to particular DSP (DSP-A..DSP-D) are generated in case any of DSP neighbour nodes of this DSP node writes to any byte of the corresponding dedicated SSRAM memory location ([SSRAM_DSPA_RQ...SSRAM_DSPD_RQ](#)) in accordance with [table 2-1](#).

ORed interrupt request via SSRAM is cleared in case the recipient DSP node reads from any byte of the corresponding dedicated SSRAM memory location ([SSRAM_DSPA_RQ...SSRAM_DSPD_RQ](#)) in accordance with [table 2-1](#).

Note, that written SSRAM data can be interpreted as the message to the recipient DSP node. Interrupt request via SSRAM is generated in case DSP neighbour writes to any byte, any 16-bit halfword, or to full 32-bit dataword of the corresponding 32-bit [SSRAM_DSPA_RQ...SSRAM_DSPD_RQ](#) SSRAM memory location.

Generally, the recipient DSP node will be unable to identify the sender DSP node, since interrupt request via SSRAM is generated at the write event to any byte of the corresponding [SSRAM_DSPA_RQ...SSRAM_DSPD_RQ](#) SSRAM memory location by any of the DSP neighbour nodes. This is applicable for most applications when the ORed interrupt request is sufficient.

However, simple software techniques will allow the recipient DSP node to exactly identify the interrupt requestor DSP node at *TORNADO-PX64xxQ* DSP coprocessor DCM. For example, this can be done in case each of the DSP neighbour nodes will write a non-zero message data to the pre-defined byte of the

corresponding `SSRAM_DSPA_RQ...SSRAM_DSPD_RQ` SSRAM memory location instead of writing to 16-bit halfword or full 32-bit word. In this case, although the message passed from each of the DSP neighbour nodes will be limited to 8-bits only, however the recipient DSP node will be able to identify the interrupt requestor by analyzing the contents of each byte of received 32-bit SSRAM dataword at the corresponding `SSRAM_DSPA_RQ...SSRAM_DSPD_RQ` SSRAM memory location.

Board-to-board communication via external serial links via MXSIOX interface connectors

TORNADO-PX64xxQ DSP coprocessor DCM has been designed with multi-board expansion in mind in order to meet demands of multi-DSP network systems comprising of more than four TMS320C64xx DSP. Moreover, other multi-DSP expansion compatible devices can be integrated into one multi-DSP network along with **TORNADO-PX64xxQ** DSP coprocessor DCM in order to meet in order to build application specific multi-DSP systems.

Board-to-board communication for **TORNADO-PX64xxQ** DSP coprocessor DCM is performed via TMS320C64xx DSP on-chip McBSP-0/1 serial ports, which are not configured as on-board 'diagonal' and/or 'vertical' serial links (refer to [tables 2-10](#) and [2-11](#)) and therefore are routed out to the corresponding on-board MXSIOX-A..D interface connectors. Board-to-board connection via serial links is performed via external optional *T/X-XSLC1* serial link converters, which connect directly to **TORNADO-PX64xxQ** on-board MXSIOX connector, and via *T/X-XSL/C* serial link cables, which connect between any serial link ports connectors of two *T/X-XSLC1* serial link converters connected to different **TORNADO-PX64xxQ** DSP coprocessor DCM.

Figure 2-6a below provides example block diagram of board-to-board connection between two different **TORNADO-PX64xxQ** DSP coprocessor DCM via unused 'diagonal' serial links of DSP-B at board #1 and DSP-A at board #2 using two *T/X-XSLC1* serial link converters and one *T/X-XSL/C* serial link cable, whereas figure 2-6b provides the picture for this board-to-board connection.

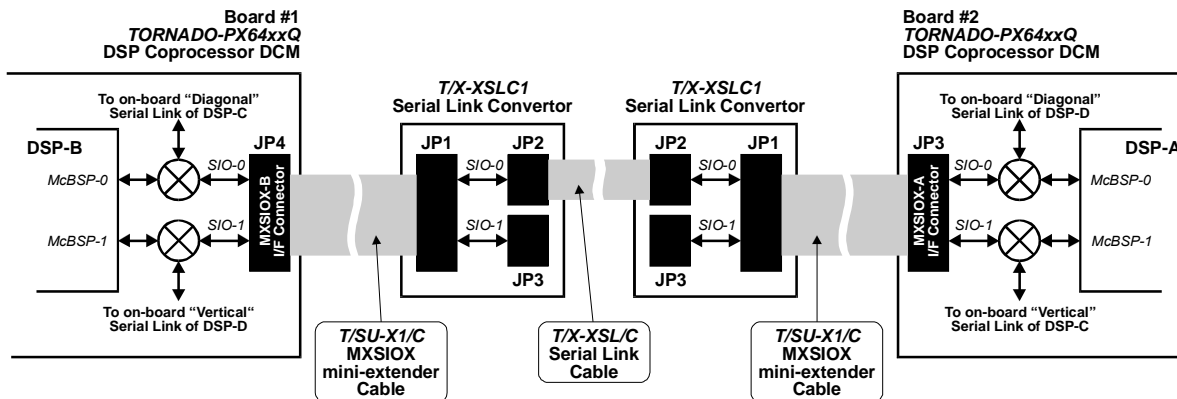


Fig. 2-6a. Block-diagram of board-to-board communication via serial link between DSP-B and DSP-A of two **TORNADO-PX64xxQ** DSP Coprocessor DCM.

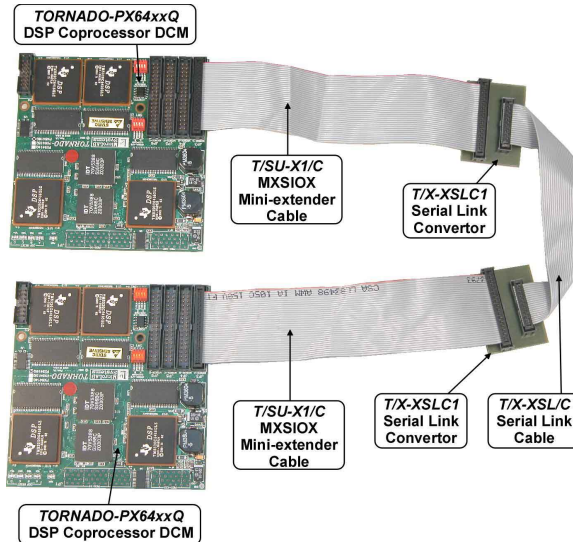


Fig.2-6b. Board-to-board connection between two **TORNADO-PX64xxQ** DSP Coprocessor DCM via optional **T/X-XSLC1** serial link converters and **T/X-XSL/C** external serial links connection cable.

Figure 2-7 below provides example block diagram of board-to-board connection between **TORNADO-PX64xxQ** DSP coprocessor DCM and a different device as **TORNADO-PX/DDC4G** quad digital radio receiver DSP coprocessor DCM, which also provides compatible external serial links for board-to-board communication. Board-to-board communication over serial link between **TORNADO-PX64xxQ** DSP coprocessor DCM and **TORNADO-PX/DDC4G** quad digital radio receiver DSP coprocessor DCM is shown to be performed via unused 'diagonal' serial link of **TORNADO-PX64xxQ** on-board DSP-B and **TORNADO-PX/DDC4G** on-board external serial link XSL-0 using one **T/X-XSLC1** serial link converter connected to MXSIOX-B interface connector at **TORNADO-PX64xxQ** DSP coprocessor DCM and one **T/X-XSL/C** serial link cable, which connects directly between XSL-0 on-board connector at **TORNADO-PX/DDC4G** quad digital radio receiver DSP coprocessor DCM and JP2 external serial link connector at **T/X-XSLC1** serial link converter board.

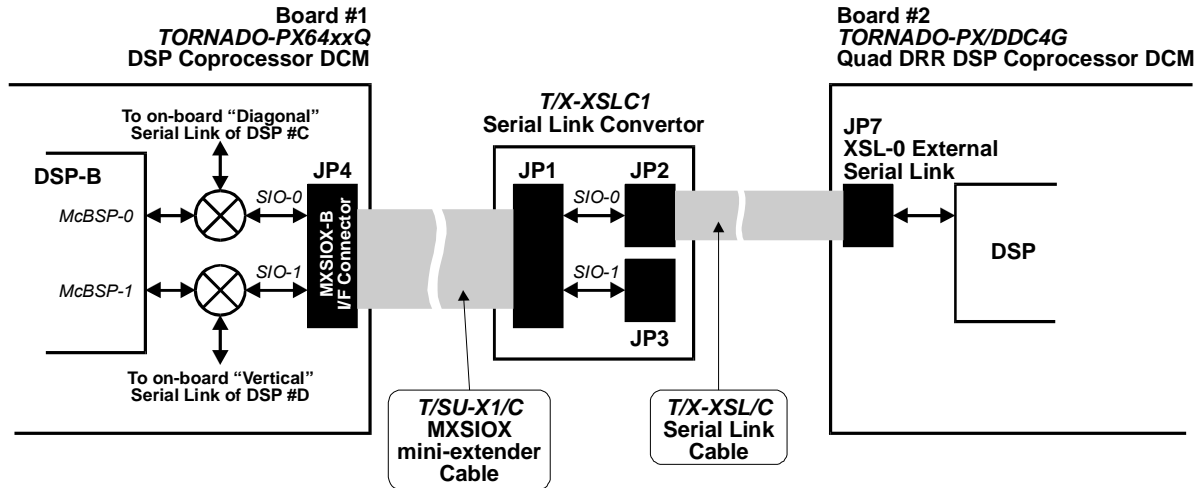


Fig.2-7. Block-diagram of board-to-board communication via serial link between DSP-B of TORNADO-PX64xxQ DSP Coprocessor DCM and external serial link XSL-0 of TORNADO-PX/DDC4G quad digital radio receiver DSP coprocessor DCM.

All board-to-board communication via bidirectional serial links of TORNADO-PX64xxQ DSP coprocessor DCM are implemented by direct connection of corresponding McBSP serial port receiver signals of two involved DSP to the McBSP serial port transmitter signals of opposite DSP nodes in accordance with fig.2-8.

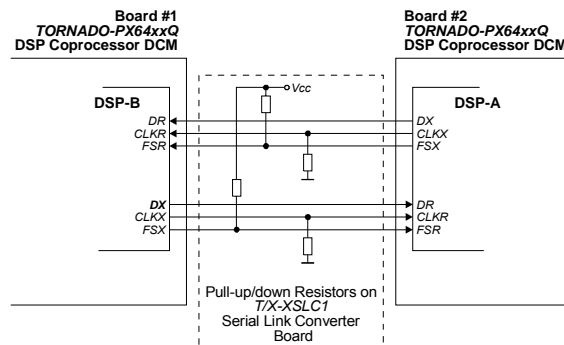


Fig.2-8. Block diagram for bidirectional board-to-board communication via serial link between two TORNADO-PX64xxQ DSP Coprocessor DCM boards.

CAUTION

FSX and FSR signals of involved McBSP serial ports for board-to-board communication via bidirectional serial links of *TORNADO-PX64xxQ* DSP coprocessor DCM are provided with pull-up resistors via *T/X-XSLC1* serial link converter board(s) and shall be configured as active low via TMS320C64xx DSP software in order to exclude false transmissions during McBSP port software configuration procedure and to increase noise immunity.

CLKX and CLKR signals of involved McBSP serial ports for board-to-board communication via bidirectional serial links of *TORNADO-PX64xxQ* DSP coprocessor DCM are provided with pull-down resistors via *T/X-XSLC1* serial link converter board(s) and shall be configured as active high via TMS320C64xx DSP software.

CAUTION

Maximum serial link data transfer speed for board-to-board communication over external serial links for *TORNADO-PX64xxQ* DSP coprocessor DCM must not exceed 50 Mbit/s.

Except for the above maximum serial link data transfer speed requirement and FSX/FSR and CLX/CLKR signal polarity requirement, it is up to the user DSP software application how to configure McBSP serial ports (number of data frames, data frame length and data word length, etc) for usage as board-to-board serial links in order to best meet customer application. However, it is recommended that the McBSP serial ports of both involved DSP nodes shall be configured as the following for usage as the board-to-board serial link of *TORNADO-PX64xxQ* DSP coprocessor DCM:

- FSR is configured as active low input
- CLKR is configured as active high input
- DR is configured as active high input
- FSX is configured as active low output, which is either generated on the DXR-to-XSR register load condition (recommended) or is generated by frame sync generator upon the customer application
- CLKX is configured as active high output generated by sample rate generator, which is recommended to be configured to 50 MHz output sample data rate for 600 MHz TMS320C64xx DSP clock frequency grade and to 45 MHz output sample data rate for 720 MHz TMS320C64xx DSP clock frequency grade
- DX is configured as active high output
- one data frame with one 32-bit data word is used.

CAUTION

It is recommended, that TMS320C64xx DSP software utility functions (refer to [Appendix 'D'](#) of this manual for more details) are used to configure DSP on-chip McBSP serial ports for DSP-to-DSP communication over 'horizontal', 'vertical' and 'diagonal' serial links.

For more details about board-to-board communication via optional external *T/X-XSLC1* serial link converters refer to [Appendix 'C'](#) later in this manual.

TMS320C64xx DSP on-chip HPI port

TMS320C64xx DSP on-chip HPI port of each *TORNADO-PX64xxQ* on-board DSP is accessed by host *TORNADO* DSP software in order to upload DSP execution code, to read/write real-time data and to provide mutual DSP-to-host and host-to-DSP interrupt generation

On-chip HPI port of each *TORNADO-PX64xxQ* on-board TMS320C64xx DSP is mapped to host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM (refer to [table 2-15](#) and to section "[Host PIOX Interface](#)" later in this chapter for more details).

For host *TORNADO* DSP systems with on-board 16-bit PIOX-16 interface site (*TORNADO-E* stand-alone DSP controllers and *TORNADO-54xx* DSP systems), on-chip HPI ports of *TORNADO-PX64xxQ* on-board DSP operate in 16-bit HPI data format mode only, whereas for host *TORNADO* DSP systems with on-board 32-bit PIOX-32 interface site (*TORNADO-3x/P3x/6x/P6x/P64xx* DSP systems for PC computers), TMS320C64xx DSP on-chip HPI ports of *TORNADO-PX64xxQ* on-board DSP can be configured to operate in both 16-bit and 32-bit data format modes with 32-bit HPI data format mode providing 2x times higher performance.

CAUTION

For more information about TMS320C64xx DSP on-chip HPI port refer to section "Host PIOX Interface" later in this chapter and to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

Support for SIOX rev.B DCM

TORNADO-PX64xxQ DSP coprocessor DCM provides on-board facilities for optional connection of up to four external SIOX rev.B DCM (one SIOX rev.B DCM per each TMS320C64xx DSP) for real-time analog/digital signal I/O, that converts *TORNADO-PX64xxQ* DSP coprocessor DCM into universal DSP and application specific I/O coprocessor.

In order to connect external SIOX rev.B DCM to *TORNADO-PX64xxQ* DSP coprocessor DCM, any of optional *T/SU-X1*, *T/SU-X2* or *T/SU-X3* SIOX rev.B mini-extendors shall be used, which can carry one full-size SIOX rev.B DCM and connects to *TORNADO-PX64xxQ* on-board MXSIOX-A..D interface connectors (JP3..JP6 at [fig.2-1](#), [2-2](#) and [A-1](#)). Each of four on-board of MXSIOX interface connectors is routed to a dedicated on-board TMS320C64xx DSP and comprises of signals for two SIO-0 and SIO-1 serial ports serial

ports, two timer/IO lines (*TM/XIO-0* and *TM/XIO-1*), two DSP external interrupt request inputs (*XIRQ-0* and *XIRQ-1*), reset control, and $\pm 5\text{V}/\pm 12\text{V}$ host power supply lines.

CAUTION

MXSIOX-A..D SIO-0 and SIO-1 serial ports are routed to McBSP-0 and McBSP-1 serial ports of the corresponding on-board TMS320C64xx DSP only in case the ‘diagonal’ and ‘vertical’ serial link(s) for this DSP is(are) disabled.

Two timer/IO signals (*TM/XIO-0* and *TM/XIO-1*) for each of MXSIOX-A..D interface connectors are actually the I/O signals of TMS320C64xx DSP on-chip timer #0 and timer #1 for the corresponding DSP. I/O direction control for DSP on-chip timers #0 and #1 input and output is controlled via *GPIO-14* and *GPIO-15* output pins of the corresponding TMS320C64xx DSP. For more details refer to subsection [“MXSIOX timer I/O and reset control”](#) later in this section.

Reset control for each MXSIOX-A..D interface connector is controlled via *GPIO-0* output pin of the corresponding TMS320C64xx DSP. For more details refer to subsection [“MXSIOX timer I/O and reset control”](#) later in this section.

For more details about MXSIOX interface connectors and external *T/SU-X1*, *T/SU-X2* and *T/SU-X3* SIOX rev.B mini-extendors refer to section [“Serial I/O Expansion Interface \(MXSIOX\)”](#) later in this chapter and to [Appendix ‘C’](#) later in this manual.

MXSIOX timer I/O and reset control via TMS320C64xx DSP General Purpose I/O (GPIO) pins

TORNADO-PX64xxQ DSP coprocessor DCM utilizes general purpose I/O (GPIO) pins *GPIO-0*, *GPIO-14* and *GPIO-15* of each on-board TMS320C64xx DSP in order to control reset signal, and direction control for MXSIOX timer/IO pins *TM/XIO-0* and *TM/XIO-1* correspondingly of the corresponding on-board MXSIOX-A..D interface connectors, which can be used for connection to external *T/SU-X1*, *T/SU-X2*, and *T/SU-X3* SIOX rev.B mini-extendors.

CAUTION

GPIO-0, *GPIO-14* and *GPIO-15* pins of each *TORNADO-PX64xxQ* on-board TMS320C64xx DSP shall be enabled as I/O pins via *GPEN* TMS320C64xx DSP on-chip register (@0x01B00000) and configured as ‘OUTPUT’ pins via *GPDIR* TMS320C64xx DSP on-chip register (@0x01B00004).

Output state for *GPIO-0*, *GPIO-14* and *GPIO-15* output pins of each *TORNADO-PX64xxQ* on-board TMS320C64xx DSP shall be set via *GPVAL* TMS320C64xx DSP on-chip register (@0x01B00008).

Table 2-12 provides required settings for *GPEN* and *GPDIR* TMS320C64xx DSP on-chip registers in order to support reset signal and direction control for MXSIOX timer/IO pins of on-board MXSIOX-A..D interface connectors of *TORNADO-PX64xxQ* DSP coprocessor DCM.

Table 2-12. *GPEN* and *GPDIR* register settings for TMS320C64xx DSP.

GPIO control register of TMS320C64xx DSP	Value	description
<i>GPEN</i> (@0x01B00000)	0x0000C0F1	Corresponds to <i>GPIO-0</i> , <i>GPIO-14</i> and <i>GPIO-15</i> pins configured as I/O pins. Also configures EXT_INT4..7 pins as inputs.
<i>GPDIR</i> (@0x01B00004)	0x0000C001	Corresponds to <i>GPIO-0</i> , <i>GPIO-14</i> and <i>GPIO-15</i> pins configured as 'OUTPUT' pins.

CAUTION

For more details about GPIO pins and *GPEN/GPDIR/GPVAL* TMS320C64xx DSP on-chip registers refer to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

Table 2-13 provides description for TMS320C64xx DSP on-chip GPIO-0/14/15 pins functions for *TORNADO-PX64xxQ* DSP coprocessor DCM.

Table 2-13. Configuration of GPIO pins for TMS320C64xx DSP cores.

GPIO pin	MXSIOX interface function	I/O mode	value on DSP reset	Description
<i>GPIO-0</i>	<i>SX_RESET</i>	OUTPUT	0@INPUT	<p><i>GPIO-0</i> pin of TMS320C64xx DSP is used as <i>SX_RESET</i> reset signal of the corresponding on-board MXSIOX interface connector.</p> <p><i>GPIO-0</i> =0 setting corresponds to active 'RESET' state of <i>SX_RESET</i> signal of the corresponding MXSIOX interface site, i.e. MSIOX reset signal is being applied. This state is set as default on DSP reset condition due to on-board pull-down resistor. This setting can be set by applying logical AND of 0xFFFFFEE value and the contents of <i>GPVAL</i> TMS320C64xx DSP on-chip register.</p> <p><i>GPIO-1</i> =1 setting corresponds to the 'RUN' state of <i>SX_RESET</i> signal of the corresponding MXSIOX interface site, i.e. MSIOX reset signal is being released. This setting can be set by means of applying logical OR of 0x00000001 value and the contents of <i>GPVAL</i> TMS320C64xx DSP on-chip register.</p>

<i>GPIO-14</i>	direction control for <i>TM/XIO-0</i>	OUTPUT	1@INPUT	<p><i>GPIO-14</i> pin of TMS320C64xx DSP is used for direction control of <i>TM/XIO-0</i> signal of the corresponding on-board MXSIOX interface connector.</p> <p><i>GPIO-14</i> =0 setting corresponds to the 'OUTPUT' state of <i>TM/XIO-0</i> signal of the corresponding MXSIOX interface site, i.e. DSP on-chip timer-0 output pin (<i>TOUT0</i>) is routed to the <i>TM/XIO-0</i> pin of MXSIOX connector. <i>TINP0</i> input signal status is also available for input via <i>TM/XIO-0</i> pin. This setting can be set by applying logical AND of 0xFFFFBFFF value and the contents of <i>GPVAL</i> TMS320C64xx DSP on-chip register.</p> <p><i>GPIO-14</i> =1 setting corresponds to the 'INPUT' state of <i>TM/XIO-0</i> signal of the corresponding MXSIOX interface site, i.e. DSP on-chip timer-0 output pin (<i>TOUT0</i>) is disabled and only <i>TINP0</i> input pin is routed to the <i>TM/XIO-0</i> pin of MXSIOX connector. This state is set as default on DSP reset condition due to on-board pull-down resistor. This setting can be set by means of applying logical OR of 0x00004000 value and the contents of <i>GPVAL</i> TMS320C64xx DSP on-chip register.</p>
<i>GPIO-15</i>	direction control for <i>TM/XIO-1</i>	OUTPUT	1@INPUT	<p><i>GPIO-15</i> pin of TMS320C64xx DSP is used for direction control of <i>TM/XIO-1</i> signal of the corresponding on-board MXSIOX interface connector.</p> <p><i>GPIO-15</i> =0 setting corresponds to the 'OUTPUT' state of <i>TM/XIO-1</i> signal of the corresponding MXSIOX interface site, i.e. DSP on-chip timer-1 output pin (<i>TOUT1</i>) is routed to the <i>TM/XIO-1</i> pin of MXSIOX connector. <i>TINP1</i> input signal status is also available for input via <i>TM/XIO-1</i> pin. This setting can be set by applying logical AND of 0xFFFF7FFF value and the contents of <i>GPVAL</i> TMS320C64xx DSP on-chip register.</p> <p><i>GPIO-15</i> =1 setting corresponds to the 'INPUT' state of <i>TM/XIO-1</i> signal of the corresponding MXSIOX interface site, i.e. DSP on-chip timer-1 output pin (<i>TOUT1</i>) is disabled and only <i>TINP1</i> input pin is routed to the <i>TM/XIO-1</i> pin of MXSIOX connector. This state is set as default on DSP reset condition due to on-board pull-down resistor. This setting can be set by means of applying logical OR of 0x00008000 value and the contents of <i>GPVAL</i> TMS320C64xx DSP on-chip register.</p>

Note:

1. I/O modes: INPUT – input; OUTPUT – output.
2. Values on DSP reset condition: 0@INPUT - output '0' state with I/O input mode; 1@INPUT - output '1' state with I/O input mode.

Generation of DSP-to-host interrupt request from TMS320C64xx DSP

TORNADO-PX64xxQ DSP coprocessor DCM allows to generate interrupt request from each on-board TMS320C64xx DSP to host **TORNADO** DSP system/controller via **DSP_x_HPI_HINT** (x=A..D) DSP-to-host interrupt request via DSP-x on-chip HPI port.

DSP_x_HPI_HINT (x=A..D) DSP-to-host interrupt request can be set by the corresponding on-board TMS320C64xx DSP software by writing of the '1' value to the **HINT** bit of DSP-x on-chip HPIC register (@0x01880000).

CAUTION

Writing of the '0' value to the *HINT* bit of TMS320C64xx DSP on-chip HPIC register (@0x01880000) by on-board TMS320C64xx DSP software has no effect.

Current state of *DSPx_HPI_HINT* (x=A..D) DSP-to-host interrupt request can be read by host via [HOST_INT_STAT_RG](#) read-only host interface control register (refer to [table 2-22](#))) and via HPIC register ([HOST_HPI32_DSPx_HPIC_RG](#), or [HOST_HPI16_DSPx_HPIC_LSW_RG](#) and [HOST_HPI16_DSPx_HPIC_MSW](#) host interface HPI registers) of on-chip HPI port of the corresponding TMS320C64xx DSP-x (refer to section [“Host PIOX Interface”](#) later in this chapter for more details).

Active *DSPx_HPI_HINT* (x=A..D) DSP-to-host interrupt request can be cleared by host *TORNADO* DSP software only by writing '1' value to the *HINT* bit of DSP-x on-chip HPIC register.

CAUTION

Writing of the '0' value to the *HINT* bit of TMS320C64xx DSP on-chip HPIC register from host *TORNADO* DSP software has no effect.

Host *DSPx_HPI_HINT* interrupt request can generate active host PIOX interrupt request via any of four *IRQ-n* (n=0..3) host PIOX interface interrupt request outputs, which are controlled via [HOST_HIRQn_SEL_RG](#) host interface control registers (n=0..3) of *TORNADO-PX64xxQ* DSP coprocessor DCM. Particular *IRQ-n* (n=0..3) host PIOX interrupt request output, which will be used to forward *DSPx_HPI_HINT* DSP-to-host interrupt request to host *TORNADO* DSP via host PIOX interface, must be enabled via *HIRQ_EN* bit and the corresponding *DSPx_HPI_HINT* (x=A..D) DSP-to-host interrupt request source must be selected via {*HIRQ_SEL-2..0*}bits of the corresponding [HOST_HIRQn_SEL_RG](#) (n=0..3) host interface control register (refer to [tables 2-23](#) and [2-24](#) for more details).

For more details about host PIOX interface interrupt control refer to section [“Host PIOX Interface”](#) later in this chapter.

CAUTION

For more information about *HINT* DSP-to-host interrupt request via TMS320C64xx DSP on-chip HPI port refer to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

Processing of host-to-DSP interrupt request to TMS320C64xx DSP

TORNADO-PX64xxQ DSP coprocessor DCM allows to generate interrupt request from host *TORNADO* DSP software to each particular on-board TMS320C64xx DSP via TMS320C64xx DSP on-chip HPI port, or can generate 'broadcast' interrupt request to all on-board DSP simultaneously.

Host-to-DSP interrupt request to particular on-board DSP-x (x=A..D) can be set by host *TORNADO* DSP software by writing of the '1' value to the *DSPINT* bit of on-chip HPIC register ([HOST HPI32 DSPx HPIC RG](#), or [HOST HPI16 DSPx HPIC LSW RG](#) and [HOST HPI16 DSPx HPIC MSW](#) host interface HPI registers) of on-chip HPI port of the corresponding TMS320C64xx DSP-X (refer to section "[Host PIOX Interface](#)" later in this chapter for more details).

CAUTION

Writing of the '0' value to the *DSPINT* bit of TMS320C64xx DSP on-chip HPIC register from host *TORNADO* DSP software has no effect.

Corresponding TMS320C64xx DSP software can either poll status of *DSPINT* bit of on-chip HPIC register (@0x01880000), or, if default DSP on-chip interrupt selection priority selection is not satisfactory, then DSP on-chip high/low interrupt multiplexer registers (@0x019C0000 and @0x019C0004) shall be used to select particular DSP on-chip interrupt request input/priority, which will be used to interrupt the DSP core on the *DSPINT* host-to-DSP interrupt request event

After TMS320C64xx DSP software has recognized active *DSPINT* host-to-DSP interrupt request via *DSPINT* bit of HPIC register (@0x01880000), it must clear *DSPINT* host-to-DSP interrupt request by writing of the '1' value to the *DSPINT* bit of HPIC register (@0x01880000).

CAUTION

Writing of the '0' value to the *DSPIN* bit of TMS320C64xx DSP on-chip HPIC register (@0x01880000) by DSP software has no effect.

CAUTION

For more information about *DSPINT* host-to-DSP interrupt request via TMS320C64xx DSP on-chip HPI port and how to configure TMS320C64xx DSP on-chip high/low interrupt multiplexer registers refer to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

In case user application requires that host *TORNADO* DSP software must generate simultaneous interrupt request to all on-board TMS320C64xx DSP in order to synchronize DSP software of all on-board TMS320C64xx DSP, then [HOST DSP BROADCAST RQ RG](#) write-only host interface control register must be used to generate 'broadcast' request from host *TORNADO* DSP software to all *TORNADO-PX64xxQ* on-board DSP simultaneously (refer to section "[Host PIOX Interface](#)" later in this chapter for more details). Data written to [HOST DSP BROADCAST RQ RG](#) write-only host interface control register is ignored. In order to detect host 'broadcast' interrupt request, corresponding on-board TMS320C64xx DSP software must configure any of [DSP EXTn INT SEL RG](#) (n=4..7) or [DSP NMI SEL RG](#) IOX control registers to select

host 'broadcast' interrupt request as external interrupt request source for the corresponding EXT_INT4..7/NMI DSP external interrupt inputs (refer to [fig.2-3](#) and [table 2-9](#) and subsection "[EXT_INT4..7/NMI DSP external interrupt selectors](#)" earlier in this chapter for more details). If default DSP on-chip interrupt selection priority is not satisfactory, then TMS320C64xx DSP on-chip high/low interrupt multiplexer registers (@0x019C0000 and @0x019C0004) can be also used to select particular DSP on-chip interrupt request input/priority, which will be used to interrupt the DSP core on external host 'broadcast' host-to-DSP interrupt request event.

CAUTION

For more information about how to configure TMS320C64xx DSP on-chip high/low interrupt multiplexer registers refer to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

2.3 Serial I/O Expansion Interface (MXSIOX)

TORNADO-PX64xxQ DSP coprocessor DCM provides four on-board MXSIOX-A..D interface connectors ([fig.2-1](#), [2-2](#) and [A-1](#)) for optional connection of either up to four external SIOX rev.B DCM (one SIOX rev.B DCM per each TMS320C64xx DSP) for real-time analog/digital signal I/O, or for board-to-board communication in multi-board *TORNADO-PX64xxQ* (or compatibles) DSP systems, that converts *TORNADO-PX64xxQ* DSP coprocessor DCM into universal DSP and application specific I/O coprocessor.

A variety of SIOX rev.B DCM for *TORNADO* DSP systems, controllers and coprocessors include speech/fax/modem AD/DA DCM, telecom interfaces, audio AD/DA, DAT interface, multi-channel instrumentation AD/DA/DIO DCM, application specific I/O coprocessors, and many more.

Connection of external SIOX rev.B DCM to *TORNADO-PX64xxQ* on-board DSP for real-time analog/digital I/O

External SIOX rev.B DCM connects to particular *TORNADO-PX64xxQ* on-board TMS320C64xx DSP via either of external *T/SU-X1*, *T/SU-X2* or *T/SU-X3* SIOX rev.B mini-extendors ([fig.2-9](#)), which connect to *TORNADO-PX64xxQ* on-board MXSIOX-A..D interface connectors (JP3..JP6). Each of external *T/SU-X1*, *T/SU-X2* or *T/SU-X3* SIOX rev.B mini-extendors can carry one full-size SIOX rev.B DCM.

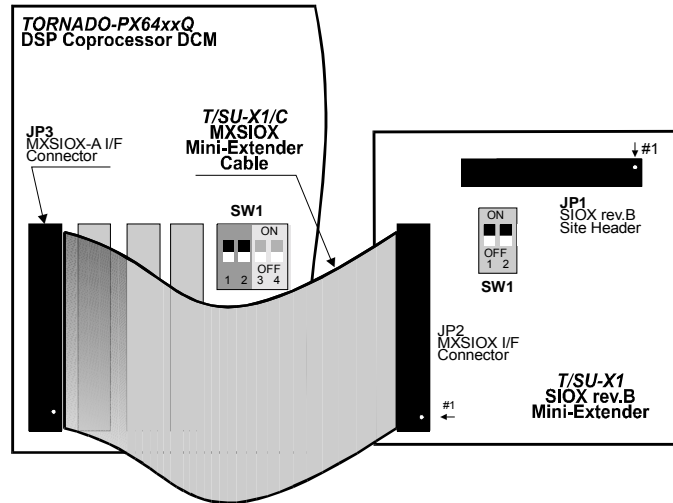


Fig.2-9a. Connection of T/SU-X1 SIOX rev.B mini-extender to TORNADO-PX64xxQ on-board TMS320C64xx DSP-A.

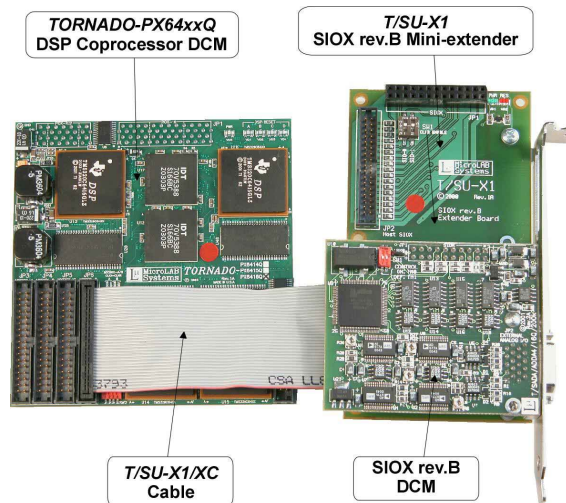


Fig.2-9b. TORNADO-PX64xxQ DCM with two T/SU-X1 SIOX rev.B mini-extenders and one installed SIOX rev.B DCM.

For more information about external T/SU-X1, T/SU-X2 or T/SU-X3 SIOX rev.B mini-extenders refer to [Appendix 'C'](#) later in this manual.

TORNADO-PX64xxQ board-to-board communication via serial links via MXSIOX interface connectors

Multiple *TORNADO-PX64xxQ* DSP coprocessor DCM boards (and serial link compatible boards) can connect into one multi-board DSP systems via optional external *T/X-XSLC1* serial link converters ([fig.2-6](#) and [fig.2-7](#)), which connect to *TORNADO-PX64xxQ* on-board MXSIOX-A..D interface connectors (JP3..JP6). Each of external *T/X-XSLC1* serial links converters provides two on-board serial links and can connect to two external boards, which provide compatible serial links.

For more details about board-to-board communication via serial links for multiple *TORNADO-PX64xxQ* DSP coprocessor DCM boards refer to section [“TMS320C64xx DSP Environment”](#) earlier in this chapter and to [Appendix ‘C’](#) later in this manual.

On-board MXSIOX interface path

SIOX rev.B and MXSIOX interfaces at *TORNADO* DSP systems, controllers and coprocessors generally comprise of signals for SIO-0 and SIO-1 serial ports, two timer/IO lines, external interrupt request inputs, SIOX reset signal and power supply lines.

TORNADO-PX64xxQ on-board MXSIOX interface path for each of four on-board TMS320C64xx DSP ([fig.2-10](#)) comprises of the following signals and components:

- DSP on-chip McBSP-0 and McBSP-1 serial ports, which are routed to MXSIOX SIO-0 and SIO-1 serial ports correspondingly in case ‘diagonal’ and/or ‘vertical’ on-board DSP-to-DSP serial links correspondingly are disabled by host *TORNADO* DSP software via *DSP-AC_LINK_EN*, *DSP-AC_LINK_EN*, *DSP-AD_LINK_EN*, and *DSP-BC_LINK_EN* bits of [HOST_DSP_LINK_CNF_RG](#) host interface control register of host PIOX interface (refer to [tables 2-10, 2-11](#) from section [“TMS320C64xx DSP Environment”](#) and to [table 2-19](#) from section [“Host PIOX Interface”](#) for more details).
- *TM/XIO-0* and *TM/XIO-1* timer/IO signals at MXSIOX connector, which connect to TMS320C64xDSP on-chip timer-0/1 I/O signals *TINP0/TOUT0* and *TINP1/TOUT1* correspondingly. Note, that TMS320C64xx DSP on-chip *GPIO-14* and *GPIO-15* outputs are used for output enable control for *TOUT0* and *TOUT1* timer outputs to *TM/XIO-0* and *TM/XIO-1* timer/IO signals of the corresponding MXSIOX interface connectors (refer to section [“TMS320C64xx DSP Environment”](#) and [tables 2-12](#) and [2-13](#) for more details).
- *XIRQ-0/1* two external DSP interrupt request inputs at MXSIOX connector, which are routed to EXT_INT4..7/NMI interrupt request selectors for the corresponding TMS320C64xx DSP (refer to section [“TMS320C64xx DSP Environment”](#) and [table 2-9](#) for more details).
- Active low *SX_RESET* MXSIOX reset control output, which connects to TMS320C64xx DSP on-chip *GPIO-0* output pin (refer to section [“TMS320C64xx DSP Environment”](#) and [tables 2-12](#) and [2-13](#) for more details).
- $\pm 5\text{v}/\pm 12\text{v}$ host PIOX-16 power supply lines.
- Corresponding on-board MXSIOX-A..D interface connector.
- two dedicated on-board switches, which enable common serial clock for transmitter and receiver (CLKX/CLKR) for each of SIO-0/1 serial port of the corresponding MXSIOX interface connector.

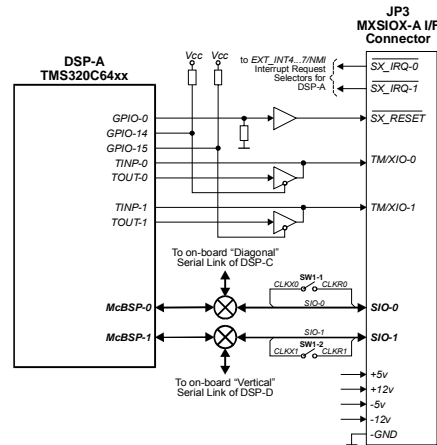


Fig.2-10. TORNADO-PX64xxQ on-board MXSIOX interface path for DSP-A.

MXSIOX interface connector pinout and signal description

TORNADO-PX64xxQ on-board MXSIOX-A..D interface connectors are 34-pin dual-row 2mm guarded male headers from Samtec Inc(www.samtec.com). Compatible MXSIOX plug (Samtec p/n TCSD-17-01-N) comes standard with T/SU-X1/XC SIOX rev.B mini-extender connection cables (refer to [Appendix 'C'](#) for more details), however optional MXSIOX mating plugs for 2mm flat cables are available either from Samtec Inc or from MicroLAB Systems upon request.

T/SU-X1, T/SU-X2, and T/SU-X3 SIOX rev.B DCM mini-extender kits can be used for installation of one SIOX rev.B DCM, therefore signal specifications for MXSIOX interface connectors are the same as that for SIOX rev.B DCM site.

MXSIOX interface connector pinout is presented at fig.2-11, whereas signal description is provided in table 2-14.

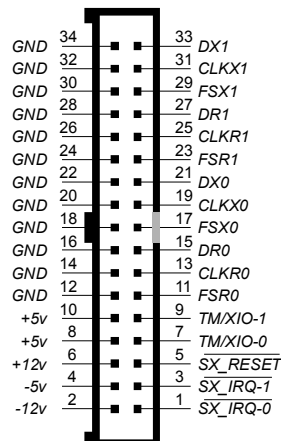


Fig.2-11. Pinout for TORNADO-PX64xxQ on-board MXSIOX interface connector (top view).

Table 2-14. Signal description for TORNADO-PX64xxQ on-board MXSIOX interface connectors.

MXSIOX interface signal	signal type	Description
SIO-0 port control		
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port, which connect to the transmitter control signals for TMS320C64xx DSP on-chip McBSP-0 serial port in case 'diagonal' serial link for this DSP is disabled.
DR0 FSR0 CLKR0	I I I	Data, frame synchronization and serial clock signals for receiver of SIO-0 port, which connect to the receiver control signals for TMS320C64xx DSP on-chip McBSP-0 serial port in case 'diagonal' serial link for this DSP is disabled.
SIO-1 port control		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port, which connect to the transmitter control signals for TMS320C64xx DSP on-chip McBSP-1 serial port in case 'vertical' serial link for this DSP is disabled.
DR1 FSR1 CLKR1	I I/O I	Data, frame synchronization and serial clock signals for receiver of SIO-1 port, which connect to the receiver control signals for TMS320C64xx DSP on-chip McBSP-1 serial port in case 'vertical' serial link for this DSP is disabled.
Timers/IO, DSP Reset and Interrupt Requests		
TM/XIO-0 TM/XIO-1	I/O	Timer/IO #0/#1 pins, which connects to TMS320C64xx DSP on-chip <i>TINP0/TOUT0</i> and <i>TINP1/TOUT1</i> timer I/O pins correspondingly as shown at fig.2-10. These pins can be configured as either INPUT or OUTPUT via TMS320C64xx DSP on-chip <i>GPIO-14</i> and <i>GPIO-15</i> output pins correspondingly (refer to section "TMS320C64xx DSP Environment" and tables 2-12 and 2-13 for more details).
$\overline{SX_RESET}$	O	Active low MXSIOX reset output pin, which connects to TMS320C64xx DSP on-chip <i>GPIO-0</i> output pin (refer to section "TMS320C64xx DSP Environment" and tables 2-12 and 2-13 for more details).
$\overline{SX_IRQ-0}$ $\overline{SX_IRQ-1}$	I	Active low external interrupt request inputs, which connect to EXT_INT4..7/NMI external interrupt selector of the corresponding TMS320C64xx DSP. Active DSP external interrupt requests are generated during high-to-low transition at these inputs.
Power Supplies		
GND		Ground.
+5v		+5v power (from host PIOX interface).
+12v		+12v power (from host PIOX interface).

-5v		-5v power (from host PIOX interface).
-12v		-12v power (from host PIOX interface).

- Note:
1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
 2. All logical signal levels and load currents correspond to that for 3v/5v CMOS signals.

Programming MXSIOX TM/XIO-0/1 and SIOX reset control pins

TORNADO-PX64xxQ DSP coprocessor DCM utilizes general purpose I/O (GPIO) pins **GPIO-0**, **GPIO-14** and **GPIO-15** of each on-board TMS320C64xx DSP in order to control MXSIOX reset signal, and direction control for MXSIOX **TM/XIO-0** and **TM/XIO-1** correspondingly.

For more details about how to configure TMS320C64xx DSP on-chip **GPIO-0/14/15** pins and how to control MXSIOX **TM/XIO-0** and **SX_RESET** pins refer to section [“TMS320C64xx DSP Environment”](#) and [tables 2-12](#) and [2-13](#).

Maximum serial clock frequency for SIOX rev.B DCM

Maximum serial clock frequency for TMS320C64xx DSP on-chip McBSP-0/1 serial ports of **TORNADO-PX64xxQ** DSP coprocessor DCM for communication with external SIOX rev.B DCM via on-board MXSIOX-A..D interface connectors and optional external **T/SU-X1**, **T/SU-X2**, and **T/SU-X3** SIOX rev.B mini-extendors is limited by the length of connection cables and serial clock distribution configuration for installed SIOX rev.B DCM.

CAUTION

In case standard 10” long (0.25m) cable is used for connection of **TORNADO-PX64xxQ** DCM to external **T/SU-X1**, **T/SU-X2**, and **T/SU-X3** SIOX rev.B mini-extendors and the corresponding **TORNADO-PX64xxQ** on-board common serial clock enable switch (SW1..SW2) is set to the ‘OFF’ state (refer to the corresponding subsection below for more details) , then the recommended maximum serial clock frequency for CLKX/CLKR signals for McBSP-0/1 serial ports is 50 MHz.

CAUTION

In case standard 10" long (0.25m) cable is used for connection of *TORNADO-PX64xxQ* DCM to external *T/SU-X1*, *T/SU-X2*, and *T/SU-X3* SIOX rev.B mini-extendors and the corresponding *TORNADO-PX64xxQ* on-board common serial clock enable switch (SW1..SW2) is set to the 'ON' state (refer to the corresponding subsection below for more details) , then the recommended maximum serial clock frequency for CLKX/CLKR signals for McBSP-0/1 serial ports is 25 MHz.

Common CLKX/CLKR serial clock enable control for SIOX rev.B DCM

TORNADO-PX64xxQ DCM provides on-board common CLKX/CLKR serial clock enable switches for each of on-board MXSIOX interface connectors ([fig.2-1](#), [2-2](#), [2-10](#) and [A-1](#)). Each MXSIOX connector has two corresponding common serial clock enable switches (one switch per each SIO port) in accordance with [table A-1](#) in [Appendix 'A'](#) (SW1-1/2 for MXSIOX-A interface connector, SW1-3/4 for MXSIOX-B interface connector, SW2-1/2 for MXSIOX-C interface connector and SW2-3/4 for MXSIOX-D interface connector).

CAUTION

In case *TORNADO-PX64xxQ* on-board common serial clock enable switch is set to the 'ON' state, then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are connected together on-board.

In case *TORNADO-PX64xxQ* on-board common serial clock enable switch is set to the 'OFF' state, then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are disconnected on-board.

TORNADO-PX64xxQ DCM on-board common serial clock enable switches shall be used in conjunction with *T/SU-X1*, *T/SU-X2*, and *T/SU-X3* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switches in accordance with general guidelines provided in [Appendix 'C'](#) of this manual and below in this subsection.

Background for usage *TORNADO-PX64xxQ* on-board common CLKX/CLKR serial clock enable switches and *T/SU-X1*, *T/SU-X2*, and *T/SU-X3* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) enable switches is the 'long-line' compensation issue for serial clock signals distribution over connection flat cable between *TORNADO-PX64xxQ* on-board MXSIOX connector and *T/SU-X1*, *T/SU-X2*, and *T/SU-X3* SIOX rev.B mini-extender due to the 'long-line wave nature' of connection flat cable.

Although the 'long-line' compensation resistors are being used for all McBSP-0/1 control signals (frame synchronization pulse, serial clock and serial data) at both *TORNADO-PX64xxQ* DCM and *T/SU-X1*, *T/SU-X2*, and *T/SU-X3* SIOX rev.B mini-extender boards in order to exclude signal reflection, a 'long-line' non-compensation for serial clock signals can still occur in case installed SIOX rev.B DCM is using common shorted serial clock for transmitter and receiver of SIO port (many SIOX rev.B DCM actually use this in order to simplify design). Note, that this problem does not occur with SIO port frame synchronization and serial data signals, since these signals always use dedicated lines of SIOX interface and can't be connected together.

CAUTION

In case installed SIOX rev.B DCM has been designed without on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and each serial clock is using its dedicated pins, then the corresponding *TORNADO-PX64xxQ* on-board common CLKX/CLKR serial clock enable switch must be set to 'OFF' and the corresponding *T/SU-X1*, *T/SU-X2*, and *T/SU-X3* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to the 'ON' state.

In case installed SIOX rev.B DCM has been designed with on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and both serial clocks are using shared pins, then the corresponding *TORNADO-PX64xxQ* on-board common CLKX/CLKR serial clock enable switch must be set to 'ON' and the corresponding *T/SU-X1*, *T/SU-X2*, and *T/SU-X3* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to the 'OFF' state.

For more information about external *T/SU-X1*, *T/SU-X2*, and *T/SU-X3* SIOX rev.B mini-extendors refer to [Appendix 'C'](#) later in this manual.

2.4 Host PIOX Interface

Host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM provides access from host *TORNADO* DSP system/controller to a set of control registers and to TMS320C64xx DSP on-chip HPI ports in order to provide real-time control of *TORNADO-PX64xxQ* on-board DSP environment from host *TORNADO* DSP software.

This section contains detail description of host PIOX interface architecture of *TORNADO-PX64xxQ* DSP coprocessor DCM.

General description for PIOX interface of host *TORNADO* DSP systems/controllers

Parallel I/O expansion (PIOX) DCM interface site comes standard on all *TORNADO* DSP systems/controllers and allows to install compatible PIOX DCM for high-speed real-time analog/digital I/O, DSP coprocessor DCM and application specific coprocessor DCM, which all feature communication with host *TORNADO* on-board DSP via asynchronous parallel data bus.

There is two types of on-board PIOX DCM interfaces for *TORNADO* DSP systems/controllers: 32-bit PIOX-32 DCM interface and 16-bit PIOX-16 DCM interface, which differ in the width of parallel data/address bus only.

TORNADO on-board 32-bit PIOX-32 DCM interface comprises of 32-bit data bus, 20-bit address bus, data strobes, two timer/IO lines, 2..4 interrupt request inputs (upon particular *TORNADO* DSP system/controller), and power supplies, whereas 16-bit PIOX-16 DCM interface is just a subset of PIOX-32 DCM interface and comprises of 16-bit data bus, 16-bit address bus, data strobes, two timer/IO lines, 2..4 interrupt request inputs (upon particular *TORNADO* DSP system/controller), and power supplies.

For more details about PIOX DCM interface for *TORNADO* DSP systems/controllers refer to [Appendix 'B'](#) of this manual and to the manual for your particular *TORNADO* DSP system/controller.

On-board JP1 connector of *TORNADO-PX64xxQ* DSP coprocessor DCM ([fig.2-1](#), [2-2](#) and [A-1](#)) is used to install into either 32-bit PIOX-32 or 16-bit PIOX-16 expansion interface site of host *TORNADO* DSP system/controller.

Host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM

Host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM has been designed for real-time control of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP environment from host *TORNADO* DSP software and comprises of the following components:

- a set of host interface control registers, which shall be used for on-board DSP control and to configure host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM:
 - ❑ [HOST_CNTR1_RG](#), [HOST_CNTR2_RG](#) and [HOST_DSP_CNF_STAT_RG](#) host interface control registers, which shall be used to [control reset signal, DSP bootmode and HPI port data format for each of on-board TMS320C64xx DSP](#)
 - ❑ [HOST_DSP_LINK_CNF_RG](#) host interface control register for enable control of on-board DSP-to-DSP 'vertical' and 'diagonal' serial links and to correspondingly disable SIO-0 and SIO-1 serial ports of on-board MXSIOX interface connectors
 - ❑ [HOST_DEV_ID_RG](#) and [HOST_DSP_XMEM_LEN_ID_RG](#) host interface control registers for read-only information about device ID and revision ID of *TORNADO-PX64xxQ* DSP coprocessor DCM, speed grade of on-board TMS320C64xx DSP and for capacity of on-board SSRAM and SDRAM memories
 - ❑ [HOST_INT_STAT_RG](#) host interface control register, which shall be used to read status information for on-board interrupt request sources for host PIOX interrupt requests
 - ❑ [HOST_CLR_DSPx_HPI_ERR_RG](#) (x=A..D) host interface control registers for clearing HPI port access timeout errors
 - ❑ [HOST_HIRQx_SEL_RG](#) (x=0..3) host interface control registers, which shall be used to control host PIOX interface interrupt requests
 - ❑ [HOST_DSP_BROADCAST_RQ_RG](#) host interface register for generation of simultaneous 'broadcast' interrupt request from host *TORNADO* DSP software to all *TORNADO-PX64xxQ* on-board DSP
- [DSP on-chip HPI port registers](#) for each of on-board TMS320C64xx DSP, which shall be used by host *TORNADO* DSP software to access DSP environment (DSP on-chip memory and registers, external SSRAM/SDRAM memories, etc) of each on-board TMS320C64xx DSP.

The corresponding subsections below provide detail information for each component of host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor.

Support for host *TORNADO* PIOX-32 and PIOX-16 DCM site interfaces

TORNADO-PX64xxQ DSP coprocessor DCM has been designed to support both host 32-bit PIOX-32 and host 16-bit PIOX-16 interfaces with automatic detection of host PIOX interface type.

Different host PIOX interface formats supported by *TORNADO-PX64xxQ* DSP coprocessor DCM allow to access TMS320C64xx DSP on-chip HPI ports using either 16-bit data format mode (for compatibility with all *TORNADO* DSP systems and controllers) or 32-bit data format mode (for x2 throughput performance). For more details refer to the corresponding subsection below.

Host PIOX interface address map

Host PIOX interface address map for accessing host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM from host *TORNADO* DSP software comprises of control register area and TMS320C64xx DSP on-chip HPI port registers area. Table 2-15 provides details about host PIOX interface address map.

Table 2-15. Host PIOX interface address map.

host PIOX interface register	default value on PIOX interface reset	access mode	address range (in 16-bit data words)
Control Registers area			
<u>HOST_CNTR1_RG</u> register (DSP reset control)	00H	r/w	BA + 0000H*WAS (bits D0..D7 only)
<u>HOST_CNTR2_RG</u> register (DSP HPI data format control and bootmode control, HPI timeout enable control)	00H	r/w	BA + 0001H*WAS (bits D0..D7 only)
<u>HOST_DSP_CNF_STAT_RG</u> register (DSP HPI data format mode and bootmode configuration status)	-	r	BA + 0004H*WAS (bits D0..D7 only)
<u>HOST_DSP_LINK_CNF_RG</u> register (DSP 'vertical'/'diagonal' serial links enable control)	00H	r/w	BA + 0007H*WAS (bits D0..D7 only)
<u>HOST_DEV_ID_RG</u> register (device/revision ID)	-	r	BA + 0008H*WAS (bits D0..D7 only)
<u>HOST_DSP_XMEM_LEN_ID_RG</u> register (DSP external memory length ID)	-	r	BA + 0009H*WAS (bits D0..D7 only)
<u>HOST_INT_STAT_RG</u> register (interrupt status for DSP-to-host interrupt requests via HPI and HPI timeout)	-	r	BA + 000BH*WAS (bits D0..D7 only)
<u>HOST_HIRQ0_SEL_RG</u> register (host PIOX interface HIRQ-0 interrupt selector and enable control)	00H	r/w	BA + 000CH*WAS (bits D0..D7 only)
<u>HOST_HIRQ1_SEL_RG</u> register (host PIOX interface HIRQ-1 interrupt selector and enable control)	00H	r/w	BA + 000DH*WAS (bits D0..D7 only)
<u>HOST_HIRQ2_SEL_RG</u> register (host PIOX interface HIRQ-2 interrupt selector and enable control)	00H	r/w	BA + 000EH*WAS (bits D0..D7 only)

<u>HOST_HIRQ3_SEL_RG</u> register (host PIOX interface HIRQ-3 interrupt selector and enable control)	00H	r/w	BA + 000FH*WAS (bits D0..D7 only)
<u>HOST_CLR_DSPA_HPI_ERR_RG</u> register (clear HPI timeout error for DSP-A)	-	w	BA + 0010H*WAS (write data is ignored)
<u>HOST_CLR_DSPB_HPI_ERR_RG</u> register (clear HPI timeout error for DSP-B)	-	w	BA + 0011H*WAS (write data is ignored)
<u>HOST_CLR_DSPC_HPI_ERR_RG</u> register (clear HPI timeout error for DSP-C)	-	w	BA + 0012H*WAS (write data is ignored)
<u>HOST_CLR_DSPD_HPI_ERR_RG</u> register (clear HPI timeout error for DSP-D)	-	w	BA + 0013H*WAS (write data is ignored)
<u>HOST_DSP_BROADCAST_RQ_RG</u> register (generate host broadcast interrupt request to all DSP)	-	w	BA + 0018H*WAS (written data is ignored)
TMS320C64xx DSP-A on-chip HPI port registers area (32-bit HPI data format mode) ²⁾			
<u>HOST_HPI32_DSPA_HPIC_RG</u> register (32-bit HPI control register)	00080008H	r/w	BA + 0080H*WAS
<u>HOST_HPI32_DSPA_HPIA_RG</u> register (32-bit HPI address register)	-	r/w	BA + 0081H*WAS
<u>HOST_HPI32_DSPA_HPID_AINC_RG</u> register (32-bit HPI data register with address postincrement)	-	r/w	BA + 0082H*WAS
<u>HOST_HPI32_DSPA_HPID_RG</u> register (32-bit HPI data register)	-	r/w	BA + 0083H*WAS
TMS320C64xx DSP-A on-chip HPI port registers area (16-bit HPI data format mode)			
<u>HOST_HPI16_DSPA_HPIC_LSW_RG</u> register (16-bit LSW of HPI control register)	0008H	r/w	BA + 0080H*WAS
<u>HOST_HPI16_DSPA_HPIC_MSW_RG</u> register (16-bit MSW of HPI control register)	0008H	r/w	BA + 0081H*WAS
<u>HOST_HPI16_DSPA_HPIA_LSW_RG</u> register (16-bit LSW of HPI address register)	-	r/w	BA + 0082H*WAS
<u>HOST_HPI16_DSPA_HPIA_MSW_RG</u> register (16-bit MSW of HPI address register)	-	r/w	BA + 0083H*WAS

<i>HOST_HPI16_DSPA_HPID_AINC_LSW_RG</i> register (16-bit LSW of HPI data register with address postincrement)	-	r/w	<i>BA + 0084H*WAS</i>
<i>HOST_HPI16_DSPA_HPID_AINC_MSW_RG</i> register (16-bit MSW of HPI data register with address postincrement)	-	r/w	<i>BA + 0085H*WAS</i>
<i>HOST_HPI16_DSPA_HPID_LSW_RG</i> register (16-bit LSW of HPI data register)	-	r/w	<i>BA + 0086H*WAS</i>
<i>HOST_HPI16_DSPA_HPID_MSW_RG</i> register (16-bit MSW of HPI data register)	-	r/w	<i>BA + 0087H*WAS</i>
<i>TMS320C64xx DSP-B on-chip HPI port registers area</i> <i>(32-bit HPI data format mode)²⁾</i>			
<i>HOST_HPI32_DSPB_HPIC_RG</i> register (32-bit HPI control register)	00080008H	r/w	<i>BA + 0088H*WAS</i>
<i>HOST_HPI32_DSPB_HPIA_RG</i> register (32-bit HPI address register)	-	r/w	<i>BA + 0089H*WAS</i>
<i>HOST_HPI32_DSPB_HPID_AINC_RG</i> register (32-bit HPI data register with address postincrement)	-	r/w	<i>BA + 008AH*WAS</i>
<i>HOST_HPI32_DSPB_HPID_RG</i> register (32-bit HPI data register)	-	r/w	<i>BA + 008BH*WAS</i>
<i>TMS320C64xx DSP-B on-chip HPI port registers area</i> <i>(16-bit HPI data format mode)</i>			
<i>HOST_HPI16_DSPB_HPIC_LSW_RG</i> register (16-bit LSW of HPI control register)	0008H	r/w	<i>BA + 0088H*WAS</i>
<i>HOST_HPI16_DSPB_HPIC_MSW_RG</i> register (16-bit MSW of HPI control register)	0008H	r/w	<i>BA + 0089H*WAS</i>
<i>HOST_HPI16_DSPB_HPIA_LSW_RG</i> register (16-bit LSW of HPI address register)	-	r/w	<i>BA + 008AH*WAS</i>
<i>HOST_HPI16_DSPB_HPIA_MSW_RG</i> register (16-bit MSW of HPI address register)	-	r/w	<i>BA + 008BH*WAS</i>
<i>HOST_HPI16_DSPA_HPID_AINC_LSW_RG</i> register (16-bit LSW of HPI data register with address postincrement)	-	r/w	<i>BA + 008CH*WAS</i>

<i>HOST_HPI16_DSPB_HPID_AINC_MSW_RG</i> register (16-bit MSW of HPI data register with address postincrement)	-	r/w	<i>BA + 008DH*WAS</i>
<i>HOST_HPI16_DSPB_HPID_LSW_RG</i> register (16-bit LSW of HPI data register)	-	r/w	<i>BA + 008EH*WAS</i>
<i>HOST_HPI16_DSPB_HPID_MSW_RG</i> register (16-bit MSW of HPI data register)	-	r/w	<i>BA + 008FH*WAS</i>
<i>TMS320C64xx DSP-C on-chip HPI port registers area</i> <i>(32-bit HPI data format mode)²⁾</i>			
<i>HOST_HPI32_DSPC_HPIC_RG</i> register (32-bit HPI control register)	00080008H	r/w	<i>BA + 0090H*WAS</i>
<i>HOST_HPI32_DSPC_HPIA_RG</i> register (32-bit HPI address register)	-	r/w	<i>BA + 0091H*WAS</i>
<i>HOST_HPI32_DSPC_HPID_AINC_RG</i> register (32-bit HPI data register with address postincrement)	-	r/w	<i>BA + 0092H*WAS</i>
<i>HOST_HPI32_DSPC_HPID_RG</i> register (32-bit HPI data register)	-	r/w	<i>BA + 0093H*WAS</i>
<i>TMS320C64xx DSP-C on-chip HPI port registers area</i> <i>(16-bit HPI data format mode)</i>			
<i>HOST_HPI16_DSPC_HPIC_LSW_RG</i> register (16-bit LSW of HPI control register)	0008H	r/w	<i>BA + 0090H*WAS</i>
<i>HOST_HPI16_DSPC_HPIC_MSW_RG</i> register (16-bit MSW of HPI control register)	0008H	r/w	<i>BA + 0091H*WAS</i>
<i>HOST_HPI16_DSPC_HPIA_LSW_RG</i> register (16-bit LSW of HPI address register)	-	r/w	<i>BA + 0092H*WAS</i>
<i>HOST_HPI16_DSPC_HPIA_MSW_RG</i> register (16-bit MSW of HPI address register)	-	r/w	<i>BA + 0093H*WAS</i>
<i>HOST_HPI16_DSPC_HPID_AINC_LSW_RG</i> register (16-bit LSW of HPI data register with address postincrement)	-	r/w	<i>BA + 0094H*WAS</i>
<i>HOST_HPI16_DSPC_HPID_AINC_MSW_RG</i> register (16-bit MSW of HPI data register with address postincrement)	-	r/w	<i>BA + 0095H*WAS</i>
<i>HOST_HPI16_DSPC_HPID_LSW_RG</i> register (16-bit LSW of HPI data register)	-	r/w	<i>BA + 0096H*WAS</i>

<i>HOST_HPI16_DSPC_HPID_MSW_RG</i> register (16-bit MSW of HPI data register)	-	r/w	BA + 0097H*WAS
TMS320C64xx DSP-D on-chip HPI port registers area (32-bit HPI data format mode) ²⁾			
<i>HOST_HPI32_DSPD_HPIC_RG</i> register (32-bit HPI control register)	00080008H	r/w	BA + 0098H*WAS
<i>HOST_HPI32_DSPD_HPIA_RG</i> register (32-bit HPI address register)	-	r/w	BA + 0099H*WAS
<i>HOST_HPI32_DSPD_HPID_AINC_RG</i> register (32-bit HPI data register with address postincrement)	-	r/w	BA + 009AH*WAS
<i>HOST_HPI32_DSPD_HPID_RG</i> register (32-bit HPI data register)	-	r/w	BA + 009BH*WAS
TMS320C64xx DSP-D on-chip HPI port registers area (16-bit HPI data format mode)			
<i>HOST_HPI16_DSPD_HPIC_LSW_RG</i> register (16-bit LSW of HPI control register)	0008H	r/w	BA + 0098H*WAS
<i>HOST_HPI16_DSPD_HPIC_MSW_RG</i> register (16-bit MSW of HPI control register)	0008H	r/w	BA + 0099H*WAS
<i>HOST_HPI16_DSPD_HPIA_LSW_RG</i> register (16-bit LSW of HPI address register)	-	r/w	BA + 009AH*WAS
<i>HOST_HPI16_DSPD_HPIA_MSW_RG</i> register (16-bit MSW of HPI address register)	-	r/w	BA + 009BH*WAS
<i>HOST_HPI16_DSPD_HPID_AINC_LSW_RG</i> register (16-bit LSW of HPI data register with address postincrement)	-	r/w	BA + 009CH*WAS
<i>HOST_HPI16_DSPD_HPID_AINC_MSW_RG</i> register (16-bit MSW of HPI data register with address postincrement)	-	r/w	BA + 009DH*WAS
<i>HOST_HPI16_DSPD_HPID_LSW_RG</i> register (16-bit LSW of HPI data register)	-	r/w	BA + 009EH*WAS
<i>HOST_HPI16_DSPD_HPID_MSW_RG</i> register (16-bit MSW of HPI data register)	-	r/w	BA + 009FH*WAS

Notes:

1. Access modes: *r* - read only, *w* - write only, *r/w* - read/write.
2. 32-bit HPI data format support is available only with those host *TORNADO* DSP systems, which provide on-board 32-bit PIOX-32 DCM interface site.
3. 'BA' denotes base address for host PIOX interface within the address map of host DSP of host *TORNADO* DSP system/controller.

4. '[WAS](#)' denotes DSP word address step: WAS=1 for TMS320C3x and TMS320C54x DSP; WAS=2 for *TORNADO-E64xx* DSP controller; WAS=4 for all *TORNADO* DSP systems/controllers with TMS320C6xxx DSP except for *TORNADO-E64xx* DSP controller.

CAUTION

Host *TORNADO* DSP software must access *TORNADO-PX64xxQ* DCM at PIOX interface base address, which is specific for particular *TORNADO* DSP system/controller (refer to documentation for your *TORNADO* DSP system/controller for more details about addressing on-board PIOX interface area).

CAUTION

When accessing *Control Register area* of host PIOX interface from host *TORNADO* DSP software, only data bits D0..D7 are valid.

When accessing *TMS320C64xx DSP on-chip HPI port registers area* of host PIOX interface from host *TORNADO* DSP software in 32-bit HPI data format mode, all D0..D31 data bits are valid.

When accessing *TMS320C64xx DSP on-chip HPI port registers area* of host PIOX interface from host *TORNADO* DSP software in 16-bit HPI data format mode, only data bits D0..D15 are valid.

CAUTION

PIOX interface reset signal from host *TORNADO* DSP system/controller must be released prior accessing host interface control registers and TMS320C64xx DSP on-chip HPI port registers areas of host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM, otherwise all host interface control registers cannot be written and DSP on-chip HPI port registers will be unavailable.

CAUTION

It is recommended, that provided host DSP software utility functions for *TORNADO-PX64xxQ* DSP coprocessor DCM (refer to [Appendix 'D'](#) of this manual for more details) are used to access all host interface control registers and TMS320C64xx DSP on-chip HPI ports of *TORNADO-PX64xxQ* host PIOX interface.

Accessing host PIOX interface of TORNADO-PX64xxQ DSP coprocessor from host TORNADO DSP software upon host TORNADO DSP platform and board type

When accessing host interface registers of *TORNADO-PX64xxQ* DSP coprocessor DCM, it is important to note host address multiplier ('WAS' parameter in table 2-15) and corresponding host DSP dataword access formats, which depends upon host *TORNADO* DSP platform and particular board type:

- 'WAS' address multiplier is equal to '1' for all TMS320C3x and TMS320C54xx DSP based *TORNADO* DSP systems/controllers. Both 16-bit PIOX-16 and 32-bit PIOX-32 host interfaces support is available with *TORNADO-3x/P3x* DSP systems, whereas only 16-bit PIOX-16 host interface is available for *TORNADO-E3x* DSP controllers. Host *TORNADO* DSP software can access host interface registers of *TORNADO-PX64xxQ* DSP coprocessor DCM using 32-bit datawords.
- 'WAS' address multiplier is equal to '2' for *TORNADO-E64xx* DSP controllers with TMS320C64xx DSP due to host PIOX-16 interface map to 16-bit EMIF-B external memory interface area of on-board TMS320C64xx DSP. Only 16-bit PIOX-16 host interface is available. Host *TORNADO* DSP software can access host interface control registers of *TORNADO-PX64xxQ* DSP coprocessor DCM using either 8-bit or 16-bit datawords, however TMS320C64xx DSP on-chip HPI port registers shall be accessed using 16-bit datawords only.
- 'WAS' address multiplier is equal to '4' for all *TORNADO-6x/P6x/P64xx/E6x* DSP systems/controllers with TMS320C6xxx/TMS320C64xx DSP except for *TORNADO-E64xx* DSP controllers with TMS320C64xx DSP. Both 16-bit PIOX-16 and 32-bit PIOX host interfaces support is available for *TORNADO-6xx/P6x/P64xx* DSP systems, whereas only 16-bit PIOX-16 host interface is available for *TORNADO-E6x* DSP controllers. Host *TORNADO-6x/P6x/P64xx* DSP software can access host interface control registers of *TORNADO-PX64xxQ* DSP coprocessor DCM using either or 8-/16-/32-bit or datawords, however TMS320C64xx DSP on-chip HPI port registers shall be accessed using 16-/32-bit datawords only for 16-bit HPI data format mode and using 32-bit datawords only for 32-bit HPI data format mode. Host *TORNADO-E6x* DSP software can access host interface control registers of *TORNADO-PX64xxQ* DSP coprocessor DCM using either or 8-/16-/32-bit or datawords, however TMS320C64xx DSP on-chip HPI port registers shall be accessed using 16-/32-bit datawords only.

HOST_CNTR1_RG host interface control register for DSP reset control

HOST_CNTR1_RG control register of host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM must be used to control individual reset signals for on-board TMS320C64xx DSP.

Note, that when accessing *HOST_CNTR1_RG* host interface control register, only data bits D0..D7 of DSP dataword are valid.

HOST_CNTR1_RG register (r/w)

0	0	0	0	$\overline{DSPD_RESET}$ (r/w, 0+)	$\overline{DSPC_RESET}$ (r/w, 0+)	$\overline{DSPB_RESET}$ (r/w, 0+)	$\overline{DSPA_RESET}$ (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-16 provides details about register bit for *HOST_CNTR1_RG* host interface control register.

Table 2-16. Register bits of *HOST_CNTR1_RG* host interface control register.

register bits	access mode	value on host PIOX interface reset	Description
$\overline{DSPA_RESET}$ $\overline{DSPB_RESET}$ $\overline{DSPC_RESET}$ $\overline{DSPD_RESET}$	r/w	0	Reset control reset signals for the corresponding on-board TMS320C64xx DSP-A..D. $\overline{DSPx_RESET} = 0$ corresponds to active RESET signal applied to the corresponding TMS320C64xx DSP-A..D (x=A..D). $\overline{DSPx_RESET} = 1$ corresponds to the RESET signal released for the corresponding TMS320C64xx DSP-A..D (x=A..D), i.e. DSP is in the 'RUN' state.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

HOST_CNTR1_RG control register of host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM allows to perform both individual and simultaneous control over reset signals for on-board TMS320C64xx DSP.

The on-board LED indicators (VD1..VD4) are provided for visual indication of current state for the reset signals for each of on-board *TORNADO-PX64xxQ* on-board DSP.

HOST_CNTR2_RG host interface control register for DSP bootmode control, HPI data format control and host-to-HPI timeout enable control

HOST_CNTR2_RG register of host PIOX interface must be used for common HPI port reset control for all TMS320C64xx DSP cores and to enable timeout error control for host-to-HPI accesses.

Note, that when accessing *HOST_CNTR2_RG* host interface control register, only data bits D0..D7 of DSP dataword are valid.

HOST_CNTR2_RG register (r/w)

$\overline{DSP_HPI_ERR_EN}$ (r/w, 0+)	$\overline{PX_FMT}$ (r)	0	0	0	0	$\overline{DSP_HPI_FMT_CNTR}$ (r/w, 0+)	$\overline{DSP_BMODE_CNTR}$ (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-17 provides details about register bits for *HOST_CNTR2_RG* host interface control register.

Table 2-17. Register bits of *HOST_CNTR2_RG* host interface control register.

register bits	access mode	value on host PIOX interface reset	Description
<i>DSP_BMODE_CNTR</i>	r/w	0	<p>DSP bootmode control for all on-board TMS320C64xx DSP, which are still held in the RESET state (refer to table 2-2 and section “TMS320C64xx DSP Environment” earlier in this chapter for more details).</p> <p><i>DSP_BMODE_CNTR</i>=0 sets ‘NO BOOT’ DSP bootmode for on-board TMS320C64xx DSP.</p> <p><i>DSP_BMODE_CNTR</i>=1 sets ‘HPI BOOT’ DSP bootmode for on-board TMS320C64xx DSP.</p>
<i>DSP_HPI_FMT_CNTR</i>	r/w	0	<p>HPI data format control for all on-board TMS320C64xx DSP, which are still held in the RESET state. This bit has effect only in case <i>TORNADO-PX64xxQ</i> DSP coprocessor DCM is installed onto host <i>TORNADO</i> DSP system with on-board 32-bit PIOX-32 interface, i.e. when <i>PX_FMT</i> read-only bit of <i>HOST_CNTR2_RG</i> host interface control register is set to the ‘1’ state, otherwise this bit is read-only and is held in the ‘0’ state.</p> <p><i>DSP_HPI_FMT_CNTR</i>=0 sets 16-bit HPI data format mode for on-board TMS320C64xx DSP. This is default setting on host PIOX interface reset condition and in case 16-bit host PIOX-16 interface is detected (<i>PX_FMT</i> read-only bit of <i>HOST_CNTR2_RG</i> register reads as ‘0’).</p> <p><i>DSP_HPI_FMT_CNTR</i>=1 sets 32-bit HPI data format mode for on-board TMS320C64xx DSP. This value can be set by host <i>TORNADO</i> DSP software only in case 32-bit host PIOX interface has been detected (<i>PX_FMT</i> read-only bit of <i>HOST_CNTR2_RG</i> register reads as ‘1’).</p>
<i>PX_FMT</i>	r	-	<p>Read-only bit, which indicates host PIOX interface data format. This bit effects <i>DSP_HPI_FMT_CNTR</i> bit functionality of <i>HOST_CNTR2_RG</i> register, which defines HPI data format control for on-board TMS320C64xx DSP.</p> <p><i>PX_FMT</i>=0 correspond to detected 16-bit host PIOX-16 interface. In this case, HPI data format for on-board TMS320C64xx DSP cannot be set to 32-bit mode via <i>DSP_HPI_FMT_CNTR</i> bit of <i>HOST_CNTR2_RG</i> register.</p> <p><i>PX_FMT</i>=1 correspond to detected 32-bit host PIOX-32 interface. In this case, HPI data format for on-board TMS320C64xx DSP cannot be set to both 16-bit and 32-bit modes via <i>DSP_HPI_FMT_CNTR</i> bit of <i>HOST_CNTR2_RG</i> register.</p>

<i>DSP_HPI_ERR_EN</i>	r/w	0	<p>Timeout error enable for host-to-HPI access to all TMS320C64xx DSP via host PIOX interface.</p> <p><i>DSP_HPI_ERR_EN</i>=0 disabled timeout error control for host-to-HPI accesses. In case any HPI access collision occurs with continuous missing HPI ready signal, then host PIOX interface access cycle will remain active until DSP HPI ready signal comes active. This can result in infinite hanging of host <i>TORNADO</i> DSP environment. Infinitely active host-to-HPI access cycle can be aborted only by applying DSP reset signal to host <i>TORNADO</i> DSP system/controller.</p> <p><i>DSP_HPI_ERR_EN</i>=1 enables timeout error control for host-to-HPI access. In case any HPI access collision occurs with continuous missing HPI ready signal, then host PIOX interface access cycle will remain active either until DSP HPI ready signal comes active or until timeout expires, whichever comes first. This will exclude possible hanging of host <i>TORNADO</i> DSP environment and exclude the need to apply reset signal to DSP of host <i>TORNADO</i> DSP system/controller in order to terminate pending host-to-HPI access cycle. In case the HPI access timeout occurs during access to any DSP core of DSP-x (x=A..D), then bit <i>DSPX_HPIn_ERR</i> of <i>HOST_INT_STAT_RG</i> register will be set and host PIOX interrupt can be generated. Timeout period for host-to-HPI access is set to 2.5 us.</p>
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Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP_BMODE_CNTR and *DSP_HPI_FMT_CNTR* bits of *HOST_CNTR2_RG* host interface control register are used to set DSP bootmode and HPI data format correspondingly for those on-board TMS320C64xx DSP, which are held in the reset state via the corresponding *DSPx_RESET* bits of *HOST_CNTR1_RG* host interface control register. These bits effect DSP bootmode and HPI data format correspondingly for particular DSP only until reset signal for this DSP is released. After DSP reset signal has been released, then DSP bootmode status and HPI data format mode status for this particular DSP are latched in *HOST_DSP_CNF_STAT_RG* read-only register. Refer to the corresponding subsection below for more details.

HPI_TMOUT_EN bit of *HOST_CNTR2_RG* register is used to enable timeout enable control for host-to-HPI access cycles of host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM. Refer to the corresponding subsection below for more details.

***HOST_DSP_CNF_STAT_RG* read-only host interface control register for read-back of DSP bootmode and HPI data format for each on-board TMS320C64xx DSP**

HOST_CNTR2_RG read-only register of host PIOX interface must be used to read-back DSP bootmode and HPI data format for each of on-board TMS320C64xx DSP, which has been already released from the reset state.

Note, that when accessing *HOST_DSP_CNF_STAT_RG* register, only data bits D0..D7 of DSP dataword are valid.

HOST_DSP_CNF_STAT_RG register (r)

<i>DSPD_HPI_FMT_STAT</i> (r,0+)	<i>DSPC_HPI_FMT_STAT</i> (r,0+)	<i>DSPB_HPI_FMT_STAT</i> (r,0+)	<i>DSPA_HPI_FMT_STAT</i> (r,0+)	<i>DSPD_BMODE_STAT</i> (r,0+)	<i>DSPC_BMODE_STAT</i> (r,0+)	<i>DSPB_BMODE_STAT</i> (r,0+)	<i>DSPA_BMODE_STAT</i> (r,0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-18 provides details about register bits for *HOST_DSP_CNF_STAT_RG* host interface control register.

Table 2-18. Register bits of *HOST_DSP_CNF_STAT_RG* host interface control register.

register bits	access mode	value on host PIOX interface reset	Description
<i>DSPA_BMODE_STAT</i> <i>DSPB_BMODE_STAT</i> <i>DSPC_BMODE_STAT</i> <i>DSPD_BMODE_STAT</i>	r	0	<p>Latched DSP bootmode status for each of on-board TMS320C64xx DSP, which has been already released from the RESET state (refer to table 2-2 and section “TMS320C64xx DSP Environment” earlier in this chapter for more details). DSP bootmode status is latched individually for each on-board DSP and is defined by the state <i>DSP_BMODE_CNTR</i> bit of <i>HOST_CNTR1_RG</i> register during release of DSP reset signal for this DSP.</p> <p><i>DSPx_BMODE_STAT</i>=0 denotes that the corresponding TMS320C64xx DSP has been booted in ‘NO BOOT’ DSP bootmode.</p> <p><i>DSPx_BMODE_STAT</i>=1 denotes that the corresponding TMS320C64xx DSP has been booted in ‘HPI BOOT’ DSP bootmode.</p>

<i>DSPA_HPI_FMT_STAT</i> <i>DSPB_HPI_FMT_STAT</i> <i>DSPC_HPI_FMT_STAT</i> <i>DSPD_HPI_FMT_STAT</i>	r	0	<p>Latched HPI data format status for each of on-board TMS320C64xx DSP, which has been already released from the RESET state. HPI data format mode status is latched individually for each on-board DSP and is defined by the state <i>DSP_HPI_FMT_CNTR</i> bit of <i>HOST_CNTR1_RG</i> register during release of DSP reset signal for this DSP. These bits have effect only in case <i>TORNADO-PX64xxQ</i> DSP coprocessor DCM is installed onto host <i>TORNADO</i> DSP system with on-board 32-bit PIOX-32 interface, i.e. when <i>PX_FMT</i> read-only bit of <i>HOST_CNTR2_RG</i> host interface control register is set to the '1' state, otherwise these bits always read as '0'.</p> <p><i>DSPx_HPI_FMT_STAT</i>=0 denotes that the corresponding on-board TMS320C64xx DSP has been initialized with 16-bit HPI data format mode for DSP on-chip HPI port. This is default setting on host PIOX interface reset condition and in case 16-bit host PIOX-16 interface is detected (<i>PX_FMT</i> read-only bit of <i>HOST_CNTR2_RG</i> register reads as '0').</p> <p><i>DSPx_HPI_FMT_STAT</i>=1 denotes that the corresponding on-board TMS320C64xx DSP has been initialized with 32-bit HPI data format mode for DSP on-chip HPI port. 32-bit HPI data format mode can be set by host <i>TORNADO</i> DSP software only in case 32-bit host PIOX interface has been detected (<i>PX_FMT</i> read-only bit of <i>HOST_CNTR2_RG</i> register reads as '1').</p>
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Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSPx_BMODE_STAT and *DSPx_HPI_FMT_STAT* bits of *HOST_DSP_CNF_STAT_RG* read-only host interface control register are actually the latched status of *DSP_BMODE_CNTR* and *DSP_HPI_FMT_CNTR* bits correspondingly of *HOST_CNTR2_RG* register of host PIOX interface, which have been latched at releases of DSP reset signal for particular on-board DSP-A..D. Refer to the corresponding subsection below for more details.

Start-up procedure for TORNADO-PX64xxQ on-board TMS320C64xx DSP

When initializing particular *TORNADO-PX64xxQ* on-board TMS320C64xx DSP, host *TORNADO* DSP software must set DSP bootmode and HPI data format mode for this DSP and then release reset signal for this DSP.

CAUTION

32-bit HPI data format mode for *TORNADO-PX64xxQ* on-board TMS320C64xx DSP can be set only in case *TORNADO-PX64xxQ* DSP coprocessor DCM is installed onto host *TORNADO* DSP system with 32-bit PIOX-32 DCM interface site, otherwise 16-bit HPI data format mode is the only default setting available for TMS320C64xx DSP on-chip HPI port.

In order to meet requirements of different applications, *TORNADO-PX64xxQ* DSP coprocessor DCM allows to configure DSP bootmode and HPI data format mode and to release DSP reset signal for on-board TMS320C64xx DSP from host *TORNADO* DSP software either independently for each of on-board DSP or

simultaneously for any number of on-board DSP. If this is required by user application, this will deliver accurate synchronization of DSP software running at different on-board TMS320C64xx DSP.

CAUTION

When performing simultaneous initialization of several on-board TMS320C64x DSP, these DSP are initialized with identical DSP bootmode and HPI data format mode.

[HOST_CNTR1_RG](#) and [HOST_CNTR2_RG](#) host interface control registers shall be used to control reset signal and to configure DSP bootmode and HPI port data format for each of on-board TMS320C64xx DSP. [HOST_DSP_CNF_STAT_RG](#) read-only host interface control register must be used to read DSP bootmode and HPI data format mode for each of on-board TMS320C64xx DSP, which have been already initialized (DSP reset signal is released for these DSP).

The following is a summary of start-up procedure for on-board TMS320C64xx DSP, which must be controlled via host *TORNADO* DSP software:

- put particular DSP, which has (have) to be initialized, into the reset state by setting corresponding $\overline{DSPx_RESET}$ ($x=A..D$) bit(s) of [HOST_CNTR1_RG](#) host interface control register to the '0' state (refer to [table 2-16](#) for more details)
- set DSP bootmode and HPI data format mode for this (these) DSP via *DSP_BMODE_CNTR* and *DSP_HPI_FMT* bits of [HOST_CNTR2_RG](#) host interface control register (refer to [table 2-17](#) for more details). Note, that host *TORNADO* DSP software will be able to set *DSP_HPI_FMT* bit to the '1' state in order to select 32-bit HPI data format mode only in case *TORNADO-PX64xxQ* DSP coprocessor DCM is installed onto host *TORNADO* DSP system with 32-bit PIOX-32 DCM interface site, i.e. in case *PX_FMT* bit of [HOST_CNTR2_RG](#) host interface control register reads as '1'.
- release reset signal for particular DSP or several DSP, which have to be initialized synchronously, i.e. set corresponding $\overline{DSPx_RESET}$ ($x=A..D$) bit(s) of [HOST_CNTR1_RG](#) host interface control register to the '1' state.

Note, that *DSP_BMODE_CNTR* and *DSP_HPI_FMT_CNTR* bits of [HOST_CNTR2_RG](#) host interface control register can be used to set DSP bootmode and HPI data format correspondingly for those on-board TMS320C64xx DSP, which are held in the reset state via the corresponding $\overline{DSPx_RESET}$ bits of [HOST_CNTR1_RG](#) host interface control register After DSP reset signal(s) for particular DSP has (have) been released, then DSP bootmode status and HPI data format mode status for this particular DSP are latched in the corresponding *DSPx_BMODE_STAT* and *DSPx_HPI_FMT_STAT* bits of [HOST_DSP_CNF_STAT_RG](#) read-only host interface control register

In case *TORNADO-PX64xxQ* on-board TMS320C64xx DSP is configured to start in '*NO BOOT*' DSP bootmode, then it will start execution from DSP on-chip memory address 0x00000000 immediately after release of the reset signal for this DSP. '*NO BOOT*' DSP bootmode is typically selected during debugging of DSP software via JTAG emulator and in case DSP execution code has been already uploaded into DSP on-chip memory.

In case '*HPI BOOT*' DSP bootmode is selected, then TMS320C64xx DSP kernel is held in the reset state after release of DSP reset signal while the remainder of the DSP devices is functional, including DSP on-chip HPI port and EMIF-A/B external memory interfaces. In '*HPI BOOT*' DSP bootmode, host *TORNADO* DSP software can access all DSP memory areas including DSP on-chip and off-chip memories and peripherals in order to upload code/data into DSP environment.

CAUTION

Accessing DSP off-chip memories (SSRAM, SDRAM) and IOX control registers during '*HPI BOOT*' DSP bootmode requires that host *TORNADO* DSP software must correctly configure all DSP on-chip EMIF-A/B control registers via DSP HPI port in accordance with [table 2-3](#) prior accessing external DSP memories.

TMS320C64xx DSP on-chip EMIF-A/B control registers can be configured by host *TORNADO* DSP application software using supplied *TORNADO-PX64xxQ* host DSP control utilities (refer to [Appendix 'D'](#) of this manual for more details).

In '*HPI BOOT*' DSP bootmode, TMS320C64xx DSP kernel will be released from the reset state and will start program execution from memory location at address 0x00000000H as soon as host *TORNADO* DSP software will set *DSPINT* bit of DSP on-chip *HPIC* register for this DSP (the corresponding *HOST_HPI32_DSPx_HPIC_RG*, or *HOST_HPI16_DSPx_HPIC_LSW_RG* and *HOST_HPI16_DSPx_HPIC_MSW_RG* registers of *TORNADO-PX64xxQ* host PIOX interface, refer to the corresponding subsection below for more details). Note, that '*HPI BOOT*' DSP bootmode is the only way to upload DSP execution code from host *TORNADO* DSP software via host PIOX interface into on-board TMS320C64xx DSP environments.

For more details and TMS320C64xx DSP bootmodes refer to original TI documentation for TMS320C6xxx DSP, which is included in either paper or electronic form along with this manual.

***HOST_DSP_LINK_CNF_RG* host interface control register for enable control of on-board DSP-to-DSP 'vertical' and 'diagonal' serial links**

HOST_DSP_LINK_CNF_RG register of host PIOX interface must be used for enable control of on-board DSP-to-DSP 'vertical' and 'diagonal' serial links (refer to fig.2-4a for more details) and to correspondingly disable/enable to route out corresponding DSP on-chip McBSP-0 and McBSP-1 serial ports to on-board MXSIOX interface connectors for board-to-board communication and for external real-time analog/digital I/O.

Note, that when accessing *HOST_DSP_LINK_CNF_RG* host interface control register, only data bits D0..D7 of DSP dataword are valid.

***HOST_DSP_LINK_CNF_RG* register (r/w)**

9	0	0	0	<i>DSP-BC_LINK_EN</i> (r/w, 0+)	<i>DSP-AD_LINK_EN</i> (r/w, 0+)	<i>DSP-BD_LINK_EN</i> (r/w, 0+)	<i>DSP-AC_LINK_EN</i> (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-19 provides details about register bits for *HOST_DSP_LINK_CNF_RG* host control interface register.

Table 2-19. Register bits of *HOST_DSP_LINK_CNF_RG* host interface control register.

register bits	access mode	value on host PIOX interface reset	Description
<i>DSP-AC_LINK_EN</i>	r/w	0	<p>Enable control for on-board 'vertical' serial link between DSP-A and DSP-C via on-chip McBSP-1 serial ports of these DSP (refer to fig.2-4a and section "TMS320C64xx DSP Environment" earlier in this chapter for more details). Read-only status copy of this bit appear as <i>VERT_LINK_EN</i> bit of <i>DSP_SYS_STAT_RG</i> IOX control register for DSP-A and DSP-C environments (refer to table 2-4 for more details).</p> <p><i>DSP-AC_LINK_EN</i>=0 disabled on-board 'vertical' serial link between DSP-A and DSP-C and route out McBSP-1 DSP on-chip serial ports to the SIO-1 serial ports of on-board MXSIOX-A and MXSIOX-C interface connectors.</p> <p><i>DSP-AC_LINK_EN</i>=1 enabled on-board 'vertical' serial link between DSP-A and DSP-C via McBSP-1 DSP on-chip serial ports and disables SIO-1 serial ports of on-board MXSIOX-A and MXSIOX-C interface connectors.</p>
<i>DSP-BD_LINK_EN</i>	r/w	0	<p>Enable control for on-board 'vertical' serial link between DSP-B and DSP-D via on-chip McBSP-1 serial ports of these DSP (refer to fig.2-4a and section "TMS320C64xx DSP Environment" earlier in this chapter for more details). Read-only status copy of this bit appear as <i>VERT_LINK_EN</i> bit of <i>DSP_SYS_STAT_RG</i> IOX control register for DSP-B and DSP-D environments (refer to table 2-4 for more details).</p> <p><i>DSP-BD_LINK_EN</i>=0 disabled on-board 'vertical' serial link between DSP-B and DSP-D and route out McBSP-1 DSP on-chip serial ports to the SIO-1 serial ports of on-board MXSIOX-B and MXSIOX-D interface connectors.</p> <p><i>DSP-BD_LINK_EN</i>=1 enabled on-board 'vertical' serial link between DSP-B and DSP-D via McBSP-1 DSP on-chip serial ports and disables SIO-1 serial ports of on-board MXSIOX-B and MXSIOX-D interface connectors.</p>

<i>DSP-AD_LINK_EN</i>	r/w	0	<p>Enable control for on-board 'diagonal' serial link between DSP-A and DSP-D via on-chip McBSP-0 serial ports of these DSP (refer to fig.2-4a and section "TMS320C64xx DSP Environment" earlier in this chapter for more details). Read-only status copy of this bit appear as <i>DIAG_LINK_EN</i> bit of <i>DSP_SYS_STAT_RG</i> IOX control register for DSP-A and DSP-D environments (refer to table 2-4 for more details).</p> <p><i>DSP-AD_LINK_EN</i>=0 disabled on-board 'diagonal' serial link between DSP-A and DSP-D and route out McBSP-0 DSP on-chip serial ports to the SIO-0 serial ports of on-board MXSIOX-A and MXSIOX-D interface connectors.</p> <p><i>DSP-AD_LINK_EN</i>=1 enabled on-board 'diagonal' serial link between DSP-A and DSP-D via McBSP-0 DSP on-chip serial ports and disables SIO-0 serial ports of on-board MXSIOX-A and MXSIOX-D interface connectors.</p>
<i>DSP-BC_LINK_EN</i>	r/w	0	<p>Enable control for on-board 'diagonal' serial link between DSP-B and DSP-C via on-chip McBSP-0 serial ports of these DSP (refer to fig.2-4a and section "TMS320C64xx DSP Environment" earlier in this chapter for more details). Read-only status copy of this bit appear as <i>DIAG_LINK_EN</i> bit of <i>DSP_SYS_STAT_RG</i> IOX control register for DSP-B and DSP-C environments (refer to table 2-4 for more details).</p> <p><i>DSP-BC_LINK_EN</i>=0 disabled on-board 'diagonal' serial link between DSP-B and DSP-C and route out McBSP-0 DSP on-chip serial ports to the SIO-0 serial ports of on-board MXSIOX-B and MXSIOX-C interface connectors.</p> <p><i>DSP-BC_LINK_EN</i>=1 enabled on-board 'diagonal' serial link between DSP-B and DSP-C via McBSP-0 DSP on-chip serial ports and disables SIO-0 serial ports of on-board MXSIOX-B and MXSIOX-C interface connectors.</p>

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

Note, that read-only status copy of the corresponding bits of *HOST_DSP_LINK_CNF_RG* host interface control register appear as read-only *VERT_LINK_EN* and *DIAG_LINK_EN* bits of *DSP_SYS_STAT_RG* IOX control register for each on-board TMS320C64xx DSP (refer to table 2-4 and section "TMS320C64xx DSP environment" earlier in this chapter).

HOST_DEV_ID_RG read-only host interface control register for device ID and revision ID information

HOST_DEV_ID_RG read-only register of host PIOX interface must be used to get device ID, revision ID and DSP speed ID information for *TORNADO-PX64xxQ* DSP coprocessor DCM. This is the same device ID, revision ID and DSP speed ID information, which are available via *DSP_DEV_ID_RG* and *DSP_REV_ID_RG* read-only IOX control registers from DSP environment (refer to tables 2-6 and 2-7 for more details).

Note, that when accessing *HOST_DEV_ID_RG* host interface control register, only data bits D0..D7 of DSP dataword are valid.

HOST_DEV_ID_RG register (r)

DSP_SPEED_ID-1 (r)	DSP_SPEED_ID-0 (r)	REV_ID-1 (r)	REV_ID-0 (r)	0	0	DEV_ID-1 (r)	DEV_ID-0 (r)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-20 provides details about register bits for *HOST_DEV_ID_RG* host interface control register.

Table 2-20. Register bits of *HOST_DEV_ID_RG* host interface control register.

register bits	access mode	value on host PIOX interface reset	Description
{DEV_ID-1..0}	r	-	<p>Returns unique device ID for each available type of <i>TORNADO-PX64xxQ</i> DSP coprocessor boards.</p> <p>{DEV_ID-1..0} = [0,0] corresponds to <i>TORNADO-PX6414Q</i> DSP coprocessor board with TMS320C6414 DSP.</p> <p>{DEV_ID-1..0} = [0,1] corresponds to <i>TORNADO-PX6415Q</i> DSP coprocessor board with TMS320C6415 DSP.</p> <p>{DEV_ID-1..0} = [1,0] corresponds to <i>TORNADO-PX6416Q</i> DSP coprocessor board with TMS320C6416 DSP.</p> <p>{DEV_ID-1..0} = [1,1] is reserved for future expansion <i>TORNADO-PX6414Q</i> DSP coprocessor product line and never reads via <i>HOST_DEV_ID_RG</i> IOX control register.</p>
{REV_ID-1..0}	r	-	<p>Returns unique revision ID for each available firmware revision of <i>TORNADO-PX64xxQ</i> DSP coprocessor boards.</p> <p>{REV_ID-1..0} = [0,0] is reserved.</p> <p>{REV_ID-1..0} = [0,1] corresponds to firmware revision 1 of <i>TORNADO-PX64xxQ</i> DSP coprocessor board. So far, this is the only available firmware revision for <i>TORNADO-PX64xxQ</i> DSP coprocessor boards.</p> <p>{REV_ID-1..0} = [1,0] is reserved.</p> <p>{REV_ID-1..0} = [1,1] is reserved.</p>

{DSP_SPEED_ID-1..0}	r	-	Returns unique ID for DSP clock frequency (speed) grade of <i>TORNADO-PX64xxQ</i> on-board TMS320C64xx DSP. {DSP_SPEED_ID-1..0} = [0,0] corresponds to 600 MHz frequency grade for on-board TMS320C64xx DSP. {DSP_SPEED_ID-1..0} = [0,1] corresponds to 720 MHz frequency grade for on-board TMS320C64xx DSP. {DSP_SPEED_ID-1..0} = [1,0] is reserved. {DSP_SPEED_ID-1..0} = [1,1] is reserved.
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Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

HOST_DSP_XMEM_LEN_ID_RG read-only host interface control register for DSP external SSRAM/SDRAM memory length information

HOST_DSP_XMEM_LEN_ID_RG read-only register of host PIOX interface must be used to get memory length ID for on-board DSP external SSRAM and SDRAM memories for *TORNADO-PX64xxQ* DSP coprocessor DCM. This is the same DSP external memory ID information, which is available via *DSP_XMEM_LEN_ID_RG* read-only IOX control registers from DSP environment (refer to table 2-8 for more details).

Note, that when accessing *HOST_DSP_XMEM_LEN_ID_RG* host interface control register, only data bits D0..D7 of DSP dataword are valid.

HOST_DSP_XMEM_LEN_ID_RG register (r)

0	0	0	0	SDRAM_LEN_ID-1 (r)	SDRAM_LEN_ID-0 (r)	SSRAM_LEN_ID-1 (r)	SSRAM_LEN_ID-0 (r)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-21 provides details about register bits for *HOST_DSP_XMEM_LEN_ID_RG* host interface control register.

Table 2-21. Register bits of *HOST_DSP_XMEM_LEN_ID_RG* host interface control register.

register bits	access mode	value on host PIOX interface reset	Description
{SSRAM_LEN_ID-1..0}	r	-	Returns unique ID for SSRAM memory capacity installed onto <i>TORNADO-PX64xxQ</i> DSP coprocessor board. {SSRAM_LEN_ID-1..0} = [0,0] denotes that SSRAM memory is not installed. {SSRAM_LEN_ID-1..0} = [0,1] denotes that on-board SSRAM memory capacity is 32Kx32 (128 kbytes). {SSRAM_LEN_ID-1..0} = [1,0] denotes that on-board SSRAM memory is 64Kx32 (256 kbytes). {SSRAM_LEN_ID-1..0} = [1,1] is reserved.
{SDRAM_LEN_ID-1..0}	r	-	Returns unique ID for SDRAM memory capacity installed onto <i>TORNADO-PX64xxQ</i> DSP coprocessor board. {SDRAM_LEN_ID-1..0} = [0,0] denotes that SDRAM memory is not installed. {SDRAM_LEN_ID-1..0} = [0,1] denotes that on-board SDRAM memory capacity is 4Mx32 (16 Mbytes). {SDRAM_LEN_ID-1..0} = [1,0] denotes that on-board SSRAM memory is 16Mx32 (64 Mbytes). {SDRAM_LEN_ID-1..0} = [1,1] is reserved.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

HOST_DSP_BROADCAST_RQ_RG write-only host interface registers for generation of ‘broadcast’ request to all on-board DSP simultaneously

HOST_DSP_BROADCAST_RQ_RG write-only host interface control register must be used to generate ‘broadcast’ request from host *TORNADO* DSP software to all *TORNADO-PX64xxQ* on-board DSP simultaneously.

Note, that when writing to *HOST_DSP_BROADCAST_RQ_RG* write-only register, write data is ignored.

HOST_DSP_BROADCAST_RQ_RG register (w)

x	X	x	X	x	x	x	x
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Host broadcast request does not provide any data passed to on-board DSP, however it can be used by on-board TMS320C64xx DSP software to generate DSP interrupt request (refer to table 2-9 for more details).

Host broadcast request to all on-board *TORNADO-PX64xxQ* DSP must be used by host *TORNADO* DSP software in order to perform software synchronization of on-board DSP.

Host PIOX interrupt requests control

TORNADO-PX64xxQ DCM can generate interrupt requests to host *TORNADO* DSP via any of available *IRQ-0..3* host PIOX interrupt request inputs. Each of *IRQ-0..3* host PIOX interrupt request outputs of *TORNADO-PX64xxQ* DSP coprocessor DCM can be individually enabled and configured to generate output interrupt request from any of available host interrupt request sources.

CAUTION

Different host *TORNADO* DSP systems/controllers can utilize different number and different connection of *IRQ-0..3* interrupt requests for on-board PIOX DCM interface site.

For more information refer to [Appendix 'B'](#) of this manual and to the user's guide for your particular *TORNADO* DSP system/controller, which is used as the host *TORNADO* board for installation of *TORNADO-PX64xxQ* DSP coprocessor DCM.

The following are *TORNADO-PX64xxQ* host interface control registers, which are used to control *TORNADO-PX64xxQ* on-board host PIOX interrupt request output and to get status of host interrupt request sources from host *TORNADO* DSP software:

- [HOST HIRQx SEL RG](#) (x=0..3) host interface control registers, which are used for enable control and to select interrupt request source for each of host PIOX interface interrupt request outputs.
- [HOST INT STAT RG](#) read-only host interface control register, which is used to read status information for each of interrupt request sources for host PIOX interrupt requests during software polling of host PIOX interrupt requests.
- [HOST CLR DSPx HPI ERR RG](#) (x=A..D) host interface control registers, which are used to clear HPI port access timeout errors, which can be configured as interrupt request source for host PIOX interrupt requests.

TORNADO-PX64xxQ DSP coprocessor DCM provides *IRQ-0..3* host PIOX interrupt request outputs, which are held in the Z-state as default state on host PIOX interface reset condition. This is required in order meet design of all host *TORNADO* DSP systems/controllers, which can be used to install *TORNADO-PX64xxQ* DSP coprocessor DCM onto it.

CAUTION

Some *TORNADO* DSP systems/controllers provide on-board shared SIOX/PIOX interrupt request, which are common for on-board SIOX and PIOX DCM interface sites.

In this case, care must be taken to ensure that the same shared SIOX/PIOX interrupt request is not active simultaneously at installed SIOX DCM and PIOX DCM. Otherwise, this may result in damage of on-board hardware of either or both SIOX or/and PIOX DCM.

For more information refer to the user's guide for your particular *TORNADO* DSP system/controller, which is used as the host *TORNADO* board for installation of *TORNADO-PX64xxQ* DSP coprocessor DCM.

Particular *IRQ-x* ($x=0..3$) host PIOX interrupt request output can be activated and the interrupt request source can be selected via the *HIRQ_EN* and *{HIRQ_SEL-2..0}* bits of the corresponding [HOST HIRQx SEL RG](#) ($x=0..3$) host interface control register. Instead, in case particular host PIOX interrupt request output of *TORNADO-PX64xxQ* host PIOX interface is disabled, then this host PIOX interrupt request output will stay in the Z-state and cannot generate interrupt request to host *TORNADO* on-board DSP.

Each of *IRQ-0..3* host PIOX interface host interrupt request outputs of *TORNADO-PX64xxQ* DSP coprocessor DCM can generate interrupt request to host *TORNADO* DSP from the following on-board host interrupt request sources:

- *DSPx_HPI_HINT* ($x=A..D$) DSP-to-host interrupt requests via DSP on-chip HPI port from the corresponding TMS320C64xx DSP, which is actually the *HINT* bit of on-chip HPIC register for this DSP. The corresponding host PIOX interrupt request will be set active as soon as the *HINT* bit of DSP- x on-chip HPIC register will be set to the '1' state by DSP- x software (refer to section "[TMS320C64xx DSP Environment](#)" earlier in this chapter for more details). *DSPx_HPI_HINT* DSP-to-host interrupt requests is available for software polling via the corresponding *DSPx_HPI_HINT* bit of [HOST INT STAT RG](#) host interface control register ([table 2-22](#)) and via the *HINT* bit of DSP- x on-chip HPIC register. *DSPx_HPI_HINT* DSP-to-host interrupt requests via DSP on-chip HPI port from the corresponding TMS320C64xx DSP can be cleared by host *TORNADO* DSP software only by writing of '1' to the *HINT* bit of DSP- x on-chip HPIC register (refer to subsection "[TMS320C64xx DSP HPI port access areas](#)" below for more details).
- From the summary (ORed) DSP HPI access timeout error event for host-to-HPI access cycles of *TORNADO-PX64xxQ* host PIOX interface, which is the logical OR of all *DSPx_HPI_ERR* timeout error flags ($x=A..D$), which are available for read via [HOST INT STAT RG](#) read-only host interface control register. *DSPx_HPI_ERR* timeout error flags are enabled only in case the *DSP_HPI_ERR_EN* bit of [HOST CNTR2 RG](#) host interface control register is set to the '1' state (refer to [table 2-17](#) for more details). *DSPx_HPI_ERR* timeout error flags can be cleared by writing to the corresponding [HOST CLR DSPx HPI ERR RG](#) ($x=A..D$) host interface control registers.

HOST_INT_STAT_RG read-only host interface control register for read-back status of DSP-to-host interrupt via HPI port and status of HPI access timeout error

HOST_INT_STAT_RG read-only register of host PIOX interface must be used to perform software polling of status information for all interrupt sources, which can generate host PIOX interrupt request, i.e. DSP-to-host interrupt requests via HPI ports (*DSPx_HPI_HINT*) and host-to-HPI access timeout errors for all on-board TMS320C64xx DSP.

Note, that when accessing *HOST_INT_STAT_RG* host interface control register, only data bits D0..D7 of DSP dataword are valid.

***HOST_INT_STAT_RG* register (r)**

<i>DSPD_HPI_ERR</i> (r,0+)	<i>DSPC_HPI_ERR</i> (r,0+)	<i>DSPB_HPI_ERR</i> (r,0+)	<i>DSPA_HPI_ERR</i> (r,0+)	<i>DSPD_HPI_HINT</i> (r,0+)	<i>DSPC_HPI_HINT</i> (r,0+)	<i>DSPB_HPI_HINT</i> (r,0+)	<i>DSPA_HPI_HINT</i> (r,0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-22 provides details about register bits for *HOST_INT_STAT_RG* host interface control register.

Table 2-22. Register bits of *HOST_INT_STAT_RG* host interface control register.

register bits	access mode	value on host PIOX interface reset	Description
<i>DSPA_HPI_HINT</i> <i>DSPB_HPI_HINT</i> <i>DSPC_HPI_HINT</i> <i>DSPD_HPI_HINT</i>	r	0	<p>Indicates current status of DSP-to-host interrupt request via DSP on-chip HPI port for the corresponding on-board TMS320C64xx DSP, which is identical to the current status of <i>HINT</i> bit of DSP on-chip HPI control register (HPIC) of the corresponding TMS320C64xx DSP..</p> <p><i>DSPx_HPI_HINT</i>=0 corresponds to no DSP-to-host interrupt request via HPI port of the corresponding TMS320C64xx DSP #x (x=A..D).</p> <p><i>DSPx_HPI_HINT</i>=1 corresponds to active DSP-to-host interrupt request via HPI port of the corresponding TMS320C64xx DSP #x (x=A..D). Each of <i>DSPx_HPI_HINT</i> DSP-to-host interrupt requests can be cleared by writing the '1' value to the <i>HINT</i> bit of the corresponding DSP on-chip HPIC register from host <i>TORNADO</i> DSP software (refer to subsection 'Host-to-HPI access timeout control' below for more details).</p>
<i>DSPA_HPI_ERR</i> <i>DSPB_HPI_ERR</i> <i>DSPC_HPI_ERR</i> <i>DSPD_HPI_ERR</i>	r	0	<p>Indicates current status of individual timeout errors for host-to-HPI access via host PIOX interface for each of on-board TMS320C64xx DSP, which is set in case of timeout condition during host access to DSP on-chip HPI port of the corresponding DSP while HPI timeout error control is enabled via <i>DSP_HPI_ERR_EN</i> bit of HOST_CNTR2_RG host interface control register (refer to table 2-17 and to subsection 'Host-to-HPI access timeout control' below for more details).</p> <p><i>DSPx_HPI_ERR</i>=0 corresponds to no timeout condition detected for host access via host PIOX interface to the corresponding DSP-x on-chip HPI port registers.</p> <p><i>DSPx_HPI_ERR</i>=1 corresponds to active timeout condition detected for host access via host PIOX interface to the corresponding DSP-x on-chip HPI port registers. Each of <i>DSPx_HPI_ERR</i> error flags can be cleared by writing to the corresponding HOST_CLR_DSPx_HPI_ERR_RG host interface control register (refer to the corresponding subsection below for more details).</p>

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

Although status information for DSP-to-host interrupt requests via DSP on-chip HPI ports (*DSPx_HPI_HINT*) is also available as the *HINT* bits of the corresponding DSP on-chip HPI control registers for each of on-board TMS320C64xx DSP (*HOST_HPI32_DSPx_HPIC_RG*, *HOST_HPI16_DSPx_HPIC_LSW_RG* and *HOST_HPI16_DSPx_HPIC_MSW_RG* host HPI port registers in [table 2-15](#)), putting all *HINT* bits for all on-board TMS320C64xx DSP together into one read-only register allows to analyze them all simultaneously (in case software polling is used) and significantly reduces host DSP time to perform this polling task.

DSP-to-host interrupt request via TMS320C64xx DSP on-chip HPI port can be set by the corresponding on-board TMS320C64xx DSP software only by writing of the '1' value to the *HINT* bit of DSP on-chip HPIC register (refer to section "[TMS320C64xx DSP Environment](#)" earlier in this chapter), whereas it can be cleared by host *TORNADO* DSP software only by writing of the '1' value to the *HINT* bit of the corresponding DSP on-chip HPIC register (*HOST_HPI32_DSPx_HPIC_RG*, *HOST_HPI16_DSPx_HPIC_LSW_RG* and *HOST_HPI16_DSPx_HPIC_MSW_RG* host HPI port registers in [table 2-15](#)) via host PIOX interface of *TORNADO-PX64xxQ* DCM.

CAUTION

For more information about *HINT* DSP-to-host interrupt request via DSP on-chip HPI port refer to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

Individual HPI timeout error flags for each of on-board TMS320C64xx DSP is set in case of timeout condition during host-to-HPI accesses to any of the DSP on-chip HPI register for the corresponding DSP while HPI timeout error control is enabled via *DSP_HPI_ERR_EN* bit of [HOST_CNTR2_RG](#) host interface control register (refer to [table 2-17](#) and to the corresponding subsection below for more details).

Once set to the '1' state, each of *DSPx_HPI_ERR* error flags can be cleared individually by writing to the corresponding [HOST_CLR_DSPx_HPI_ERR_RG](#) host interface control register (refer to the corresponding subsection below for more details).

HOST_CLR_DSPx_HPI_ERR_RG write-only host interface registers for clearing host-to-HPI access timeout error flags

HOST_CLR_DSPx_HPI_ERR_RG write-only host interface control registers (x=A..D) shall be used to clear the corresponding *DSPx_HPI_ERR* timeout error flags, which are set in case of timeout error condition during host-to-HPI access cycle to any of the DSP on-chip HPI registers of the corresponding TMS320C64xx DSP.

DSPx_HPI_ERR timeout error flags are available via [HOST_INT_STAT_RG](#) read-only host interface control register (refer to [table 2-22](#) for more details).

Note, that when writing to *HOST_CLR_DSPx_HPI_ERR_RG* write-only registers (x=A..D), write data is ignored.

HOST_CLR_DSPx_HPI_ERR_RG register (w)
(x=A..D)

x	x	x	x	x	x	x	x
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

HOST_HIRQ0_SEL_RG..HOST_HIRQ3_SEL_RG registers for control of host PIOX interface interrupt requests

HOST_HIRQ0_SEL_RG, HOST_HIRQ1_SEL_RG, HOST_HIRQ2_SEL_RG, and HOST_HIRQ3_SEL_RG host interface control registers shall be used to select particular interrupt request source and to enable (activate) corresponding IRQ-0..3 host PIOX interrupt requests of TORNADO-PX64xxQ DSP coprocessor DCM, which shall be used to generate interrupt requests from TORNADO-PX64xxQ DCM to host DSP at host TORNADO DSP system/controller.

CAUTION

Different host TORNADO DSP systems/controllers can utilize different number and different connection of IRQ-0..3 interrupt requests for on-board PIOX DCM interface site.

For more information refer to [Appendix ‘B’](#) of this manual and to the user’s guide for your particular TORNADO DSP system/controller, which is used as the host TORNADO board for installation of TORNADO-PX64xxQ DSP coprocessor DCM.

Note, that when accessing HOST_HIRQ0_SEL_RG, HOST_HIRQ1_SEL_RG, HOST_HIRQ2_SEL_RG, and HOST_HIRQ3_SEL_RG host interface control registers, only data bits D0..D7 of DSP dataword are valid.

HOST_HIRQ0_SEL_RG register (r/w)
HOST_HIRQ1_SEL_RG register (r/w)
HOST_HIRQ2_SEL_RG register (r/w)
HOST_HIRQ3_SEL_RG register (r/w)

HIRQ_EN (r/w, 0+)	0	0	0	0	HIRQ_SEL-2 (r/w, 0+)	HIRQ_SEL-1 (r/w, 0+)	HIRQ_SEL-0 (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-23 provides details about register bits for HOST_HIRQ0_SEL_RG, HOST_HIRQ1_SEL_RG, HOST_HIRQ2_SEL_RG, and HOST_HIRQ3_SEL_RG host interface control registers.

Table 2-23. Register bits of *HOST_HIRQ0_SEL_RG*, *HOST_HIRQ1_SEL_RG*, *HOST_HIRQ2_SEL_RG*, and *HOST_HIRQ3_SEL_RG* host interface control registers.

register bits	access mode	value on host PIOX interface reset	Description
<i>HIRQ_EN</i>	r/w	0	Controls output enable (activation) feature for the corresponding <i>IRQ-0..3</i> host PIOX interrupt request output of <i>TORNADO-PX64xxQ</i> host PIOX interface. <i>HIRQ_EN</i> =0 disables corresponding host PIOX interrupt request output and puts it into the Z-state. This is default setting on host PIOX interface reset conditions. <i>HIRQ_EN</i> =1 enables (activates) corresponding host PIOX interrupt request output with the host interrupt request source defined via <i>{HIRQ_SEL-2..0}</i> bits of the corresponding <i>HOST_HIRQn_SEL_RG</i> host interface control register (n=0..3)
<i>{HIRQ_SEL-2..0}</i>	r/w	{0,0,0}	Selects particular interrupt request source for the corresponding <i>IRQ-0..3</i> host PIOX interrupt request output of <i>TORNADO-PX64xxQ</i> host PIOX interface in accordance with table 2-24 .

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

Table 2-24. Interrupt request source selection for host PIOX interrupt requests.

<i>{HIRQ_SEL-2..0}</i> bits of HOST_HIRQx_SEL_RG host interface control registers			Description
<i>HIRQ_SEL-2</i>	<i>HIRQ_SEL-2</i>	<i>HIRQ_SEL-2</i>	
0	0	0	Corresponds to no interrupt request source selected for the corresponding host PIOX interrupt request output, i.e. this host PIOX interrupt request output is disabled. This is default setting for host PIOX interface reset condition.
0	0	1	Corresponds to the summary (ORed) DSP HPI access timeout error event is selected as interrupt request source for the corresponding host PIOX interrupt request output. Summary (ORed) DSP HPI access timeout error event for host-to-HPI access cycles of <i>TORNADO-PX64xxQ</i> host PIOX interface is the logical OR of all <i>DSPx_HPI_ERR</i> timeout error flags (x=A..D), which are available via HOST_INT_STAT_RG host interface control register (table 2-22). Refer to subsection ' Host-to-HPI access timeout control ' below for more details.
0	1	0	Reserved setting, do not use. Results in no interrupt request source selected for the corresponding host PIOX interrupt request output, i.e. this host PIOX interrupt request output is disabled.

0	1	1	Reserved setting, do not use. Results in no interrupt request source selected for the corresponding host PIOX interrupt request output, i.e. this host PIOX interrupt request output is disabled.
1	0	0	Corresponds to the <i>DSPA_HPI_HINT</i> DSP-to-host interrupt request from the on-board DSP-A selected as the source for the corresponding host PIOX interrupt request output. <i>DSPA_HPI_HINT</i> DSP-to-host interrupt request is actually the <i>HINT</i> bit of DSP-A on-chip HPIC register.
1	0	1	Corresponds to the <i>DSPB_HPI_HINT</i> DSP-to-host interrupt request from the on-board DSP-B selected as the source for the corresponding host PIOX interrupt request output. <i>DSPB_HPI_HINT</i> DSP-to-host interrupt request is actually the <i>HINT</i> bit of DSP-B on-chip HPIC register.
1	1	0	Corresponds to the <i>DSPC_HPI_HINT</i> DSP-to-host interrupt request from the on-board DSP-C selected as the source for the corresponding host PIOX interrupt request output. <i>DSPC_HPI_HINT</i> DSP-to-host interrupt request is actually the <i>HINT</i> bit of DSP-C on-chip HPIC register.
1	1	1	Corresponds to the <i>DSPD_HPI_HINT</i> DSP-to-host interrupt request from the on-board DSP-D selected as the source for the corresponding host PIOX interrupt request output. <i>DSPD_HPI_HINT</i> DSP-to-host interrupt request is actually the <i>HINT</i> bit of DSP-D on-chip HPIC register.

Note: 1. Highlighted configurations correspond to default settings on PIOX interface reset condition.

Once particular *IRQ-n* ($n=0..3$) host PIOX interrupt request output of *TORNADO-PX64xxQ* host PIOX interface is enabled via the *HIRQ_EN* bit of the corresponding *HOST_HIRQx_SEL_RG* host interface control register (*HIRQ_EN*=1), then this interrupt request output can generate interrupt requests to host *TORNADO* on-board DSP in accordance with the interrupt request source, which is selected via *{HIRQ_SEL-2..0}* bits of the corresponding *HOST_HIRQx_SEL_RG* host interface control register.

In case particular *IRQ-n* ($n=0..3$) host PIOX interrupt request output of *TORNADO-PX64xxQ* host PIOX interface is disabled via the *HIRQ_EN* bit of *HOST_HIRQx_SEL_RG* host interface control register (*HIRQ_EN*=0), then this host PIOX interrupt request output will stay in the Z-state and cannot generate interrupt request to host *TORNADO* on-board DSP. The contents of *{HIRQ_SEL-2..0}* bits of the corresponding *HOST_HIRQx_SEL_RG* host interface control register is ignored in this case.

CAUTION

Some *TORNADO* DSP systems/controllers provide on-board shared SIOX/PIOX interrupt request, which are common for on-board SIOX and PIOX DCM interface sites.

In this case, care must be taken to ensure that the same shared SIOX/PIOX interrupt request is not active simultaneously at installed SIOX DCM and PIOX DCM. Otherwise, this may result in damage of on-board hardware of either or both SIOX or/and PIOX DCM.

For more information refer to the user's guide for your particular *TORNADO* DSP system/controller, which is used as the host *TORNADO* board for installation of *TORNADO-PX64xxQ* DSP coprocessor DCM.

TMS320C64xx DSP HPI port access areas

Host PIOX interface memory map of *TORNADO-PX64xxQ* DSP coprocessor DCM provides four TMS320C64xx DSP HPI port access areas (refer to [table 2-15](#)) each corresponding to the DSP on-chip HPI port registers of particular TMS320C64xx DSP.

TMS320C64xx DSP HPI port areas of host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM shall be used to perform the following operations:

- to access DSP environment (DSP on-chip memory and registers, external SSRAM/SDRAM memories, etc) of each on-board TMS320C64xx DSP from host *TORNADO* DSP software concurrently with the DSP program execution
- to generate host-to-DSP interrupt request via *DSPINT* bit of HPIC register to each on-board TMS320C64xx DSP
- to receive DSP-to-host interrupt request via *HINT* bit of HPIC register from each on-board TMS320C64xx DSP.

Each of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP can be configured to start with either 16-bit HPI data format mode or with 32-bit HPI data format mode for access to DSP on-chip HPI port registers from host *TORNADO* DSP software. HPI data format mode can be set by host *TORNADO* DSP software via *DSP_HPI_FMT* bit of [HOST_CNTR2_RG](#) host interface control register (refer to subsection [‘Start-up procedure for TORNADO-PX64xxQ on-board DSP’](#) earlier in this section and to [table 2-17](#) for more details).

CAUTION

Host *TORNADO* DSP software will be able to set *DSP_HPI_FMT* bit to the '1' state in order to select 32-bit HPI data format mode only in case *TORNADO-PX64xxQ* DSP coprocessor DCM is installed onto host *TORNADO* DSP system with 32-bit PIOX-32 DCM interface site (i.e. *TORNADO* TMS20C3xC6x DSP systems for host PCI-bus and ISA-bus PC), i.e. in case *PX_FMT* bit of [HOST_CNTR2_RG](#) host interface control register reads as '1'.

Host *TORNADO* DSP software will be able to use 16-bit HPI data format mode only in case *TORNADO-PX64xxQ* DSP coprocessor DCM is installed onto host *TORNADO* DSP system/controller with 16-bit PIOX-16 DCM interface site (i.e. *TORNADO-54x* DSP systems for host ISA-bus PC and *TORNADO-Exxxx* stand-alone DSP controllers), i.e. in case *PX_FMT* bit of [HOST_CNTR2_RG](#) host interface control register reads as '0'.

Universal 16-bit HPI data format mode for access to DSP on-chip HPI port provides compatibility with different host *TORNADO* DSP systems, whereas 32-bit HPI data format mode delivers x2 higher HPI port registers access performance.

Due to two different HPI data format modes available (16-bit and 32-bit HPI data format modes), each of four DSP HPI port access areas of host PIOX interface memory map (refer to [table 2-15](#)), which correspond to particular on-board TMS320C64x DSP, actually comprises of two overlapped sub-areas each corresponding to particular HPI data format modes:

- *32-bit HPI port registers sub-area*, which corresponds to 32-bit HPI data format mode and comprises of the following 32-bit HPI port registers for TMS320C64xx DSP:
 - ❑ *HOST_HPI32_DSPx_HPIC_RG* (x=A..D) DSP on-chip HPI port control register (HPIC)
 - ❑ *HOST_HPI32_DSPx_HPIA_RG* (x=A..D) DSP on-chip HPI address register (HPIA)
 - ❑ *HOST_HPI32_DSPx_HPID_AINC_RG* (x=A..D) DSP on-chip HPI data access register with HPI address postincrement feature (HPID_AINC)
 - ❑ *HOST_HPI32_DSPx_HPID_RG* (x=A..D) DSP on-chip HPI data access register (HPID)
- *16-bit HPI port registers area*, which corresponds to universal 16-bit HPI data format mode and comprises of the following 16-bit least significant words (LSW) and most significant words (MSW) for each of TMS320C64xx DSP on-chip 32-bit HPI port registers:
 - ❑ *HOST_HPI16_DSPx_HPIC_LSW_RG* and *HOST_HPI16_DSPx_HPIC_MSW_RG* (x=A..D) registers, which are the LSW and MSW 16-bit words of DSP on-chip 32-bit HPI port control register (HPIC)
 - ❑ *HOST_HPI16_DSPx_HPIA_LSW_RG* and *HOST_HPI16_DSPx_HPIA_MSW_RG* (x=A..D) registers, which are the LSW and MSW 16-bit words of DSP on-chip 32-bit HPI address register (HPIA)
 - ❑ *HOST_HPI16_DSPx_HPID_AINC_LSW_RG* and *HOST_HPI16_DSPx_HPID_AINC_MSW_RG* (x=A..D) registers, which are the LSW and MSW 16-bit words of DSP on-chip 32-bit HPI data access register with HPI address postincrement feature (HPID_AINC)
 - ❑ *HOST_HPI16_DSPx_HPID_LSW_RG* and *HOST_HPI16_DSPx_HPID_MSW_RG* (x=A..D) registers, which are the LSW and MSW 16-bit words of DSP on-chip 32-bit HPI data access register (HPID).

CAUTION

Host PIOX address for any of TMS320C64xx DSP on-chip 32-bit HPI port register may not match host PIOX address for the corresponding 16-bit LSW/MSW for this HPI port register.

CAUTION

Host *TORNADO* DSP software must use 32-bit data words only to access DSP on-chip HPI port registers in 32-bit HPI data format mode via host 32-bit PIOX-32 interface.

Host *TORNADO-3x/P3x/E3x* DSP software must use 32-bit data words to access 16-bit LSW/MSW of TMS320C64xx DSP on-chip 32-bit HPI port registers in 16-bit HPI data format mode. 16-bit LSW/MSW data of DSP on-chip 32-bit HPI port registers are aligned at 16-bit LSW of 32-bit DSP datawords.

Host *TORNADO-6x/P6x/P64xx/E6x* DSP software can use either 16-bit (recommended) or 32-bit data words to access 16-bit LSW/MSW of TMS320C64xx DSP on-chip 32-bit HPI port registers in 16-bit HPI data format mode via host PIOX interface. If 32-bit data words are used to access 16-bit LSW/MSW of DSP on-chip 32-bit HPI port registers in 16-bit HPI data format mode, then 16-bit LSW/MSW data of DSP on-chip 32-bit HPI port registers are aligned at 16-bit LSW of 32-bit DSP datawords.

Host *TORNADO-E64xx* DSP software must use 16-bit data words only to access 16-bit LSW/MSW of TMS320C64xx DSP on-chip 32-bit HPI port registers in 16-bit HPI data format mode via host 16-bit PIOX-16 interface.

CAUTION

When accessing TMS320C64xx DSP on-chip HPI port registers in 16-bit HPI data format mode via host PIOX interface, host *TORNADO* DSP software must perform sequential access to 16-bit LSW and 16-bit MSW of the corresponding DSP on-chip 32-bit HPI port register (with 16-bit LSW of DSP on-chip 32-bit HPI port register being accessed first) in order to complete access to this DSP on-chip 32-bit HPI port register.

It is not allowed to access 16-bit LSW/MSW of any other 32-bit HPI port register of the same on-board TMS320C64xx DSP until completing access to 16-bit LSW and 16-bit MSW of the currently accessed 32-bit HPI port register for this DSP.

For more information about TMS320C64xx DSP on-chip HPI port refer to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

Host-to-HPI access timeout control

TMS320C64xx DSP on-chip HPI port has been designed as simple asynchronous parallel data device with input HPI strobe signal (*HPI_STB* at [fig.2-12](#)), which is used by host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM to activate host-to-HPI access cycle/request, and output HPI ready signal (*HRDY* at [fig.2-12](#)), which is used by accessed on-board TMS320C64xx DSP to acknowledge that the currently active host-to-HPI access request has been processed by DSP on-chip HPI DMA controller and host-to-HPI access cycle can be terminated by host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM.

However, there are known conditions when active host-to-HPI access request cannot be completed by TMS320C64xx DSP on-chip HPI DMA controller and TMS320C64xx DSP output HPI ready signal (*HRDY* at [fig.2-12](#)) is not generated, that results in infinite pending of host-to-HPI access, and therefore, infinite stall and unreliable operation of host controller software. The following is the list of conditions, which result in infinite pending of host-to-HPI access for TMS320C64xx DSP:

- DSP on-chip HPI port register is accessed while DSP is in the reset state
- Host-to-HPI access cycle is currently addressing on-board DSP external memory (SSRAM or SDRAM), which contains executable DSP code, which is currently executed by this DSP (this is known as the DSP EMIF access conflict)
- DSP has executed IDLE2 or IDLE3 instruction
- Sometime when DSP is executing invalid code due to the software bug.

TORNADO-PX64xxQ host PIOX-16 interface has been designed to provide reliable operation of host *TORNADO* DSP software and exclude its infinite stall, which is caused by probable infinite pending of host-to-HPI access cycles, by means of on-board hardware timeout control for host-to-HPI access cycles of *TORNADO-PX64xxQ* host PIOX interface.

Hardware timeout controller for host-to-HPI access cycles of *TORNADO-PX64xxQ* host PIOX interface is enabled via *DSP_HPI_ERR_EN* bit of [HOST_CNTR2_RG](#) host interface control register, which defaults to the 'OFF' state on host PIOX interface reset condition.

In case *DSP_HPI_ERR_EN* bit of [HOST_CNTR2_RG](#) host interface control register is set to the '0' ('OFF') state, then hardware timeout controller for host-to-HPI access cycles is disabled and there is no timeout restriction during access from host *TORNADO* DSP software to any on-chip HPI port register of any *TORNADO-PX64xxQ* on-board TMS320C64xx DSP. Although this provides infinite wait time for normal termination of host-to-HPI access cycle and therefore all host-to-HPI accesses shall generally complete normally while on-board DSP is executing valid code, this is completely user responsibility to guarantee that there will be no infinite stall for host *TORNADO* DSP software due to the listed above known conditions for infinite pending of host-to-HPI access.

In case *DSP_HPI_ERR_EN* bit of [HOST_CNTR2_RG](#) host interface control register is set to the '1' state, then hardware timeout controller for host-to-HPI access cycles is enabled and every access from host *TORNADO* DSP software to any on-chip HPI port register of any *TORNADO-PX64xxQ* on-board TMS320C64xx DSP will be either terminated normally on HPI ready condition, or will be aborted on HPI access timeout error condition.

Hardware timeout interval for host-to-HPI access cycles of *TORNADO-PX64xxQ* host PIOX interface is set to 2.55 μ s, that meets requirements of generally all applications. In case the timeout error condition occurs during host-to-HPI access for any of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP, then the corresponding

DSPx_HPI_ERR timeout error flag (x=A..D) of [HOST INT STAT RG](#) read-only host interface control register will be set to the '1' state (refer to [table 2-22](#) for more details).

CAUTION

DSPx_HPI_ERR timeout error flags (x=A..D) are available for software polling via [HOST INT STAT RG](#) host interface control register of host PIOX-16 interface, and can generate host PIOX interrupt requests to host *TORNADO* on-board DSP via *IRQ-n* (n=0..3) host PIOX interrupt request output in case this *IRQ-n* (n=0..3) host PIOX interrupt request output is enabled via *HIRQ_EN* bit and the summary (ORed) DSP HPI access timeout error event is selected as interrupt request source for the this host PIOX interrupt request output via corresponding [HOST HIRQn_SEL RG](#) (n=0..3) host interface control register (refer to [tables 2-23](#) and [2-24](#) for more details).

Summary (ORed) DSP HPI access timeout error event for host-to-HPI access cycles of *TORNADO-PX64xxQ* host PIOX interface is the logical OR of all *DSPx_HPI_ERR* timeout error flags (x=A..D), which are available via [HOST INT STAT RG](#) host interface control register.

Once *DSPx_HPI_ERR* (x=A..D) timeout error flag has been set during access to any on-chip HPI port register of any particular TMS320C64xx DSP, then it remains active until it will be cleared by host *TORNADO* DSP software by writing to the corresponding [HOST CLR DSPx HPI ERR RG](#) write-only host interface control register.

Figure 2-12a below illustrates normal termination of host-to-HPI access cycle of *TORNADO-PX64xxQ* host PIOX interface, whereas figure 2-12b illustrates termination of host-to-HPI access cycle of *TORNADO-PX64xxQ* host PIOX interface on timeout condition.

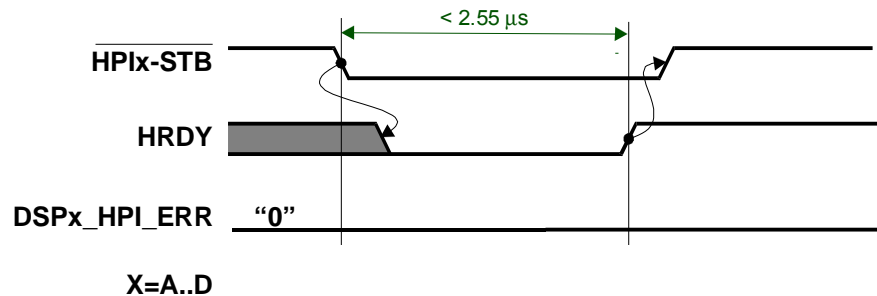


Fig.2-12a. Normal termination of host-to-HPI access cycle of *TORNADO-PX64xxQ* host PIOX interface without timeout condition.

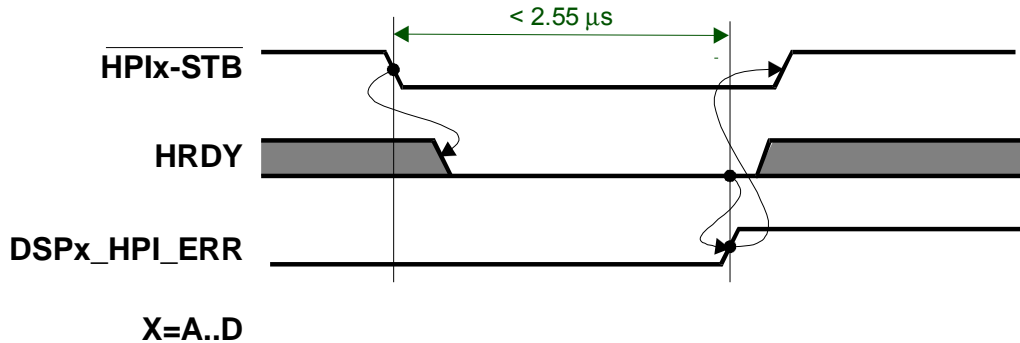


Fig.2-12b. Termination of host-to-HPI access cycle of *TORNADO-PX64xxQ* host PIOX interface on timeout condition.

Processing of DSP-to-host PIOX interrupt requests from on-board TMS320C64xx

TORNADO-PX64xxQ DSP coprocessor DCM allows to generate interrupt request from each on-board TMS320C64xx DSP to host *TORNADO* DSP system/controller via *DSPx_HPI_HINT* (x=A..D) DSP-to-host interrupt request via DSP-x on-chip HPI port.

DSPx_HPI_HINT (x=A..D) DSP-to-host interrupt request can be set by the corresponding on-board TMS320C64xx DSP software by writing of the '1' value to the *HINT* bit of DSP-x on-chip HPIC register (@0x01880000).

CAUTION

Writing of the '0' value to the *HINT* bit of TMS320C64xx DSP on-chip HPIC register (@0x01880000) by on-board TMS320C64xx DSP software has no effect.

Current state of *DSPx_HPI_HINT* (x=A..D) DSP-to-host interrupt request can be read by host via [HOST_INT_STAT_RG](#) read-only host interface control register (refer to [table 2-22](#))) and via HPIC register ([HOST_HPI32_DSPx_HPIC_RG](#), or [HOST_HPI16_DSPx_HPIC_LSW_RG](#) and [HOST_HPI16_DSPx_HPIC_MSW](#) host interface HPI registers) of on-chip HPI port of the corresponding TMS320C64xx DSP-x (refer to subsection [“TMS320C64xx DSP HPI port access areas”](#) earlier in this section for more details).

Active *DSPx_HPI_HINT* (x=A..D) DSP-to-host interrupt request can be cleared by host *TORNADO* DSP software only by writing '1' value to the *HINT* bit of DSP-x on-chip HPIC register.

CAUTION

Writing of the '0' value to the *HINT* bit of TMS320C64xx DSP on-chip HPIC register from host *TORNADO* DSP software has no effect.

Host *DSPx_HPI_HINT* interrupt request can generate active host PIOX interrupt request via any of four *IRQ-n* ($n=0..3$) host PIOX interface interrupt request outputs, which are controlled via [HOST_HIRQn_SEL_RG](#) host interface control registers ($n=0..3$) of *TORNADO-PX64xxQ* DSP coprocessor DCM. Particular *IRQ-n* ($n=0..3$) host PIOX interrupt request output, which will be used to forward *DSPx_HPI_HINT* DSP-to-host interrupt request to host *TORNADO* DSP via host PIOX interface, must be enabled via *HIRQ_EN* bit and the corresponding *DSPx_HPI_HINT* ($x=A..D$) DSP-to-host interrupt request source must be selected via {*HIRQ_SEL-2..0*} bits of the corresponding [HOST_HIRQn_SEL_RG](#) ($n=0..3$) host interface control register (refer to tables [2-23](#) and [2-24](#) for more details).

CAUTION

For more information about *HINT* DSP-to-host interrupt request via TMS320C64xx DSP on-chip HPI port refer to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

Generation of host-to-DSP interrupt request to on-board TMS320C64xx DSP

TORNADO-PX64xxQ DSP coprocessor DCM allows to generate interrupt request from host *TORNADO* DSP software to each particular on-board TMS320C64xx DSP via TMS320C64xx DSP on-chip HPI port, or can generate 'broadcast' interrupt request to all on-board DSP simultaneously.

Host-to-DSP interrupt request to particular on-board DSP- x ($x=A..D$) can be set by host *TORNADO* DSP software by writing of the '1' value to the *DSPINT* bit of on-chip HPIC register ([HOST_HPI32_DSPx_HPIC_RG](#), or [HOST_HPI16_DSPx_HPIC_LSW_RG](#) and [HOST_HPI16_DSPx_HPIC_MSW](#) host interface HPI registers) of on-chip HPI port of the corresponding TMS320C64xx DSP- x (refer to subsection ["TMS320C64xx DSP HPI port access areas"](#) earlier in this section for more details).

CAUTION

Writing of the '0' value to the *DSPINT* bit of TMS320C64xx DSP on-chip HPIC register from host *TORNADO* DSP software has no effect.

Corresponding TMS320C64xx DSP software can either poll status of *DSPINT* bit of on-chip HPIC register (@0x01880000), or, if default DSP on-chip interrupt selection priority selection is not satisfactory, then DSP on-chip high/low interrupt multiplexer registers (@0x019C0000 and @0x019C0004) shall be used to select particular DSP on-chip interrupt request input/priority, which will be used to interrupt the DSP core on the *DSPINT* host-to-DSP interrupt request event

After TMS320C64xx DSP software has recognized active *DSPINT* host-to-DSP interrupt request via *DSPINT* bit of HPIC register (@0x01880000), it must clear *DSPINT* host-to-DSP interrupt request by writing of the '1' value to the *DSPINT* bit of HPIC register (@0x01880000).

CAUTION

Writing of the '0' value to the *DSPINT* bit of TMS320C64xx DSP on-chip HPIC register (@0x01880000) by DSP software has no effect.

CAUTION

For more information about *DSPINT* host-to-DSP interrupt request via TMS320C64xx DSP on-chip HPI port and how to configure TMS320C64xx DSP on-chip high/low interrupt multiplexer registers refer to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

In case user application requires that host *TORNADO* DSP software must generate simultaneous interrupt request to all on-board TMS320C64xx DSP in order to synchronize DSP software of all on-board TMS320C64xx DSP, then [HOST DSP BROADCAST RQ RG](#) write-only host interface control register must be used to generate 'broadcast' request from host *TORNADO* DSP software to all *TORNADO-PX64xxQ* on-board DSP simultaneously. Data written to [HOST DSP BROADCAST RQ RG](#) write-only host interface control register is ignored. In order to detect host 'broadcast' interrupt request, corresponding on-board TMS320C64xx DSP software must configure any of [DSP EXTn INT SEL RG](#) (n=4..7) or [DSP NMI SEL RG](#) IOX control registers to select host 'broadcast' interrupt request as external interrupt request source for the corresponding EXT_INT4..7/NMI DSP external interrupt inputs (refer to [fig.2-3](#) and [table 2-9](#) from section "[TMS320C64xx DSP Environment](#)" earlier in this chapter for more details). If default DSP on-chip interrupt selection priority is not satisfactory, then TMS320C64xx DSP on-chip high/low interrupt multiplexer registers (@0x019C0000 and @0x019C0004) can be also used to select particular DSP on-chip interrupt request input/priority, which will be used to interrupt the DSP core on external host 'broadcast' host-to-DSP interrupt request event.

CAUTION

For more information about how to configure TMS320C64xx DSP on-chip high/low interrupt multiplexer registers refer to original TI TMS320C64xx user's guides, which are supplied in either paper or electronic form together with this manual.

2.5 Emulation Tools for *TORNADO-PX64xxQ DSP Coprocessor DCM*

TORNADO-PX64xxQ DSP coprocessor DCM has been designed to use scan-path emulation technique for on-board TMS320C64xx DSP in order to debug on-board TMS320C64xx DSP environment and software. This delivers non-intrusive debugging of on-board DSP software at full DSP speed.

Connection of external JTAG emulator to *TORNADO-PX64xxQ* on-board TMS320C64xx DSP

Compatible scan-path emulation tools include TI XDS510/XDS560 JTAG emulators and MicroLAB Systems *MIRAGE-510DX/P510D* JTAG emulators, which shall connect to *TORNADO-PX64xxQ* on-board JTAG connector (JP2) via optional external *T/X-JTAG/C1* JTAG converter cable as shown at figure 2-13.

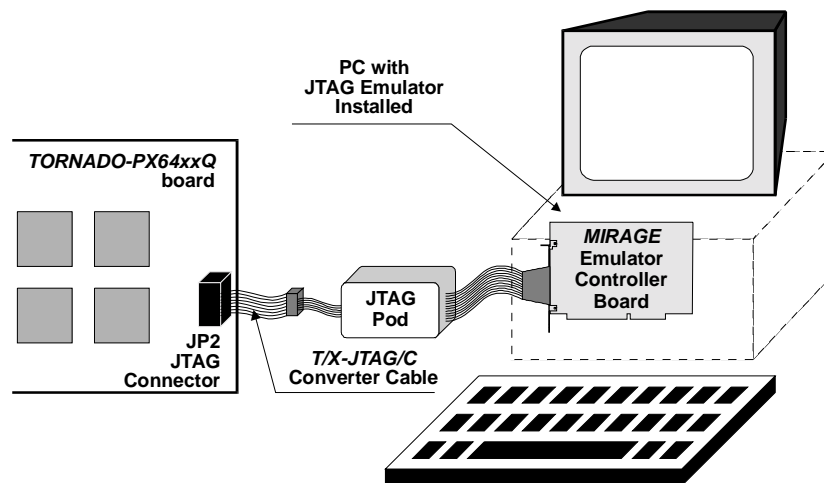


Fig. 2-13. Connection of external JTAG emulator to *TORNADO-PX64xxQ* on-board TMS320C64xx DSP.

External *T/X-JTAG/C1* JTAG converter cable comes standard with *TORNADO-PX64xxQ* DSP coprocessor DCM and is required for connection of *TORNADO-PX64xxQ* on-board DSP to external JTAG emulator due to a very compact design of *TORNADO-PX64xxQ* DSP coprocessor DCM, which provides on-board miniature JTAG 14-pin 2mm connector (JP2) that is not directly plug-in compatible with the industry-standard TI 14-pin 0.1"x0.1" JTAG connector coming standard with all JTAG emulators.

CAUTION

For more details about how to install and connect your JTAG emulator, which is used for debugging of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP environment and software, refer to original user's guide for your JTAG emulator.

On-board JTAG path for connection to external JTAG emulator

TORNADO-PX64xxQ on-board JTAG path for connection to external JTAG emulator, which comprises of on-board JTAG connector (JP2) and JTAG ports of four on-board TMS320C64xx DSP (DSP-A..D), is shown at figure 2-14.

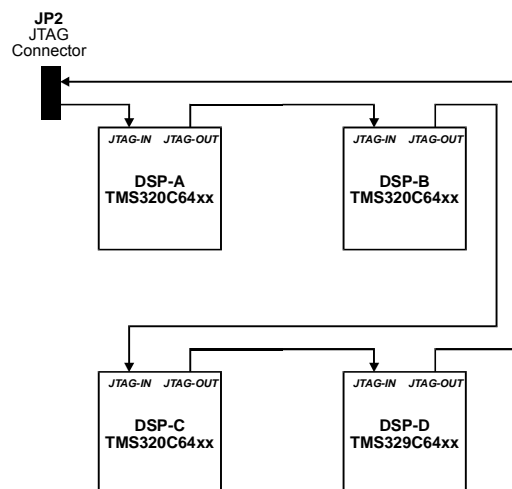


Fig. 2-14. *TORNADO-PX64xxQ* on-board JTAG path for connection to external JTAG emulator.

CAUTION

TORNADO-PX64xxQ on-board JTAG path has been designed with JTAG port of on-board TMS320C64xx DSP-A being the first JTAG port in JTAG path, and JTAG port of on-board DSP-D being the last JTAG port in JTAG path.

CAUTION

TORNADO-PX64xxQ on-board JTAG connector (JP2) provides 3v/5v compatible JTAG interface signals.

CAUTION

TORNADO-PX64xxQ on-board JTAG path supports external JTAG clock frequency (TCK) up to 20 MHz in case *TORNADO-PX64xxQ* DSP coprocessor DCM is the only device in JTAG path.

Maximum external JTAG clock frequency (TCK) can be reduced if either several *TORNADO-PX64xxQ* DSP coprocessor DCM or other JTAG compatible devices are connected into one JTAG path along with *TORNADO-PX64xxQ* DSP coprocessor DCM.

Configuring TI Code Composer Studio TMS320C64xx emulator driver to debug *TORNADO-PX64xxQ* on-board DSP

Industry standard TI 'C6000 Code Composer Studio (CCS) debug tools v.2.1 or later (as the part of TI 'C6000 Code Composer Studio tools) are required in order to debug *TORNADO-PX64xxQ* on-board DSP software via external JTAG emulator. TI CCS emulator driver used must support TMS320C64xx DSP.

Note, that TI CCS TMS320C64xx emulator driver can be configured to debug any combination of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP:

- Anyone of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP can be included as the only active JTAG device into on-board JTAG path with JTAG port of other unused on-board TMS320C64xx DSP being put in 'JTAG BYPASS' mode
- Any combination of either two or three *TORNADO-PX64xxQ* on-board TMS320C64xx DSP can be included as the only active JTAG devices into on-board JTAG path with JTAG port of other unused on-board TMS320C64xx DSP being put in 'JTAG BYPASS' mode
- All *TORNADO-PX64xxQ* on-board TMS320C64xx DSP can be included as active JTAG devices into on-board JTAG path.

CAUTION

When including particular *TORNADO-PX64xxQ* TMS320C64xx DSP as active JTAG device into on-board JTAG path use default 'TMS320C64xxx' setting in 'JTAG configuration' folder of TI CCS TMS320C64xx emulator driver setup dialog via CCS SETUP utility.

When including particular *TORNADO-PX64xxQ* TMS320C64xx DSP as not active JTAG device into on-board JTAG path use 'BYPASS' setting with command register length equal to the 38 value in 'JTAG configuration' folder of TI CCS TMS320C64xx emulator driver dialog via CCS SETUP utility.

CAUTION

Each of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP, which are included as active JTAG device(s) into on-board JTAG path, shall be released from the reset state prior starting TI CCS TMS320C64xx debugger (refer to section ["Host PIOX Interface"](#) and description for [HOST_CNTR1_RG](#) host interface register earlier in this chapter for more details).

Although not required, but it is recommended that those of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP, which are included as not active JTAG device(s) into on-board JTAG path, shall be held in the reset state prior starting TI CCS TMS320C64xx debugger (refer to section ["Host PIOX Interface"](#) and description for [HOST_CNTR1_RG](#) host interface register earlier in this chapter for more details).

CAUTION

It is recommended that provided either *PX64XXQ_SDRAM4M.GEL* or *PX64XXQ_SDRAM16M.GEL* CCS GEL-files (which one corresponds to on-board SDRAM capacity) is be specified as start-up CCS GEL-file in 'Start-up GEL' folder of TI CCS TMS320C64xx emulator driver dialog via CCS SETUP utility for each of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP, which are included as active JTAG device(s) into on-board JTAG path (refer to [Appendix 'D'](#) in this manual for more details).

CAUTION

For more information about TI 'C6000 CCS debug tools refer to original TI user's guides for TI 'C6000 CCS compiler/debug tools, which are supplied with TI 'C6000 CCS tools.

Chapter 3. Installation and Configuration

This chapter includes instructions for installation and configuration of *TORNADO-PX64xxQ* DSP coprocessor DCM.

3.1 Installation onto host *TORNADO* DSP System/Controller Mainboard

TORNADO-PX64xxQ DSP coprocessor DCM must be installed as standard PIOX DCM onto host *TORNADO* DSP system/controller mainboard.

For installation of *TORNADO-PX64xxQ* DCM into PIOX DCM site of *TORNADO* DSP system/controller follow the recommendations below:

1. Switch off the power of host PC or of host *TORNADO* DSP controller.
2. Remove *TORNADO* mainboard from PC slot.
3. Ensure that two *TORNADO* on-board spacers for mounting PIOX DCM are installed into the corresponding holes on *TORNADO* mainboard (fig.3-1). If spacers are not installed, then install spacers, which are enclosed with *TORNADO-PX64xxQ* DSP coprocessor DCM.
4. Pick-up *TORNADO-PX64xxQ* DSP coprocessor DCM and orient it parallel to *TORNADO* mainboard above the PIOX DCM area. Safely plug-in on-board JP1 host PIOX interface connector of *TORNADO-PX64xxQ* DSP coprocessor DCM into the corresponding PIOX DCM site header of host *TORNADO* mainboard. In case host *TORNADO* mainboard provides on-board 16-bit PIOX-16 interface DCM site, then you have to plug 16-bit PIOX-16 sub-connector of *TORNADO-PX64xxQ* on-board PIOX interface connector (JP1) into the PIOX-16 DCM site header at host *TORNADO* mainboard (fig.3-1a). In case host *TORNADO* mainboard provides on-board 32-bit PIOX-32 interface DCM site, then you have to plug both sub-connectors of *TORNADO-PX64xxQ* on-board PIOX interface connector (JP1) into the PIOX-32 DCM site headers at host *TORNADO* mainboard (fig.3-1b).

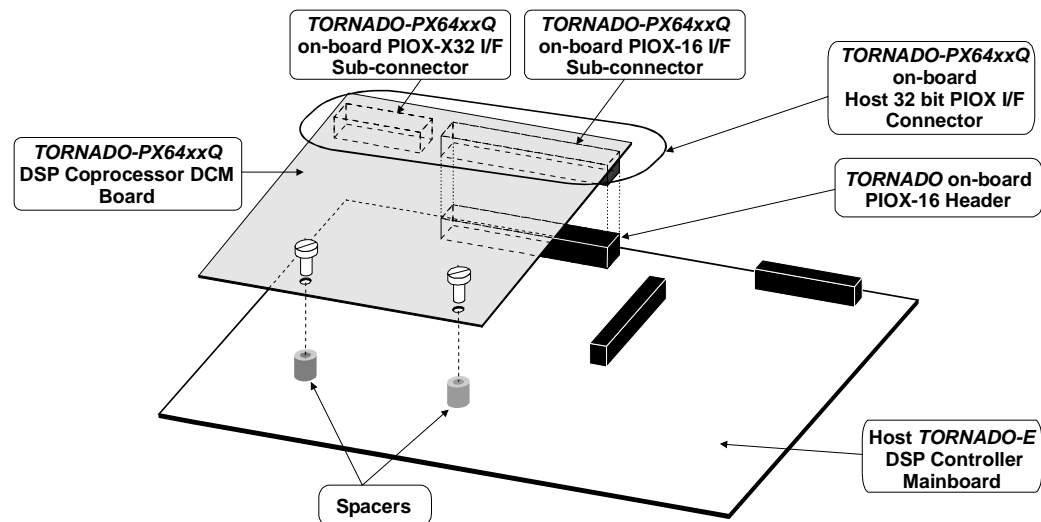


Fig. 3-1a. Installation of *TORNADO-PX64xxQ* DCM into 16-bit PIOX-16 DCM site of host *TORNADO* DSP system/controller.

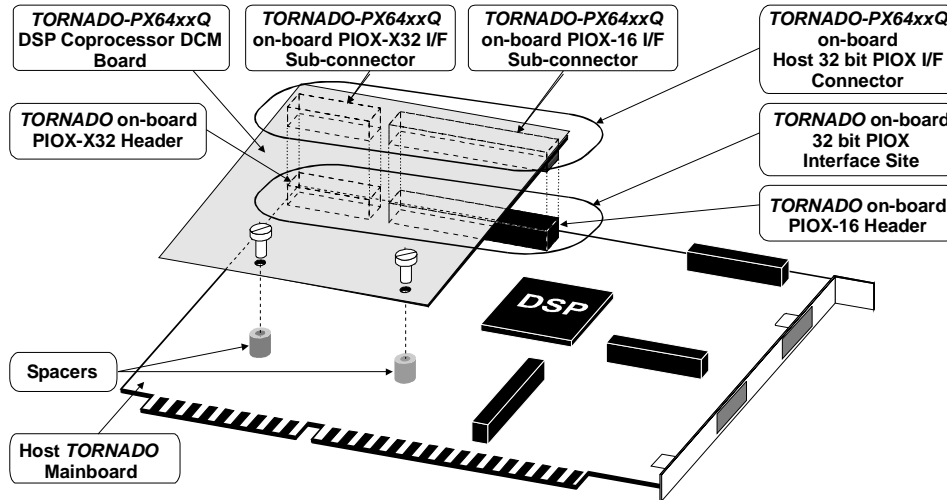


Fig. 3-1b. Installation of *TORNADO-PX64xxQ* DCM into 32-bit PIOX-32 DCM site of host *TORNADO* DSP system.

5. Screw in *TORNADO-PX64xxQ* DSP coprocessor DCM to the spacers at host *TORNADO* mainboard.
6. If real-time AD/DA/DIO is required by user application, connect optional either of *T/SU-X1*, *T/SU-X2*, or *T/SU-X3* external SIOX rev.B DCM mini-extender(s) to *TORNADO-PX64xxQ* DSP coprocessor DCM via on-board JP3..6 MXSIOX interface connectors (refer to section [“Serial I/O Expansion Interface \(MXSIOX\)”](#) and [Appendix ‘C’](#) of this manual for more details). Install SIOX rev.B AD/DA/DIO DCM onto *T/SU-X1*, *T/SU-X2*, or *T/SU-X3* external SIOX rev.B mini-extenders and configure SIOX rev.B DCM in accordance with its manual. Configure *TORNADO-PX64xxQ* on-board SW1..2 switches to meet serial clock configuration for connected SIOX rev.B DCM (refer to section [“Serial I/O Expansion Interface \(MXSIOX\)”](#) and [Appendix ‘C’](#) of this manual for more details).
7. If board-to-board communication with either another *TORNADO-PX64xxQ* DSP coprocessor DCM or compatible board is required by user application, connect optional *T/U-XSLC1* external serial link converter(s) to *TORNADO-PX64xxQ* DSP coprocessor DCM via on-board JP3..6 MXSIOX interface connectors (refer to section [“TMS320C64xx DSP Environment”](#), [fig.2-6](#), [fig.2-7](#), and [Appendix ‘C’](#) of this manual for more details). Connect on-board JP2 and/or JP3 connectors at *T/U-XSLC1* external serial link converter board(s) to external serial links connectors of another *TORNADO* boards, which are integrated into multi-board multi-DSP system along with this *TORNADO-PX64xxQ* DSP coprocessor DCM.
8. In case *TORNADO* PC plug-in DSP system is used for installation of *TORNADO-PX64xxQ* DSP coprocessor DCM, then install *TORNADO* mainboard into PC chassis slot and screw it to the rear panel of PC.
9. In case *TORNADO* PC plug-in DSP system is used for installation of *TORNADO-PX64xxQ* DCM and in case optional *T/SU-X1*, *T/SU-X2*, or *T/SU-X3* external SIOX rev.B mini-extender(s) are

connected to MXSIOX interface connector(s) at *TORNADO-PX64xxQ* DSP coprocessor DCM, then install and screw mounting bracket of *T/SU-X1*, *T/SU-X2*, or *T/SU-X3* external SIOX rev.B mini-extender(s) to the rear panel of PC.

10. If optional *T/SU-X1*, *T/SU-X2*, or *T/SU-X3* external SIOX rev.B mini-extender(s) with installed SIOX rev.B DCM are connected to *TORNADO-PX64xxQ* DCM, then connect external I/O cables to installed SIOX rev.B DCM.
11. Switch on power of host PC or of host *TORNADO* DSP controller.

	SW1-3	Common CLKX/CLKR serial clock enable for transmitter and receiver of SIO-0 serial port of MXSIOX-B interface connector (JP3).	Section 2.3
	SW1-4	Common CLKX/CLKR serial clock enable for transmitter and receiver of SIO-1 serial port of MXSIOX-B interface connector (JP5).	Section 2.3
SW2	SW2-1	Common CLKX/CLKR serial clock enable for transmitter and receiver of SIO-0 serial port of MXSIOX-C interface connector (JP5).	Section 2.3
	SW2-2	Common CLKX/CLKR serial clock enable for transmitter and receiver of SIO-1 serial port of MXSIOX-C interface connector (JP5).	Section 2.3
	SW2-3	Common CLKX/CLKR serial clock enable for transmitter and receiver of SIO-0 serial port of MXSIOX-D interface connector (JP6).	Section 2.3
	SW2-4	Common CLKX/CLKR serial clock enable for transmitter and receiver of SIO-1 serial port of MXSIOX-D interface connector (JP6).	Section 2.3

A.2 On-board Connectors

Table A-2 contains the list of *TORNADO-PX64xxQ* on-board connectors.

Table A-2. On-board connectors for *TORNADO-PX64xxQ* DSP coprocessor DCM.

connector ID	Description	Reference information
<i>JP1</i>	Host PIOX interface site male header. Pinout of on-board host PIOX connector is presented in Appendix B of this manual and in the user's guide of host <i>TORNADO</i> DSP system/controller, which is used for installation of <i>TORNADO-PX64xxQ</i> DSP coprocessor DCM.	Section 2.4 Appendix B
<i>JP2</i>	JTAG male mini-header for connection to external TI XDS or MicroLAB Systems <i>MIRAGE</i> JTAG emulator. External optional <i>T/X-JTAG/C1</i> JTAG converter cable is required to connect <i>TORNADO-PX64xxQ</i> JTAG mini-header to external JTAG emulator. <i>T/X-JTAG/C1</i> JTAG converter cable provides JTAG connector that meets TI connector specifications for connection to JTAG emulators, which is used for debugging of on-board DSP environment and software.	Section 2.5
<i>JP3</i>	MXSIOX-A interface connector for connection to optional external <i>T/SU-X1</i> , <i>T/SU-X2</i> , <i>T/SU-X3</i> external SIOX rev.B mini-extendors or <i>T/X-XSL1</i> serial link converter to on-board TMS320C64xx DSP-A.	Section 2.3 Appendix C
<i>JP4</i>	MXSIOX-B interface connector for connection to optional external <i>T/SU-X1</i> , <i>T/SU-X2</i> , <i>T/SU-X3</i> external SIOX rev.B mini-extendors or <i>T/X-XSL1</i> serial link converter to on-board TMS320C64xx DSP-B.	Section 2.3 Appendix C
<i>JP5</i>	MXSIOX-C interface connector for connection to optional external <i>T/SU-X1</i> , <i>T/SU-X2</i> , <i>T/SU-X3</i> external SIOX rev.B mini-extendors or <i>T/X-XSL1</i> serial link converter to on-board TMS320C64xx DSP-C.	Section 2.3 Appendix C
<i>JP6</i>	MXSIOX-D interface connector for connection to optional external <i>T/SU-X1</i> , <i>T/SU-X2</i> , <i>T/SU-X3</i> external SIOX rev.B mini-extendors or <i>T/X-XSL1</i> serial link converter to on-board TMS320C64xx DSP-D.	Section 2.3 Appendix C

A.3 On-board LED

Table A-3 contains the list of *TORNADO-PX64xxQ* on-board LED indicators.

Table A-3. On-board LED indicators for *TORNADO-PX64xxQ* DCM.

LED ID	LED color	function description
<i>VD1</i>	<i>RED</i>	Reset indicator for on-board TMS320C64xx DSP-A.
<i>VD2</i>	<i>RED</i>	Reset indicator for on-board TMS320C64xx DSP-B.
<i>VD3</i>	<i>RED</i>	Reset indicator for on-board TMS320C64xx DSP-C.

<i>VD4</i>	<i>RED</i>	Reset indicator for on-board TMS320C64xx DSP-D.
<i>VD5</i>	<i>GREEN</i>	Host power indicator.

Appendix B. PIOX Interface Site

This appendix contains information about *TORNADO* 16-bit PIOX-16 and 32-bit PIOX-32 DCM site interface specifications.

CAUTION

Provided description of 16-bit PIOX-16 and 32-bit PIOX-32 DCM site interfaces is general for all *TORNADO* DSP systems/controllers, whereas different *TORNADO* DSP systems/controllers may differ in the number of interrupts requests via on-board PIOX DCM site interface and in the timer/IO pins specifications.

For more details refer to the user's guide for your particular *TORNADO* DSP system/controller.

B.1 General Description

Architecture of *TORNADO* DSP systems/controllers allows expansion of on-board I/O resources via on-board parallel I/O expansion DCM site (PIOX), which is designed to carry compatible PIOX DCM.

TORNADO on-board PIOX DCM site can appear as either 16-bit PIOX-16 DCM site (fig.B-1a) or 32-bit PIOX-32 DCM site (fig.B-1b).

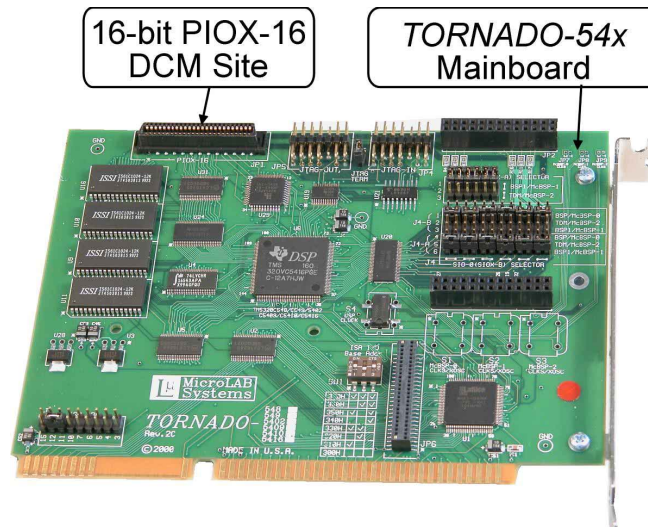


Fig.B-1a. 16-bit PIOX-16 DCM site at *TORNADO*-54x DSP system board.

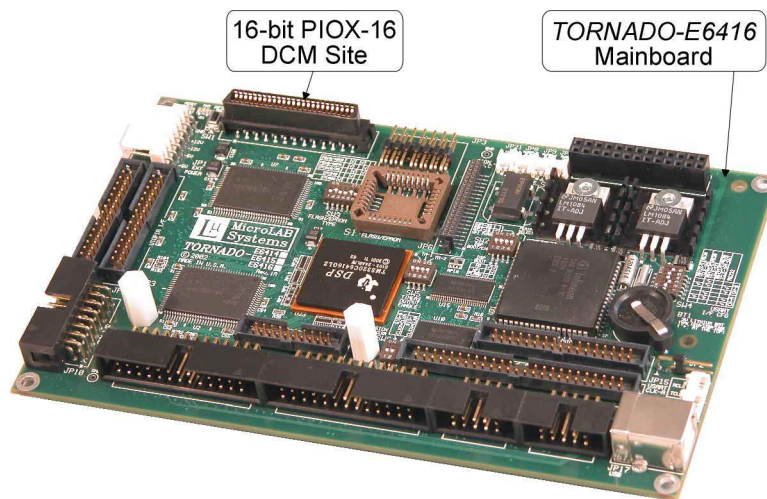


Fig.B-1b. 16-bit PIOX-16 DCM site at *TORNADO-E6416* stand-alone DSP controller board.

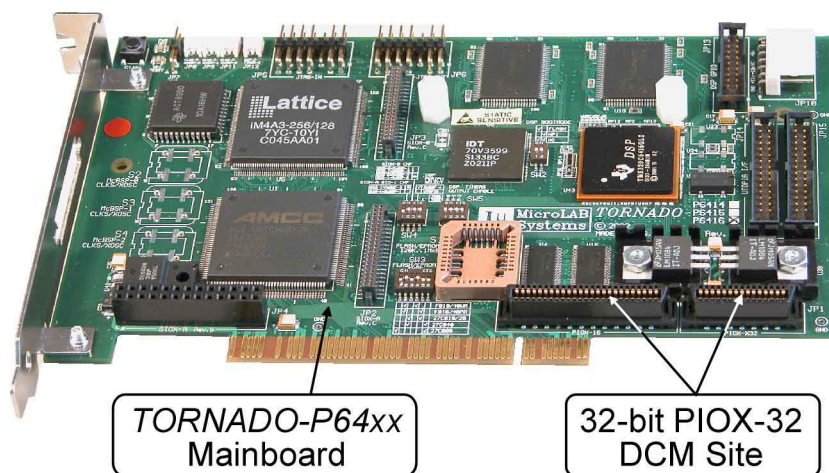


Fig.B-1c. 32-bit PIOX-32 DCM site at *TORNADO-P6416* DSP system board.

16-bit PIOX-16 DCM site is provided as the only available PIOX DCM site with *TORNADO* DSP systems with 16-bit fixed-point DSP (as *TORNADO-54x*) for PC plug-in applications and with all *TORNADO-Exxxx* stand-alone DSP controllers with different on-board DSP (*TORNADO-E3x/E54x/E6x/E64xx*).

32-bit PIOX-16 DCM site is an upward compatible 32-bit expansion of 16-bit PIOX-16 DCM site and is available with all *TORNADO* DSP systems for PC plug-in applications with 32-bit fixed- and floating-point TMS320C3x and TMS320C6000 DSP (*TORNADO-3x/P3x/P6x/P64xx*).

Note, that 16-bit PIOX-16 DCM site is a subset of 32-bit PIOX-32 DCM site, and therefore, it is also available with all *TORNADO* DSP systems/controllers.

CAUTION

PIOX DCM boards with host 16-bit PIOX-16 interface can plug into both 16-bit PIOX-16 DCM site and 16-bit PIOX-16 subset of 32-bit PIOX-32 DCM site of host *TORNADO* DSP systems/controllers, and are therefore compatible with all *TORNADO* DSP systems/controllers.

Instead, PIOX DCM boards with host 32-bit PIOX-32 interface can generally plug only into 32-bit PIOX-32 DCM site of *TORNADO* DSP systems, and are therefore not compatible with all host *TORNADO* DSP systems/controllers.

However, some of PIOX DCM boards with universal host 16-bit/32-bit PIOX DCM site interface (as *TORNADO-PX64xxQ* DSP coprocessor DCM, *TORNADO-PX/DDC4G* quad DRR coprocessor DCM, etc) provide on-board automatic hardware configuration in accordance with detected type of host PIOX DCM site interface and are therefore compatible with both 16-bit PIOX-16 and 32-bit PIOX-32 DCM sites of host *TORNADO* DSP systems/controllers.

Refer to the user's guide for your particular used PIOX DCM boards for more details about compatibility with 16-bit PIOX-16 and 32-bit PIOX-32 DCM site interfaces of host *TORNADO* DSP systems/controllers.

Figure B-2a demonstrates installation of different DCM with host PIOX-16 and PIOX-32 interfaces into host PIOX DCM site of host *TORNADO* DSP systems/controllers.

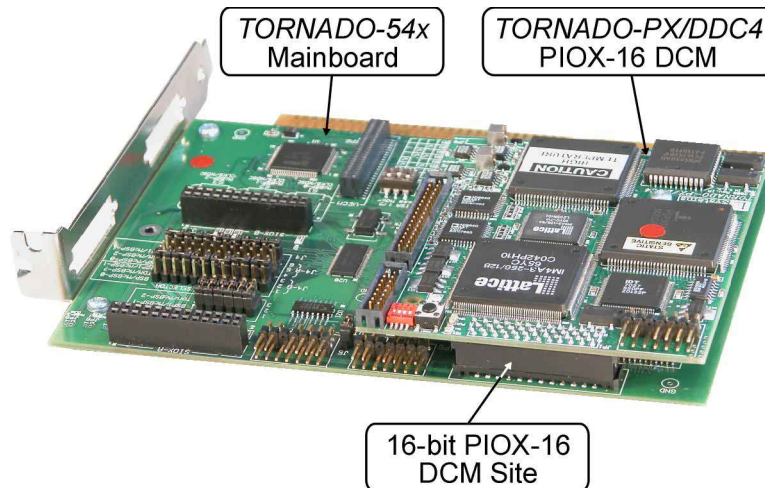


Fig.B-2a. *TORNADO-54x* DSP system board with on-board 16-bit PIOX-16 DCM site and PIOX-16 DCM (*TORNADO-PX/DDC4*) installed.

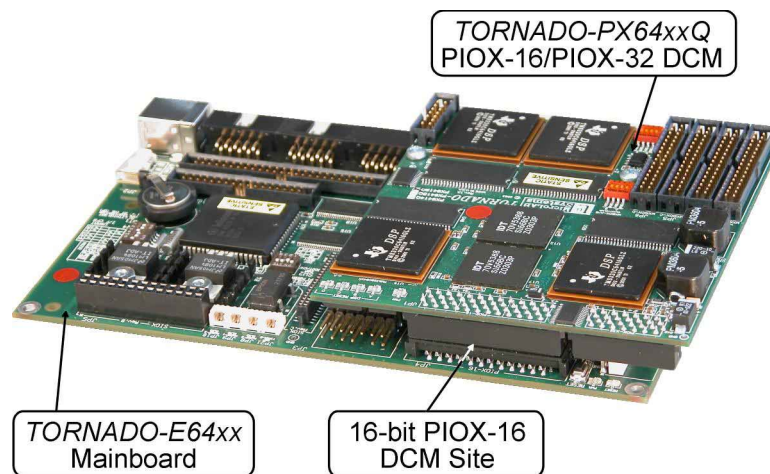


Fig.B-2b. TORNADO-E64xx DSP controller board with on-board 16-bit PIOX-16 DCM site and universal PIOX-16/PIOX-32 DCM (TORNADO-PX64xxQ) installed.

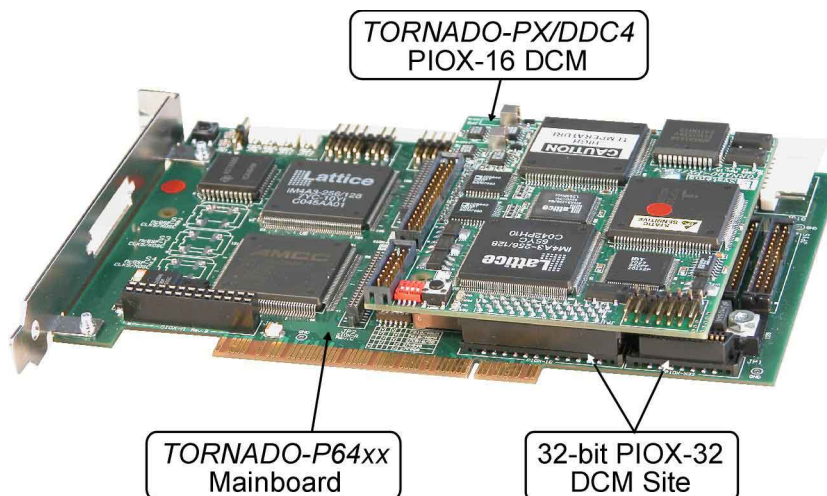


Fig.B-2c. TORNADO-P64xx DSP system board with on-board 32-bit PIOX-32 DCM site and PIOX-16 DCM (TORNADO-PX/DDC4) installed.

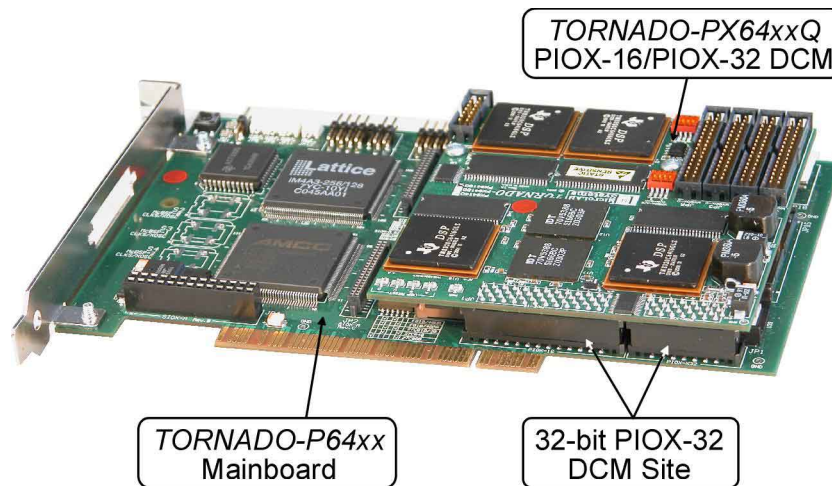


Fig.B-2c. *TORNADO-P64xx* DSP system board with on-board 32-bit PIOX-32 DCM site and universal PIOX-16/PIOX-32 DCM (*TORNADO-PX64xxQ*) installed.

B.2 PIOX DCM Site Interface Connectors and Signals

16-bit PIOX-16 DCM site interface at *TORNADO* DSP systems/controllers comprises of signals for 16-bit data bus, 16-bit address bus, data transfer strobes and acknowledge signals, two timer/IO signals, 2..4 interrupt request inputs, reset control, and $\pm 5V/\pm 12V$ power supplies. PIOX-16 DCM site interface supports 16-bit data transfer cycles only.

32-bit PIOX-32 DCM site interface at *TORNADO* DSP systems/controllers comprises of signals for 32-bit data bus, 20-bit address bus, data transfer strobes and acknowledge signals, data format control, two timer/IO signals, 2..4 interrupt request inputs, reset control, and $\pm 5V/\pm 12V$ power supplies. PIOX-32 DCM site interface supports 8-bit, 16-bit and 32-bit data transfer cycles.

Both PIOX-16 and PIOX-32 DCM site interfaces appears as the corresponding sub-area inside *TORNADO* on-board DSP memory map or I/O map.

PIOX DCM site interface connectors and signals description

Basic PIOX-16 16-bit interface connector p/n is DHB-RB50-S13NN, which is a high-density 50-pin DHB-series dual-row female connector with 0.05" pin pitch from Fujikura-DDK Ltd (www.ddkconnectors.com). Compatible PIOX-16 plug is DHB-PK50-S13NN, which is available upon request from MicroLAB Systems for design custom 16-bit PIOX-16 DCM.

PIOX-16 DCM site interface connector is a high-density DDK 50-pin DHB-series dual-row female connector with 0.05" pin pitch. Compatible PIOX-16 plugs for customer designed DCM are available upon request from MicroLAB Systems.

PIOX-X32 add-on 32-bit interface connector p/n is DHB-RB30-S13NN, which is a high-density 30-pin DHB-series dual-row female connector with 0.05" pin pitch from Fujikura-DDK Ltd (www.ddkconnectors.com).

Compatible PIOX-X32 plug is DHB-PK30-S13NN, which is available upon request from MicroLAB Systems for design custom 32-bit PIOX DCM.

Pinout for PIOX-16 and PIOX-32 DCM site interface connectors are presented at fig B-3a and B-3b correspondingly, whereas signal description is presented in table B-1.

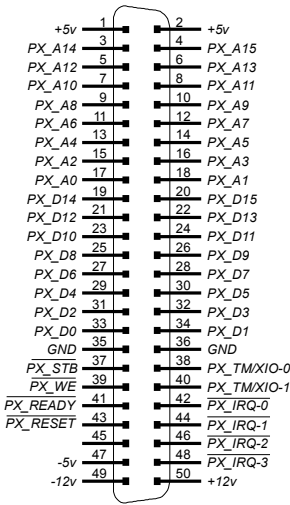


Fig.B-3a. PIOX-16 DCM site interface connector pinout (top view).

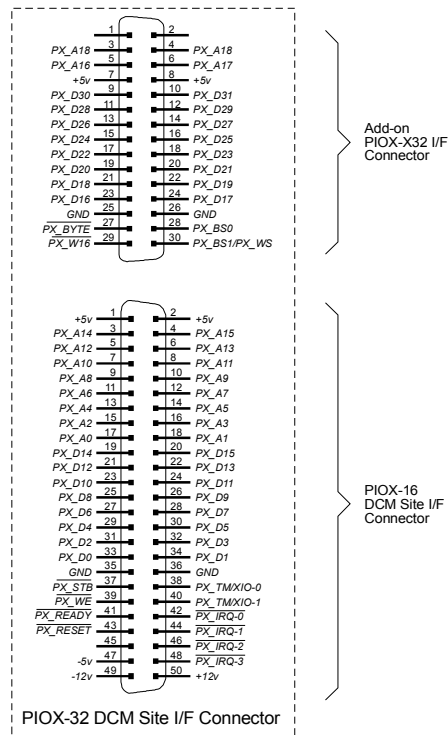


Fig.B-3b. PIOX-32 DCM site interface connector pinout (top view).

Table B-1a. Signal description for 16-bit PIOX-16 DCM site interface connector (common for both PIOX-16 and PIOX-32 DCM site interfaces).

Signal name	signal type	Description
$PX_A[0..15]$	O	16-bit PIOX address bus.
$PX_D[0..15]$	I/O	16-bit PIOX data bus.
$\overline{PX_STB}$	O	Active low PIOX data transfer strobe, which is generated by <i>TORNADO</i> on-board I/O controller.
$\overline{PX_WE}$	O	Active low PIOX write enable signal, which is generated by <i>TORNADO</i> on-board I/O controller.
$\overline{PX_READY}$	I	Active low pulled-up PIOX data ready acknowledge input signal, which must be generated by installed PIOX DCM in order to terminate current PIOX data transfer cycle in accordance with the timing requirements for PIOX DCM site interface. This input has pull-up resistor.

$PX_TM/XIO-0$ $PX_TM/XIO-1$	I/O/Z	These signals may vary upon particular <i>TORNADO</i> DSP board type, but most typically they are DSP on-chip timer/I/O pins, which are connected to the corresponding DSP on-chip timer I/O pins. Most typically, each of these pins can be used as either timer input, or timer output, or general purpose I/O pin. Refer to the user's guide for your particular <i>TORNADO</i> DSP system/controller for more details about these pins.
$\overline{PX_RESET}$	O	Active low reset signal for the PIOX DCM site. Some <i>TORNADO</i> boards (for example <i>TORNADO-3x</i> boards) wires this signal directly to the DSP reset signal, and reset for PIOX DCM is asserted simultaneously with <i>TORNADO</i> on-board DSP reset. However, some <i>TORNADO</i> boards (for example <i>TORNADO-54x/6x</i> etc. boards) feature dedicated PIOX site reset signal, which is controlled by <i>TORNADO</i> on-board DSP for better synchronization between the DSP software and PIOX DCM operation.
$\overline{PX_IRQ-0}$, $\overline{PX_IRQ-1}$ $\overline{PX_IRQ-2}$ $\overline{PX_IRQ-3}$	I	Active low pulled-up interrupt request inputs from installed PIOX DCM to <i>TORNADO</i> on-board DSP. All <i>TORNADO</i> DSP systems/controller provide at least two of those PIOX interrupt request inputs, however the number of these signals and their particular on-board routing may vary upon particular <i>TORNADO</i> board type. Refer to the user's guide for your particular <i>TORNADO</i> DSP system/controller for more details about these pins.
GND		Ground.
+5v		+5v power (from host PC interface or external power connector).
+12v		+12v power (from host PC interface or external power connector).
-5v		-5v power (from host PC interface or external power connector, or on-board voltage regulator sourced from -12v on-board power). Refer to the user's guide for your particular <i>TORNADO</i> DSP system/controller for more details about this power supply.
-12v		-12v power (from host PC interface or external power connector).

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
2. All logic I/O signal levels and load currents correspond to that for 3v/5v TTL logic.

Table B-1b. Signal description for 32-bit add-on PIOX-X32 interface connector of PIOX-32 DCM site interface.

Signal name	signal type	Description
$PX_A[16..20]$	O	Extended PIOX-32 address bus. Particular number or extended PIOX-32 address bits may vary upon particular <i>TORNADO</i> board type. Refer to the user's guide for your particular <i>TORNADO</i> DSP system for more details about number of PIOX-32 extended address pins.
$PX_D[16..31]$	I/O	Extended PIOX-32 data bus.

$\overline{PX_BYTE}$	O	Active low 8-bit (byte) data transfer cycle indicator. Byte selection signals $PX_BS0/BS1$ define actual byte #0..#3 (byte #0 is LSB) inside 32-bit PIOX-32 data word, which will be selected during PIOX data transfer cycle.
$\overline{PX_W16}$	O	Active low 16-bit (halfword) data transfer cycle selector. 16-bit halfword selection signal PX_WS define actual 16-bit halfword #0/#1 (halfword #0 is LSW) inside 32-bit PIOX-32 data word, which will be selected during PIOX data transfer cycle.
PX_BS0	O	Least significant bit of byte selection signals (PX_BS0 , PX_BS1) for selection of particular byte during 8-bit (byte) data transfer cycle.
PX_BS1/PX_WS	O	Most significant bit of byte selection signals (PX_BS0 , PX_BS1) for selection of particular byte during 8-bit (byte) data transfer cycle, and selector of particular 16-bit halfword selection signal (WS) for 16-bit data transfer cycle.
GND	-	Ground.
+5v	-	+5v power (from host PC interface or external power connector).

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
2. All logic I/O signal levels and load currents correspond to that for 3v/5v TTL logic.

PIOX DCM site interface signal levels

Signal levels for PIOX-16/PIOX-32 DCM site interface signals correspond to that for the 3v/5v CMOS/TTL signals with $I_{OL}=2\text{ma}$ and $I_{OH}=-0.3\text{ma}$ load currents.

CAUTION

Some *TORNADO* boards with TMS320C30/C31/C32/C542 DSP (*TORNADO-30/31/32L/542L*) provide PIOX DCM site interface signal levels compatible with that for 5v CMOS/TTL only, whereas other *TORNADO* boards with TMS320VC33/VC54xx/C6xxx DSP (*TORNADO-33/54xx/6x/P33/P6x/P64xxE33/E6x/E64xx*) provide 3v/5v PIOX DCM site interface signal levels, which are compatible with both 3V TLL and standard 5v TTL.

Refer to documentation for your particular *TORNADO* DSP system/controller for more information about PIOX DCM site interface signal levels.

timing diagram for PIOX data transmission cycle

Figure B-4 presents timing diagram for typical PIOX data transmission cycle for *TORNADO-54x* DSP system. This data transfer timing is known as the industry standard MOTOROLA mode and assumes usage of data strobe signal and write enable signal.

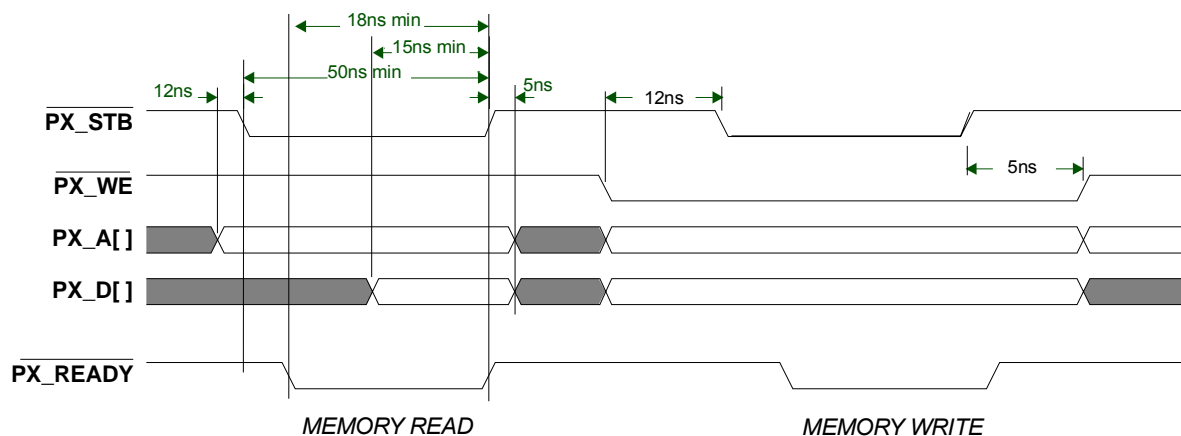


Fig.B-4. Timing diagram of PIOX-16 data transfer for *TORNADO-54x* DSP system.

CAUTION

Although different *TORNADO* DSP systems/controllers provide similar timing for PIOX data access cycles, however different values for specific timing parameters may apply.

Refer to documentation for your particular *TORNADO* DSP system/controller for more information about PIOX timing specifications.

B.3 Physical Dimensions for PIOX-16/PIOX-32 DCM

Physical dimensions for PIOX-16 and PIOX-32 DCM are presented at figure B-5. This information is intended for those customers, who need to design custom PIOX DCM.

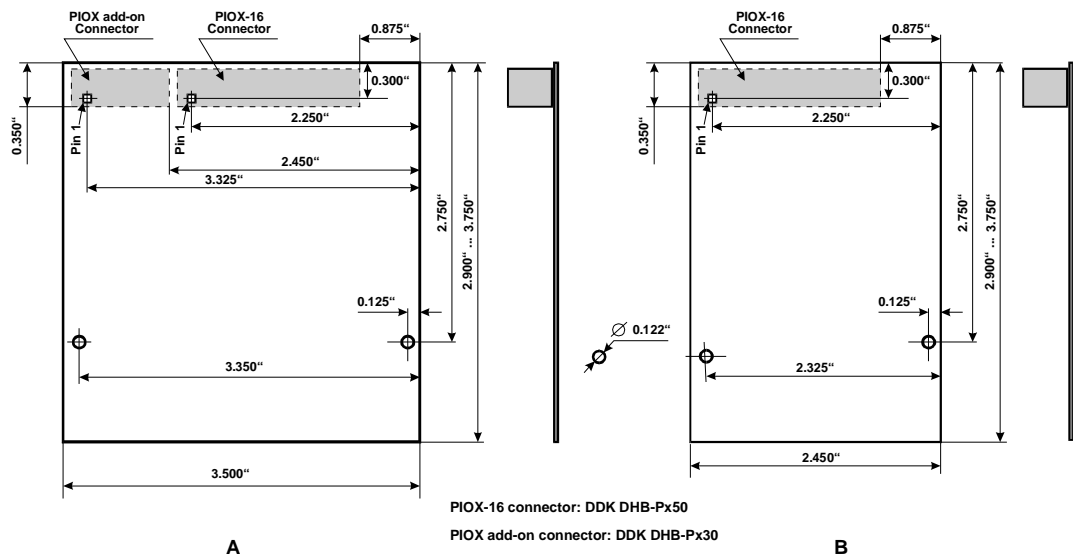


Fig.B-5. Physical dimensions for PIOX-32 (A) and PIOX-16 (B) DCM.

Appendix C. *T/SU-X1 SIOX rev.B Mini-Extender Kit*

This appendix contains description for *T/SU-X1* external SIOX rev.B mini-extender kit, which can be used to connect external SIOX rev.B AD/DA/DIO and application specific DCM to *TORNADO* DSP controllers and coprocessors, which provide on-board compatible connector for connection to external *T/SU-X1* SIOX rev.B mini-extendors.

C.1 General Description

T/SU-X1 SIOX rev.B mini-extender kit is normally provided as dual SIOX rev.B mini-extender kit (fig.C-1), which comprises of the following components:

- two identical *T/SU-X1* SIOX rev.B mini-extender carrier boards
- PC chassis mounting bracket
- two *T/SU-X1/XC* 10" (0.25m) long connection cables.

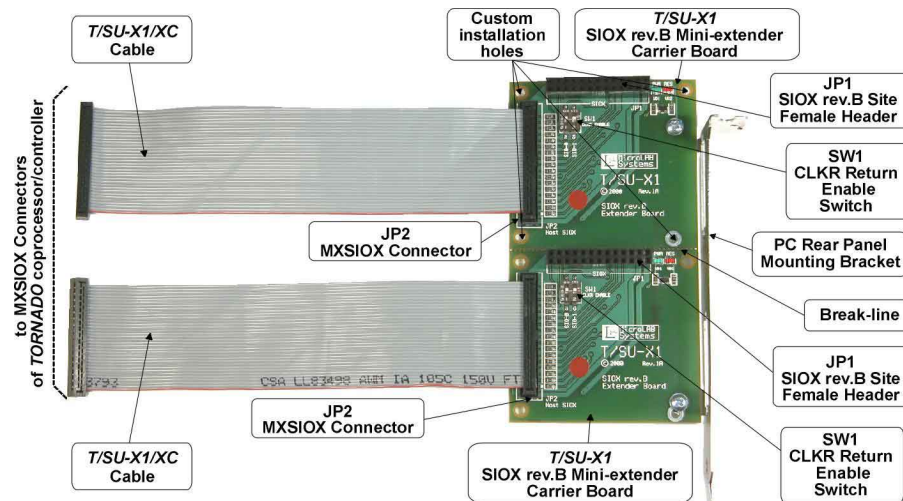


Fig.C-1. Dual *T/SU-X1* SIOX rev.B mini-extender with mounting bracket and connection cables.

Each *T/SU-X1* SIOX rev.B mini-extender carrier board provides on-board site for one full-size SIOX rev.B DCM (fig.C-2), which can be either fixed to the *T/SU-X1* carrier board via optional spacers, or screwed to the mounting bracket.

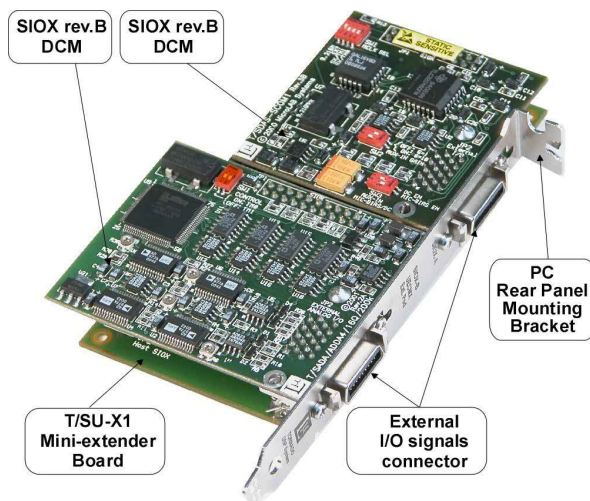


Fig.C-2. Dual *T/SU-X1* SIOX rev.B mini-extender with two installed SIOX rev.B DCM.

connection of *T/SU-X1* SIOX rev.B mini-extender to host *TORNADO* DSP controllers and coprocessors

T/SU-X1 SIOX rev.B mini-extender connects to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* 10" (0.25m) long connection cable (fog.C-3), which connects to the MXSIOX connectors on the *T/SU-X1* SIOX rev.B mini-extender on one side and to with the corresponding MXSIOX matching connector host *TORNADO* DSP controller/coprocessor.

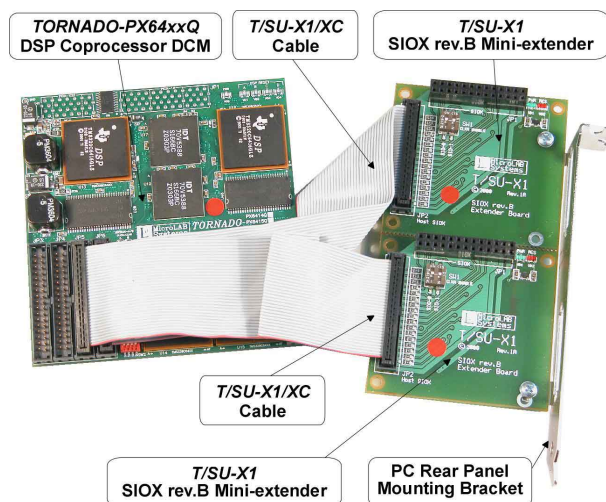


Fig.C-3. Connection of dual *T/SU-X1* SIOX rev.B mini-extender to *TORNADO-PX64xxQ* DSP coprocessor PIOX DCM.

installation

Dual *T/SU-X1 SIOX rev.B* mini-extender can either mount at the rear panel of PC using installed mounting bracket, or can be hand-broken into two identical *T/SU-X1 SIOX rev.B* mini-extenders using on-board perforated broke line (fig.C-1).

Single *T/SU-X1 SIOX rev.B* mini-extender, which appears as the broken half of dual *T/SU-X1 SIOX rev.B* mini-extender, can be installed into the embedded custom chassis environment.

physical dimensions

Figure C-4 provides physical dimensions for single *T/SU-X1 SIOX rev.B* mini-extender and positions for all installation holes and connectors.

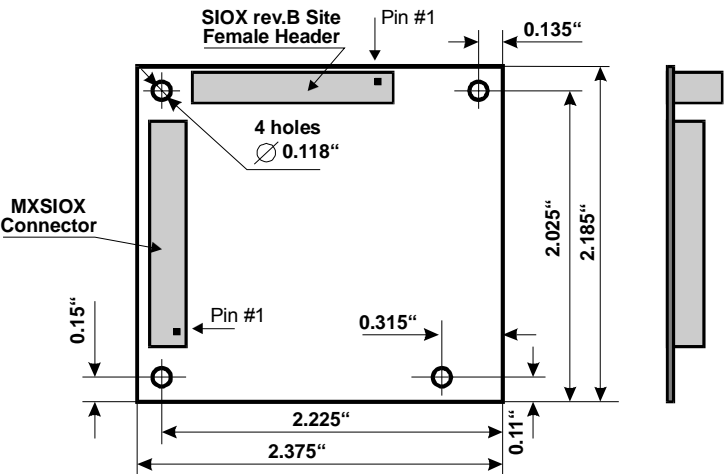


Fig.C-4. Physical dimensions of *T/SU-X1 SIOX rev.B* mini-extender.

C.2 Technical Specifications

The following are technical specifications for *T/SU-X1 SIOX rev.B* mini-extenders.

<u>Parameter description</u>	<u>parameter value</u>
number of SIO ports	2
number of TM/XIO I/O lines	2
number of external interrupt request inputs (<i>XIRQ</i>)	2
number of SIOX reset signals (<i>RESET</i>)	1

maximum serial clock frequency for transmitter/receiver of SIO ports	50 MHz
power supply outputs	$\pm 5\text{v}$, $\pm 12\text{v}$
optional features	LED indicators for power and SIOX reset control CLKR0/CLKR1 serial receiver clock enable switches
Dimensions	2.16"x2.36" (55x60 mm)
length of <i>T/SU-X1/XC</i> extender cable	10" (0.25m)

C.3 Technical Description

Figure C-5 presents block diagram of *T/SU-X1* SIOX rev.B mini-extender kit.

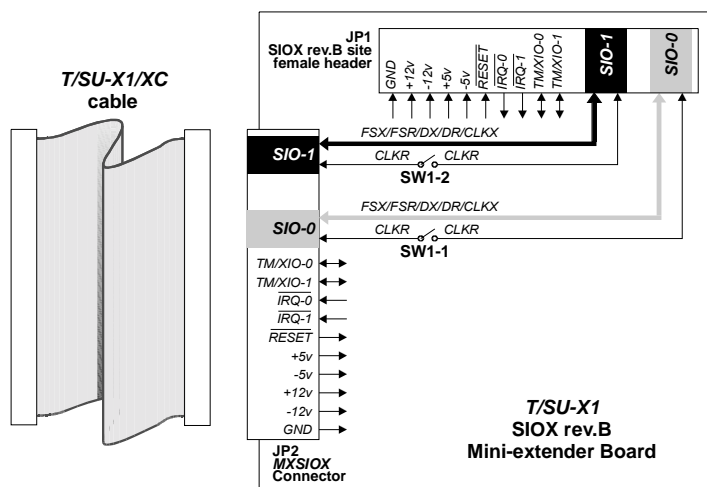


Fig.C-5. Block diagram of *T/SU-X1* SIOX rev.B mini-extender.

T/SU-X1 SIOX rev.B mini-extender carrier board

T/SU-X1 SIOX rev.B mini-extender carrier board comprises of the following components:

- SIOX rev.B site header (JP1)
- MXSIOX connector (JP2) for connection to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* connection cable
- on-board SW1 switch, which is used to enable serial receiver clock (CLKR) for each serial port.

T/SU-X1 on-board JP1 SIOX rev.B site header and JP2 MXSIOX connector for connection to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* connection cable comprise of the signals for two serial ports (SIO-0 and SIO-1), two timer/IO lines (*TM/XIO-0/1*), two external interrupt request inputs (*IRQ-0/1*), SIOX interface reset control output (*RESET*), and host $\pm 5V/\pm 12V$ power supply lines.

Pinout information for JP1 SIOX rev.B site header and JP2 MXSIOX connector is provided in the corresponding subsections below and figures C-6 and C-5 correspondingly. Common signal description is provided in table C-1.

T/SU-X1 on-board SW1 switch shall be used in conjunction with host *TORNADO* DSP coprocessor/controller on-board common serial clock enable switches in order to enable return of receiver' serial clock for each of two serial ports of SIOX interface to host *TORNADO* DSP coprocessor/controller depending upon the type of installed SIOX rev.B DCM. Refer to the corresponding subsection below for more details.

MXSIOX connector pinout and signal description

T/SU-X1 on-board MXSIOX connector is used for connection to host *TORNADO* DSP coprocessor/controller via *T/SU-X1/XC* connection cable.

MXSIOX connector is Samtec 34-pin dual-row 2mm guarded male header. Although MXSIOX plugs come standard with *T/SU-X1/XC* SIOX rev.B mini-extender connection cables, optional MXSIOX plugs for 2mm flat cables are available from MicroLAB Systems upon request.

MXSIOX connector pinout is presented at fig.C-6, whereas signal description is provided in table C-1.

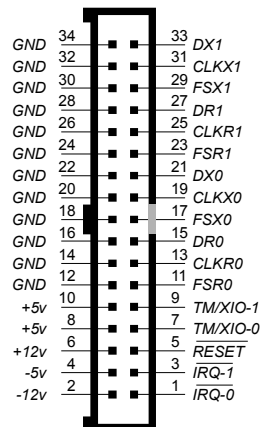


Fig.C-6. Pinout for *T/SU-X1* SIOX rev.B mini-extender on-board MXSIOX connector (top view).

Table C-1. Signal description for T/SU-X1 SIOX rev.B mini-extender on-board MXSIOX connector.

SIOX rev.B interface signal	signal type	Description
<i>SIO-0 port control</i>		
<i>DX0</i> <i>FSX0</i> <i>CLKX0</i>	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port, which connect to the transmitter control signals for SIO-0 serial port.
<i>DR0</i> <i>FSR0</i> <i>CLKR0</i>	I I I	Data, frame synchronization and serial clock signals for receiver of SIO-0 port, which connect to the receiver control signals for SIO-0 serial port.
<i>SIO-1 port control</i>		
<i>DX1</i> <i>FSX1</i> <i>CLKX1</i>	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port, which connect to the transmitter control signals for SIO-1 serial port.
<i>DR1</i> <i>FSR1</i> <i>CLKR1</i>	I I/O I	Data, frame synchronization and serial clock signals for receiver of SIO-1 port, which connect to the receiver control signals for SIO-2 serial port.
<i>Timers/IO, DSP Reset and Interrupt Requests</i>		
<i>TM/XIO-0</i> <i>TM/XIO-1</i>	I/O	Timer/IO pins.
\overline{RESET}	O	Active low SIOX reset output pin.
$\overline{IRQ-0}$ $\overline{IRQ-1}$	I	Active low external interrupt request inputs. Active DSP core' external interrupt requests are generated on the falling edge (1→0) of $\overline{IRQ-0}$ and $\overline{IRQ-1}$.. inputs.
<i>Power Supplies</i>		
<i>GND</i>		Ground.
<i>+5v</i>		+5v power supply.
<i>+12v</i>		+12v power supply.
<i>-5v</i>		-5v power supply.
<i>-12v</i>		-12v power supply.

- Note:
1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
 3. All logical signal levels and load currents correspond to that for 3v/5v CMOS signals.

SIOX rev.B site header

T/SU-X1 on-board SIOX rev.B site header with two serial ports is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM must be the industry standard either 26-pin 0.1"x0.1" male header (in case both SIO-0 and SIO-1 serial ports are used on SIOX plugged-in DCM) or 20-pin 0.1"x0.1" male header (in case only SIO-0 serial port is used on SIOX plugged-in DCM).

SIOX rev.B site connector pinout with two serial ports is shown at fig.C-7 and signal specifications are listed in table C-1.

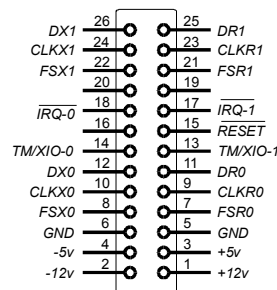


Fig.C-7. SIOX rev.B connector pinout (top view).

Signal levels for SIOX interface signals of T/SU-X1 SIOX rev.B mini-extender is defined by host **TORNADO** DSP coprocessor/controller and correspond to that for the CMOS/TTL signals with $I_{OL}=2\text{ma}$ and $I_{OH}=-0.3\text{ma}$ load currents.

CAUTION

Some **TORNADO** boards provide SIOX interface signal levels for CMOS/TTL only, whereas other **TORNADO** boards provide SIOX interface signal levels universal for both 3V TTL and standard 5V TTL. Refer to documentation for your particular **TORNADO** board for information about SIOX interface signal levels.

T/SU-X1/XC mini-extender connection cable

T/SU-X1 SIOX rev.B mini-extender carrier board connects to host **TORNADO** DSP coprocessor/controller via T/SU-X1/XC 10" (0.25m) long 34-pin 2mm flat cable.

T/SU-X1/XC mini-extender connection cable plugs to MXSIOX connector of T/SU-X1 SIOX rev.B mini-extender carrier board on one side and to MXSIOX connector of host **TORNADO** DSP coprocessor/controller on the other side (fig.C-3).

on-board receiver serial clock return enable switches

T/SU-X1 SIOX rev.B mini-extender carrier board provides on-board SW1-1 and SW1-2 switches in order to enable return of SIO-0 and SIO-1 receiver serial clock (CLKR0 and CLKR1 correspondingly) SIOX interface to host *TORNADO* DSP coprocessor/controller depending upon the type of installed SIOX rev.B DCM.

T/SU-X1 SIOX rev.B mini-extender on-board SW1-1 and SW1-2 switches shall be used in conjunction with host *TORNADO* DSP coprocessor/controller on-board common serial clock enable switches using general recommendations below.

Host *TORNADO* DSP coprocessor/controller provides on-board common CLKX/CLKR serial clock enable switches for each of serial ports of MXSIOX connectors.

CAUTION

In case on-board common serial clock enable switch of host *TORNADO* DSP coprocessor/controller is set to 'ON', then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are connected together on-board.

In case on-board common serial clock enable switch of host *TORNADO* DSP coprocessor/controller is set to 'OFF', then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are disconnected on-board.

Background for usage on-board common CLKX/CLKR serial clock enable switches of host *TORNADO* DSP coprocessor/controller and *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKR) return enable switches is the 'long-line' compensation issue for serial clock signals distribution over connection flat cable between host *TORNADO* DSP coprocessor/controller on-board MXSIOX connector and *T/SU-X1* SIOX rev.B mini-extender due to the 'long-line wave nature' of connection flat cable.

Although the 'long-line' compensation resistors are being used for control signals for serial ports at both host *TORNADO* DSP coprocessor/controller and *T/SU-X1* SIOX rev.B mini-extender boards in order to exclude signal reflection, a 'long-line' non-compensation for serial clock signals can still occur in case installed SIOX rev.B DCM is using common shorted serial clock for transmitter and receiver of SIO port (many SIOX rev.B DCM actually use this in order to simplify design). Note, that this problem does not occur with SIO port frame synchronization and serial data signals, since these signals always use dedicated lines of SIOX interface and can't be connected together.

CAUTION

In case installed SIOX rev.B DCM has been designed without on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and each serial clock is using its dedicated pins, then the corresponding host *TORNADO* DSP coprocessor/controller on-board common CLKX/CLKR serial clock enable switch must be set to 'OFF' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'ON'.

In case installed SIOX rev.B DCM has been designed with on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and both serial clocks are using shared pins, then the corresponding host *TORNADO* DSP coprocessor/controller on-board common CLKX/CLKR serial clock enable switch must be set to 'ON' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'OFF'.

LED indicators

T/SU-X1 SIOX rev.B carrier board also provides two on-board LED indicators for host power (V1) and for SIOX reset state (V2).

C.4 Physical Dimensions for SIOX DCM

Physical dimensions for SIOX DCM are presented at fig.C-8. This information is intended for those customers, who need to design customized SIOX DCMs.

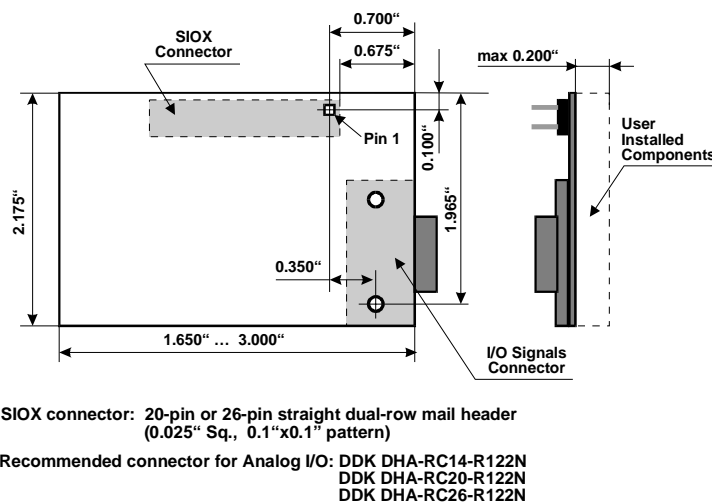


Fig.C-8. Physical dimensions for SIOX DCM.

Appendix D. Software Utilities for *TORNADO-PX64xxQ*

TORNADO-PX64xxQ DSP coprocessor DCM comes standard with software utilities that can be used by the user to speed up development of his application and to provide compatibility between different applications.

All software utilities for *TORNADO-PX64xxQ* DSP coprocessor DCM come in source C-code for easy understanding and modification by the user, are well commented, and include the following software components:

- Software utilities for *TORNADO-PX64xxQ* on-board TMS320C64xx DSP, which come in *PX64XXQ_DSP.H* C/C++ header file and include definitions, macros and API functions for control of on-board DSP environment.
- Software utilities for host *TORNADO* DSP system/controller, which is used to install *TORNADO-PX64xxQ* DSP coprocessor DCM onto it. Host *TORNADO* DSP software utilities support both TMS320C3x and TMS320C6000 host *TORNADO* DSP platforms and come in *PX64XXQ_HDSP.H* C/C++ header file, which include definitions, macros and API functions for access to host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM, for access to on-chip HPI ports of on-board TMS320C64xx DSP, and to load executable code and/or data into on-board DSP environment.
- A comprehensive set of software demos and tests for both *TORNADO-PX64xxQ* on-board DSP and host *TORNADO* DSP, which will guide user thru how to design different applications for *TORNADO-PX64xxQ* DSP coprocessor DCM and will allow user to provide reliable test of on-board hardware.
- CCS GEL-files for automatic configuration of *TORNADO-PX64xxQ* on-board DSP environment from TI CCS TMS320C64xx emulator debugger, which is used to debug *TORNADO-PX64xxQ* on-board DSP software via external JTAG emulator.

CAUTION

This manual does not provide detail description neither for *TORNADO-PX64xxQ* resident TMS320C64xx DSP software utilities, nor for host *TORNADO* DSP system/controller software utilities.

For more details refer to instructions and comments provided in the source code for the corresponding software utilities for *TORNADO-PX64xxQ* DSP coprocessor DCM.

D.1 Resident TMS320C64xx DSP Software Utilities for *TORNADO-PX64xxQ* DSP Coprocessor DCM

TORNADO-PX64xxQ resident TMS320C64xx DSP software utilities come in source code in *PX64xxQ_DSP.H* header file for TI C6000 CCS C/C++ Compiler tools.

CAUTION

TORNADO-PX64xxQ resident TMS320C64xx DSP software utilities, which are provided in *PX64xxQ_DSP.H* header file, shall be configured via run-time compiler keys (definitions) in order to include extended API functions.

For more details refer to instructions and comments provided in *PX64xxQ_DSP.H* header file.

PX64xxQ_DSP.H header file includes definitions, macros and utility API functions, which can be used to control on-board TMS320C64xx DSP environment as the following:

- properly configure TMS320C64xx DSP on-chip EMIF-A/B control registers
- provide access to all DSP IOX control registers for DSP environment ID, DSP-to-DSP communication, and configuration of DSP external interrupt request sources
- control *RESET*, *TMXIO-0* and *XIO-1* signals for on-board MXSIOX interface connectors
- provide access to dedicated SSRAM locations for generation of interrupt requests to particular DSP
- provide access to DSP on-chip HPIC register for generation interrupt requests to host *TORNADO* DSP and to clear host-to-DSP interrupt request
- configure and transfer data over 'horizontal', 'vertical', and 'diagonal' serial links for DSP-to-DSP communication.

D.2 Host *TORNADO* DSP Software Utilities for *TORNADO-PX64xxQ* DSP Coprocessor DCM

Host *TORNADO* DSP software utilities for *TORNADO-PX64xxQ* DSP coprocessor DCM come in source code in *PX64xxQ_HDSP.H* header file for both TI 'C3x Code Composer C Compiler tools (for *TORNADO-3x/P3x/E3x* DSP systems/controllers) and TI 'C6000 Code Composer Studio C/C++ Compiler tools (for *TORNADO-6x/P6x/P64xx/E6x/E64xx* DSP systems/controllers).

CAUTION

Host *TORNADO* DSP software utilities for *TORNADO-PX64xxQ* DSP coprocessor DCM, which are provided in *PX64xxQ_HDSP.H* header file, shall be configured via run-time compiler keys (definitions) in order to meet particular host *TORNADO* DSP platform and the board type, PIOX base address for host *TORNADO* DSP system/controller, and to include extended API functions.

For more details refer to instructions and comments provided in *PX64xxQ_HDSP.H* header file.

PX64xxQH.H header file includes definitions, macros and utility API functions, which can be used to control host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM from host *TORNADO* DSP software as the following:

- provide access to all host interface control registers and to DSP on-chip HPI port registers
- initialize host PIOX interface of *TORNADO-PX64xxQ* DSP coprocessor DCM
- configure DSP reset signals, DSP bootmode and HPI data format mode for each on-board TMS320C64xx DSP
- identify on-board DSP environment and on-board SSRAM/SDRAM memory capacity
- enable and process HPI timeout error flags for host-to-HPI access cycles
- configure host PIOX interface interrupt requests
- transfer data through HPI ports of on-board TMS320C64xx DSP
- initialize TMS320C64xx DSP on-chip EMIF-A/B control registers for access to on-board SSRAM and SDRAM memories from host *TORNADO* DSP software
- generate host-to-DSP interrupt requests to on-board DSP via DSP on-chip HPI ports and generate host ‘broadcast’ interrupt request to on-board DSP
- load resident executable code for each on-board TMS320C64xx DSP via HPI port using ‘C6000 C-BSF32 program/data loader (refer to subsection [“Loading resident executable code to TMS320C64xx DSP environment via HPI port”](#) below for more details).

Loading resident executable code and data to TMS320C64xx DSP environment via HPI port

Host *TORNADO* DSP software utilities for *TORNADO-PX64xxQ* DSP coprocessor DCM provide program/data loader API function, which shall be used to load resident executable code and data to the DSP environment (DSP on-chip memory and registers, external SSRAM and SDRAM memories) of any on-board TMS320C64xx DSP via DSP on-chip HPI port.

In order to load of resident executable code and data to TMS320C64xx DSP environment via DSP on-chip HPI port, the following steps shall be performed:

1. Application code and/or data for *TORNADO-PX64xx* on-board TMS320C64xx DSP shall be compiled using TI C6000 CCS C/C++ and Assembler compiler tools, and the corresponding output C6000 .OUT file is being generated. Output .OUT file must meet TI COFF2 format, which is so far the only format for executable files for TMS320C6000 DSP platforms.
2. Output C6000 executable .OUT file, which has been generated at step #1, shall be converted to output *C6000 C-BSF32* data array using *C6X_CBSF.EXE* Windows command line utility, which is provided with *TORNADO-PX64xxQ* software utilities. Output *C6000 C-BSF32* data array is placed into output C-code compatible file and contains binary data for each non-empty section of input C6000 executable .OUT file. Output C-code file with generated *C6000 C-BSF32* data array can be compiled using TI C3x and C6000 C/C++ compiler tools.
3. *C6000 C-BSF32* data array, which has been generated at step #2 and is placed into C-code compatible file, must be included into user application C-code for host *TORNADO* DSP, which shall be compiled using TI C3x and C6000 C-compiler tools. Note, that host *TORNADO* DSP environment must provide enough memory to allocate all *C6000 C-BSF32* data arrays, which correspond to executable code and/or data for each *TORNADO-PX64xxQ* on-board TMS320C64xx DSP.
4. *C6000 C-BSF32* program/data loader API function from *PX64xxQ_HDSP.H* header file shall be called from host *TORNADO* DSP application in order to transfer TMS320C64xx DSP executable code and/or data from *C6000 C-BSF32* data array to the DSP environment (DSP on-chip memory and registers, external SSRAM and SDRAM memories) of the corresponding *TORNADO-PX64xxQ* on-board TMS320C64xx DSP via DSP on-chip HPI port.

C6000 program/data C-BSF32 data arrays

C-BSF32 data array is a *binary section format 32-bit data array for C-compiler*, which appears as 32-bit data array in source text file and shall be included into user application source C-code for host **TORNADO DSP**.

Although **C-BSF32** data array appears as predefined linear data array of 32-bit unsigned long data, it features internal structure as a series of data sections. Each data section comprises of section header and section data. Section header contains information about DSP platform, load address and section data length, which are used to properly load section data into target DSP environment. Termination section header is provided at the end of **C-BSF32** data array in order to terminate code/data upload.

CAUTION

This manual does not provide details for **C6000 C-BSF32** data array format.

For more details refer to the program/data loader API function (`HPX64XXQ_load_dsp_program()`) in `PX64XXQ_HDSP.H` C/C++ header file with host **TORNADO DSP** software utilities for **TORNADO-PX64xxQ DSP coprocessor DCM**.

TORNADO-PX64xxQ C6000 C-BSF32 program/data loader for host TORNADO DSP

Host **TORNADO DSP** software utilities for **TORNADO-PX64xxQ DCM** include **C6000 C-BSF32** program/data loader API function (`HPX64XXQ_load_dsp_program()`), which can be used to transfer TMS320C64xx DSP executable code and/or data for **TORNADO-PX64xxQ** on-board TMS320C64xx DSP from **C6000 C-BSF32** data array to the DSP environment of the corresponding **TORNADO-PX64xxQ** on-board TMS320C64xx DSP.

`HPX64XXQ_load_dsp_program()` **C6000 C-BSF32** program/data loader API function reads and interprets contents of **C6000 C-BSF32** program/data array on section-by-section basis and loads provided section data to the DSP environment (DSP on-chip memory and registers, external SSRAM and SDRAM memories) of target **TORNADO-PX64xxQ TMS320C64xx DSP** via DSP on-chip HPI port.

C6X_CBSF.EXE Windows command-line utility for conversion of C6000 .OUT file to C6000 C-BSF32 data array

C6X_CBSF.EXE Windows command line utility runs under all Windows 9x/NT/2000/XP platforms and shall be used to convert input C6000 .OUT file, which is generated by TI C6000 CCS C/C++ and/or Assembler compiler tools, into output C-code compatible file with **C6000 C-BSF32** data array.

The following is the Windows command line synopsis for invoking **C6X_CBSF.EXE** Windows command line utility::

```
C6X_CBSF INPUT_FILENAME[.OUT] OUTPUT_FILENAME
```

The '-D' command line option for Windows **C6X_CBSF.EXE** Windows command line utility can be used to display detail section information for input C6000 .OUT file:

```
C6X_CBSF INPUT_FILENAME[.OUT] -d
```

D.3 TORNADO-PX64xxQ GEL-files for TI CCS TMS320C64xx debugger

TORNADO-PX64xxQ software utilities include GEL-files for TI CCS TMS320C64xx emulator debugger for automatic configuration of *TORNADO-PX64xxQ* DSP on-chip EMIF-A/B control registers and DSP environment at the debugger start and software reset command. TI CCS TMS320C64xx emulator debugger is the part of TI C6000 CCS tools and shall be used to debug TORNADO-PX64xxQ on-board DSP software via external JTAG emulator.

The following GEL-files for TI CCS TMS320C64xx debugger are provided with *TORNADO-PX64xxQ* software utilities:

- *PX64XXQ_SDRAM4M.GEL* file, which must be used for *TORNADO-PX64xxQ* DSP coprocessor DCM with on-board installed 4Mx32 SDRAM for each on-board TMS320C64xx DSP
- *PX64XXQ_SDRAM16M.GEL* file, which must be used for *TORNADO-PX64xxQ* DSP coprocessor DCM with on-board installed 16Mx32 SDRAM for each on-board TMS320C64xx DSP

CAUTION

Only one of provided *PX64XXQ_SDRAM4M.GEL* or *PX64XXQ_SDRAM16M.GEL* CCS GEL-files must be included as start-up CCS GEL-file in 'Start-up GEL' folder of TI CCS TMS320C64xx emulator driver dialog via CCS SETUP utility for each of *TORNADO-PX64xxQ* on-board TMS320C64xx DSP, which are included as active JTAG device(s) into on-board JTAG path (refer to section [“Emulation tools for TORNADO-PX64xxQDSP coprocessor DCM”](#) for more details).

Appendix E. Glossary of Terms.

This Glossary contains definition for terms and other synchronism used along in this databook.

A

B

Bootmode Configuration

TMS320C64xx DSP bootmode. Refer to [section 2.2](#) and [table 2-2](#) for more details.

C

C6000 C-BSF32 data array

‘C6000 32-bit binary section format data array, which appears as 32-bit unsigned long predefined data array in C-code compatible format for inclusion into user application C-code for host *TORNADO* DSP. *C6000 C-BSF32* data array may contain executable code and/or data for target TMS320C64xx DSP environment and must be transferred to target DSP environment using *C-BSF32* program/data loader from host *TORNADO* DSP software utilities. Refer to [Appendix ‘D’](#) for more details.

C6X_CBSF.EXE

Windows command line utility, which runs under all Windows 9x/NT/2000/XP platforms, and shall be used to convert input C6000 .OUT file, which is generated by TI C6000 CCS C/C++ and/or Assembler compiler tools, into output C-code compatible file with *C6000 C-BSF32* data array. This utility is the part of *TORNADO-PX64xxQ* software utilities. Refer to [Appendix ‘D’](#) for more details.

CLKX, CLKR

Serial clock for transmitter and receiver of TMS320C64xx DSP on-chip McBSP serial ports. Refer to [section 2.3](#) and [Appendix ‘C’](#) for more details.

D

DCM

Daughter-card module. *TORNADO-PX64xxQ* is PIOX DCM, which plugs into PIOX DCM site of host *TORNADO* DSP system/controller.

DSP

On-board TI TMS320C64xx Digital Signal Processor. Refer to [sections 2.1](#), and [2.2](#) for more details.

DSP_BROADCAST_RQ_RG

Write-only IOX control register from DSP environment, which is used to generate interrupt request to all 'horizontal', 'vertical' and 'diagonal' DSP neighbour nodes simultaneously. Refer to [section 2.2](#) for more details.

***DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG,
DSP_EXT_INT7_SEL_RG***

IOX control registers from DSP environment, which are used to select interrupt request source for DSP EXT_INT4..7 external interrupt request inputs correspondingly. Refer to [section 2.2](#) for more details.

DSP_DEV_ID_RG

Read-only IOX control register from DSP environment, which is used to get device ID. Refer to [section 2.2](#) for more details.

DSP_DIAG_RQ_RG

Write-only IOX control register from DSP environment, which is used to generate interrupt request to the 'diagonal' DSP neighbour node. Refer to [section 2.2](#) for more details.

DSP_HORIZ_RQ_RG

Write-only IOX control register from DSP environment, which is used to generate interrupt request to the 'horizontal' DSP neighbour node. Refer to [section 2.2](#) for more details.

DSP_NMI_SEL_RG

IOX control registers from DSP environment, which are used to select interrupt request source for DSP NMI external interrupt request input. Refer to [section 2.2](#) for more details.

DSP_NODE_ID_RG

Read-only IOX control register from DSP environment, which is used to get on-board node ID for particular on-board DSP. Refer to [section 2.2](#) for more details.

DSP_REV_ID_RG

Read-only IOX control register from DSP environment, which is used to get revision ID and DSP speed grade ID. Refer to [section 2.2](#) for more details.

DSP_SYS_STAT_RG

Read-only IOX control register from DSP environment, which is used to get DSP bootmode, HPI data format mode and enable status for 'vertical' and 'diagonal' DSP-to-DSP serial links. Refer to [section 2.2](#) for more details.

DSP_VERT_RQ_RG

Write-only IOX control register from DSP environment, which is used to generate interrupt request to the 'vertical' DSP neighbour node. Refer to [section 2.2](#) for more details.

DSP_XMEM_LEN_ID_RG

Read-only IOX control register from DSP environment, which is used to get memory capacity for on-board SSRAM and SDRAM memories. Refer to [section 2.2](#) for more details.

DSP-to-DSP interrupt request

TORNADO-PX64xxQ on-board ‘horizontal’, ‘vertical’ and ‘diagonal’ DSP-to-DSP interrupt requests for DSP-to-DSP communication. Refer to [section 2.2](#) for more details.

DSP-to-DSP serial link

TORNADO-PX64xxQ on-board ‘horizontal’, ‘vertical’ and ‘diagonal’ serial links for DSP-to-DSP communication via TMS320C64xx DSP on-chip McBSP-2, McBSP-1 and McBSP-0 serial ports. Refer to [section 2.2](#) for more details.

DSPINT

Host-to-DSP interrupt request via TMS320C64xx DSP on-chip HPI port, which appears as the *DSPINT* bit of TMS320C64xx DSP on-chip HPIC register. Refer to [sections 2.2](#) and [2.4](#) for more details.

E***EMIF-A/B***

TMS320C64xxx DSP external memory interfaces #A and #B, which are used to connect to on-board SSRAM and SDRAM memories and IOX control registers. Refer to [section 2.2](#) and to TI TMS320C6x documentation for more details.

EXT_INT4..EXT_INT7

TMS320C6xxx DSP external interrupt request inputs, which are used for generation the DSP interrupts via *DSP_EXT_INT4_SEL_RG..DSP_EXT_INT7_SEL_RG* interrupt selector registers. Refer to [section 2.2](#) and to TI TMS320C6x documentation for more details.

F**G*****GPIO***

General purpose I/O pins of TMS320C64xx DSP, which are used to control *TM/XIO-0*, *XIO-1* and *RESET* signals of on-board MXSIOX interface connector. Refer to [sections 2.2](#) and [2.3](#) for more details.

H***HINT***

DSP-to-host interrupt request via TMS320C64xx DSP on-chip HPI port, which appears as the *HINT* bit of TMS320C64xx DSP on-chip HPIC register. Refer to [sections 2.2](#) and [2.3](#) for more details.

Host PIOX interface

TORNADO-PX64xxQ on-board host PIOX interface, which is used to install onto host *TORNADO* DSP system/controller and for communication with host *TORNADO* on-board DSP. Refer to [section 2.4](#) and [Appendix 'B'](#) for more details.

HOST_DEV_ID_RG

Read-only register of host PIOX interface, which is used to get device ID, revision ID and DSP speed grade ID. Refer to [section 2.4](#) for more details.

HOST_DSP_BROADCAST_RQ_RG

Write-only register of host PIOX interface, which is used to generate 'broadcast' interrupt request from host *TORNADO* DSP application to all on-board TMS320C64xx DSP simultaneously. Refer to [sections 2.2](#) and [2.4](#) for more details.

HOST_DSP_CNF_STAT_RG

Read-only register of host PIOX interface, which is used to get status information for DSP bootmode and HPI data format for each of on-board TMS320C64xx DSP. Refer to [section 2.4](#) for more details.

HOST_DSP_LINK_CNF_RG

Register of host PIOX interface, which is used to enable on-board DSP-to-DSP 'vertical' serial links. Refer to [sections 2.2](#) and [2.4](#) for more details.

HOST_DSP_XMEM_LEN_ID_RG

Read-only register of host PIOX interface, which is used to get memory capacity for on-board SSRAM and SDRAM memories. Refer to [section 2.4](#) for more details.

*HOST_CLR_DSPA_HPI_ERR_RG, HOST_CLR_DSPB_HPI_ERR_RG,
HOST_CLR_DSPC_HPI_ERR_RG, HOST_CLR_DSPD_HPI_ERR_RG*

Write-only registers of host PIOX interface, which are used to clear timeout error flags for host-to-HPI accesses. Refer to [section 2.4](#) for more details.

HOST_CNTR1_RG

Register of host PIOX interface, which is used to control reset signals for each TMS320C64xx DSP. Refer to [section 2.4](#) for more details.

HOST_CNTR2_RG

Register of host PIOX interface, which is used to control DSP bootmode and HPI data format for on-board TMS320C64xx DSP and to enable timeout control for host-to-HPI access cycle. Refer to [section 2.4](#) for more details.

*HOST_HIRQ0_SEL_RG, HOST_HIRQ1_SEL_RG, HOST_HIRQ2_SEL_RG,
HOST_HIRQ3_SEL_RG*

Host PIOX interrupt selector/enable registers from host PIOX interface. Refer to [section 2.4](#) for more details.

HOST_HINT_STAT_RG

Read-only register of host PIOX interface, which contains status information for all DSP-to-host interrupt requests and all host-to-HPI access timeout error flags. Refer to [section 2.4](#) for more details.

*HOST_HPI16_DSPx_HPIC_LSW_RG, HOST_HPI16_DSPx_HPIC_MSW_RG,
HOST_HPI16_DSPx_HPIA_LSW_RG, HOST_HPI16_DSPx_HPIA_MSW_RG,
HOST_HPI16_DSPx_HPID_LSW_RG, HOST_HPI16_DSPx_HPID_MSW_RG,
HOST_HPI16_DSPx_HPID_AINC_LSW_RG, HOST_HPI16_DSPx_HPID_AINC_MSW_RG*

On-chip 16-bit HPI port registers for TMS320C64xx DSP-x (x=A..D), which can be accessed from host PIOX interface for 16-bit HPI data format mode. Refer to [section 2.4](#) for more details.

*HOST_HPI32_DSPx_HPIC_RG, HOST_HPI32_DSPx_HPIA_RG,
HOST_HPI32_DSPx_HPID_RG, HOST_HPI32_DSPx_HPID_AINC_RG*

On-chip 32-bit HPI port registers for TMS320C64xx DSP-x (x=A..D), which can be accessed from host PIOX interface for 32-bit HPI data format mode. Refer to [section 2.4](#) for more details.

HPI

TMS320C64xx DSP on-chip host port interface, which is used to access DSP environment from host PIOX interface environment. Refer to [section 2.4](#) for more details.

HPI access timeout error flag

Error flag, which is set in case of timeout condition for host-to-HPI access cycles of host PIOX interface. HPI access timeout flags can be read via *HOST_INT_STAT_STAT_RG* read-only register and can be cleared via *HOST_CLR_DSPn_HPI_ERR_RG* (n=A..D) write-only registers. Refer to [section 2.4](#) for more details.

I

IRQ-0, IRQ-1, IRQ-2, IRQ-3

Host PIOX interface interrupt request outputs. Refer to [section 2.4](#) and [Appendix 'B'](#) for more details.

IOX control registers

On-board I/O expansion control registers, which are local for each on-board TMS320C64xx DSP and are used on-board DSP environment control from DSP application. Refer to [section 2.2](#) for more details.

J

JTAG

Joint Test Action Group interface, which is a part of the TMS320C2xx/VC33/C4x/C5x/C54xx/C55xx/C6xxx/C8x DSP silicon, and is used to debug *TORNADO-PX64xxQ* on-board TMS320C64xx DSP software using external JTAG emulator (TI XDS and MicroLAB Systems *MIRAGE*). Refer to [section 2.5](#) for more details.

K

L

LED

Light emitting diode indicator. Refer to [Appendix 'A'](#) for more details.

M

McBSP

TMS320C64xx DSP on-chip serial ports. Refer to [sections 2.2](#) and [2.3](#) for more details.

MXS/IOX

On-board interface connectors for connection to external *T/SU-X1*, *T/SU-X2*, and *T/SU-X3* SIOX rev.B mini-extenders for real-time analog/digital I/O and *T/X-XSLC1* external serial link converter for board-to-board communication in multi-board multi-DSP systems. Refer to [sections 2.2](#) and [2.3](#) and [Appendix 'C'](#) for more details.

N

NMI

TMS320C6xxx DSP external non-maskable interrupt request input, which are used for generation the DSP non-maskable interrupt via *DSP_NMI_SEL_RG* interrupt selector register. Refer to [section 2.2](#) and to TI TMS320C6x documentation for more details.

O

P

PIOX

16-bit or 32-bit Parallel I/O eXpansion DCM site interface for compatible daughter-card modules (DCM) at *TORNADO* PC plug-in DSP systems. Refer to [section 2.4](#) and [Appendix 'B'](#) for more details.

Pod

Connects external JTAG emulator with *TORNADO-PX64xxQ* on-board JTAG connector for uploading and debugging of on-board DSP software. Refer to [section 2.5](#) for more details.

Q

R

S

SDRAM

TORNADO-PX64xxQ on-board synchronous dynamic RAM, which is local for each on-board TMS320C64xx DSP and which can be used to store large run-time data arrays. Refer to [section 2.2](#) for more details.

SIO-0, SIO-1

Serial ports at SIOX rev.B interface, which are typically connected to the corresponding DSP on-chip serial ports. Refer to [section 2.3](#) and [Appendix 'C'](#) for more details.

SIOX rev.B

Serial I/O eXpansion DCM site interface revision B for compatible daughter-card modules (DCM) at *TORNADO* DSP systems, controllers, and SIOX extenders. Refer to [section 2.3](#) and [Appendix 'C'](#) for more details.

SSRAM

TORNADO-PX64xxQ on-board synchronous shared static RAM for high-speed DSP-to-DSP communication via shared memory area. Refer to [section 2.2](#) for more details.

T

T/SU-X1, T/SU-X2, T/SU-X3

External SIOX rev.B mini-extenders, which can carry one SIOX rev.B DCM and connect to *TORNADO-PX64xxQ* on-board MXSIOX interface connector. Refer to [section 2.3](#) and [Appendix 'C'](#) for more details.

T/SU-X1/XC

Extender connector cable, which is used to connect external SIOX rev.B mini-extender and *TORNADO-PX64xxQ* DCM. Refer to [section 2.3](#) and [Appendix 'C'](#) for more details.

TM/XIO-0, TM/XIO-1

Timer/IO pins of SIOX rev. B interface site at *TORNADO* DSP systems, controllers, and SIOX extenders. Refer to [section 2.2](#) and [2.3](#) and [Appendix 'C'](#) for more details.

U

V

W

X

Y

Z