MicroLAB Systems

Ultimate DSP Development Solutions

DIGITAL SIGNAL PROCESSING

TORNADO-PX5421Q

800 MIPS Quad TMS320VC5421 Dual-core 16-bit Fixed-point DSP
PIOX-16 Coprocessor DCM
for *TORNADO* DSP Systems/Controllers

User's Guide

covers:
TORNADO-PX5421Q rev.1A

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DOC: MLS-SPUG-208E revision 1A
June 2001

About this Document

This user's guide contains description for *TORNADO-PX5421Q* PIOX-16 quad TMS320VC5421 dual-core 16-bit fixed-point DSP coprocessor daughter-card module (DCM) for *TORNADO* DSP systems/controllers.

This document does not include detail description neither for the on-board components nor for the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C54x. CPU and Peripherals. Reference Guide.*** Texas Instruments Inc, SPRU131F, 2000.
2. ***TMS320VC5421 DSP.*** Texas Instruments Inc, SPRS098A, 2000.
3. ***TMS320C54x DSP Reference Set. Volume 5: Enhanced Peripherals.*** Texas Instruments Inc, SPRU302, 1999.
4. ***TMS320C5000 DSP Family Functional Overview.*** Texas Instruments Inc, SPRU307, 1999.

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Chapter 1. Introduction

This chapter contains general description for *TORNADO-PX5421Q* PIOX-16 quad TMS320VC5421 dual-core 16-bit fixed-point DSP coprocessor DCM for *TORNADO* DSP systems and controllers.

1.1 General Information

TORNADO-PX5421Q is PIOX-16 (parallel I/O expansion) 800 MIPS quad TMS320VC5421 dual-core 16-bit fixed-point DSP coprocessor DCM (fig.1-1) for *TORNADO* PC plug-in DSP systems and *TORNADO-E* stand-alone DSP controllers from MicroLAB Systems Ltd.

Fig. 1-1. TORNADO-PX5421Q DCM.

Installation onto TORNADO DSP System/Controller

TORNADO-PX5421Q DCM installs into the PIOX-16 site onto *TORNADO* DSP system/controller mainboard (fig.1-2).

Fig. 1-2. TORNADO-PX5421Q DCM installed onto *TORNADO-31* DSP system.

Overview

TORNADO-PX5421Q DCM is based around of four 200 MIPS dual-core 16-bit fixed-point TMS320VC5421 DSP from Texas Instruments Inc. Each TMS320VC5421 DSP runs at 100 MHz and comprises of two TMC320C54x compatible identical DSP cores and features 256Kx32 on-chip RAM, six McBSP serial ports, twelve DMA channels, two timers, and inter-core communication via on-chip shared RAM, bi-directional FIFO and inter-core interrupts.

Host PIOX-16 interface provides access to HPI port of each on-board TMS320VC5421 DSP, and contains a set of control registers for DSP reset, host interrupt selection, and for error processing.

External signal I/O

TORNADO-PX5421Q DCM provides optional facility for connection of up to eight external SIOX rev.B (serial I/O expansion) AD/DA and application specific DCM (one SIOX rev.B DCM per each DSP core) via eight *T/SU-X1* SIOX rev.B mini-extenders (fig.1-3). This feature allows to use *TORNADO-PX5421Q* DCM as application specific I/O DSP coprocessor depending upon the type of connected SIOX rev.B DCM and to unload host *TORNADO* DSP system/controller from signal I/O operations.

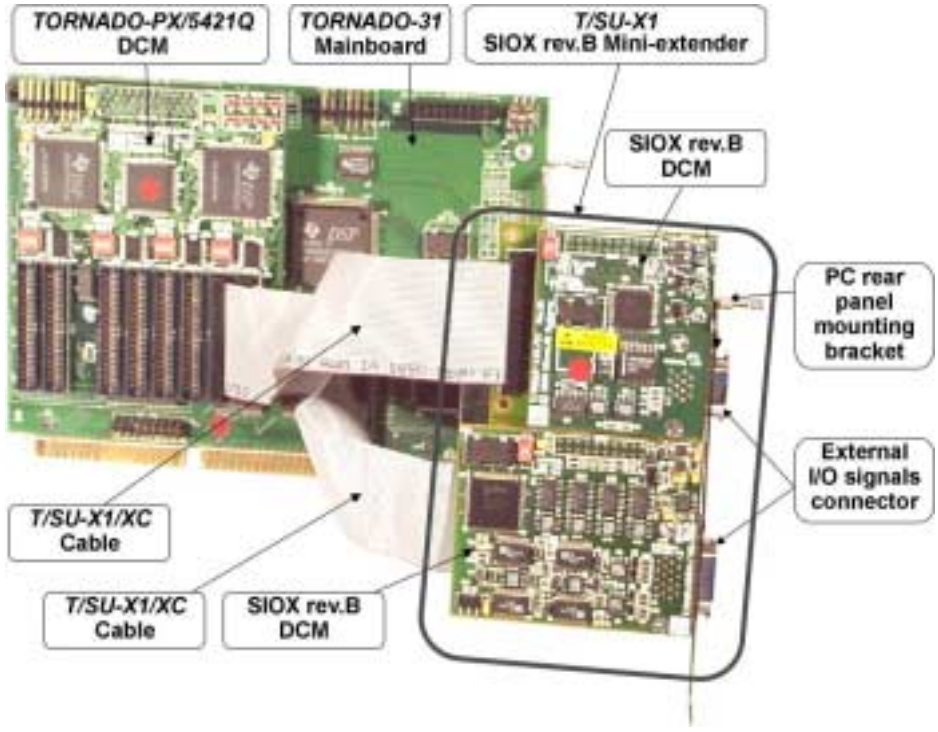


Fig. 1-3. TORNADO-31 DSP system with *TORNADO-PX5421Q* DCM with two optional *T/SU-X1* SIOX rev.B mini-extenders and two SIOX rev.B DCM

Optional *T/SU-X1* SIOX rev.B mini-extenders connect directly to *TORNADO-PX5421Q* DCM via on-board dedicated connectors and *T/SU-X1/XC* extender cable, and can install either at the rear-panel of host PC chassis or into custom chassis.

Applications

TORNADO-PX5421Q DCM has been designed for multi-channel general purpose DSP with optional signal I/O. Application areas include multi-channel speech/fax/modem signal processing, multi-channel digital radio, multi-channel IP telephony, etc applications, which require multi-channel DSP with optional signal I/O.

1.2 Technical Specification

The following are technical specifications for *TORNADO-PX5421Q* PIOX-16 quad TMS320VC5421 DSP coprocessor DCM for *TORNADO* DSP systems/controllers.

Parameter description	*parameter value*
DSP	

DSP type	TMS320VC5421 DSP from Texas Instruments Inc
DSP input clock (CLKIN) frequency	50 MHz
maximum DSP internal clock frequency via PLL	100 MHz
number of on-board DSP	4
External SIOX rev.B interface options	
support for external SIOX rev.B DCM	via *T/SU-X1* SIOX rev.B mini-extenders
number of on-board MXSIOX connectors for *T/SU-X1* external SIOX rev.B mini-extenders	8 (one MXSIOX connector per each DSP core)
maximum recommended CLKX/CLKR frequency (for 0.25m long SIOX rev.B mini-extender cable)	33 MHz
Host PIOX-16 Interface	
number of occupied I/O ports	64
software configurable PIOX-16 interrupt request inputs	IRQ-0, IRQ-1, IRQ-2, IRQ-3
I/O ports	8-bit control registers (32) 16-bit DSP HPI ports (32)
access time	< 20 ns (control registers access) < 40ns..180ns (HPI access)
physical and power:	
dimensions	2.55" x 3.34" (65 x 85 mm)
power consumption via host PIOX interface (without installed SIOX rev.B DCM at *T/SU-X1* external SIOX rev.B mini-extenders)	+5v @ 0.7 A ±12v/-5v are routed to MXSIOX connectors for *T/SU-X1* external SIOX rev.B mini-extenders
external operating temperature	0°C .. +60°C

Chapter 2. System Architecture and Construction

This chapter contains detail description for architecture and construction of *TORNADO-PX5421Q* PIOX-16 DSP coprocessor DCM for *TORNADO* DSP systems/controllers.

2.1 System Architecture

System architecture and construction for *TORNADO-PX5421Q* PIOX-16 coprocessor DCM are presented at fig.2-1 and fig.2-2.

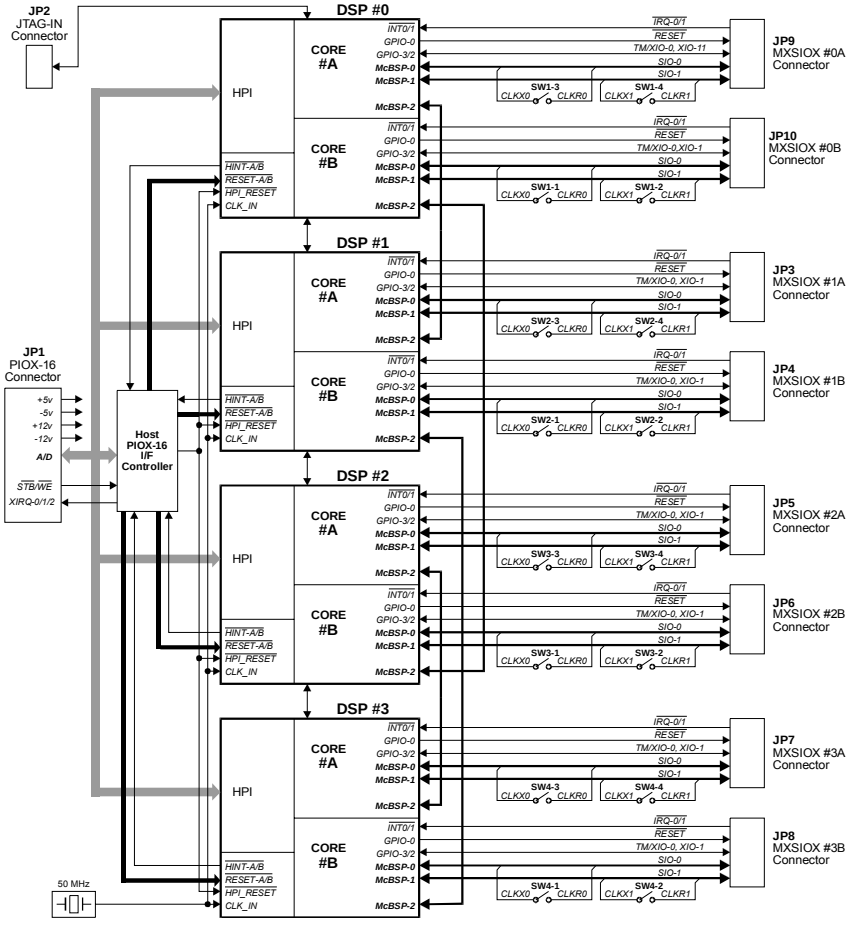


Fig.2-1. Block diagram of *TORNADO-PX5421Q* DSP Coprocessor DCM.

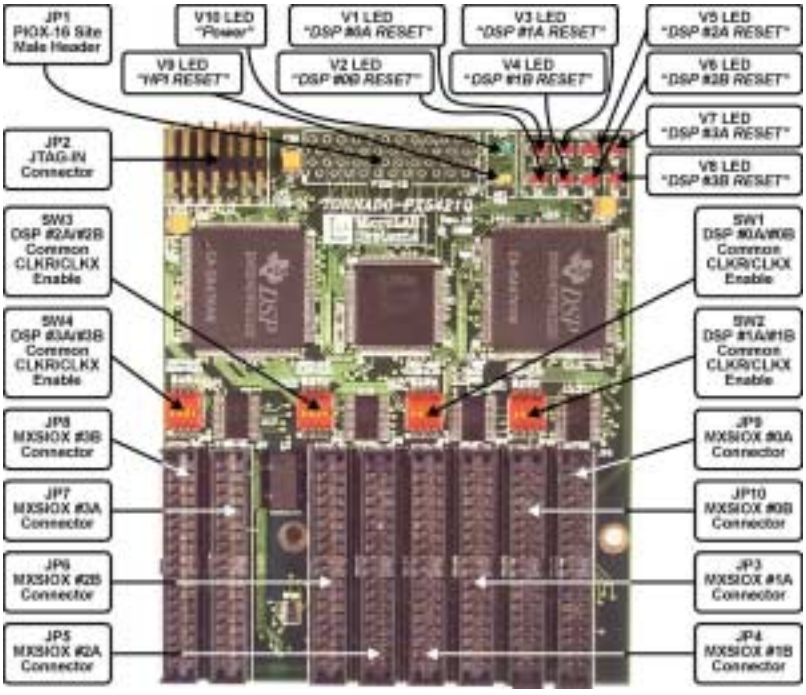


Fig.2-2. Construction of *TORNADO-PX5421Q* DSP Coprocessor DCM.

TORNADO-PX5421Q DCM installs as PIOX-16 DCM onto host *TORNADO* DSP system/controller and comprises of the following components:

- four 200 MIPS TMS320VC5421 dual-core DSP (DSP0..DSP3) each comprising of DSP cores #A and #B
- MXSIOX-0A..3B on-board expansion site connectors for optional external *T/SU-X1* SIOX rev.B mini-extenders (JP3..JP10), which can be used to connect any SIOX rev.B DCM to the corresponding DSP core
- common serial clock enable switches (SW1..SW4) for external *T/SU-X1* SIOX rev.B mini-extenders
- JTAG-IN connector (JP2) for connection to external JTAG emulator
- host PIOX-16 interface header (JP1) for installation onto *TORNADO* DSP systems/controllers and host PIOX-16 interface controller.

DSP pool

On-board DSP pool comprises of four state of the art dual-core TI TMS320C5421 DSP (DSP-0..3), which are an ideal solution for multi-channel parallel DSP with DSP on-chip core-to-core communication. Total DSP performance of on-board DSP pool is 800 MIPS.

Data transfers between host *TORNADO* DSP system/controller and TMS320VC5421 DSP on-chip memory, as well as DSP boot are performed via host PIOX-16 interface via TMS320VC5421 DSP on-chip HPI port.

For more details about TMS320VC5421 DSP refer to the corresponding original TI documentation and to section "DSP Environment" later in this chapter.

Inter-DSP core-to-core communication

TORNADO-PX5421Q DCM offers inter-DSP core-to-core communication via McBSP-2 serial ports, which are connected on-board between DSP cores of different DSP chips as shown at fig.2-1.

For more details about DSP-to-DSP communication via McBSP-2 serial ports refer to section “DSP Environment” later in this chapter.

Support for SIOX rev.B DCM

TORNADO-PX5421Q DCM provides on-board facilities for optional connection of up to eight external *T/SU-X1* SIOX rev.B mini-extenders (one mini-extender per each DSP core) via on-board dedicated MXSIOX-0A..3B connectors (JP3..JP10). Each *T/SU-X1* SIOX rev.B mini-extender can carry one SIOX rev.B DCM. This allows to add AD/DA and application specific I/O front-end feature to each TMS320VC5421 DSP core and to convert *TORNADO-PX5421Q* DCM into universal DSP and application specific I/O coprocessor.

A variety of SIOX rev.B DCM include speech/fax/modem AD/DA DCM, telecom interfaces, audio AD/DA, DAT interface, multi-channel instrumentation AD/DA/DIO DCM, application specific I/O coprocessors, and many more.

SIOX rev.B site of *T/SU-X1* SIOX rev.B mini-extender comprises of signals for two serial ports, two timer/IO lines, two external interrupt request inputs, reset control, and power supplies.

For more details about support for external SIOX rev.B DCM sites refer to section “Serial I/O Expansion (SIOX) Interface” later in this chapter, and appendix ‘C’ later in this manual.

Host PIOX-16 interface and controller

Host PIOX-16 interface controller comprises of a set of control and status registers for DSP reset control, host PIOX-16 interrupt control, and for error processing.

Host 16-bit PIOX-16 interface (JP1 connector) provides access to DSP on-chip HPI ports and to a set of control and status registers inside host PIOX-16 interface controller.

For more details about host PIOX-16 interface and controller refer to section “Host PIOX-16 Interface” later in this chapter and to appendix ‘B’ later in this manual.

DSP reset control and LED indicators

Individual reset signals for each TMS320VC5421 DSP core and common HPI reset signal for all TMS320VC5421 DSP can be set by host *TORNADO* DSP software via the corresponding control registers of host PIOX-16 interface controller of *TORNADO-PX5421Q* DCM.

For user convenience, on-board LED indicators (V1..V10) are used in order to display current state of all individual DSP reset signals, common HPI reset signal, and of host power.

Debugging of TMS320C5421 DSP software

On-board TMS320C5421 DSP software for *TORNADO-PX5421Q* DCM can be developed and debugged using either TI XDS510 or MicroLAB’ *MIRAGE-510DX* scan-path emulators via on-board JTAG-IN connector (JP2) and TI C5000 Code Composer Studio IDE.

2.2 DSP Environment

TORNADO-PX5421Q DCM on-board DSP environment is based around the DSP pool, which comprises of four high-performance TMS320VC5421 dual-core 16-bit fixed point DSP from TI. Maximum total DSP performance of on-board DSP pool is 800 MIPS.

On-board DSP pool can be used for general purpose multi-channel DSP, for communication with host *TORNADO* DSP system/controller, and for communication with optional external SIOX rev.B DCM during external analog or digital I/O.

TMS320VC5421 DSP

TORNADO-PX5421Q on-board DSP pool comprises of four state of the art TI TMS320C5421 DSP (DSP-0..3).

Each TMS320VC5421 DSP can run at 100 MHz and comprises of two identical DSP cores (#A and #B). Each DSP core includes the following components:

- 16-bit fixed-point TMS320C54xx compatible CPU
- three McBSP ports
- six programmable DMA controllers
- one timer
- 64K dedicated RAM (32K of data/program DARAM and 32K of data SARAM).

Shared TMS320VC5421 DSP on-chip resources include 128K shared RAM, which has been originally designed as shared program RAM for both DSP cores in order to execute common DSP program. However, on-chip shared program RAM can be also used to store shared data, which can be transferred to/from shared RAM via DMA controllers of each DSP core.

TMS320VC5421 DSP on-chip bi-directional FIFO and mutual core-to-core interrupts can be used for fast core-core data transfers and communication.

CAUTION

This manual does not contain description and programming details
for on-board TI TMS320C5421 DSP.

For more information refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TMS320VC5421 DSP clock

On-board external common TMS320C5421 DSP source clock is 50 MHz. TMS320C5421 DSP cores boot in PLL bypass x1 mode, i.e. internal DSP clock frequency is set to 50 MHz.

DSP on-chip software programmable PLL can be used in order to set any DSP internal clock frequency up to 100 MHz. Note, that DSP on-chip PLL can be configured via DSP core #A only.

CAUTION

For more information about TMS320C5421 DSP on-chip PLL refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TMS320VC5421 DSP start-up configuration and memory map

On-board TMS320VC5421 DSP are on-board configured in start-up multiplexed HPI mode (*XIO*=0, *HMODE*=0), which corresponds to HPI boot process and allows to use all DSP on-chip memory. External TMS320VC5421 DSP memory and I/O ports are not available.

CAUTION

For more information about TMS320C5421 DSP start-up configuration and memory map refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TMS320VC5421 DSP reset control

Individual reset signals for each TMS320VC5421 DSP core and common HPI reset signal for all TMS320VC5421 DSP are controlled by host *TORNADO* DSP software via *DSP0A_GO.. DSP3B_GO* bits of *HOST_CNTR1_RG* register and *HPI_GO* bit of *HOST_CNTR2_RG* register of host PIOX-16 interface controller of *TORNADO-PX5421Q* DCM (refer to section "Host PIOX-16 Interface" later in this chapter for more details).

The on-board LED indicators (V1..V9) are used in order to display current state of all individual DSP reset signals and common HPI reset signal.

TMS320VC5421 DSP cores start-up procedure

Host *TORNADO* DSP system/controller can upload code and data to *TORNADO-PX5421Q* on-board TMS320VC5421 DSP on-chip memory while TMS320VC5421 DSP is in the reset state.

The host can release the DSP core from reset by either of the following ways:

- In case TMS320VC5421 DSP core reset signal is held in the 'RESET' state while HPI reset transitions from 'RESET' to 'GO' state, then the DSP core reset will be controlled by DSP core reset signal. After host will finish uploading code via HPI port, it must set DSP core reset signal to the 'GO' state in order to release DSP core from reset. DSP core will start execution from 0x00ff80 program address location, which corresponds to page #0 of TMS320VC5421 DSP on-chip shared program RAM. *This is the recommended DSP core reset release procedure*, since it allows to release simultaneously any number of DSP cores from the 'RESET' state by means of writing the corresponding value to *HOST_CNTR1_RG* register of host PIOX-16 interface controller while keeping HPI reset signal in the 'GO' state.

- In case TMS320VC5421 DSP core reset signal is held in the 'GO' state while HPI reset signal transitions from 'RESET' to 'GO', then the DSP core will stay in the 'RESET' state until host writes any data at the HPI address 0x2F. This method can be only used for individual release of DSP cores from the 'RESET' state.

CAUTION

For more information about release of TMS320C5421 DSP cores from the reset state refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

Setting PMST, SWWSR, SWCR, BSCR, GPIOCR and CLKMD Control Registers of TMS320VC5421 DSP

In order to benefit of full performance of TMS320C5421 DSP and provide correct operation of on-board hardware, user TMS320VC5421 DSP application must set TMS320VC5421 DSP on-chip SWWSR, SWCR, BSCR, GPIOCR and CLKMD control registers as the following:

- The MP/MC, OVLY and DROM bits of PMST register for each TMS320VC5421 DSP core shall be set to the '0', '1' and '1' values correspondingly. This is required in order to set HPI mode and enable DSP on-chip shared program RAM, map DARAMA and DARAMB DSP on-chip data RAM areas into program memory address space, and to enable SARAMA and SARAMB in-chip data RAM areas.
- The SWWSR register (hex address 0028H) of each TMS320VC5421 DSP core must be set to the 0x0000 value.
- The SWCR register (hex address 002BH) of each TMS320VC5421 DSP core must be set to the 0x0000 value.
- The BSCR register (hex address 0029H) of each TMS320VC5421 DSP core must be set to the 0x8000 value.
- The GPIO0_DIR bit (bit #D8) of GPIOCR register (hex address 003CH) of each TMS320VC5421 DSP core must be set to the '1' value in order configure GPIO0 I/O pin as the output pin for optional SIOX rev.B DCM reset control (refer to the corresponding subsection below for more details).
- The *CLKMD* register (hex address 0058H) of TMS320VC5421 DSP core #A must be set to the 0x17F7H value in order to configure PLLx2 mode and 100 MHz internal DSP clock.

CAUTION

For more information about PMST, SWWSR, SWCR, BSCR, GPIOCR and CLKMD TMS320VC5421 DSP on-chip registers refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TMS320VC5421 DSP on-chip core-to-core communication and inter-DSP core-to-core communication

Each on-board TMS320VC5421 DSP provides on-chip facilities for core-to-core communication via on-chip 128K shared RAM, on-chip bi-directional FIFO and mutual core-to-core interrupts.

CAUTION

For more information about TMS320C5421 DSP on-chip core-to-core communication refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TORNADO-PX5421Q DCM also offers inter-DSP core-to-core communication via McBSP-2 serial ports, which are connected on-board between DSP cores of different DSP chips. The following inter-DSP core-to-core communications via McBSP-2 ports are supported:

- core #A or DSP #0 (DSP core #0A) can communicate with core #A of DSP #1 (DSP core #1A) via McBSP-2 ports
- core #B or DSP #0 (DSP core #0B) can communicate with core #B of DSP #2 (DSP core #2B) via McBSP-2 ports
- core #A or DSP #2 (DSP core #2A) can communicate with core #A of DSP #3 (DSP core #3A) via McBSP-2 ports
- core #B or DSP #1 (DSP core #1B) can communicate with core #B of DSP #3 (DSP core #3B) via McBSP-2 ports.

TORNADO-PX5421Q DCM provides direct wire-to-wire connection of McBSP-2 ports of DSP cores for inter-DSP core-to-core communication as shown at fig.2-3.

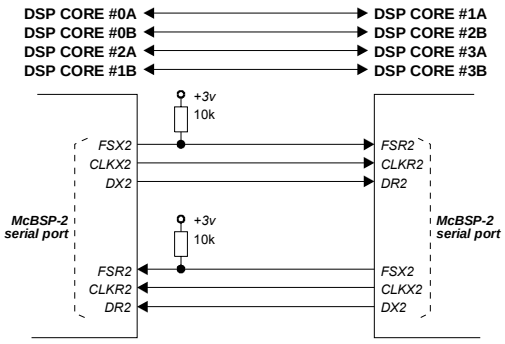


Fig.2-3. McBSP-2 port connection for inter-DSP core-to-core communication.

Note that all frame synchronization signals (FSX and FSR) are pulled-up in order to exclude false transmissions during McBSP-2 port software configuration procedure and to increase noise immunity.

CAUTION

Polarity of transmitter and receiver frame synchronization signals (FSX/FSR) shall be configured as active low via McBSP-2 PCR register of all TMS320VC5421 DSP cores.

It is up to user DSP software application how to configure TMS320VC5421 DSP on-chip McBSP-2 ports for inter-DSP core-to-core communication (clock source, clock frequency, frame synchronization source, data word length, data frame length, etc) in order to best meet customer application.

TMS320C5421 HPI port

TORNADO-PX5421Q DCM offers access from host *TORNADO* DSP system/controller to TMS320C5421 DSP on-chip multiplexed HPI port via host PIOX-16 interface in order to upload executable code and read/write real-time data.

TMS320C5421 DSP features enhanced HPI16 HPI port and allows access from host *TORNADO* to all DSP on-chip memory. All HPI port features are supported, including mutual interrupt generation between host *TORNADO* DSP system/controller and each TMS320C5421 DSP core.

CAUTION

For more information about TMS320C5421 DSP HPI port refer to section “Host PIOX-16 Interface” later in this chapter and to original TI TMS320VC5421 datasheet and user’s guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

Support for SIOX rev.B DCM

TORNADO-PX5421Q DCM provides on-board facilities for optional connection of up to eight external SIOX rev.B DCM (one SIOX rev.B DCM per each TMS320VC5421 DSP core) for real-time signal I/O, that converts *TORNADO-PX5421Q* DCM into universal DSP and application specific I/O coprocessor.

Each external *T/SU-X1* SIOX rev.B mini-extender can carry one full-size SIOX rev.B DCM and connects to any of *TORNADO-PX5421Q* DCM on-board MXSIOX-0A..3B connectors (JP3..JP10) (fig.2-1 and 2-2). Each of eight on-board of MXSIOX connectors connects to particular TMS320VC5421 DSP core and comprises of signals for two McBSP-0 and McBSP-1 serial ports, timer/IO lines, DSP interrupt request inputs, SIOX reset control, and ±5v/±12v host power supply lines.

For more details about MXSIOX connectors and external *T/SU-X1* SIOX rev.B mini-extenders refer to section “Serial I/O Expansion (SIOX) Interface” later in this chapter and appendix ‘C’ later in this manual.

TMS320VC5421 DSP General Purpose I/O (GPIO) pins

TORNADO-PX5421Q DCM utilizes general purpose I/O (GPIO) pins GPIO0, GPIO2 and GPIO3 of each TMS320VC5421 DSP core as SIOX reset, *XIO-1* and *TM/XIO-0* signals correspondingly of on-board MXSIOX-0A..3B connectors for connection to external *T/SU-X1* SIOX rev.B mini-extenders.

CAUTION

Neither GPIO1 nor XF general purpose I/O pins of TMS320VC5421 DSP cores are not used by *TORNADO-PX5421Q* DCM.

For more details about usage of GPIO0, GPIO2 and GPIO3 general purpose I/O pins of TMS320VC5421 DSP cores in SIOX rev.B DCM interfaces of *TORNADO-PX5421Q* DCM refer to section “Serial I/O Expansion (SIOX) Interface” later in this chapter and appendix ‘C’ later in this manual.

External interrupt inputs for TMS320VC5421 DSP cores

TORNADO-PX5421Q DCM utilizes INT0 and INT1 active low external interrupt request inputs of each TMS320VC5421 DSP core as *IRQ-0* and *IRQ-1* external active low interrupt request inputs at optional external SIOX rev.B DCM site via on-board MXSIOX-0A..3B connectors and external *T/SU-X1* SIOX rev.B mini-extenders (fig.2-1).

CAUTION

TORNADO-PX5421Q DCM does not utilize NMI active low external non-maskable interrupt request inputs of each TMS320VC5421 DSP core.

For more details about usage of INT0 and INT1 external interrupt request for TMS320VC5421 DSP cores in SIOX rev.B DCM interfaces of *TORNADO-PX5421Q* DCM refer to section "Serial I/O Expansion (SIOX) Interface" later in this chapter and appendix 'C' later in this manual.

CAUTION

For more information about external interrupt request inputs of TMS320VC5421 DSP refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

Generating DSP-to-host interrupt request from TMS320VC5421 DSP core to-host TORNADO DSP system/controller

TORNADO-PX5421Q DCM allows to generate interrupt request from each TMS320VC5421 DSP core to host *TORNADO* DSP system/controller via the corresponding *HPIxx_HINT* DSP-to-host interrupt request via DSP on-chip HPI port (*xx* suffix of *HPIxx_HINT* interrupt request denotes number of TS320VC5421 DSP core and is within *0A..3B* range).

HPIxx_HINT interrupt request can be set by TMS320VC5421 DSP software by writing to bit *HINT* of HPIC register of the corresponding TMS320VC5421 DSP core. Current state of *HPIxx_HINT* interrupt request can be read by host via *HOST_HPI_HINT_STAT_RG* DSP-to-host interrupt requests status register of host PIOX-16 interface and via HPIC register of HPI port of TMS320VC5421 DSP core *#xx*. Active *HPIxx_HINT* interrupt request can be cleared by host *TORNADO* DSP system/controller by means of writing to the *HINT* bit of HPIC register of TMS320VC5421 DSP core *#xx*.

HPIxx_HINT interrupt request can generate active host PIOX-16 interrupt request via any of four PIOX-16 interrupt request inputs. Particular #N-th host PIOX-16 interrupt request input, which is used to forward *HPIxx_HINT* DSP-to-host interrupt request to host *TORNADO* DSP system/controller, must be enabled via *HOST_HIRQ_EN_RG* register of host PIOX-16 interface and the corresponding *HOST_HIRQn_IE_RG* host #N-th interrupt enable mask register of host PIOX-16 interface must have *HPIxx_HINT_IE* bit set to '1' state.

For more details about how to enable host PIOX-16 interrupts refer to section "Host PIOX-16 Interface" later in this chapter.

CAUTION

For more information about *HINT* DSP-to-host interrupt request via HPI port of TMS320VC5421 DSP refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

Processing host-to-DSP interrupt request from host TORNADO DSP system/controller to TMS320VC5421 DSP core

TORNADO-PX5421Q DCM allows to generate interrupt request from *TORNADO* DSP system/controller to each TMS320VC5421 DSP core via the *DSPINT* host-to-DSP interrupt request of the corresponding HPI port.

Particular host-to-DSP interrupt request can be set by software of host *TORNADO* DSP system/controller by writing to the *DSPINT* bit of HPIC register of the corresponding TMS320VC5421 DSP core. Although *DSPINT* bit is not available for read-back polling neither via host PIOX-16 interface, nor for the corresponding TMS320VC521 DSP software, it can generate active DSP core internal interrupt in case bit *HPINT* of TMS320VC5421 DSP on-chip IMR register is set to the '1' state.

CAUTION

For more information about *DSPINT* host-to-DSP interrupt request via HPI port of TMS320VC5421 DSP refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

2.3 Serial I/O Expansion Interface (SIOX)

TORNADO-PX5421Q DCM provides on-board facilities for optional connection of up to eight external SIOX rev.B DCM (one SIOX rev.B DCM per each TMS320VC5421 DSP core) for real-time signal I/O, that converts *TORNADO-PX5421Q* DCM into universal DSP and application specific I/O coprocessor.

A variety of SIOX rev.B DCM for *TORNADO* DSP systems, controllers and coprocessors include speech/fax/modem AD/DA DCM, telecom interfaces, audio AD/DA, DAT interface, multi-channel instrumentation AD/DA/DIO DCM, application specific I/O coprocessors, and many more.

Connection of SIOX rev.B DCM to TORNADO-PX5421Q on-board DSP cores

SIOX rev.B DCM connect to particular TMS320VC5421 DSP cores of *TORNADO-PX5421Q* on-board DSP via external *T/SU-X1* SIOX rev.B mini-extenders (fig.2-4), which connect to *TORNADO-PX5421Q* DCM via on-board MXSIOX-0A..3B connectors (JP3..JP10). Each *T/SU-X1* SIOX rev.B mini-extender can carry one full-size SIOX rev.B DCM.

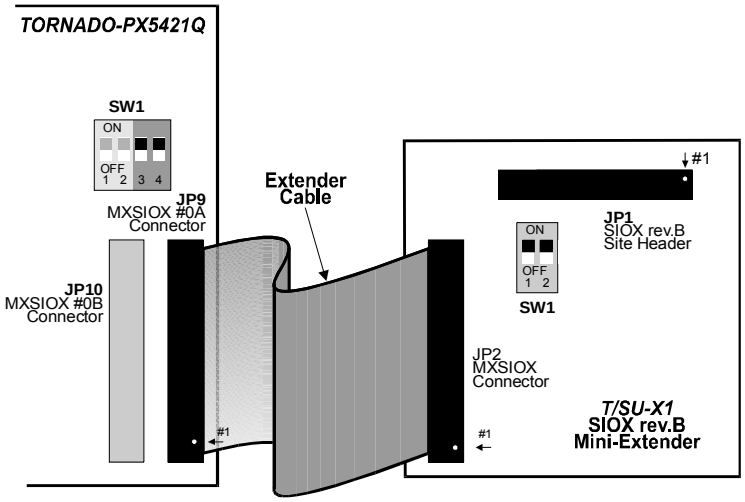


Fig.2-4a. Connection of *T/SU-X1* SIOX rev.B mini-extender to *TORNADO-PX5421Q* on-board TMS320VC5421 DSP core #0A.

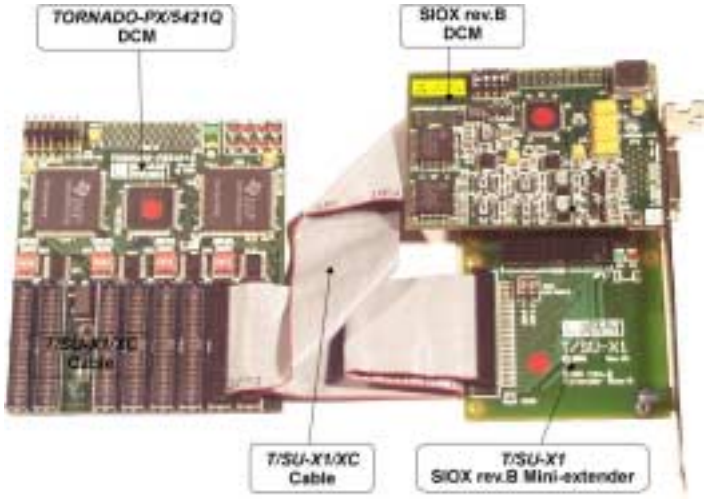


Fig.2-4b. *TORNADO-PX5421Q* DCM with two *T/SU-X1* SIOX rev.B mini-extenders and one installed SIOX rev.B DCM.

For more information about external *T/SU-X1* SIOX rev.B mini-extenders refer to appendix 'C' later in this manual.

On-board SIOX rev.B interface path for connection to external T/SU-X1 SIOX rev.B mini-extenders

SIOX rev.B interface sites for *TORNADO* DSP systems, controllers and coprocessors generally comprise of signals for SIO-0 and SIO-1 serial ports, two timer/IO lines, external interrupt request inputs, SIOX reset signal and power supply lines.

TORNADO-PX5421Q on-board SIOX rev.B interface path for connection to external *T/SU-X1* SIOX rev.B mini-extenders for each of eight TMS320VC5421 DSP cores (fig.2-5) comprises of the following signals and components:

- DSP core' McBSP-0 and McBSP-1 serial ports, which connect to SIO-0 and SIO-1 serial ports at MXSIOX connector
- *TM/XIO-0* and *XIO-1* timer/IO lines at MXSIOX connector, which connect to the DSP core' GPIO3 and GPIO2 pins correspondingly
- *IRQ-0/1* two external DSP interrupt request inputs at MXSIOX connector, which connect to the DSP core' INT0 and INT1 pins correspondingly
- Active low *RESET* SIOX reset control output at MXSIOX connector, which connects to the DSP core' GPIO0 pin
- ±5v/±12v host PIOX-16 power supply lines
- dedicated on-board MXSIOX connector
- two dedicated on-board switches, which enable common serial clock for transmitter and receiver (CLKX/CLKR) for each SIO port of MXSIOX connector.

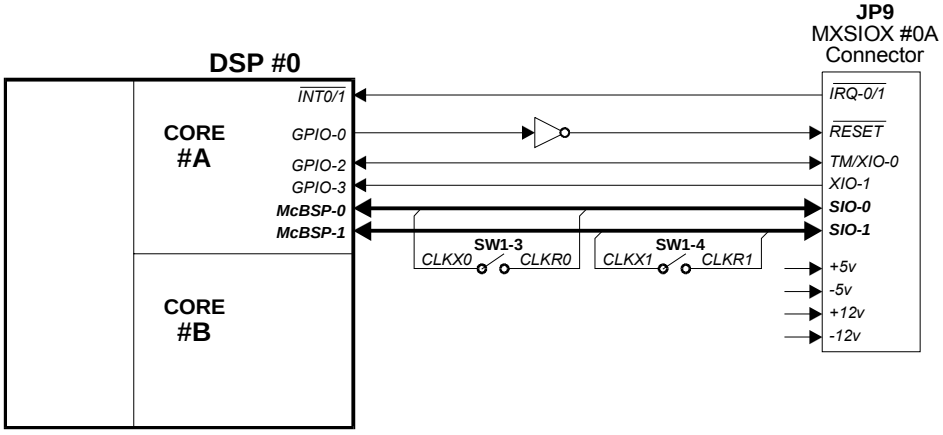


Fig.2-5. SIOX rev.B interface path for connection to external *T/SU-X1* SIOX rev.B mini-extenders for TMS320VC5421 DSP core #0A.

MXSIOX connector pinout and signal description

TORNADO-PX5421Q on-board MXSIOX connectors are Samtec 34-pin dual-row 2mm guarded male headers. Although MXSIOX plugs come standard with *T/SU-X1/XC* SIOX rev.B mini-extender connection cables (refer to appendix "C" for more details), optional MXSIOX plugs for 2mm flat cables are available from MicroLAB Systems upon request.

MXSIOX connector pinout is presented at fig.2-6, whereas signal description is provided in table 2-1.

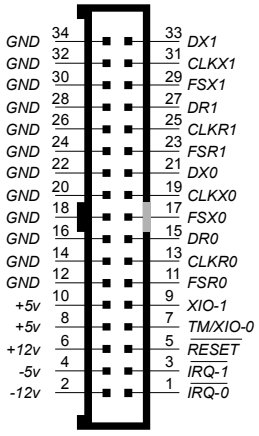


Fig.2-6. Pinout for *TORNADO-PX5421Q* on-board MXSIOX connector (top view).

Table 2-1. Signal description for *TORNADO-PX5421Q* on-board MXSIOX connector.

SIOX rev.B interface signal	signal type	Description
		SIO-0 port control
DX0 *FSX0* *CLKX0*	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port, which connect to the transmitter control signals for TMS320VC5421 DSP core' on-chip McBSP-0 serial port.
DR0 *FSR0* *CLKR0*	I I I	Data, frame synchronization and serial clock signals for receiver of SIO-0 port, which connect to the receiver control signals for TMS320VC5421 DSP core' on-chip McBSP-0 serial port.
		SIO-1 port control
DX1 *FSX1* *CLKX1*	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port, which connect to the transmitter control signals for TMS320VC5421 DSP core' on-chip McBSP-1 serial port.
DR1 *FSR1* *CLKR1*	I I/O I	Data, frame synchronization and serial clock signals for receiver of SIO-1 port, which connect to the receiver control signals for TMS320VC5421 DSP core' on-chip McBSP-1 serial port.
		Timers/IO, DSP Reset and Interrupt Requests
TM/XIO-0	I/O	Timer/IO pin, which connects to TMS320VC5421 DSP core' GPIO3 pin. This pin can be configured via TMS320VC5421 DSP core' GPIOCR register as either timer output, or input, or output pin. Refer to the corresponding subsection below for more details.

XIO-1	I/O	I/O pin, which connects to TMS320VC5421 DSP core' GPIO2 pin. This pin can be configured via TMS320VC5421 DSP core' GPIOCR register as either input or output pin. Refer to the corresponding subsection below for more details.
$\overline{RESET}$	O	Active low SIOX reset output pin, which connects to TMS320VC5421 DSP core' GPIO0 pin. This pin must be configured via TMS320VC5421 DSP core GPIOCR register as output pin. Refer to the corresponding subsection below for more details.
$\overline{IRQ-0}$ $\overline{IRQ-1}$	I	Active low external interrupt request inputs, which connect to the for TMS320VC5421 DSP core' *INT0* and *INT0* inputs correspondingly. Active DSP core' external interrupt requests are generated on the falling edge (1→0) of $\overline{IRQ-0}$ and $\overline{IRQ-1}$.. inputs.
Power Supplies		
GND		Ground.
+5v		+5v power (from host PIOX-16 interface).
+12v		+12v power (from host PIOX-16 interface).
-5v		-5v power (from host PIOX-16 interface).
-12v		-12v power (from host PIOX-16 interface).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v CMOS signals.

Programming MXSIOX TM/XIO and SIOX reset control pins

TORNADO-PX5421Q DCM utilizes general purpose I/O (GPIO) pins GPIO0, GPIO2 and GPIO3 of each TMS320VC5421 DSP core as SIOX reset, *XIO-1* and *TM/XIO-0* signals correspondingly of on-board MXSIOX-0A..3B connectors for connection to external *T/SU-X1* SIOX rev.B mini-extenders in accordance with table 2-2. Note, that GPIO0, GPIO2 and GPIO3 pins of each TMS320VC5421 DSP core shall be configured via GPIOCR TMS320VC521 DSP on-chip register for *TORNADO-PX5421Q* DCM.

Table 2-2. Configuration of GPIO pins for TMS320VC5421 DSP cores.

DSP GPIO pin	SIOX rev.B site function	I/O mode (GPIOCR setting)	value on DSP reset	Description
GPIO0	*RESET*	OUT (GPIOCR |= 0x0100)	1@IN	GPIO0 pin of TMS320VC5421 DSP core is used as *SX_RESET* reset signal for optional external SIOX rev.B site of the corresponding TMS320VC5421 DSP core via the corresponding MXSIOX on-board connector and external *T/SU-X1* external SIOX rev.B mini-extender. DSP software controlled SIOX reset signal allows correct initialization of the SIOX DCM hardware and correct synchronization with the DSP software.*GPIO0 pin must be always configured as output* in case external *T/SU-X1* external SIOX rev.B mini-extender is connected to the corresponding MXSIOX on-board connector and SIOX rev.B DCM is installed. GPIO0 pin has on-board pull-up in order to set active SX_RESET on DSP reset condition. *GPIO0* =0 while GPIO0 pin is configured as the output pin corresponds to the 'RUN' state of the corresponding *SX_RESET* signal of external SIOX rev.B site, i.e. SIOX reset signal is being released. *GPIO0* =1 while GPIO0 pin is configured as the output pin corresponds to active 'RESET' state of the corresponding *SX_RESET* signal of external SIOX rev.B site, i.e. SIOX reset signal is being set. This state is set as default on DSP reset condition due to the on-board pull-up resistor.
GPIO3	*TM/XIO-0*	IN/OUT/TMOUT IN (GPIOCR &= ~0x8800) OUT (GPIOCR &= ~0x8000; GPIOCR |= 0x0800) TMOUT (GPIOCR |= 0x8000)	x@IN	GPIO3 pin of TMS320VC5421 DSP core is used as *TM/XIO-0* timer/IO signal for optional external SIOX rev.B site of the corresponding TMS320VC5421 DSP core via the corresponding MXSIOX on-board connector and external *T/SU-X1* external SIOX rev.B mini-extender. *GPIO3 pin can be configured either as input, or output, or timer output pin* in case external *T/SU-X1* external SIOX rev.B mini-extender is connected to the corresponding MXSIOX on-board connector and SIOX rev.B DCM is installed.
GPIO2	*XIO-1*	IN/OUT IN (GPIOCR &=~ 0x0400) OUT (GPIOCR |= 0x0400)	x@IN	GPIO2 pin of TMS320VC5421 DSP core is used as *XIO-1* IO signal for optional external SIOX rev.B site of the corresponding TMS320VC5421 DSP core via the corresponding MXSIOX on-board connector and external *T/SU-X1* external SIOX rev.B mini-extender. *GPIO2 pin can be configured either as input or output pin* in case external *T/SU-X1* external SIOX rev.B mini-extender is connected to the corresponding MXSIOX on-board connector and SIOX rev.B DCM is installed.

Note: 1. I/O modes: IN – input; OUT – output, TMOUT – timer output.
2. Values on DSP reset condition: 1@IN - output '1' state with I/O input mode; x@IN - unknown output state with I/O input mode.
3. GPIOCR denotes TMS320VC5421 DSP on-chip GPIO control register (hex address 003CH).

CAUTION

For more information about GPIO pins and GPIOCR TMS320VC5421 DSP on-chip register refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

Maximum serial clock frequency for SIOX rev.B DCM

Although maximum output serial clock frequency for McBSP serial ports of TMS320VC5421 DSP cores is 50 MHz, maximum serial clock frequency for McBSP-0/1 port of *TORNADO-PX5421Q* DCM is limited by the length of connection cables, which are used for connection to external *T/SU-X1* SIOX rev.B mini-extenders, and particular by serial clock distribution configuration for installed SIOX rev.B DCM.

CAUTION

In case standard 10" long (0.25m) cable is used for connection of *TORNADO-PX5421Q* DCM to external *T/SU-X1* SIOX rev.B mini-extenders and the corresponding *TORNADO-PX5421Q* on-board common serial clock enable switch (SW1..SW4) is set to 'OFF' (refer to the corresponding subsection below for more details) , then the recommended maximum serial clock frequency for CLKX/CLKR signals for McBSP-0/1 serial ports is 33 MHz.

CAUTION

In case standard 10" long (0.25m) cable is used for connection of *TORNADO-PX5421Q* DCM to external *T/SU-X1* SIOX rev.B mini-extenders and the corresponding *TORNADO-PX5421Q* on-board common serial clock enable switch (SW1..SW4) is set to 'ON' (refer to t (refer to the corresponding subsection below for more details) , then the recommended maximum serial clock frequency for CLKX/CLKR signals for McBSP-0/1 serial ports is 20 MHz.

Common CLKX/CLKR serial clock enable control for SIOX rev.B DCM

TORNADO-PX5421Q DCM provides on-board common CLKX/CLKR serial clock enable switches (SW1..SW4) for each of on-board MXSIOX connectors (fig.2-1 and fig.2-5). Each MXSIOX connector has two corresponding common serial clock enable switches (one switch per each SIO port) in accordance with table A-1.

CAUTION

In case *TORNADO-PX5421Q* on-board common serial clock enable switch is set to 'ON', then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are connected together on-board.

In case *TORNADO-PX5421Q* on-board common serial clock enable switch is set to 'OFF', then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are disconnected on-board.

TORNADO-PX5421Q DCM on-board common serial clock enable switches shall be used in conjunction with *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switches (SW1 and SW2) in accordance with general guidelines provided in appendix 'C' of this manual and below in this subsection.

Background for usage *TORNADO-PX5421Q* on-board common CLKX/CLKR serial clock enable switches and *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) enable switches is the 'long-line' compensation issue for serial clock signals distribution over connection flat cable between *TORNADO-PX5421Q* on-board MXSIOX connector and *T/SU-X1* SIOX rev.B mini-extender due to the 'long-line wave nature' of connection flat cable.

Although the 'long-line' compensation resistors are being used for all McBSP-0/1 control signals (frame synchronization pulse, serial clock and serial data) at both *TORNADO-PX5421Q* DCM and *T/SU-X1* SIOX rev.B mini-extender boards in order to exclude signal reflection, a 'long-line' non-compensation for serial clock signals can still occur in case installed SIOX rev.B DCM is using common shorted serial clock for transmitter and receiver of SIO port (many SIOX rev.B DCM actually use this in order to simplify design). Note, that this problem does not occur with SIO port frame synchronization and serial data signals, since these signals always use dedicated lines of SIOX interface and can't be connected together.

CAUTION

In case installed SIOX rev.B DCM has been designed without on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and each serial clock is using its dedicated pins, then the corresponding *TORNADO-PX5421Q* on-board common CLKX/CLKR serial clock enable switch must be set to 'OFF' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'ON'.

In case installed SIOX rev.B DCM has been designed with on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and both serial clocks are using shared pins, then the corresponding *TORNADO-PX5421Q* on-board common CLKX/CLKR serial clock enable switch must be set to 'ON' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'OFF'.

For more information about external *T/SU-X1* SIOX rev.B mini-extenders refer to appendix 'C' later in this manual.

2.4 Host PIOX-16 Interface

Host 16-bit PIOX-16 interface of *TORNADO-PX5421Q* DCM provides access from host *TORNADO* DSP system/controller to a set of control registers and to TMS320VC5421 DSP on-chip HPI ports. On-board JP1 connector of *TORNADO-PX5421Q* DCM (fig.2-2 and A-1) is used to install into PIOX-16 site of host *TORNADO* DSP system/controller.

host PIOX-16 interface address map

Host PIOX-16 interface address map for *TORNADO-PX5421Q* DCM comprises of control register area and TMS320VC5421 DSP on-chip HPI ports area. Table 2-3 specifies details about host PIOX-16 interface address map.

Table 2-3. Host PIOX-16 interface address map.

host PIOX-16 interface register	default value on PIOX-16 interface reset condition	access mode	address range (in 16-bit data words)
Control Registers area			
HOST_CNTR1_RG register (DSP cores reset control)	00H	r/w	*BA* + 0000H**WAS* (bits D0..D7 only)
HOST_CNTR2_RG register (DSP HPI reset and HPI access timeout enable control)	00H	r/w	*BA* + 0001H**WAS* (bits D0..D7 only)

HOST_HIRQ_EN_RG register (host PIOX-16 interrupt lines enable control)	00H	r/w	*BA* + 0004H**WAS* (bits D0..D7 only)
HOST_HPI_HINT_STAT_RG register (status of DSP-to-host interrupt requests via HPI)	-	r	*BA* + 0008H**WAS* (bits D0..D7 only)
HOST_HPI_TMOUT_ERR_STAT_RG register (HPI access error status)	-	r	*BA* + 0009H**WAS* (bits D0..D7 only)
HOST_CLR_HPI0_TMOUT_ERR_RG register (clear HPI timeout error for DSP0)	-	w	*BA* + 000CH**WAS* (written data is ignored)
HOST_CLR_HPI1_TMOUT_ERR_RG register (clear HPI timeout error for DSP1)	-	w	*BA* + 000CH**WAS* (written data is ignored)
HOST_CLR_HPI2_TMOUT_ERR_RG register (clear HPI timeout error for DSP2)	-	w	*BA* + 000CH**WAS* (written data is ignored)
HOST_CLR_HPI3_TMOUT_ERR_RG register (clear HPI timeout error for DSP3)	-	w	*BA* + 000CH**WAS* (written data is ignored)
HOST_HIRQ0_IE1_RG register (interrupt enable/mask register #1 for host PIOX-16 interrupt request line IRQ-0)	00H	r/w	*BA* + 0010H**WAS* (bits D0..D7 only)
HOST_HIRQ0_IE2_RG register (interrupt enable/mask register #2 for host PIOX-16 interrupt request line HIRQ-0)	00H	r/w	*BA* + 0011H**WAS* (bits D0..D7 only)
HOST_HIRQ1_IE1_RG register (interrupt enable/mask register #1 for host PIOX-16 interrupt request line IRQ-1)	00H	r/w	*BA* + 0012H**WAS* (bits D0..D7 only)
HOST_HIRQ1_IE2_RG register (interrupt enable/mask register #2 for host PIOX-16 interrupt request line HIRQ-1)	00H	r/w	*BA* + 0013H**WAS* (bits D0..D7 only)
HOST_HIRQ2_IE1_RG register (interrupt enable/mask register #1 for host PIOX-16 interrupt request line IRQ-2)	00H	r/w	*BA* + 0014H**WAS* (bits D0..D7 only)
HOST_HIRQ2_IE2_RG register (interrupt enable/mask register #2 for host PIOX-16 interrupt request line HIRQ-2)	00H	r/w	*BA* + 0015H**WAS* (bits D0..D7 only)
HOST_HIRQ3_IE1_RG register (interrupt enable/mask register #1 for host PIOX-16 interrupt request line IRQ-3)	00H	r/w	*BA* + 0016H**WAS* (bits D0..D7 only)
HOST_HIRQ3_IE2_RG register (interrupt enable/mask register #2 for host PIOX-16 interrupt request line HIRQ-3)	00H	r/w	*BA* + 0017H**WAS* (bits D0..D7 only)

TMS320VC5421 DSP core #0A on-chip HPI ports area *(refer to TMS320VC5421 DSP documentation for more details about DSP on-chip HPI port)*			
HOST_HPIC0A_RG register (HPI control register)	0000H	r/w	*BA* + 0020H**WAS*
HOST_HPID0A_AINC_RG register (HPI data register with address postincrement)	-	r/w	*BA* + 0021H**WAS*
HOST_HPIA0A_RG register (HPI address register)	-	r/w	*BA* + 0022H**WAS*
HOST_HPID0A_RG register (HPI data register)	-	r/w	*BA* + 0023H**WAS*
TMS320VC5421 DSP core #0B on-chip HPI ports area *(refer to TMS320VC5421 DSP documentation for more details about DSP on-chip HPI port)*			
HOST_HPIC0B_RG register (HPI control register)	0000H	r/w	*BA* + 0024H**WAS*
HOST_HPID0B_AINC_RG register (HPI data register with address postincrement)	-	r/w	*BA* + 0025H**WAS*
HOST_HPIA0B_RG register (HPI address register)	-	r/w	*BA* + 0026H**WAS*
HOST_HPID0B_RG register (HPI data register)	-	r/w	*BA* + 0027H**WAS*
TMS320VC5421 DSP core #1A on-chip HPI ports area *(refer to TMS320VC5421 DSP documentation for more details about DSP on-chip HPI port)*			
HOST_HPIC1A_RG register (HPI control register)	0000H	r/w	*BA* + 0028H**WAS*
HOST_HPID1A_AINC_RG register (HPI data register with address postincrement)	-	r/w	*BA* + 0029H**WAS*
HOST_HPIA1A_RG register (HPI address register)	-	r/w	*BA* + 002AH**WAS*
HOST_HPID1A_RG register (HPI data register)	-	r/w	*BA* + 002BH**WAS*
TMS320VC5421 DSP core #1B on-chip HPI ports area *(refer to TMS320VC5421 DSP documentation for more details about DSP on-chip HPI port)*			
HOST_HPIC1B_RG register (HPI control register)	0000H	r/w	*BA* + 002CH**WAS*
HOST_HPID1B_AINC_RG register (HPI data register with address postincrement)	-	r/w	*BA* + 002DH**WAS*

HOST_HPIA1B_RG register (HPI address register)	-	r/w	*BA* + 002EH**WAS*
HOST_HPID1B_RG register (HPI data register)	-	r/w	*BA* + 002FH**WAS*
TMS320VC5421 DSP core #2A on-chip HPI ports area *(refer to TMS320VC5421 DSP documentation for more details about DSP on-chip HPI port)*			
HOST_HPIC2A_RG register (HPI control register)	0000H	r/w	*BA* + 0030H**WAS*
HOST_HPID2A_AINC_RG register (HPI data register with address postincrement)	-	r/w	*BA* + 0031H**WAS*
HOST_HPIA2A_RG register (HPI address register)	-	r/w	*BA* + 0032H**WAS*
HOST_HPID2A_RG register (HPI data register)	-	r/w	*BA* + 0033H**WAS*
TMS320VC5421 DSP core #2B on-chip HPI ports area *(refer to TMS320VC5421 DSP documentation for more details about DSP on-chip HPI port)*			
HOST_HPIC2B_RG register (HPI control register)	0000H	r/w	*BA* + 0034H**WAS*
HOST_HPID2B_AINC_RG register (HPI data register with address postincrement)	-	r/w	*BA* + 0035H**WAS*
HOST_HPIA2B_RG register (HPI address register)	-	r/w	*BA* + 0036H**WAS*
HOST_HPID2B_RG register (HPI data register)	-	r/w	*BA* + 0037H**WAS*
TMS320VC5421 DSP core #3A on-chip HPI ports area *(refer to TMS320VC5421 DSP documentation for more details about DSP on-chip HPI port)*			
HOST_HPIC3A_RG register (HPI control register)	0000H	r/w	*BA* + 0038H**WAS*
HOST_HPID3A_AINC_RG register (HPI data register with address postincrement)	-	r/w	*BA* + 0039H**WAS*
HOST_HPIA3A_RG register (HPI address register)	-	r/w	*BA* + 003AH**WAS*
HOST_HPID3A_RG register (HPI data register)	-	r/w	*BA* + 003BH**WAS*

TMS320VC5421 DSP core #3B on-chip HPI ports area *(refer to TMS320VC5421 DSP documentation for more details about DSP on-chip HPI port)*			
HOST_HPIC3B_RG register (HPI control register)	0000H	r/w	*BA* + 003CH**WAS*
HOST_HPID3B_AINC_RG register (HPI data register with address postincrement)	-	r/w	*BA* + 003DH**WAS*
HOST_HPIA3B_RG register (HPI address register)	-	r/w	*BA* + 003EH**WAS*
HOST_HPID3B_RG register (HPI data register)	-	r/w	*BA* + 003FH**WAS*

Notes:
1. Access modes: *r* - read only, *w* - write only, *r/w* - read/write.
2. '*BA*' denotes base address for host PIOX-16 interface within the address map of host DSP of host *TORNADO* DSP system/controller.
3. '*WAS*' denotes DSP word address step: *WAS*=1 for TMS320C3x and TMS320C54x DSP; *WAS*=4 for TMS320C6x DSP.

CAUTION

Host *TORNADO* DSP system/controller software must access *TORNADO-PX5421Q* DCM at PIOX-16 interface base address, which is specific for particular *TORNADO* DSP system/controller
(refer to documentation for your *TORNADO* DSP system/controller for more details about addressing PIOX-16 interface area).

CAUTION

When accessing *Control Register area* of host PIOX-16 interface from host *TORNADO* DSP system/controller, only data bits D0..D7 are valid.

When accessing *TMS320VC5421 DSP on-chip HPI ports area* of host PIOX-16 interface from host *TORNADO* DSP system/controller, data bits D0..D15 are valid.

CAUTION

PIOX-16 reset signal of host *TORNADO* DSP system/controller must be released prior communication with *TORNADO-PX5421Q* DCM.

HOST_CNTR1_RG register for DSP cores reset control

TORNADO-PX5421Q on-board TMS320VC5421 DSP core reset control is performed via *HOST_CNTR1_RG* register of host PIOX-16 interface. Note, that when accessing *HOST_CNTR1_RG* register, only data bits D0..D7 are valid.

HOST_CNTR1_RG register (r/w)

X	*DSP3B_GO (r/w, 0+)*	*DSP3A_GO (r/w, 0+)*	*DSP2B_GO (r/w, 0+)*	*DSP2A_GO (r/w, 0+)*	*DSP1B_GO (r/w, 0+)*	*DSP1A_GO (r/w, 0+)*	*DSP0B_GO (r/w, 0+)*	*DSP0A_GO (r/w, 0+)*
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-4 describes details about *HOST_CNTR1_RG* register bits.

Table 2-4. Register bits of *HOST_CNTR1_RG* register.

register bits	access mode	value on host PIOX-16 interface reset	Description
DSP0A_GO *DSP0B_GO* *DSP1A_GO* *DSP1B_GO* *DSP2A_GO* *DSP2B_GO* *DSP3A_GO* *DSP3B_GO*	r/w	0	Control reset signal for the corresponding TMS320VC5421 DSP cores #0A..#3B. *DSPxx_GO*=0 corresponds to the RESET state of the corresponding TMS320VC5421 DSP core. *DSPxx_GO*=1 corresponds to the 'GO' state of the corresponding TMS320VC5421 DSP core, i.e. no active reset signal is applied.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSPxx_GO bits of *HOST_CNTR1_RG* register control the individual reset signals for all TMS320VC5421 DSP cores. *HOST_CNTR1_RG* register allows to simultaneously release any combination of TMS320VC5421 DSP cores from the reset state and to synchronize on-board DSP cores operation. Refer to the corresponding subsection below for more details.

HOST_CNTR2_RG register for HPI reset control and host-to-HPI timeout enable control

HOST_CNTR2_RG register of host PIOX-16 interface must be used for common HPI port reset control for all TMS320V5421 DSP cores and to enable timeout control for host-to-HPI accesses. Note, that when accessing *HOST_CNTR2_RG* register, only data bits D0..D2 are valid.

HOST_CNTR2_RG register (r/w)

X	*HPI_TMOUT_EN (r/w, 0+)*	*0*	*0*	*0*	*0*	*0*	*0*	*HPI_GO (r/w, 0+)*
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-5 describes details about *HOST_CNTR2_RG* register bits.

Table 2-5. Register bits of *HOST_CNTR2_RG* register.

register bits	access mode	value on host PIOX-16 interface reset	Description
HPI_GO	r/w	0	Controls common reset signal for HPI ports of all on-board TMS320VC5421 DSP. *HPI_GO*=0 corresponds to the RESET state of HPI ports for all TMS320VC5421 DSP. *HPIxx_GO*=1 corresponds to the 'GO' state of HPI ports for all TMS320VC5421 DSP, i.e. no active HPI reset signal is applied and host *TORNADO* DSP system/controller can access HPI port data.
HPI_TMOUT_EN	r/w	0	Timeout enable for host-to-HPI access via host PIOX-16 interface for HPI ports of all TMS320VC5421 DSP cores. *HPI_TMOUT_EN*=0 corresponds to disabled timeout control for host-to-HPI accesses. In case any HPI access collision occurs with continuous missing HPI ready signal, then host PIOX-16 interface access cycle will remain active until DSP HPI ready signal comes active. This can result in infinite hanging of host *TORNADO* DSP environment. Infinitely active host-to-HPI access cycle can be aborted only by applying DSP reset signal to host *TORNADO* DSP system/controller. *HPI_TMOUT_EN*=0 corresponds to enabled timeout control for host-to-HPI access. In case any HPI access collision occurs with continuous missing HPI ready signal, then host PIOX-16 interface access cycle will remain active either until DSP HPI ready signal comes active or until timeout expires, whichever comes first. This will exclude possible hanging of host *TORNADO* DSP environment and exclude the need to apply reset signal to DSP of host *TORNADO* DSP system/controller in order to terminate pending host-to-HPI access cycle. In case the HPI access timeout occurs during access to any DSP core of DSP #n (n=0..3), then bit *HPIn_TMOUT_ERR* of *HOST_HI_TMOUT_ERR_STAT_RG* will be set and host PIOX-16 interrupt can be generated. Timeout period for host-to-HPI access is set to 640 ns.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

HPI_GO bit of *HOST_CNTR2_RG* register controls common HPI ports reset signal for all TMS320VC5421 DSP cores. It must be used in order to enable HPI ports operation. Refer to the corresponding subsection below for more details.

HPI_TMOUT_EN bit of *HOST_CNTR2_RG* register is used to enable the timeout control for host-to-HPI access cycles of host PIOX-16 interface of *TORNADO-PX5421Q* DCM. Refer to the corresponding subsection below for more details.

TMS320VC5421 DSP cores start-up procedure

Reset signals for on-board TMS320VC5421 DSP cores (which are controlled via *DSPxx_GO* bits of *HOST_CNTR1_RG* register) shall be used along with common HPI ports reset signal for all TMS320VC5421 DSP (which is controlled via *HPI_GO* bit *HOST_CNTR2_RG* register) in order to upload DSP code from host *TORNADO* DSP system/controller and to start-up the DSP cores.

Start-up procedure for TMS320VC5421 DSP cores is described in the corresponding subsection of "DSP Environment" section earlier in this chapter.

Host-to-HPI access timeout control

Timeout control for host-to-HPI access cycles of *TORNADO-PX5421Q* host PIOX-16 interface allows to exclude infinite hanging of host *TORNADO* DSP software due to probable infinite pending of host-to-HPI access cycles.

Infinite pending of host-to-HPI access cycle and of host *TORNADO* DSP environment can occur in case host performs access to the HPI port of the DSP chip whereas each DSP core (#A and #B) of this DSP chip has already executed IDLE3 instruction.

In case the HPI access timeout is enabled via *HPI_TMOUT_EN* bit of *HOST_CNTR2_RG* register, then host-to-HPI access cycle will be terminated either on the normal HPI ready condition or on the HPI access timeout condition.

Timeout interval for host-to-HPI access cycles is 640 ns. In case the timeout condition occurs, then the corresponding *HPIn_TMOUT_ERR* timeout error flag (n=0..3) of *HOST_HPI_TMOUT_ERR_STAT_RG* register will be set.

CAUTION

HPIn_TMOUT_ERR timeout error flags (n=0..3) are available for software polling via *HOST_HPI_TMOUT_ERR_STAT_RG* register of host PIOX-16 interface, and can generate interrupt requests to host *TORNADO* DSP system/controller via host PIOX-16 interface in case the corresponding interrupt enable bits are set in *HOST_HIRQx_IE2_RG* register (x=0..3) and the corresponding *IRQ-x* host PIOX-16 interrupt request line is selected via *HOST_HIRQ_EN_RG* register.

Once *HPIn_TMOUT_ERR* timeout error flag (n=0..3) has been set, it remains active until it will be cleared by host *TORNADO* DSP system/controller by writing to the corresponding *HOST_CLR_HPIn_TMOUT_ERR_RG* registers of host PIOX-16 interface.

Figure 2-7 illustrates operation of timeout controller for host-to-HPI access cycle of host PIOX-16 interface of *TORNADO-PX5421Q* DCM.

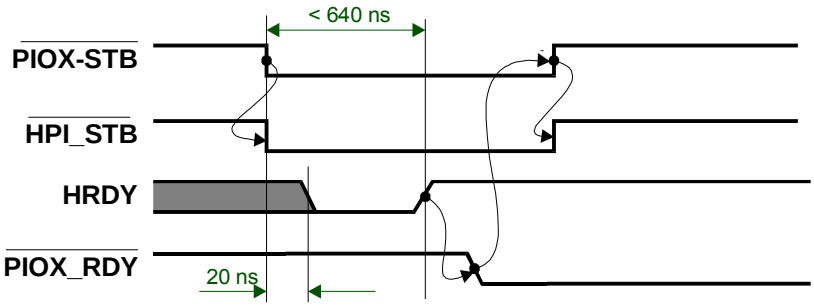


Fig.2-7a. Normal host-to-HPI access cycle without timeout condition.

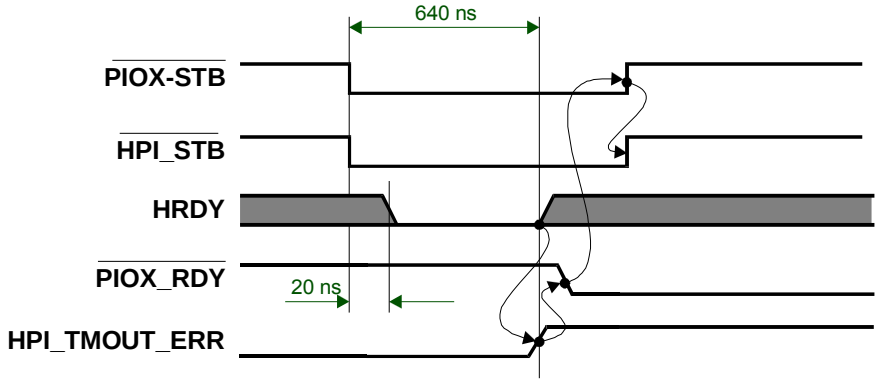


Fig.2-7b. Host-to-HPI access cycle terminated on timeout condition.

HOST_HPI_TMOUT_ERR_STAT_RG register for polling timeout flags for host-to-HPI access cycles

HOST_HPI_TMOUT_ERR_STAT_RG read-only register of host PIOX-16 interface must be used for software polling of timeout flags for host-to-HPI access cycles. Note, that when reading *HOST_HPI_TMOUT_ERR_STAT_RG* register, only data bits D0..D7 are valid.

HOST_HPI_TMOUT_ERR_STAT_RG register (r)

X	*0*	*0*	*0*	*0*	*HPI3_TMOUT_ERR (r, 0+)*	*HPI2_TMOUT_ERR (r, 0+)*	*HPI1_TMOUT_ERR (r, 0+)*	*HPI0_TMOUT_ERR (r, 0+)*
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-6 describes details about *HOST_HPI_TMOUT_ERR_STAT_RG* register bits.

Table 2-6. Register bits of *HOST_HPI_TMOUT_ERR_STAT_RG* register.

register bits	access mode	value on host PIOX-16 interface reset	description
HPI0_TMOUT_ERR *HPI1_TMOUT_ERR* *HPI2_TMOUT_ERR* *HPI3_TMOUT_ERR*	R	0	Indicates current status of individual timeout errors for host-to-HPI access via host PIOX-16 interface for DSP #0..#3. Note, that *HPIn_TMOUT_ERR* error flag is set in case of timeout condition during host access to the HPI port of either DSP #n (n=0..3) on-chip cores #A/#B. *HPIn_TMOUT_ERR*=0 corresponds to no timeout condition detected for host-to-HPI access via host PIOX-16 interface to the DSP #n on-chip cores #A/#B. *HPIn_TMOUT_ERR*=1 corresponds to active timeout condition detected for host-to-HPI access via host PIOX-16 interface to either of the DSP #n on-chip cores #A/#B. *HPIn_TMOUT_ERR* error flag remains in the '1' state until it will be cleared via host write to *HOST_CLR_HPIn_TMOUT_ERR_RG* register.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

HOST_CLR_HPIn_TMOUT_ERR_RG registers for clearing timeout errors of host-to-HPI access cycles

HOST_CLR_HPIn_TMOUT_ERR_RG write-only registers (n=0..3) of host PIOX-16 interface shall be used to clear *HPIn_TMOUT_ERR* timeout error flags of *HOST_HPI_TMOUT_ERR_STAT_RG* register. Note, that when writing to *HOST_CLR_HPIn_TMOUT_ERR_RG* write-only registers (n=0..3), written data is ignored.

HOST_CLR_HPIn_TMOUT_ERR_RG register (w)

X	x	X	x	x	x	x	x	x
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

host PIOX-16 interrupt requests control

TORNADO-PX5421Q DCM can generate interrupt requests to host *TORNADO* DSP system/controller using any combination of *IRQ-0..3* interrupt request inputs of host PIOX-16 interface. Each of host PIOX-16 interface *IRQ-0..3* host interrupt request outputs of *TORNADO-PX5421Q* DCM can be individually enabled and configured to generate output interrupt request as the logical OR of selected interrupt request sources.

The following are the control registers of *TORNADO-PX5421Q* host PIOX-16 interface, which are involved in generation of interrupt requests to host *TORNADO* DSP system/controller:

- *HOST_HIRQ_EN_RG* register, which is used to enable each of host PIOX-16 interface *IRQ-0..3* host interrupt request outputs. In case host PIOX-16 interface request output is disabled, then its output driver is in the Z-state, which meets on-board configuration of external interrupt request inputs via host PIOX-16 and SIOX interfaces of host *TORNADO* DSP system/controller.
- *HOST_HIRQn_IE1_RG* and *HOST_HIRQn_IE2_RG* registers (n=0..3), which are used to set interrupt request masks for each of host PIOX-16 interface *IRQ-0..3* host interrupt request outputs.

- *HOST_HPI_HINT_STAT_RG* and *HOST_HPI_TMOUT_ERR_STAT_RG* registers, which can be used for software polling of interrupt request sources for host PIOX-16 interrupt requests.

Each of host PIOX-16 interface *IRQ-0..3* host interrupt request outputs of *TORNADO-PX5421Q* DCM can be generated as the logical OR of the following individually maskable interrupt request sources:

- *HPIxx_HINT* (xx=0A..3B) DSP-to-host interrupt requests via DSP on-chip HPI port for each TMS320VC5421 DSP core, i.e. via *HINT* bit of HPIC register. Refer to section "DSP Environment" earlier in this chapter and original TI TMS320C54x documentation for more details.
- Logical OR of all timeout conditions occurred during host host-to-HPI access via host PIOX-16 interface.

CAUTION

IRQ-n host PIOX-16 interrupt requests (n=0..3)are generated as the logical OR of enabled interrupt request sources via *HOST_HIRQn_IE1_RG* and *HOST_HIRQn_IE2_RG* registers (n=0..3) in case this host interrupt request output of *TORNADO-PX5421Q* host PIOX-16 interface is enabled via *HIRQn_EN bit* of *HOST_HIRQ_EN_RG* register.

HOST_HPI_HINT_STAT_RG register for software polling of DSP-to-host interrupt requests via TMS320VC5421 DSP on-chip HPI ports

HOST_HPI_HINT_STAT_RG read-only register of host PIOX-16 interface must be used for software polling of DSP-to-host interrupt requests via HPI ports of TMS320VC5421 DSP on-chip cores. Note, that when reading *HOST_HPI_HINT_STAT_RG* register, only data bits D0..D7 are valid.

HOST_HPI_HINT_STAT_RG register (r)

X	*HPI3B_HINT (r, 0+)*	*HPI3A_HINT (r, 0+)*	*HPI2B_HINT (r, 0+)*	*HPI2A_HINT (r, 0+)*	*HPI1B_HINT (r, 0+)*	*HPI1A_HINT (r, 0+)*	*HPI0B_HINT (r, 0+)*	*HPI0A_HINT (r, 0+)*
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-7 describes details about *HOST_HPI_HINT_STAT_RG* register bits.

Table 2-7. Register bits of *HOST_HPI_HINT_STAT_RG* register.

register bits	access mode	value on host PIOX-16 interface reset	Description
HPI0A_HINT *HPI0B_HINT* *HPI1A_HINT* *HPI1B_HINT* *HPI2A_HINT* *HPI2B_HINT* *HPI3A_HINT* *HPI3B_HINT*	r	0	Indicates current status of DSP-to-host interrupt request via HPI port for each TMS320VC5421 DSP core, which corresponds to the current status of *HINT* bit of HPIC register of the corresponding TMS320VC5421 DSP core. *HPIxx_HINT*=0 corresponds to no DSP-to-host interrupt request via HPI port of the corresponding TMS320VC5421 DSP core #xx (xx=0A..3B). *HPIxx_HINT*=1 corresponds to active DSP-to-host interrupt request via HPI port of the corresponding TMS320VC5421 DSP core #xx (xx=0A..3B).

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DSP-to-host interrupt request via TMS320VC5421 DSP on-chip HPI port is actually the state of *HINT* bit of DSP core on-chip HPIC register. DSP-to-host interrupt request via TMS320VC5421 DSP on-chip HPI port can be set by DSP core only by means of writing '1' to *HINT* bit of DSP core on-chip HPIC register, whereas it can be cleared by host *TORNADO* DSP system/controller only by means of writing '1' to the HINT bit of the corresponding *HOST_HPICxx_RG* of host PIOX-16 interface of *TORNADO-PX5421Q* DCM.

Although current status of *HINT* bit of TMS320VC5421 DSP cores on-chip HPIC registers can be obtained by host *TORNADO* DSP system/controller by reading corresponding *HOST_HPICxx_RG* of host PIOX-16 interface of *TORNADO-PX5421Q* DCM, this requires up to eight read cycles in order to get current status of all DSP-to-host interrupt requests via HPI port for all TMS320VC5421 DSP cores. Instead, *HOST_HPI_HINT_STAT_RG* register allows to read current status of all DSP-to-host interrupt requests via HPI ports for all TMS320VC5421 DSP cores in one read cycle, which is important in order to increase systems performance in case software polling technique is used to recognize DSP-to-host interrupt requests via HPI ports of all TMS320VC5421 DSP cores.

CAUTION

For more information about *HINT* DSP-to-host interrupt request via HPI port of TMS320VC5421 DSP refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

HOST_HIRQ_EN_RG register for enabling host PIOX-16 interrupt request outputs

HOST_HPI_HIRQ_EN_RG register of host PIOX-16 interface must be used to enable (activate) particular *IRQ-0..3* host PIOX-16 interrupt request outputs, which will be used to generate interrupt requests from *TORNADO-PX5421Q* DCM to host *TORNADO* DSP system/controller. Note, that when accessing *HOST_HIRQ_EN_RG* register, only data bits D0..D7 are valid.

HOST_HIRQ_EN_RG register (r/w)

X	*0*	*0*	*0*	*0*	*HIRQ3_EN (r/w, 0+)*	*HIRQ2_EN (r/w, 0+)*	*HIRQ_EN (r/w, 0+)*	*HIRQ0_EN (r/w, 0+)*
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-8 describes details about *HOST_HIRQ_EN_RG* register bits.

Table 2-8. Register bits of *HOST_HIRQ_EN_RG* register.

register bits	access mode	value on host PIOX-16 interface reset	Description
HIRQ0_EN *HIRQ1_EN* *HIRQ2_EN* *HIRQ3_EN*	r/w	0	Controls output enable (activation) feature for the corresponding *IRQ-0..3* host interrupt request outputs of *TORNADO-PX5421Q* host PIOX-16 interface. *HIRQn_EN*=0 (n=0..3) disables corresponding *IRQ-n* host interrupt request output. *HIRQn_EN*=1 (n=0..3) enables (activates) corresponding *IRQ-n* host interrupt request output.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

Once particular *IRQ-n* (n=0..3) host interrupt request output of *TORNADO-PX5421Q* host PIOX-16 interface is enabled via the *HIRQx_EN* bit of *HOST_HIRQ_EN_RG* register, then this interrupt request output can generate interrupt requests to host *TORNADO* DSP system/controller in case any of unmasked interrupt sources via *HOST_HIRQn_IE1_RG* and *HOST_HIRQn_IE2_RG* registers comes active.

In case particular *IRQ-n* (n=0..3) host interrupt request output of *TORNADO-PX5421Q* host PIOX-16 interface is disabled via the *HIRQx_EN* bit of *HOST_HIRQ_EN_RG* register, then this interrupt request output will stay in the Z-state and cannot generate interrupt request to host TORNADO DSP system/controller. The contents of *HOST_HIRQn_IE1_RG* and *HOST_HIRQn_IE2_RG* registers are ignored in this case.

HOST_HIRQn_IE1_RG and HOST_HIRQn_IE2_RG interrupt mask registers for host PIOX-16 interrupt request outputs

HOST_HIRQn_IE1_RG and *HOST_HIRQn_IE2_RG* registers (x=0..3) of host PIOX-16 interface shall be used as interrupt mask registers for each of *IRQ-x* host PIOX-16 interrupt request outputs in order to enable generation of active *IRQ-x* host PIOX-16 interrupt requests as a logical OR of different enabled interrupt request source events. Note, that when accessing *HOST_HIRQn_IE1_RG* and *HOST_HIRQn_IE2_RG* registers, only data bits D0..D7 are valid.

HOST_HIRQ0_IE1_RG, HOST_HIRQ1_IE1_RG, HOST_HIRQ2_IE1_RG, and HOST_HIRQ3_IE1_RG registers (r/w)

X	*HPI3B_ HINT_IE (r/w, 0+)*	*HPI3A_ HINT_IE (r/w, 0+)*	*HPI2B_ HINT_IE (r/w, 0+)*	*HPI2A_ HINT_IE (r/w, 0+)*	*HPI1B_ HINT_IE (r/w, 0+)*	*HPI1A_ HINT_IE (r/w, 0+)*	*HPI0B_ HINT_IE (r/w, 0+)*	*HPI0A_ HINT_IE (r/w, 0+)*
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

HOST_HIRQ0_IE2_RG, HOST_HIRQ1_IE2_RG, HOST_HIRQ2_IE2_RG, and HOST_HIRQ3_IE2_RG registers (r/w)

bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
X	*TMOUT_IE (r/w, 0+)*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

Table 2-9 describes details about *HOST_HIRQn_IE1_RG* and *HOST_HIRQn_IE2_RG* registers bits.

Table 2-9. Register bits of *HOST_HIRQn_IE1_RG* and *HOST_HIRQn_IE2_RG* registers.

register bits	access mode	value on host PIOX-16 interface reset	Description
HPI0A_HINT_IE *HPI0B_HINT_IE* *HPI1A_HINT_IE* *HPI1B_HINT_IE* *HPI2A_HINT_IE* *HPI2B_HINT_IE* *HPI3A_HINT_IE* *HPI3B_HINT_IE*	r/w	0	Interrupt enable mask for generation of host PIOX-16 interrupt request on DSP-to-host interrupt request via HPI port of TMS320VC5421 DSP core #xx (xx=0A..3B). Host *IRQ-n* PIOX-16 interrupt request output (n=0..3), which owns this interrupt enable mask, is defined by the corresponding *HOST_HIRQn_IE1_RG* register. *HPIxx_HINT_IE*=0 (x=0A..3B) disables generation of corresponding host interrupt request on active DSP-to-host interrupt request via HPI port of TMS320VC5421 DSP core #xx. *HPIxx_HINT_IE*=1 (x=0A..3B) enables generation of corresponding host interrupt request on active DSP-to-host interrupt request via HPI port of TMS320VC5421 DSP core #xx.
TMOUT_IE	r/w	0	Interrupt enable mask for generation of host PIOX-16 interrupt request on summary timeout error event for host-to-HPI access cycles of *TORNADO-PX5421Q* host PIOX-16 interface. Summary timeout error event for host-to-HPI access cycles of *TORNADO-PX5421Q* host PIOX-16 interface is the logical OR of all *HPIx_TMOUT_ERR* timeout error flag (x=0..3) of *HOST_HPI_TMOUT_ERR_STAT_RG* register. Host *IRQ-n* interrupt request output, which owns this interrupt enable mask (n=0..3), is defined by the corresponding *HOST_HIRQn_IE2_RG* register. *TMOUT_IE*=0 disables generation of corresponding host interrupt request on summary timeout event for host-to-HPI access cycles. *TMOUT_IE*=1 enables generation of corresponding host interrupt request on summary timeout event for host-to-HPI access cycles.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

Once particular interrupt enable mask bit of either of *HOST_HIRQn_IE1_RG* and *HOST_HIRQn_IE2_RG* registers (n=0..3) is set to the '1' state and the *HIRQn_EN* bit of *HOST_HIRQ_EN_RG* register is to the '1' state, then active event at the corresponding host interrupt request source will generate active *IRQ-n* host interrupt request output of *TORNADO-PX5421Q* host PIOX-16 interface.

CAUTION

IRQ-n host PIOX-16 interrupt requests (n=0..3)are generated as the logical OR of enabled interrupt request sources via *HOST_HIRQn_IE1_RG* and *HOST_HIRQn_IE2_RG* registers (n=0..3) in case this host interrupt request output of *TORNADO-PX5421Q* host PIOX-16 interface is enabled via *HIRQn_EN bit* of *HOST_HIRQ_EN_RG* register.

TMS320VC5421 DSP core HPI areas

Host PIOX-16 interface of *TORNADO-PX5421Q* DCM provides eight TMS320VC5421 DSP core HPI areas each corresponding to particular TMS320VC5421 DSP core.

CAUTION

Each on-board TMS320VC5421 DSP of *TORNADO-PX5421Q* DCM is on-board configured to start in multiplexed HPI mode.

TMS320VC5421 DSP features on-chip enhanced HPI16 port, which operates in 16-bit mode and allows access to all DSP on-chip memory areas.

Each of eight TMS320VC5421 DSP core HPI areas comprises of four 16-bit HPI port registers for particular TMS320VC5421 DSP core #xx (xx=0A..3B):

- *HOST_HPICxx_RG* HPI control register (HPIC)
- *HOST_HPIAxx_RG* HPI address register (HPIA)
- *HOST_HPIDxx_RG* HPI data access register (HPID)
- *HOST_HPIDxx_AINC_RG* HPI data access register with HPI address postincrement feature (HPID_AINC).

TMS320VC5421 DSP on-chip HPI port allows access from host PIOX-16 interface of *TORNADO-PX5421Q* DCM to all DSP on-chip memory areas and memory-mapped McBSP ports register, allows to load DSP application code directly to DSP on-chip memory, and allows to generate host-to-DSP interrupt request via *DSPINT* bit of HPIC register for each on-board TMS320VC5421 DSP core.

Figure 2-8 shows HPI port memory map for each of the *TORNADO-PX5421Q* on-board TMS320VC5421 DSP cores.

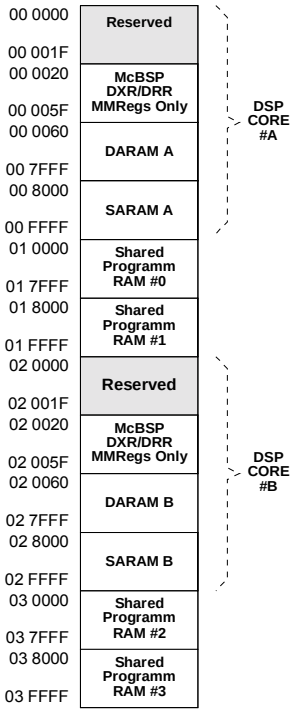


Fig.2-8. HPI port memory map for TMS320VC5421 DSP.

CAUTION

Although HPI ports for each of TMS320VC5421 DSP on-chip cores #A and #B features the same memory map and allows access to DSP on-chip memory areas of both DSP on-chip cores, access to dedicated DARAM and SARAM areas of particular DSP on-chip core and to the owned shared program RAM areas is performed faster via the HPI port of this DSP on-chip core.

CAUTION

For more information about TMS320VC5421 DSP on-chip HPI ports refer to original TI TMS320VC5421 datasheet and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

2.5 Emulation Tools for *TORNADO-PX5421Q*

TORNADO-PX5421Q uses scan-path emulation technique for on-board TMS320VC5421 DSP in order to debug on-board TMS320VC5421 DSP environment and software.

Compatible scan-path emulation tools include TI XDS510 or MicroLAB' *MIRAGE-510DX* universal JTAG/MPSD emulators with JTAG pod, which must connect to JP3 JTAG-IN connector on *TORNADO-PX5421Q* mainboard.

CAUTION

C5000 Code Composer Studio debugging tools shall use *TMS320C5000 SHARED MEMORY* driver and for multi-device JTAG path with eight C5000 DSP cores in order to provide correct operation of JTAG emulator hardware.

Each of *TORNADO-PX5421Q* on-board TMS320VC5421 DSP cores must be released from the RESET state prior running JTAG emulator software.

For more information about TMS320C5000 DSP debugging tools refer to original TI TMS320VC5421 datasheet and user's guides for C5000 Code Composer Studio development tools, which are supplied in either paper or electronic form together with this manual.

Chapter 3. Installation and Configuration

This chapter includes instructions for installation of *TORNADO-PX5421Q* DCM.

3.1 Installation onto *TORNADO* DSP System/Controller Mainboard

TORNADO-PX5421Q DCM must be installed as standard PIOX-16 DCM onto host *TORNADO* DSP system/controller mainboard.

For installation of *TORNADO-PX5421Q* DCM into PIOX-16 site of *TORNADO* DSP system/controller follow the recommendations below:

1. Switch off the power of host PC or of host *TORNADO* DSP controller.
2. Remove *TORNADO* mainboard from PC slot.
3. Ensure that two *TORNADO* on-board spacers for mounting PIOX-16 DCM are installed into the corresponding holes on *TORNADO* mainboard (fig.3-1). If spacers are not installed, then install spacers, which are enclosed with *TORNADO-PX5421Q* DCM kit.
4. Pick-up *TORNADO-PX5421Q* DCM AND orient it parallel to *TORNADO* mainboard over PIOX-16 DCM area. Safely plug-in on-board JP1 host PIOX-16 connector of *TORNADO-PX5421Q* DCM into the corresponding PIOX-16 site header of host *TORNADO* mainboard (fig.3-1a). In case host *TORNADO* mainboard provides on-board 32-bit PIOX interface site, then you have to plug *TORNADO-PX5421Q* DCM into the PIOX-16 sub-connector of host PIOX interface site at host *TORNADO* mainboard (fig.3-1b).

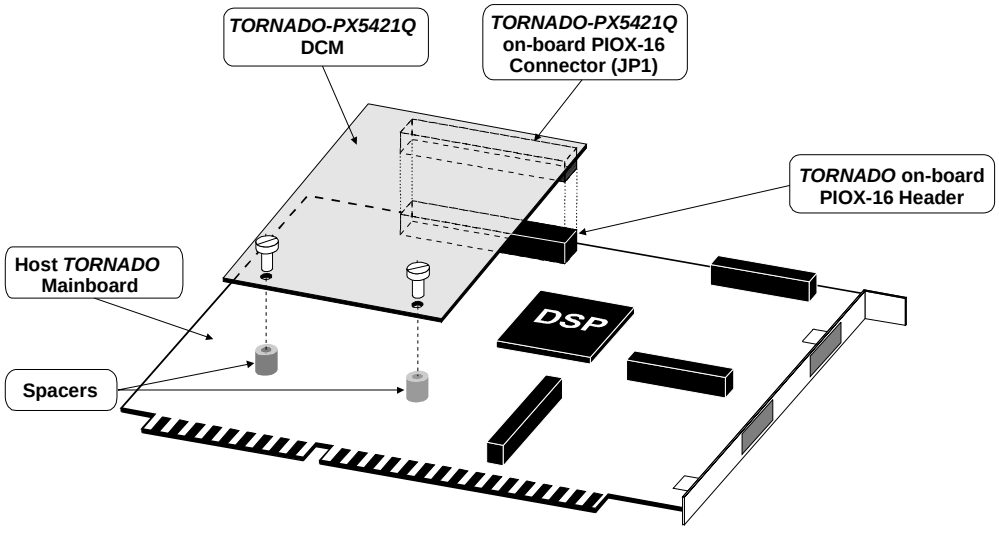


Fig. 3-1a. Installation of *TORNADO-PX5421Q* DCM into PIOX-16 site of host *TORNADO* DSP system.

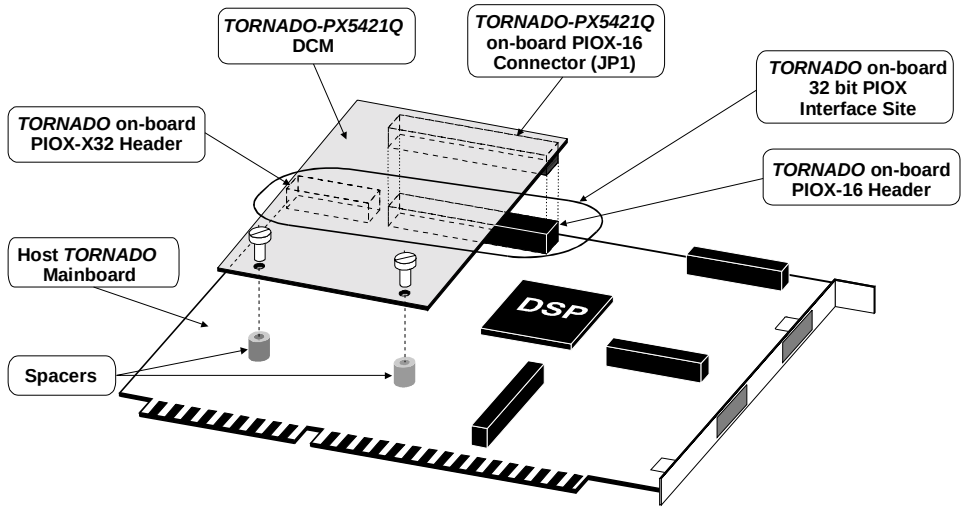


Fig. 3-1b. Installation of *TORNADO-PX5421Q* DCM into 32-bit PIOX site of host *TORNADO* DSP system.

5. Screw in *TORNADO-PX5421Q* DCM to the spacers at *TORNADO* mainboard.
6. If required, connect optional *T/SU-X1* external SIOX rev.B mini-extenders to *TORNADO-PX5421Q* DCM via on-board JP3..10 MXSIOX connectors (refer to section 2.3 and Appendix C).
7. If optional *T/SU-X1* external SIOX rev.B mini-extenders are connected to *TORNADO-PX5421Q* DCM, then install SIOX rev.B DCM onto *T/SU-X1* external SIOX rev.B mini-extenders and configure SIOX rev.B DCM in accordance with manuals.
8. If optional *T/SU-X1* external SIOX rev.B mini-extenders are connected to *TORNADO-PX5421Q* DCM, then configure *TORNADO-PX5421Q* on-board SW1..4 switches to meet serial clock configuration for connected SIOX rev.B DCM (refer to section 2.3 for more details).
9. In case *TORNADO* PC plug-in DSP system is used for installation of *TORNADO-PX5421Q* DCM, then install *TORNADO* mainboard into PC chassis slot and screw it to the rear panel of PC.
10. In case *TORNADO* PC plug-in DSP system is used for installation of *TORNADO-PX5421Q* DCM and in case optional *T/SU-X1* external SIOX rev.B mini-extenders are connected to *TORNADO-PX5421Q* DCM, then install and screw mounting bracket of *T/SU-X1* external SIOX rev.B mini-extenders at the rear panel of PC.
11. If optional *T/SU-X1* external SIOX rev.B mini-extenders with installed SIOX rev.B DCM are connected to *TORNADO-PX5421Q* DCM, then connect external I/O cables to installed SIOX rev.B DCM.
12. Switch on power of host PC or of host *TORNADO* DSP controller.

Appendix A. On-board Switches and Connectors.

This Appendix includes a summary description for *TORNADO-PX5421Q* on-board switches, connectors and LED.

Board layout for *TORNADO-PX5421Q* on-board switches, connectors and LED is presented at fig.A-1.

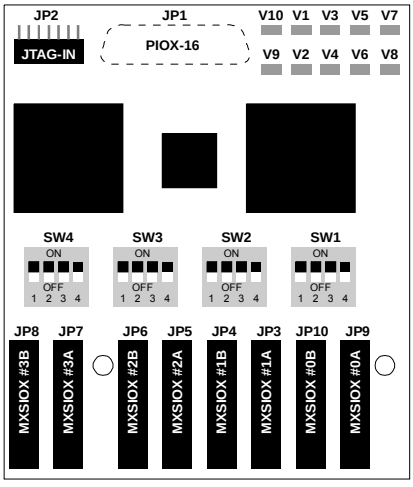


Fig.A-1. On-board switches, connectors and LED for *TORNADO-PX5421Q* DCM.

A.1 On-board Switches

Table A-1 contains the list of on-board switches.

Table A-1. On-board switches for *TORNADO-PX5421Q* DCM.

switch ID	switch button	switch function description	reference information
SW1	*SW1-1*	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-0 serial port of TMS320VC5421 DSP core #0B.	Section 2.3
	SW1-2	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-1 serial port of TMS320VC5421 DSP core #0B.	Section 2.3
	SW1-3	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-0 serial port of TMS320VC5421 DSP core #0A.	Section 2.3

	SW1-4	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-1 serial port of TMS320VC5421 DSP core #0A.	Section 2.3
SW2	*SW2-1*	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-0 serial port of TMS320VC5421 DSP core #1B.	Section 2.3
	SW2-2	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-1 serial port of TMS320VC5421 DSP core #1B.	Section 2.3
	SW2-3	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-0 serial port of TMS320VC5421 DSP core #1A.	Section 2.3
	SW2-4	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-1 serial port of TMS320VC5421 DSP core #1A.	Section 2.3
SW3	*SW3-1*	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-0 serial port of TMS320VC5421 DSP core #2B.	Section 2.3
	SW3-2	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-1 serial port of TMS320VC5421 DSP core #2B.	Section 2.3
	SW3-3	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-0 serial port of TMS320VC5421 DSP core #2A.	Section 2.3
	SW3-4	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-1 serial port of TMS320VC5421 DSP core #2A.	Section 2.3
SW4	*SW4-1*	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-0 serial port of TMS320VC5421 DSP core #3B.	Section 2.3
	SW4-2	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-1 serial port of TMS320VC5421 DSP core #3B.	Section 2.3
	SW4-3	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-0 serial port of TMS320VC5421 DSP core #3A.	Section 2.3
	SW4-4	Common CLKX/CLKR serial clock enable for transmitter and receiver of McBSP-1 serial port of TMS320VC5421 DSP core #3A.	Section 2.3

A.2 On-board Connectors

Table A-2 contains the list of on-board connectors.

Table A-2. On-board connectors for *TORNADO-PX5421Q* DCM.

connector ID	Description
JP1	Host PIOX-16 interface site male header. Pinout of JP1 host PIOX-16 connector is presented in Appendix B of this manual and in the user's guide of host *TORNADO* DSP system/controller, which is used for installation of *TORNADO-PX5421Q* DCM.
JP2	JTAG-IN male header for connection to external TI XDS510 or MicroLAB Systems *MIRAGE-510DX* JTAG emulator. JTAG-IN connector meets TI connector specifications for connection to JTAG emulator, which must be used for debugging of on-board DSP software.
JP3	MXSIOX connector for connection to optional T/SU-X1 external SIOX rev.B mini-extender for TMS320VC5421 DSP core #1A. Refer to section 2.3, fig.2-6 and appendix C for more details.
JP4	MXSIOX connector for connection to optional T/SU-X1 external SIOX rev.B mini-extender for TMS320VC5421 DSP core #1B. Refer to section 2.3, fig.2-6 and appendix C for more details.
JP5	MXSIOX connector for connection to optional T/SU-X1 external SIOX rev.B mini-extender for TMS320VC5421 DSP core #2A. Refer to section 2.3, fig.2-6 and appendix C for more details.
JP6	MXSIOX connector for connection to optional T/SU-X1 external SIOX rev.B mini-extender for TMS320VC5421 DSP core #2B. Refer to section 2.3, fig.2-6 and appendix C for more details.
JP7	MXSIOX connector for connection to optional T/SU-X1 external SIOX rev.B mini-extender for TMS320VC5421 DSP core #3A. Refer to section 2.3, fig.2-6 and appendix C for more details.
JP8	MXSIOX connector for connection to optional T/SU-X1 external SIOX rev.B mini-extender for TMS320VC5421 DSP core #3B. Refer to section 2.3, fig.2-6 and appendix C for more details.
JP9	MXSIOX connector for connection to optional T/SU-X1 external SIOX rev.B mini-extender for TMS320VC5421 DSP core #0A. Refer to section 2.3, fig.2-6 and appendix C for more details.
JP10	MXSIOX connector for connection to optional T/SU-X1 external SIOX rev.B mini-extender for TMS320VC5421 DSP core #0B. Refer to section 2.3, fig.2-6 and appendix C for more details.

A.3 On-board LED

On-board LED for *TORNADO-PX5421Q* DCM are presented in table A-3.

Table A-3. On-board LED indicators for *TORNADO-PX5421Q* DCM.

LED ID	LED color	function description
V1	*RED*	Reset indicator for TMS320VC5421 DSP core #0A.
V2	*RED*	Reset indicator for TMS320VC5421 DSP core #0B.
V3	*RED*	Reset indicator for TMS320VC5421 DSP core #1A.
V4	*RED*	Reset indicator for TMS320VC5421 DSP core #1B.
V5	*RED*	Reset indicator for TMS320VC5421 DSP core #2A.
V6	*RED*	Reset indicator for TMS320VC5421 DSP core #2B.
V7	*RED*	Reset indicator for TMS320VC5421 DSP core #3A.
V8	*RED*	Reset indicator for TMS320VC5421 DSP core #3B.
V9	*YELLOW*	Reset indicator for HPI ports of all TMS320VC5421 DSP cores.
V10	*GREEN*	Host power indicator.

Appendix B. PIOX-16 Interface Site

This appendix contains information about *TORNADO* PIOX-16 interface site specifications. This description is general to all *TORNADO* DSP systems/controllers, whereas different *TORNADO* boards with different DSP platforms may differ in the number of interrupts requests via PIOX-16 interface and in timer/IO pin specifications. Refer to your particular *TORNADO* user's guide for more details.

B.1 General Description

TORNADO architecture allows expansion of the on-board DSP I/O resources via on-board 16-bit parallel I/O expansion interface site (PIOX-16) (fig.B-1), which is designed to carry compatible DCM (DCM).

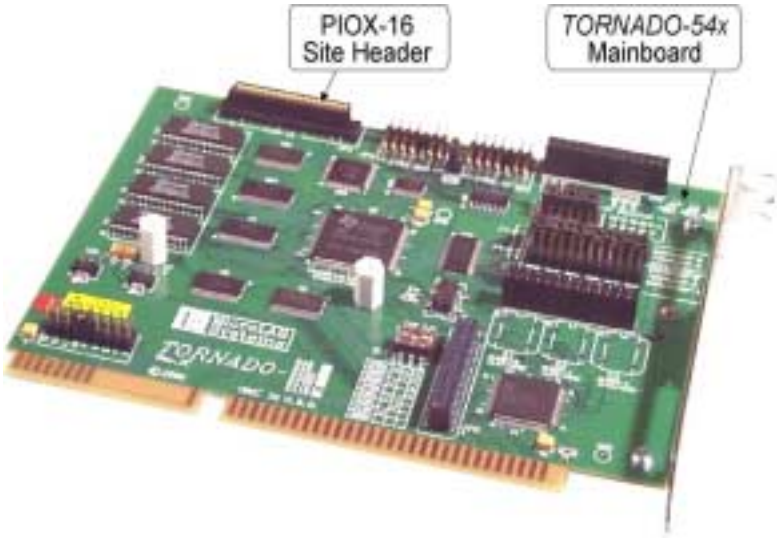


Fig.B-1. PIOX-16 site at *TORNADO-54x* board.

Some *TORNADO* boards (typically 32-bit *TORNADO* DSP systems for PC) provide 16-bit PIOX-16 site as a subset of on-board 32-bit PIOX interface site, whereas other *TORNADO* boards (typically *TORNADO* stand-alone DSP controllers and 16-bit *TORNADO* DSP systems for PC) provide PIOX-16 site only. Refer to your host *TORNADO* board user's guide for information about particular PIOX or PIOX-16 interface site installed.

Figure B-2 demonstrates installation of PIOX-16 DCM into PIOX-16 site of host *TORNADO* DSP system/controller.

Fig.B-2. TORNADO-54x board with PIOX-16 DCM installed.

B.2 PIOX-16 Interface Site Connector and Signals

TORNADO PIOX-16 interface site comprises of signals for SIO-0 and SIO-1 logical serial ports, DSP on-chip TM/XIO-0/1 timers/IO pins, three DSP interrupts, PIOX-16 reset control, and power ±5V/±12V power supplies.

PIOX-16 interface appears as the 64Kx16 sub-area of DSP external memory or I/O resources. PIOX-16 features 16-bit data transfer cycles.

PIOX-16 connector and signal description

PIOX-16 connector is a high-density DDK 50-pin DHB-series dual-row female connector with 0.05" pin pitch. Compatible PIOX-16 plugs for customer designed DCM are available upon request from MicroLAB Systems.

PIOX-16 connector pinout is presented at fig B-3, whereas signal description for PIOX-16 connector is presented in table B-1.

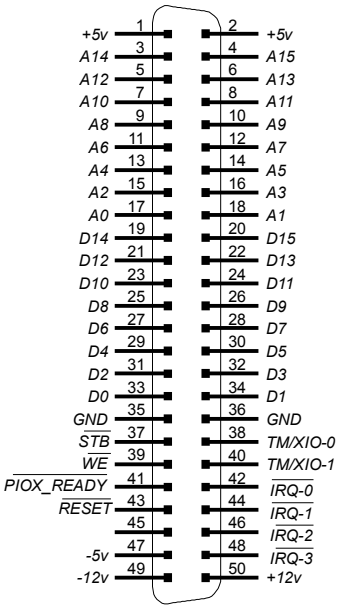


Fig.B-3. PIOX-16 connector pinout (top view).

Table B-1. PIOX-16 signal description.

Signal name	signal type	description
Address and Data Bus		
A0..A15	O	DSP address bus.
D0..D15	I/O	DSP data bus.
Data Transfer Control		
$\overline{STB}$	O	Active low PIOX-16 data transfer strobe.
$\overline{WE}$	O	Active low PIOX-16 write enable signal.
$\overline{PIOX\_READY}$	I	Active low PIOX-16 data ready acknowledge signal. This signal is generated by PIOX-16 DCM in order to complete transmission cycle over PIOX-16 interface. This input has pull-up resistor.
DSP Timers, Reset and Interrupt Requests		

TM/XIO-0 *TM/XIO-1*	I/O/Z	These signals are typically connected to the DSP on-chip TIMER-0 and TIMER-1 I/O pins and can be software configured by DSP as either timer or I/O pin. However, in some *TORNADO* boards (for example *TORNADO-54x* board) these signals can be controlled by on-board I/O controller.
$\overline{RESET}$	O	Active low PIOX-16 reset signal. Some *TORNADO* boards (for example *TORNADO-3x* boards) wires this signal directly from the DSP reset signal, and PIOX-16 plugged-in DCM reset is asserted simultaneously with *TORNADO* on-board DSP reset. However some *TORNADO* boards (for example *TORNADO-54x/6x* etc. boards) feature dedicated PIOX-16 site reset signal, which is controlled by *TORNADO* on-board DSP for better synchronization between the DSP software and PIOX-16 DCM operation.
$\overline{IRQ-0}$ $\overline{IRQ-1}$ $\overline{IRQ-2}$ $\overline{IRQ-3}$	I	Active low external interrupt request lines for *TORNADO* on-board DSP. These lines are pulled up. . Note, that IRQ-2 and IRQ-3 interrupt request input are not available for all *TORNADO* DSP systems/controllers (refer to your *TORNADO* DSP system/controller user's guide for details about on-board PIOX-16 interface).
Power Supplies		
GND		Ground.
+5v		+5v power (from host PC interface).
+12v		+12v power (from host PC interface).
-5v		-5v power (from host PC interface).
-12v		-12v power (from host PC interface).

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.

PIOX-16 site signal levels

Signal levels for PIOX-16 interface signals correspond to that for the CMOS/TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

CAUTION

Some *TORNADO* boards (*TORNADO-30/31/32L/542L*) provide PIOX-16 interface signal levels compatible with that for CMOS/TTL only, whereas other *TORNADO* boards (*TORNADO-33/54xx/6x/E6x/P6x/E3x/E6x*) provide PIOX-16 interface signal levels universal for both 3V TLL and standard TTL. Refer to documentation for your particular *TORNADO* board for information about PIOX-16 interface signal levels.

timing diagram for PIOX-16 data transmission cycle

Figure B-4 presents timing diagram for typical PIOX-16 data transmission cycle for *TORNADO-54x* DSP system. This data transfer timing is known as the industry standard MOTOROLA mode and assumes usage of data strobe signal and write enable signal.

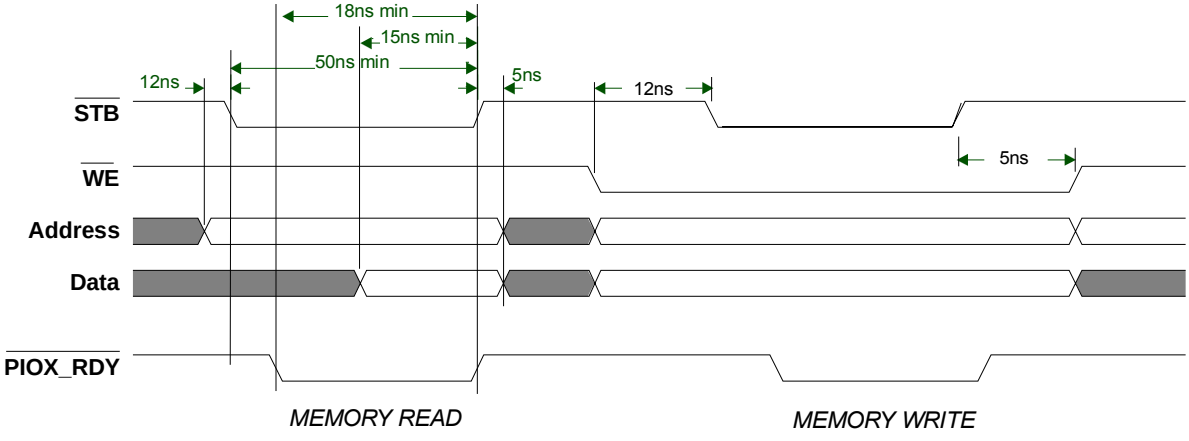


Fig.B-4. Timing diagram of PIOX-16 data transfer for *TORNADO-54x*.

CAUTION

Although different *TORNADO* DSP systems/controllers provide similar timing for PIOX-16 data access cycles, different values for specific timing parameters may apply.

Refer to documentation for your particular *TORNADO* DSP system/controller for information about PIOX-16 timing specifications.

B.3 Physical Dimensions for PIOX-16 DCM

Physical dimensions for PIOX-16 DCM are presented at fig.B-5. This information is intended for those customers, who need to design custom PIOX-16 DCM.

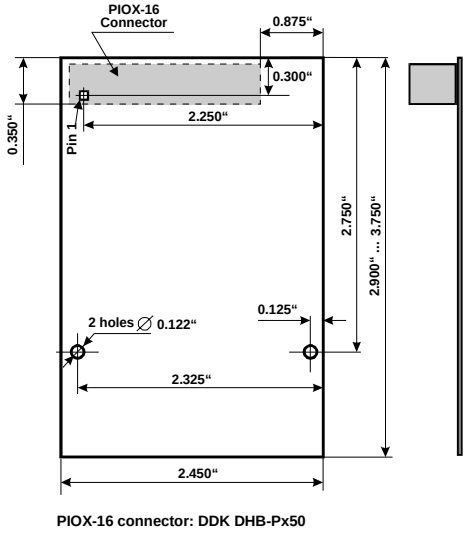


Fig.B-5. Physical dimensions for PIOX-16 DCM.

Appendix C. *T/SU-X1* SIOX rev.B Mini-Extender Kit

This appendix contains description for *T/SU-X1* external SIOX rev.B mini-extender kit, which can be used to connect external SIOX rev.B AD/DA/DIO and application specific DCM to *TORNADO* DSP controllers and coprocessors, which provide on-board compatible connector for connection to external *T/SU-X1* SIOX rev.B mini-extenders.

C.1 General Description

T/SU-X1 SIOX rev.B mini-extender kit is normally provided as dual SIOX rev.B mini-extender kit (fig.C-1), which comprises of the following components:

- two identical *T/SU-X1* SIOX rev.B mini-extender carrier boards
- PC chassis mounting bracket
- two *T/SU-X1/XC* 10” (0.25m) long connection cables.

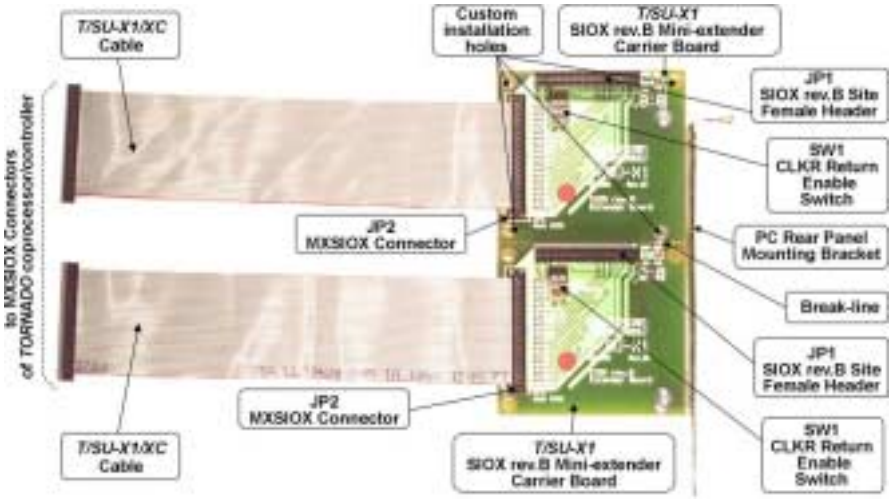


Fig.C-1. Dual *T/SU-X1* SIOX rev.B mini-extender with mounting bracket and connection cables.

Each *T/SU-X1* SIOX rev.B mini-extender carrier board provides on-board site for one full-size SIOX rev.B DCM (fig.C-2), which can be either fixed to the *T/SU-X1*carrier board via optional spacers, or screwed to the mounting bracket.

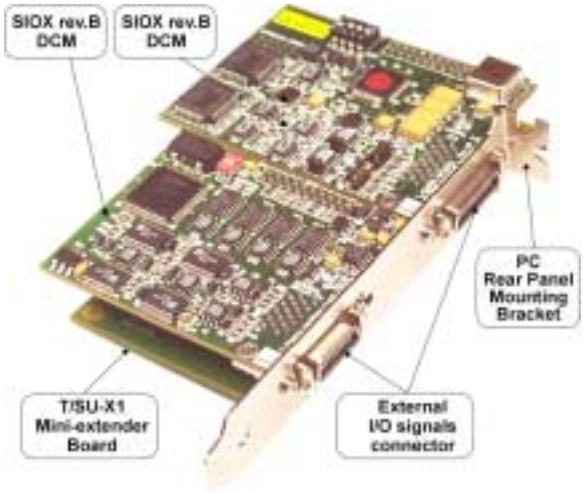


Fig.C-2. Dual *T/SU-X1* SIOX rev.B mini-extender with two installed SIOX rev.B DCM.

connection of T/SU-X1 SIOX rev.B mini-extender to host TORNADO DSP controllers and coprocessors

T/SU-X1 SIOX rev.B mini-extender connects to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* 10" (0.25m) long connection cable (fog.C-3), which connects to the MXSIOX connectors on the *T/SU-X1* SIOX rev.B mini-extender on one side and to with the corresponding MXSIOX matching connector host *TORNADO* DSP controller/coprocessor.

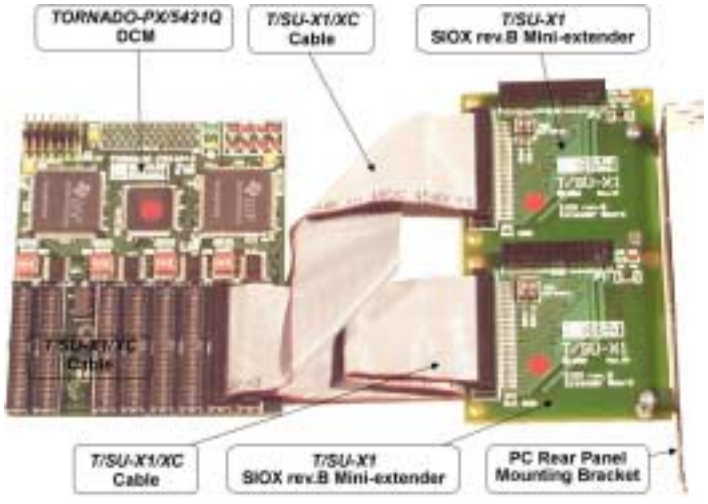


Fig.C-3. Connection of dual *T/SU-X1* SIOX rev.B mini-extender to host *TORNADO-PX5421Q* PIOX-16 DSP coprocessor DCM.

installation

Dual *T/SU-X1* SIOX rev.B mini-extender can either mount at the rear panel of PC using installed mounting bracket, or can be hand-broken into two identical *T/SU-X1* SIOX rev.B mini-extenders using on-board perforated broke line (fig.C-1).

Single *T/SU-X1* SIOX rev.B mini-extender, which appears as the broken half of dual *T/SU-X1* SIOX rev.B mini-extender, can be installed into the embedded custom chassis environment.

physical dimensions

Figure C-4 provides physical dimensions for single *T/SU-X1* SIOX rev.B mini-extender and positions for all installation holes and connectors.

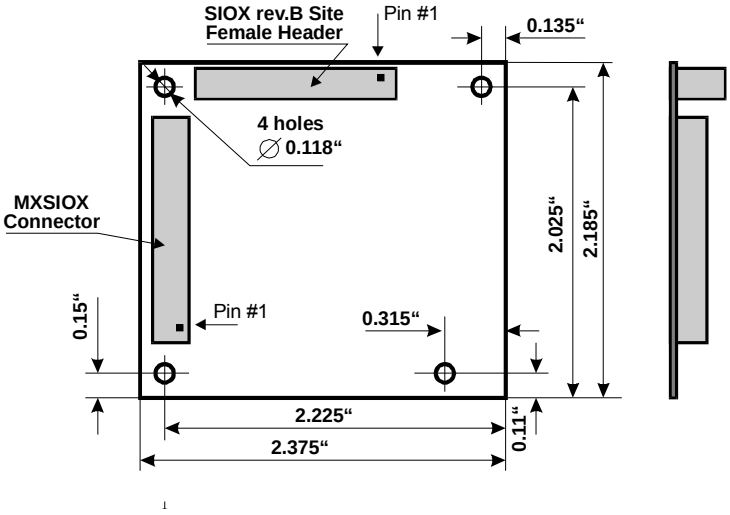


Fig.C-4. Physical dimensions of *T/SU-X1* SIOX rev.B mini-extender.

C.2 Technical Specifications

The following are technical specifications for *T/SU-X1* SIOX rev.B mini-extenders.

Parameter description	*parameter value*
number of SIO ports	2
number of TM/XIO I/O lines	2
number of external interrupt request inputs (*XIRQ*)	2
number of SIOX reset signals (*RESET*)	1

maximum serial clock frequency for transmitter/receiver of SIO ports	50 MHz
power supply outputs	±5v, ±12v
optional features	LED indicators for power and SIOX reset control CLKR0/CLKR1 serial receiver clock enable switches
Dimensions	2.16"x2.36" (55x60 mm)
length of *T/SU-X1/XC* extender cable	10" (0.25m)

C.3 Technical Description

Figure C-5 presents block diagram of *T/SU-X1* SIOX rev.B mini-extender kit.

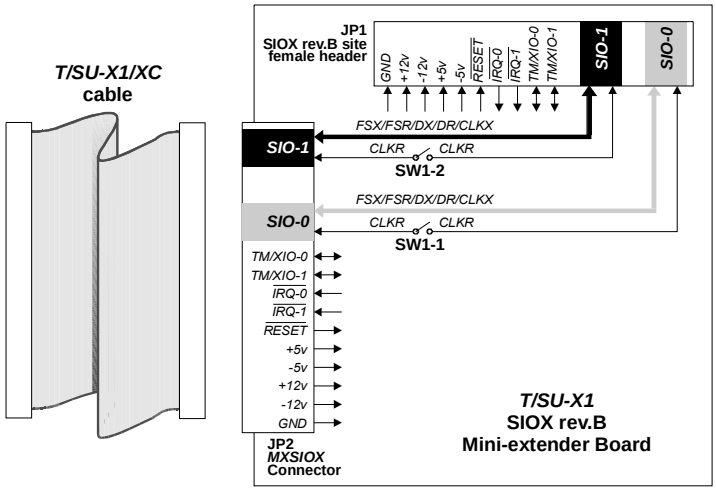


Fig.C-5. Block diagram of *T/SU-X1* SIOX rev.B mini-extender.

T/SU-X1 SIOX rev.B mini-extender carrier board

T/SU-X1 SIOX rev.B mini-extender carrier board comprises of the following components:

- SIOX rev.B site header (JP1)
- MXSIOX connector (JP2) for connection to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* connection cable
- on-board SW1 switch, which is used to enable serial receiver clock (CLKR) for each serial port.

T/SU-X1 on-board JP1 SIOX rev.B site header and JP2 MXSIOX connector for connection to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* connection cable comprise of the signals for two serial ports (SIO-0 and SIO-1), two timer/IO lines (*TM/XIO-0/1*), two external interrupt request inputs (*IRQ-0/1*), SIOX interface reset control output (*RESET*), and host ±5V/±12V power supply lines.

Pinout information for JP1 SIOX rev.B site header and JP2 MXSIOX connector is provided in the corresponding subsections below and figures C-6 and C-5 correspondingly. Common signal description is provided in table C-1.

T/SU-X1 on-board SW1 switch shall be used in conjunction with host *TORNADO* DSP coprocessor/controller on-board common serial clock enable switches in order to enable return of receiver' serial clock for each of two serial ports of SIOX interface to host *TORNADO* DSP coprocessor/controller depending upon the type of installed SIOX rev.B DCM. Refer to the corresponding subsection below for more details.

MXSIOX connector pinout and signal description

T/SU-X1 on-board MXSIOX connector is used for connection to host *TORNADO* DSP coprocessor/controller via *T/SU-X1/XC* connection cable.

MXSIOX connector is Samtec 34-pin dual-row 2mm guarded male header. Although MXSIOX plugs come standard with *T/SU-X1/XC* SIOX rev.B mini-extender connection cables, optional MXSIOX plugs for 2mm flat cables are available from MicroLAB Systems upon request.

MXSIOX connector pinout is presented at fig.C-6, whereas signal description is provided in table C-1.

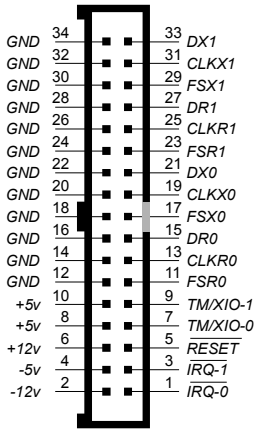


Fig.C-6. Pinout for *T/SU-X1* SIOX rev.B mini-extender on-board MXSIOX connector (top view).

Table C-1. Signal description for *T/SU-X1* SIOX rev.B mini-extender on-board MXSIOX connector.

SIOX rev.B interface signal	signal type	Description
		SIO-0 port control
DX0 *FSX0* *CLKX0*	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port, which connect to the transmitter control signals for SIO-0 serial port.
DR0 *FSR0* *CLKR0*	I I I	Data, frame synchronization and serial clock signals for receiver of SIO-0 port, which connect to the receiver control signals for SIO-0 serial port.
		SIO-1 port control
DX1 *FSX1* *CLKX1*	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port, which connect to the transmitter control signals for SIO-1 serial port.
DR1 *FSR1* *CLKR1*	I I/O I	Data, frame synchronization and serial clock signals for receiver of SIO-1 port, which connect to the receiver control signals for SIO-2 serial port.
		Timers/IO, DSP Reset and Interrupt Requests
TM/XIO-0 *TM/XIO-1*	I/O	Timer/IO pins.
$\overline{RESET}$	O	Active low SIOX reset output pin.
$\overline{IRQ-0}$ $\overline{IRQ-1}$	I	Active low external interrupt request inputs. Active DSP core' external interrupt requests are generated on the falling edge (1→0) of $\overline{IRQ-0}$ and $\overline{IRQ-1}$.. inputs.
		Power Supplies
GND		Ground.
+5v		+5v power supply.
+12v		+12v power supply.
-5v		-5v power supply.
-12v		-12v power supply.

Note:

1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
3. All logical signal levels and load currents correspond to that for 3v/5v CMOS signals.

SIOX rev.B site header

T/SU-X1 on-board SIOX rev.B site header with two serial ports is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM must be the industry standard either 26-pin 0.1"x0.1"male header (in case both SIO-0 and SIO-1 serial ports are used on SIOX plugged-in DCM) or 20-pin 0.1"x0.1"male header (in case only SIO-0 serial port is used on SIOX plugged-in DCM).

SIOX rev.B site connector pinout with two serial ports is shown at fig.C-7 and signal specifications are listed in table C-1.

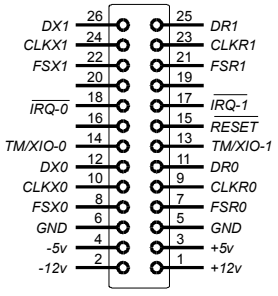


Fig.C-7. SIOX rev.B connector pinout (top view).

Signal levels for SIOX interface signals of T/SU-X1 SIOX rev.B mini-extender is defined by host *TORNADO* DSP coprocessor/controller and correspond to that for the CMOS/TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

CAUTION

Some *TORNADO* boards provide SIOX interface signal levels for CMOS/TTL only, whereas other *TORNADO* boards provide SIOX interface signal levels universal for both 3V TTL and standard 5V TTL. Refer to documentation for your particular *TORNADO* board for information about SIOX interface signal levels.

T/SU-X1/XC mini-extender connection cable

T/SU-X1 SIOX rev.B mini-extender carrier board connects to host *TORNADO* DSP coprocessor/controller via *T/SU-X1/XC* 10" (0.25m) long 34-pin 2mm flat cable.

T/SU-X1/XC mini-extender connection cable plugs to MXSIOX connector of *T/SU-X1* SIOX rev.B mini-extender carrier board on one side and to MXSIOX connector of host *TORNADO* DSP coprocessor/controller on the other side (fig.C-3).

on-board receiver serial clock return enable switches

T/SU-X1 SIOX rev.B mini-extender carrier board provides on-board SW1-1 and SW1-2 switches in order to enable return of SIO-0 and SIO-1 receiver serial clock (CLKR0 and CLKR1 correspondingly) SIOX interface to host *TORNADO* DSP coprocessor/controller depending upon the type of installed SIOX rev.B DCM.

T/SU-X1 SIOX rev.B mini-extender on-board SW1-1 and SW1-2 switches shall be used in conjunction with host *TORNADO* DSP coprocessor/controller on-board common serial clock enable switches using general recommendations below.

Host *TORNADO* DSP coprocessor/controller provides on-board common CLKX/CLKR serial clock enable switches for each of serial ports of MXSIOX connectors.

CAUTION

In case on-board common serial clock enable switch of host *TORNADO* DSP coprocessor/controller is set to 'ON', then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are connected together on-board.

In case on-board common serial clock enable switch of host *TORNADO* DSP coprocessor/controller is set to 'OFF', then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are disconnected on-board.

Background for usage on-board common CLKX/CLKR serial clock enable switches of host *TORNADO* DSP coprocessor/controller and *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKR) return enable switches is the 'long-line' compensation issue for serial clock signals distribution over connection flat cable between host *TORNADO* DSP coprocessor/controller on-board MXSIOX connector and *T/SU-X1* SIOX rev.B mini-extender due to the 'long-line wave nature' of connection flat cable.

Although the 'long-line' compensation resistors are being used for control signals for serial ports at both host *TORNADO* DSP coprocessor/controller and *T/SU-X1* SIOX rev.B mini-extender boards in order to exclude signal reflection, a 'long-line' non-compensation for serial clock signals can still occur in case installed SIOX rev.B DCM is using common shorted serial clock for transmitter and receiver of SIO port (many SIOX rev.B DCM actually use this in order to simplify design). Note, that this problem does not occur with SIO port frame synchronization and serial data signals, since these signals always use dedicated lines of SIOX interface and can't be connected together.

CAUTION

In case installed SIOX rev.B DCM has been designed without on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and each serial clock is using its dedicated pins, then the corresponding host *TORNADO* DSP coprocessor/controller on-board common CLKX/CLKR serial clock enable switch must be set to 'OFF' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'ON'.

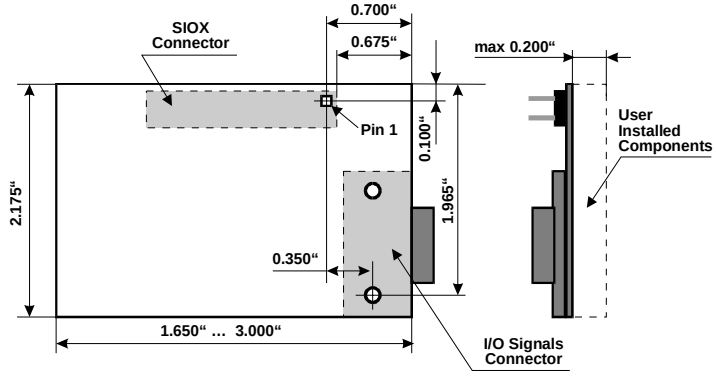
In case installed SIOX rev.B DCM has been designed with on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and both serial clocks are using shared pins, then the corresponding host *TORNADO* DSP coprocessor/controller on-board common CLKX/CLKR serial clock enable switch must be set to 'ON' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'OFF'.

LED indicators

T/SU-X1 SIOX rev.B carrier board also provides two on-board LED indicators for host power (V1) and for SIOX reset state (V2).

C.4 Physical Dimensions for SIOX DCM

Physical dimensions for SIOX DCM are presented at fig.C-8. This information is intended for those customers, who need to design customized SIOX DCMs.



SIOX connector: 20-pin or 26-pin straight dual-row mail header (0.025“ Sq., 0.1“x0.1” pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.C-8. Physical dimensions for SIOX DCM.

Appendix D. Software Utilities for *TORNADO-PX5421Q*

This appendix provides general information about software utilities for *TORNADO-PX5421Q* DCM, which comprise from software utilities for *TORNADO-PX5421Q* on-board TMS320VC5421 DSP and of software utilities for host *TORNADO* DSP system/controller.

CAUTION

This manual does not provide detail description neither for *TORNADO-PX5421Q* resident TMS320VC5421 DSP software nor for host *TORNADO* DSP system/controller software.

For software details refer to the corresponding software source codes for *TORNADO-PX5421Q* DCM, which come standard with *TORNADO-PX5421Q* DCM.

D.1 Resident TMS320VC5421 DSP Software Utilities for *TORNADO-PX5421Q*

TORNADO-PX5421Q resident TMS320VC5421 DSP software utilities come in source code and are provided in *PX5421QD.H* header file for TI C5000 C Compiler.

PX5421QD.H header file includes definitions, macros and utility functions, which allow to perform the following control over TMS320VC5421 DSP core environment:

- properly configure TMS320VC5421 DSP core on-chip PMST, SWWSR, SWCR, BSCR, GPIOCR and CLKMD configuration registers
- control *RESET*, *TM/XIO-0* and *XIO-1* signals of optional SIOX site via *T/SU-X1* external SIOX rev.B mini-extender
- configure and transfer data over McBSP-2 serial port for inter-DSP core-to-core communication.

D.2 Host *TORNADO* DSP System/Controller Software Utilities for *TORNADO-PX5421Q*

Host *TORNADO* DSP software utilities for *TORNADO-PX5421Q* DCM come in source code and are provided in *PX5421QH.H* header file for TI DSP C Compilers.

PX5421QH.H header file includes definitions, macros and utility functions, which allow to perform the following control over host PIOX-16 interface of *TORNADO-PX5421Q* DCM via host *TORNADO* DSP environment:

- initialize host PIOX-16 interface of *TORNADO-PX5421Q* DCM
- control reset signals for each TMS20VC5421 DSP core and common HPI port reset signal
- control and process timeout error flags for host-to-HPI access cycles

- configure host PIOX-16 interrupt requests
- transfer data over HPI ports of TMS320VC5421 DSP cores
- load resident executable code for each TMS320VC5421 DSP core on-chip memory via HPI port using *C-BSF32* program/data loader (refer to the corresponding subsections below for more details).

loading resident executable code to TMS320VC5421 DSP core on-chip memory via HPI port

Host *TORNADO* DSP software utilities for *TORNADO-PX5421Q* DCM allow to load resident executable code to TMS320VC5421 DSP core on-chip memory via DSP core' HPI port.

In order to load of resident executable code to TMS320VC5421 DSP core on-chip memory via DSP core' HPI port, the following steps shall be performed:

1. TMS320VC5421 DSP code must be compiled using TI C5000 C/Assembler Compiler and the output C5000 compatible .OUT file must be generated either in TI COFF1 or TI COFF2 format.
2. Source C5000 compatible .OUT file must be converted to output C-code compatible file with *C-BSF32* data array using *C54CBSF.EXE* PC command line utility. Output *C-BSF32* data array will contain corresponding binary data for each non-empty section of source C5000 program .OUT file.
3. C-code compatible file with *C-BSF32* data array must be included into user source .C code for DSP environment of host *TORNADO* DSP system/controller.
4. *C-BSF32* program/data loader function from *PX5421QH.H* header file must be invoked in user "C"-code for DSP environment of host *TORNADO* DSP system/controller in order to transfer TMS320VC5421 DSP core code from host *TORNADO* DSP environment to *TORNADO-PX5421Q* on-board TMS320VC5421 DSP core on-chip memory via DSP core on-chip HPI port.
4. Source .C code for DSP environment of host *TORNADO* DSP system/controller must be compiled using the corresponding TI DSP C Compiler.

C5000 program/data C-BSF32 data arrays

C-BSF32 data array is a *binary section format 32-bit data array for "C" compiler*, which appears as 32-bit data array in source text file, which can be included into user source "C"-code during compilation using "C" compiler.

Although *C-BSF32* data array appears as predefined linear data array of 32-bit unsigned long data, it features internal structure as a series of data sections. Each data section comprises of section header and section data. Section header contains information about load address and section data length, which are used to properly load section data. Termination section header is provided at the end of *C-BSF32* data array.

C-BSF32 data arrays for C5000 DSP program/data code pack two 16-bit data words for C5000 DSP environment into one 32-bit unsigned long data word. This allows to save occupied data memory for host *TORNADO* DSP environment and to unify host software utilities source code for different TI DSP platforms, since TI C Compilers for TI C3x/C4x DSP allocates 8-bit byte, 16-bit short integer and 32-bit long data as 32-bit data words.

CAUTION

This manual does not provide detail description for *C-BSF32* data array format. For more information refer to source codes for host *TORNADO* DSP system/controller software utilities, , which come standard with *TORNADO-PX5421Q* DCM.

C5000 C-BSF32 program/data loader for host TORNADO DSP environment

Host *TORNADO* DSP software utilities for *TORNADO-PX5421Q* DCM include C5000 *C-BSF32* program/data loader in order to in order to transfer TMS320VC5421 DSP core code from host *TORNADO* DSP environment to *TORNADO-PX5421Q* on-board TMS320VC5421 DSP core on-chip memory via DSP core on-chip HPI port.

C5000 *C-BSF32* program/data loader reads and interprets source *C-BSF32* program/data array in host *TORNADO* DSP data memory on section-by-section basis and loads source section data to on-chip memory of selected TMS320VC5421 DSP core via HPI port.

C54CBSF.EXE PC command-line utility for conversion C5000 .OUT files to C-BSF32 data array

C54CBSF.EXE PC command line utility runs under DOS and all Windows 9x/NT/2000 platforms and must be used in order to convert source C5000 compatible .OUT file (output file of TI C5000 C/Assembler Compiler) into output C-code compatible file with *C-BSF32* data array.

The following is command line format for invoking *C54CBSF.EXE* PC command line utility in order to convert source C5000 compatible .OUT file into output C-code compatible file with *C-BSF32* data array:

C54CBSF INPUT_FILENAME[.OUT] OUTPUT_FILENAME

C54CBSF.EXE PC command line utility can be also used in order to display section information for source C5000 compatible .OUT file:

C54CBSF INPUT_FILENAME[.OUT] -d

Appendix E. Glossary of Terms.

This Glossary contains definition for terms and other synchronism used along in this databook.

A

B

C

C-BSF32 data array

C5000 32-bit binary section format data array "C" compiler, which appears as 32-bit unsigned long predefined data array in source text format for inclusion into user "C"-code for host *TORNADO* DSP environment. C5000 *C-BSF32* data array can contain program/data code for target TMS320VC5421 DSP environment and must be transferred to target DSP environment using *C-BSF32* program/data loader from host *TORNADO* DSP software utilities. Refer to Appendix D for more details.

CLKX, CLKR

Serial clock for transmitter and receiver of TMS320VC5421 DSP on-chip McBSP serial ports. Refer to section 2.3 and appendix C for more details.

D

DCM

Daughter-card module. *TORNADO-PX5421Q* is DCM, which plugs into PIOX-16 interface site of host *TORNADO* DSP system/controller.

DSP

On-board TI TMS320VC5421 dual-core Digital Signal Processor. Refer to sections 2.1, 2.2 and 2.3 for more details.

DSPINT

Host-to-DSP interrupt request via TMS320VC5421 DSP core on-chip HPI port, which appears as the *DSPINT* bit of TMS320VC5421 DSP core HPIC register. Refer to sections 2.2 and 2.3 for more details.

E

F

G

GPIO

General purpose I/O pins of TMS320VC5421 DSP, which are used to control *TM/XIO-0, XIO-1* and *RESET* signals of optional SIOX rev.B interface via T/SU-X1 external SIOX rev.B mini-extender. Refer to section 2.2 for more details.

H

HINT

DSP-to-host interrupt request via TMS320VC5421 DSP core on-chip HPI port, which appears as the *HINT* bit of TMS320VC5421 DSP core HPIC register. Refer to sections 2.2 and 2.3 for more details.

Host PIOX-16 interface

TORNADO-PX5421Q on-board host PIOX-16 interface, which is used to install onto host *TORNADO* DSP system/controller and for communication with host DSP. Refer to section 2.5 and Appendix B for more details.

HOST_CLR_HPI0_TMOUT_ERR_RG, HOST_CLR_HPI1_TMOUT_ERR_RG, HOST_CLR_HPI2_TMOUT_ERR_RG, HOST_CLR_HPI3_TMOUT_ERR_RG

Write-only registers of host PIOX-16 interface, which is used to clear timeout error flags for host-to-HPI accesses. Refer to section 2.4 for more details.

HOST_CNTR1_RG

Register of host PIOX-16 interface, which is used to control reset signals for each TMS320VC5421 DSP cores. Refer to section 2.4 for more details.

HOST_CNTR2_RG

Register of host PIOX-16 interface, which is used to control common HPI port reset signal for all TMS320VC5421 DSP cores and to enable timeout control for host-to-HPI access cycle. Refer to section 2.4 for more details.

HOST_HIRQn_IE1_RG, HOST_HIRQn_IE2_RG,

Host interrupt mask registers of host PIOX-16 interface environment for host interrupt request #n (n=0..3). Refer to section 2.4 for more details.

HOST_HIRQ_EN_RG

Register of host PIOX-16 interface, which is used to enable interrupt request outputs of host PIOX-16 interface in order to set interrupt requests from *TORNADO-PX5421Q* DCM to host *TORNADO* DSP system/controller. Refer to section 2.4 for more details.

HOST_HPI_HINT_STAT_RG

Read-only register of host PIOX-16 interface environment, which can be used to read current status of DSP-to-host interrupt requests from all TMS320VC5421 DSP cores. Refer to section 2.4 for more details.

HOST_HPI_TMOUT_ERR_STAT_RG

Read-only register of host PIOX-16 interface environment, which can be used to read current status of timeout error flags for host-to-HPI access cycles. Refer to section 2.4 for more details.

HOST_HPICxx_RG, HOST_HPIAxx_RG, HOST_HPIDxx_RG, HOST_HPIDxx_AINC_RG

HPI port registers for TMS320VC5421 DSP core #xx (xx=0A..3B), which are mapped to host PIOX-16 interface. Refer to section 2.4 for more details.

HPI

TMS320VC5421 DSP on-chip 16-bit host port interface, which is used to access DSP on-chip memory and registers from host PIOX-16 interface environment. Refer to section 2.4 for more details.

HPI access timeout error flag

Error flag, which is set in case of timeout condition for host-to-HPI access cycles of host PIOX-16 interface. HPI access timeout flags can be read via *HOST_HPI_TMOUT_ERR_STAT_RG* read-only register and can be cleared via *HOST_CLR_HPIn_TMOUT_ERR_RG* write-only registers. Refer to section 2.4 for more details.

I

IRQ-0, IRQ-1, IRQ-2, IRQ-3

Host PIOX-16 interface interrupt request inputs and optional SIOX rev.B interrupt request inputs. Refer to sections 2.3 and 2.4, and Appendixes B and C for more details.

J

JTAG

Joint Test Action Group interface, which is a part of the TMS320C2xx/VC33/C4x/C5x/C54x/C6x/C8x DSP on-chip hardware, and is used to debug *TORNADO-PX5421Q* on-board TMS320VC5421 DSP software using external JTAG emulators (TI XDS510 and MicroLAB' *MIRAGE-510DX*, *UECMX*). Refer to section 2.5 for more details.

JTAG-IN

On-board input connector, which is used for connection to external JTAG emulator. Refer to section

2.5 and Appendix A for more details.

K

L

LED
Light emitting diode indicator. Refer to Appendix A for more details.

M

McBSP
TMS320VC5421 DSP on-chip serial ports. Refer to sections 2.2 and 2.3 for more details.

MXSIOX
On-board connectors for *T/SU-X1/XC* extender connection cable at *TORNADO-PX5421Q* DCM and at *T/SU-X1* SIOX rev.B mini-extender. Refer to section 2.3 and Appendix C for more details.

N

O

P

PIOX
32-bit Parallel I/O eXpansion interface site for compatible daughter-card modules (DCM) at *TORNADO* PC plug-in DSP systems. PIOX comprises of 16-bit PIOX-16 interface site and PIOX-X32 32-bit extension interface site. Refer to sections 2.6 and 3.1, and Appendix B for more details.

PIOX-16
16-bit Parallel I/O eXpansion interface site for compatible daughter-card modules (DCM) at *TORNADO* PC plug-in DSP systems and controllers. *TORNADO-PX5421Q* DCM plugs into PIOX-16 interface site on host *TORNADO* DSP system/controller. Refer to sections 2.6 and 3.1, and Appendix B for more details.

Pod

Electronic device, which connects external JTAG emulator with *TORNADO-PX5421Q* on-board JTAG-IN connector for uploading and debugging of on-board DSP software.

Q

R

S

SIO-0, SIO-1

High-speed serial ports at SIOX rev.B interface, which are typically connected to the corresponding DSP on-chip serial ports. Refer to section 2.3 and Appendix C for more details.

SIOX rev.B

Serial I/O eXpansion interface site revision B for compatible daughter-card modules (DCM) at *TORNADO* DSP systems, controllers, and SIOX extenders. Refer to sections 2.2 and 2.3, and Appendix C for more details.

T

T/SU-X1

External SIOX rev.B mini-extender, which can carry one SIOX rev.B DCM and connect to *TORNADO-PX5421Q* on-board MXSIOX connector. Refer to section 2.3 and Appendix C for more details.

T/SU-X1/XC

Extender connector cable, which is used to connect external SIOX rev.B mini-extender and *TORNADO-PX5421Q* DCM. Refer to section 2.3 and Appendix C for more details.

TM/XIO-0, TM/XIO-1

Timer/IO pins of SIOX rev. B interface site at *TORNADO* DSP systems, controllers, and SIOX extenders. Refer to sections 2.2 and 2.3, and Appendix C for more details.

U

V

W

X

Y

Z