TORNADO-E6x

Stand-alone DSP Controllers with
Ultra-High Performance 32-bit Fixed-/Floating-Point TMS320C6xxx DSP

User's Guide

covers:
TORNADO-E62/E67 rev.2A
TORNADO-E6202/E6203 rev.1B
TORNADO-E6414/E6415/E6416 rev.1A

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About this Document

This user's guide contains description for *TORNADO-E6x* (*TORNADO-E62/E67* rev.2A, *TORNADO-E6202/E6203* rev.1B and *TORNADO-E6414/E6415/E6416* rev.1A) stand-alone controllers with ultra-high performance 32-bit fixed-/floating-point TMS320C6201/C6202/C6203/C6414/C6415/C6416/C6701 digital signal processors (DSP) from Texas Instruments Inc (TI).

This document does not include detail description neither for TI TMS320C6x DSP nor for the other on-board peripherals and the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. *TMS320C6xxx Peripheral Reference Guide.* Texas Instruments Inc, SPRU190D, 2000.
2. *TMS320C6000 CPU and Instruction Set.* Texas Instruments Inc, SPRU189F, 2000.
3. *TMS320C6201 DSP Data Sheet.* Texas Instruments Inc, SPRS051F, 1999.
4. *TMS320C6202 DSP Data Sheet.* Texas Instruments Inc, SPRS104C, 2000.
5. *TMS320C6203 DSP Data Sheet.* Texas Instruments Inc, SPRS086F, 2001.
6. *TMS320C6701 DSP Data Sheet.* Texas Instruments Inc, SPRS067E, 2000.
7. *TMS320C6414 DSP Data Sheet.* Texas Instruments Inc, SPRS134C, 2001.
8. *TMS320C6415 DSP Data Sheet.* Texas Instruments Inc, SPRS146C, 2001.
9. *TMS320C6416 DSP Data Sheet.* Texas Instruments Inc, SPRS164C, 2001.
10. *DS1284/DS1286 Watchdog Timekeeper.* Dallas Semiconductor, 1999.
11. *Enhanced Serial Communication Controller ESCC2 SAB82532.* Siemens, 1994.
12. *USS-820/USS-825 USB Device Controller.* Lucent Technologies, 1999.

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Contents

Figures

Tables

Chapter 1.   Introduction

This chapter contains general description for *TORNADO-E6x* stand-alone DSP controllers product line, which comprises of *TORNADO-E62/E67/E6202/E6203/E6414/E6415/E6416* DSP controllers.

CAUTION

TORNADO-E6x DSP controllers have been designed to accommodate either 32-bit fixed-point TMS320C6201/TMS320C6202/TMS320C6203/C6414/C6415/C6416 DSP or compatible 32-bit floating-point TMS320C6701 DSP from TI.

The particular DSP installed onto *TORNADO-E6x* DSP controller specifies the final name of this *TORNADO-E6x* DSP controller, i.e. *TORNADO-E62* (with TMS320C6201 DSP), *TORNADO-E67* (with TMS320C6701 DSP), *TORNADO-E6202* (with TMS320C6202 DSP), or *TORNADO-E6203* (with TMS320C6203 DSP), or *TORNADO-E6414* (with TMS320C6414 DSP), or *TORNADO-E6415* (with TMS320C6415 DSP) , or *TORNADO-E6416* (with TMS320C6416 DSP) .

CAUTION

'TMS320C620x' notation denotes that the supplied information is applicable to all TMS320C6201, TMS320C6202, TMS320C6203 DSP.

'TMS320C64xx' notation denotes that the supplied information is applicable to all TMS320C6414, TMS320C6415, TMS320C6416 DSP.

Should the provided information be a DSP type specific, then either the name of the corresponding DSP (TMS320C6201, TMS320C6202, TMS320C6203, TMS320C6701, TMS320C6414, TMS320C6415, TMS320C6416) , or the name of the corresponding product group (TMS320C620x, TMS320C64xx) will be highlighted.

CAUTION

'*TORNADO-E6x*' notation denotes that the supplied information is applicable to all *TORNADO-E6x* DSP controllers.

'*TORNADO-E62xx*' notation denotes that the supplied information is applicable to all *TORNADO-E62/E6202/E6203* DSP controllers.

'*TORNADO-E64xx*' notation denotes that the supplied information is applicable to all *TORNADO-E6414/E6415/E6416* DSP controllers.

Should the provided information be a product specific, then either the name of the corresponding product (*TORNADO-E62*, *TORNADO-E67*, *TORNADO-E6202*, *TORNADO-E6203*, *TORNADO-E6414*, *TORNADO-E6415*, *TORNADO-E6416*) , or the name of the corresponding product group (*TORNADO-E62xx*, *TORNADO-E64xx*) will be highlighted.

1.1   General Information

TORNADO-E6x are ultra-high performance fixed- and floating-point DSP controllers for stand-alone DSP applications. *TORNADO-E6x* DSP controllers meet industry standard 3U form-factor and feature compatible flexible modular system construction with daughter-card modules (DCM), compatible system architecture and compatible DSP environments in order to meet requirements for multiple applications while keeping a cost to a minimum. System architecture and construction of *TORNADO-E6x* DSP controllers are compatible with that of *TORNADO-E* DSP controllers product line, and the only specific imply to the DSP type and on-board memory type and capacity.

TORNADO-E6x DSP controllers appear as two different boards (fig.1-1):

- *TORNADO-E62* and *TORNADO-E67* DSP controllers have been designed using the 1st common board (fig.1-1a) with either 200 MHz 32-bit fixed-point TMS320C6201 DSP or 167 MHz 32-bit floating-point TMS320C6701 DSP installed correspondingly.
- *TORNADO-E6202* and *TORNADO-E6203* DSP controllers have been designed using the 2nd common board (fig.1-1b) with either 250 MHz TMS320C6202 or 300 MHz TMS320C6203 32-bit fixed-point DSP installed correspondingly.
- *TORNADO-E6414, TORNADO-E6415* and *TORNADO-E6416* DSP controllers have been designed using the 3rd common board (fig.1-1c) with either TMS320C6414, TMS320C6415 or TMS320C6416 600 MHz 32-bit fixed-point DSP installed correspondingly.

Fig.1-1a.   TORNADO-E62/E67 DSP controllers board.

Fig.1-1b.   TORNADO-E6202/E6203 DSP controllers board.

Fig.1-1c.   TORNADO-E6414/E6415/E6416 DSP controllers board.

CAUTION

TORNADO-E62 and *TORNADO-E67* DSP controllers share common board design and actually differ in the DSP chip installed. Therefore, information provided for either of *TORNADO-E62/E67* DSP controllers except for the DSP on-chip details, is applicable for both *TORNADO-E62/E67* DSP controllers.

TORNADO-E6202 and *TORNADO-E6203* DSP controllers share common board design and actually differ in the DSP chip installed. Therefore, information provided for either of *TORNADO-E6202/E6203* DSP controllers except for the DSP on-chip details, is applicable for both *TORNADO-E6202/E6203* DSP controllers.

TORNADO-E6414, TORNADO-E6415 and *TORNADO-E6416* DSP controllers share common board design and actually differ in the DSP chip installed. Therefore, information provided for either of *TORNADO-E6414/E6415E6416* DSP controllers except for the DSP on-chip details, is applicable for all *TORNADO-E6414/E6415/E6416* DSP controllers.

All *TORNADO-E6x* DSP controllers feature software/hardware compatible on-board DSP environment, except for the minor differences, which imply to the number of DSP on-chip McBSP ports, number of DSP on-chip timers, on-board dynamic RAM (SDRAM) capacity, on-board real-time clock (RTC), DSP on-chip UTOPIA interface, DSP on-chip general purpose I/O, and programming of the DSP on-chip HPI port.

Overview

TORNADO-E6x DSP controllers are based around TI 32-bit code compatible fixed-point TMS320C6201/C6202/C6203/C6414/C6415/C6416 DSP and floating-point TMS320C6701 DSP running at

200MHz (TMS320C6201), 250MHz (TMS320C6202), 300MHz (TMS320C6203), 600MHz (TMS320C6414/C6415/C6416) and 167MHz (TMS320C6701) correspondingly, and featuring 1600MIPS (TMS320C6201), 2000MIPS (TMS320C6202), 2400MIPS (TMS320C6203), 4800MIPS (TMS320C6414/C6415/C6416) and 1000MFLOPS (TMS320C6701) correspondingly. The only differences between DSP chips imply to capacity of DSP on-chip RAM, number of DSP on-chip McBSP ports, number of DSP on-chip timers, DSP on-chip UTOPIA interface, DSP on-chip general purpose I/O, and DSP on-chip HPI port programming.

On-board memory comprises of up to 1Mx32 (*TORNADO-E62xx/E67*) or 1Mx64 (*TORNADO-E64xx*) on-board static RAM (SBSRAM) for program and data, 4Mx32 (*TORNADO-E62/E67*) or 8Mx32 (*TORNADO-E6202/E6203*) or 16Mx64 (*TORNADO-E64xx*) on-board synchronous dynamic RAM (SDRAM) for program and data, and of up to up to 1Mx8 on-board FLASH/EPROM for boot code and non-volatile data.

TORNADO-E6x DSP controllers offer extensive set of on-board interfaces for communication with external host computers and peripherals:

- dual-channel 10Mbit/s USART (universal synchronous/asynchronous receiver/transmitter) with and external RS232C/RS422 interfaces, which allows direct connections to host computers, networks, and peripherals using industry standard HDLC/SDLC/BISYNC/MONOSYNC synchronous and ASYNC asynchronous protocols.
- 12 Mbit/s USB rev.1.1 slave interface, which offers industry-standard connection to host computers and can be used for fast bulk data transfers
- TMS320C6x DSP on-chip either 16-bit (*TORNADO-E62/E67*) or 32-bit (*TORNADO-E6202/E6203*), or programmable 16-bit/32-bit (*TORNADO-E64xx* only) HPI port, which allows access to DSP on-chip memory and DSP boot from any host controller/computer using simple asynchronous parallel 16-/32-bit interface
- TMS320C64xx DSP on-chip 8-bit UTOPIA slave interface (*TORNADO-E6415/E6416* only).

TORNADO-E6x on-board TMS320C6x DSP can start either without boot, or can boot from either on-board 8-bit FLASH/EPROM or DSP on-chip HPI port. *TORNADO-E62xx/E67* DSP controllers support both MAP0 and MAP1 memory map configurations of on-board TMS320C6x DSP.

A set of on-board peripherals also include general purpose 8-bit general purpose digital I/O for local system control, watchdog timer, real-time clock (RTC) (*TORNADO-E64xx* only), 10-bit DSP on-chip general purpose I/O (*TORNADO-E64xx* only), and a set of configuration and control registers.

external real-time analog/digital I/O

TORNADO-E6x DSP controller has been designed with modular construction in mind and provides different on-board I/O expansion facilities for installation of optional DCM. This allows quick system configuration using a variety of 'of-the-shelf' DCM in order to meet customer application requirements.

At first, on-board SIOX (serial I/O expansion) rev.B and SIOX rev.C sites allows installation of one SIOX rev.B/C DCM. A variety of 'of-the-shelf' *TORNADO* SIOX rev.B/C DCM comprises of AD/DA/DIO and application specific DCM for real-time telecom, speech/fax/modem, audio, instrumentation, industrial, digital radio, etc signal processing applications.

At second, on-board MXSIOX connector allows connection to external *T/SU-X1* SIOX rev.B mini-extender kit, which can be used for installation of one SIOX rev.B DCM. This facility is available for *TORNADO-E6202/E6203/E64xx* DSP controllers only with TMS320C6202/C6203/C6414/C6415/C6416 DSP, which feature three DSP on-chip McBSP serial ports.

Finally, one site for *TORNADO* parallel I/O expansion (PIOX-16) DCM can be used for installation of one PIOX-16 DCM. A variety of 'of-the-shelf' *TORNADO* PIOX-16 DCM comprises of AD/DA/DIO, application-specific and DSP coprocessor DCM for real time multi-channel high-speed telecom, instrumentation, industrial, digital radio, etc signal processing applications.

Figure 1-2 illustrates installation of different DCM at *TORNADO-E6x* DSP controller board and connection of external *T/SU-X1* SIOX rev.B mini-extender kit with one SIOX rev.B DCM (*TORNADO-E6202/E6203* only).

Fig.1-2a.   TORNADO-E62/E67 DSP controller with SIOX rev.B and PIOX-16 DCM installed.
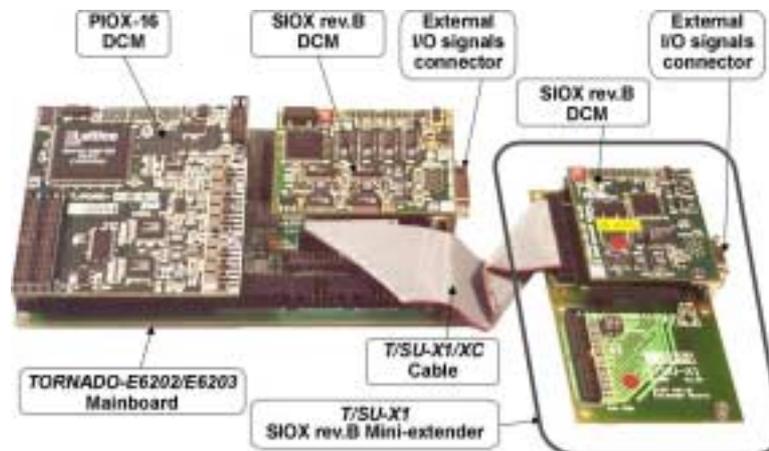
Fig.1-2b.   TORNADO-E6202/E6203 DSP controller with SIOX rev.B and PIOX-16 DCM installed and *T/SU-X1* external SIOX rev.B mini-extender kit with one SIOX rev.B DCM installed.
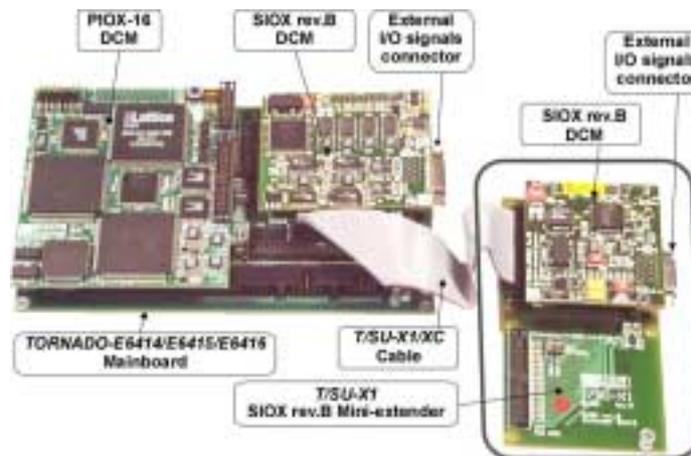
Fig.1-2c. TORNADO-E6414/E6415/E6416 DSP controller with SIOX rev.B and PIOX-16 DCM installed and *T/SU-X1* external SIOX rev.B mini-extender kit with one SIOX rev.B DCM installed.

Applications

TORNADO-E6x stand-alone DSP controllers have been designed for high-performance embedded DSP applications with communication with external host computers/peripherals and real-time signal I/O. The following are only few of many applications for *TORNADO-E6x* DSP controllers:

- *real-time general purpose DSP and analog signal acquisition*
- *high-speed multichannel fax/modem communication*
- *multichannel vocoders and speech signal processing*
- *cellular base stations*
- *computer telephony*
- *networking*
- *audio and acoustics signal processing*
- *multimedia*
- *radars and sonars*
- *digital radio*
- *instrumentation and industrial*
- *biomedical signal processing and medical imaging*
- *evaluation and education*
- many more ...

1.2   Technical Specification

The following are the technical specifications for *TORNADO-E6x* DSP controllers.

Parameter description	*parameter value*
power supply voltage	+5V for *TORNADO-E6x* board,
	optional -5V and ±12V power supply inputs are routed to SIOX/PIOX-16 DCM sites only and are used upon installed DCM requirements
power consumption	+5V@1.8A (t=+20°C) (*TORNADO-E62xx/E67*)
	+5V@2.4A (t=+20°C) (*TORNADO-E64xx*)
DSP performance	1600 MIPS (*TORNADO-E62*)
	2000 MIPS (*TORNADO-E6202*)
	2400 MIPS (*TORNADO-E6203*)
	4800 MIPS (*TORNADO-E64xx*)
	1000 MFLOPS (*TORNADO-E67*)
Dimensions	3U (100x160 mm)
operating temperature	0°C..+60°C
I/O expansion sites for daughter-card modules (DCM)	one SIOX rev.B site (3v/5v TTL)
	one SIOX rev.C site (3v/5v TTL)
	one PIOX-16 site (3v/5v TTL)
	TORNADO-E6202/E6203/E64xx :
	one MXSIOX site (3v/5v TTL)
on-board memory:	
SBSRAM capacity	*TORNADO-E62xx/E67:* 128K/512K/1Mx32
	TORNADO-E64xx: 128K/256K/512K/1Mx64
SBSRAM wait states	*TORNADO-E62/E67* : 0ws/1ws depending upon the SBSRAM chips installed (contact MicroLAB Systems for more details)
	TORNADO-E6202/E6203 : 1ws
	TORNADO-E64xx : 4ws
SDRAM capacity	*TORNADO-E62/E67* : 0M/4Mx32 1ws
	TORNADO-E6202/E6203 : 0M/4M/8Mx32 1ws
	TORNADO-E64xx : 0M/4M/16Mx64 4ws
FLASH/EPROM memory capacity	128K/512Kx8 (Ta=100ns) 5v-only FLASH memory chip, PLCC-32 IC package
	on-board FLASH write-protection feature
recommended FLASH memory chips	AMD:
	Am29F010B-90JC 128Kx8 FLASH
	Am29F040B-90JC 512Kx8 FLASH
watchdog timer (WDT) and reset controller:	
WDT latency period	1.6 sec typical

duration of the WDT reset signal (generated by the DSP software)	>100 ns
duration of the output DSP reset signal	>0.2 sec

external RESET input:

active low signal duration	>0.5uS
input signal level	3v/5v TTL

on-board USART (universal synchronous/asynchronous receiver/transmitter):

number of channels	2
supported protocols for each channel	*synchronous:* HDLC/X.25, SDLC, MONOSYNC, BISYNC *asynchronous*: ASYNC
external electrical interfaces for each channel	RS232C or RS422 (EIA-530 pinout) with the corresponding signal I/O levels
Maximum data transfer speed for synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) with external RS422 interface	10 Mbit/s
Maximum data transfer speed for asynchronous protocol (ASYNC) with external RS232C interface	115 kBaud
Maximum data transfer speed for asynchronous protocol (ASYNC) with external RS422 interface	2.5 Mbaud
maximum frequency of on-board USART master clock oscillator (socket S4)	10 MHz (factory default 1.8432 MHz USART master clock oscillator installed into on-board S4 socket)
I/O signal levels for external T/R clock outputs (JP15 and JP16 connectors)	5v TTL

on-board TMS320C6x HPI interface

TORNADO-E62/E67:
   16-bit TMS320C6x HPI port (3v/5v TTL)

TORNADO-E6202/E6203:
   TMS320C6202/C6203 X-Bus configured as
   slave 32-bit HPI port (3v/5v TTL)

TORNADO-E64xx:
   user selected 16-bit/32-bit HPI port (3v/5v TTL)

on-board USB interface

12 Mbit/s USB device interface, meets USB rev.1.1 specifications, USB type 'B' connector

on-board real-time clock (RTC) *(TORNADO-E64xx only))*	battery backed-up real-time clock with 2100 year calendar, programmable ring interrupt and programmable watch-dog timer interrupt
general purpose digital I/O	8 bits (5v TTL, I_{OL}=2mA, I_{OH} =-0.4mA)
DSP general purpose I/O *(TORNADO-E64xx only))*	10-bit (3v/5v TTL, I_L=3.2mA)
UTOPIA interface *(TORNADO-E64xx only))*	50MHz 8-bit UTOPIA level 2 slave interface
I/O signal level for JTAG-IN interface	3v/5v TTL

Chapter 2. System Architecture and Construction

This chapter contains description for *TORNADO-E6x* system architecture, construction, host interfaces, and I/O expansion DCM sites.

CAUTION

This manual does not contain description and programming details
for on-board TI TMS320C6x DSP.

For more details about TI TMS320C6x DSP refer to original TI datasheets and user's guides
for TMS320C6x DSP, which are supplied in either paper or electronic form together with this
manual.

2.1   *TORNADO-E6x* System Architecture

System architectures for different *TORNADO-E6x* DSP controllers are presented at figures 2-1, whereas constructions for corresponding *TORNADO-E6x* DSP controllers are presented at figures 2-2.

TORNADO-E6x DSP controller comprises of the following components:
- 32-bit fixed-point TMS320C6201 DSP *(TORNADO-E62)*, 32-bit fixed-point TMS320C6202 DSP *(TORNADO-E6202)*, 32-bit fixed-point TMS320C6203 DSP *(TORNADO-E6203)*, 32-bit fixed-point TMS320C6414 DSP *(TORNADO-E6414)*, 32-bit fixed-point TMS320C6415 DSP *(TORNADO-E6415)*, 32-bit fixed-point TMS320C6416 DSP *(TORNADO-E6416)*, 32-bit floating-point TMS320C6701 DSP *(TORNADO-E67)*
- synchronous burst static RAM (SBSRAM) for program and data, which has 32-bit data format for *TORNADO-E62xx/E67* and 64-bit data format for *TORNADO-E64xx*
- synchronous DRAM (SDRAM) for program and data, which has 32-bit data format for *TORNADO-E62xx/E67* and 64-bit data format for *TORNADO-E64xx*
- socket for plug-in 8-bit FLASH/EPROM memory chip (PLCC-32 IC package) for DSP source boot code and/or non-volatile data
- dual-channel multiprotocol 10 Mbit/s USART (universal synchronous/asynchronous receiver/transmitter), which supports HDLC/X.25, SDLC, MONOSYNC, BISYNC, ASYNC protocols
- interface multiplexer for each of USART channel, which connects the I/O pins of the corresponding USART channel to either to 115 kBaud RS232C or 10 Mbit/s RS422/EIA-530 front-end interfaces
- 8-bit general purpose I/O (as the part of USART) with individual polarity and mask for generation of DSP interrupt generation
- 12 Mbit/s USB device controller for communication with host computers
- battery backed-up real-time clock (RTC) *(TORNADO-E64xx* only)
- 8-bit UTOPIA slave interface I/O connectors for *(TORNADO-E64xx* only)
- 10-bit DSP on-chip general purpose I/O connectors for *(TORNADO-E64xx* only)

- connector for external connection to TMS320C6x DSP host port interface (HPI)
- serial I/O expansion (SIOX) interface sites for SOX rev.B and SIOX rev.C DCM
- parallel I/O expansion (PIOX-16) interface site for PIOX-16 DCM
- MXSIOX connector (*TORNADO-E6202/E6203/E64xx* only) for connection to external *T/SU-X1*
  SIOX rev.B mini-extender kit for installation of one SIOX rev.B DCM
- watch-dog timer (WDT)
- external RESET connector and on-board RESET switch
- I/O controller (IOC)
- JTAG-IN connector for connection to external JTAG emulator
- external power connector.
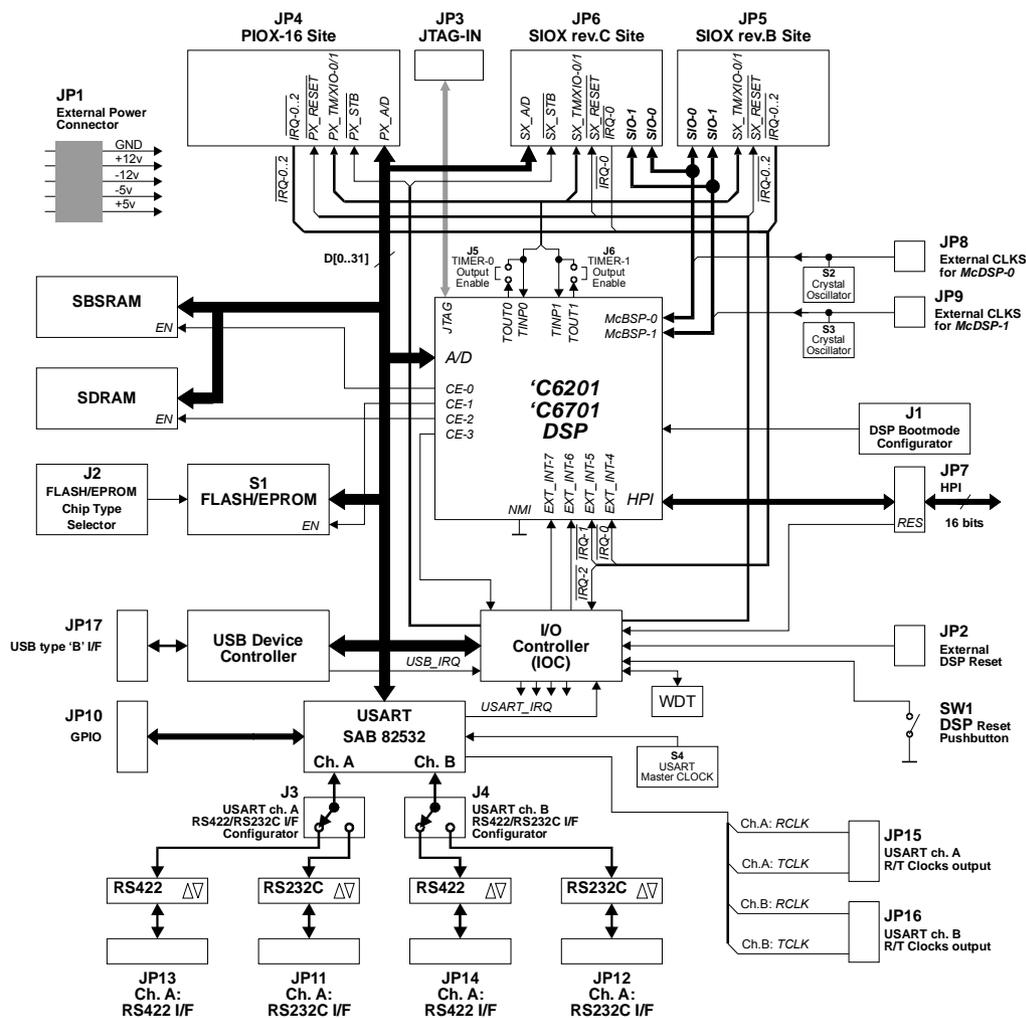
Fig.2-1a. System architecture of *TORNADO-E62/E67* DSP controllers.
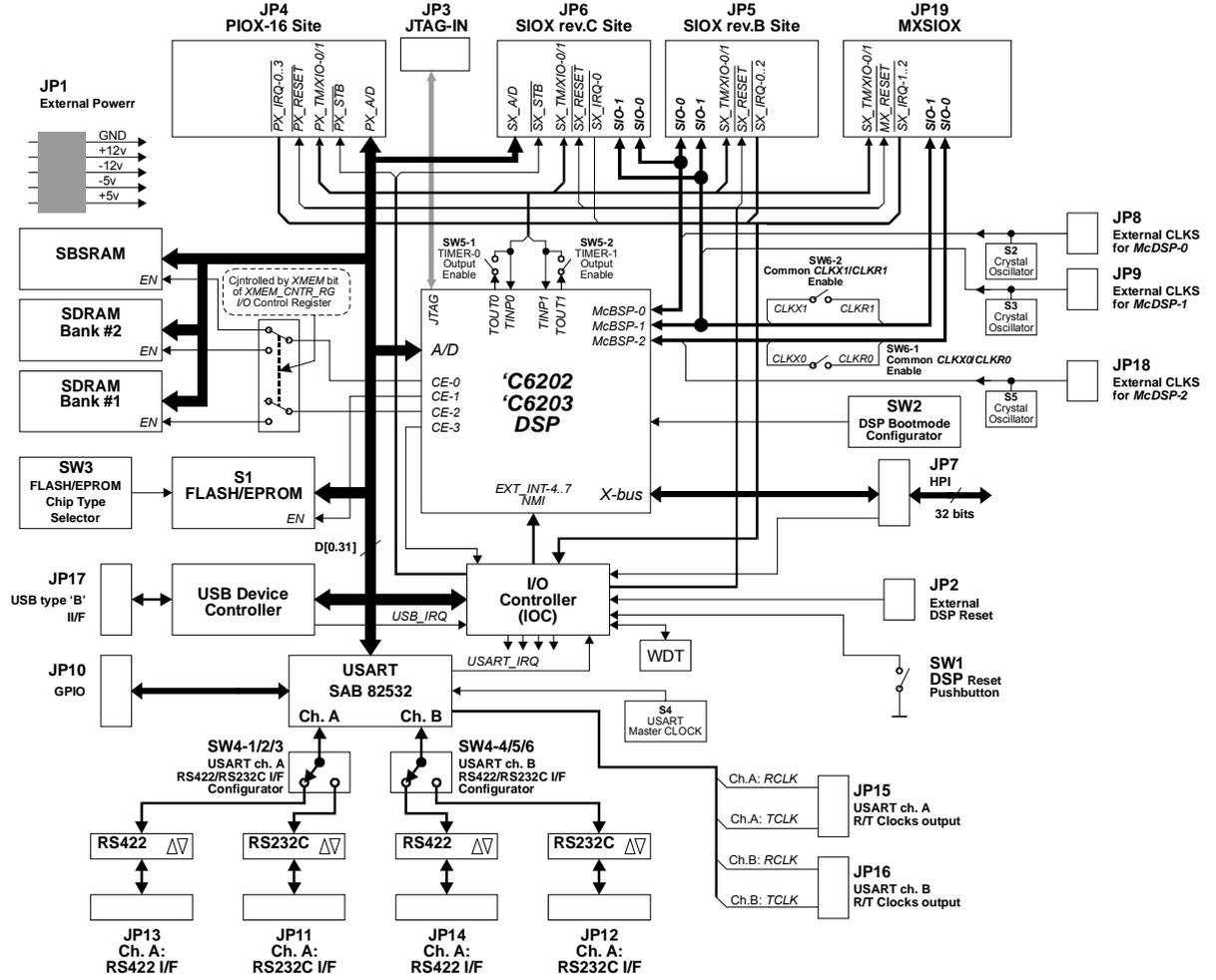
Fig.2-1b. System architecture of *TORNADO-E6202/E6203* DSP controllers.

JP4
PIOX-16 Site

JP3
JTAG-IN

JP6
SIOX rev.C Site

JP5
SIOX rev.B Site

JP19
MXSIOX

JP1
External Power
GND
+12v
-12v
-5v
+5v

PX_IRQ-0..3
PX_RESET
PX_TMXIO-0/1
PX_STB
PX_A/D

SX_A/D
SX_STB
SX_TMXIO-0/1
SX_RESET
SX_IRQ-0
SIO-1
SIO-0

SIO-0
SIO-1
SX_TMXIO-0/1
SX_RESET
SX_IRQ-0..2

SX_TMXIO-0/1
MX_RESET
SX_IRQ-1..2
SIO-1
SIO-0

JP21
DSP
TIMER-2 I/O

JP8
External CLKS
for McDSP-0

JP9
External CLKS
for McDSP-1

JP18
External CLKS
for McDSP-2

SBSRAM
EN

SDRAM
EN

D[0..15]

D[0..63]

SW5-1
TIMER-0
Output
Enable

SW5-2
TIMER-1
Output
Enable

SW5-3
TIMER-2
Output
Enable

SW6-2
Common CLKX1/CLKR1 Enable
CLKX1 CLKR1

JTAG
TOUT0
TINP0
TINP1
TOUT1
TINP2
TOUT2

McBSP-0
McBSP-1
McBSP-2

CLKX0 CLKR0
SW6-1
Common CLKX0/CLKR0
Enable

SW3
FLASH/EPROM
Chip Type
Selector

S1
FLASH/EPROM

EMIF-A
CE-0
CE-1
CE-2
CE-3

'C6414
'C6415
'C6416
DSP

GPIO

JP20
DSP GPIO

EMIF-B
CE-0
CE-1
CE-2
CE-3

HPI

JP7
HPI
RES
16/32 bits

SW2
● SW2-1..2 - DSP Bootmode Configurator
● SW2-3 - McBSP-1 / UTOPIA I/F Selector
● SW2-4 - HPI Data Mode

UTOPIA I/F
RECEIVER

UTOPIA I/F
TRANSMITTER

EN

EN

JP22
UTOPIA I/F
RECEIVER

JP23
UTOPIA I/F
TRANSMITTER

BT1

RTC

EXT_INT-4..7
NMI

RTC_WDT_IRQ
RTC_ALARM_IRQ

JP17
USB type "B"
I/F

USB Device
Controller

USB_IRQ

I/O
Controller
(IOC)

JP2
External
DSP Reset

WDT

SW1
DSP Reset
Pushbutton

JP10
GPIO

USART
SAB 82532
Ch. A   Ch. B

USART_IRQ

S4
USART
Master CLOCK

Ch.A: RCLK
Ch.A: TCLK

JP15
USART ch. A
R/T Clocks output

Ch.B: RCLK
Ch.B: TCLK

JP16
USART ch. B
R/T Clocks output

SW4-1/2/3
USART ch. A
RS422/RS232C I/F
Configurator

SW4-4/5/6
USART ch. B
RS422/RS232C I/F
Configurator

RS422

RS232C

RS422

RS232C

JP13
Ch. A:
RS422 I/F

JP11
Ch. A:
RS232C I/F

JP14
Ch. A:
RS422 I/FJP14

JP12
Ch. A:
RS232C I/F

Fig.2-1c. System architecture of *TORNADO-E6414/E6415/E6416* DSP controllers.
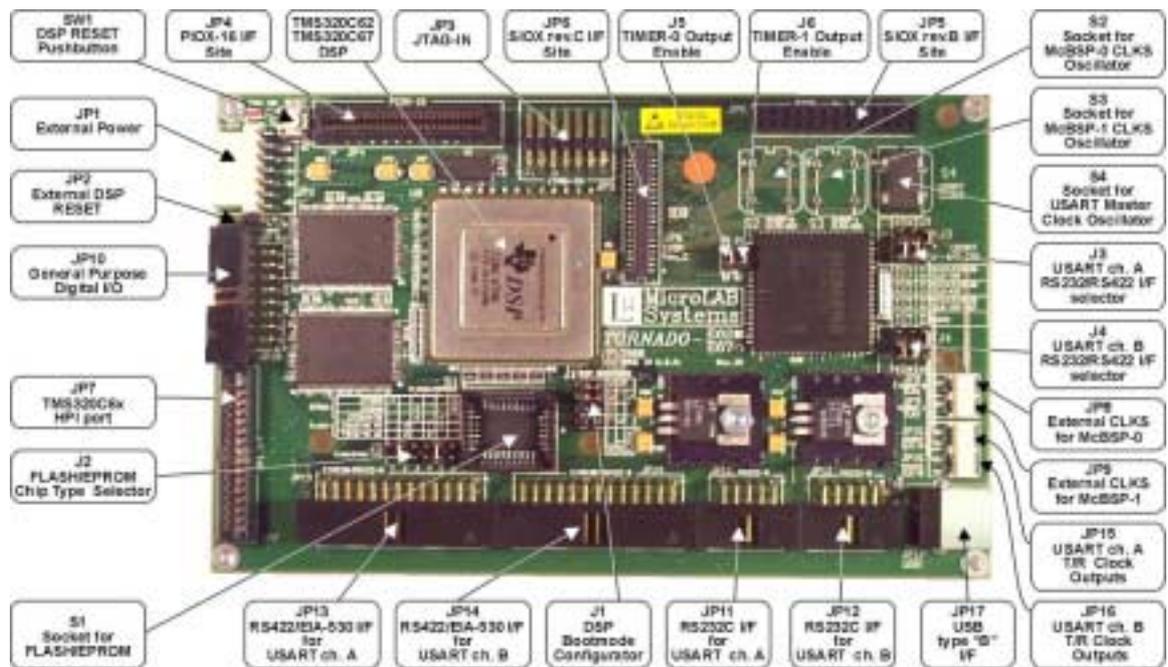
Fig.2-2a. Construction of *TORNADO-E62/E67* DSP controllers.
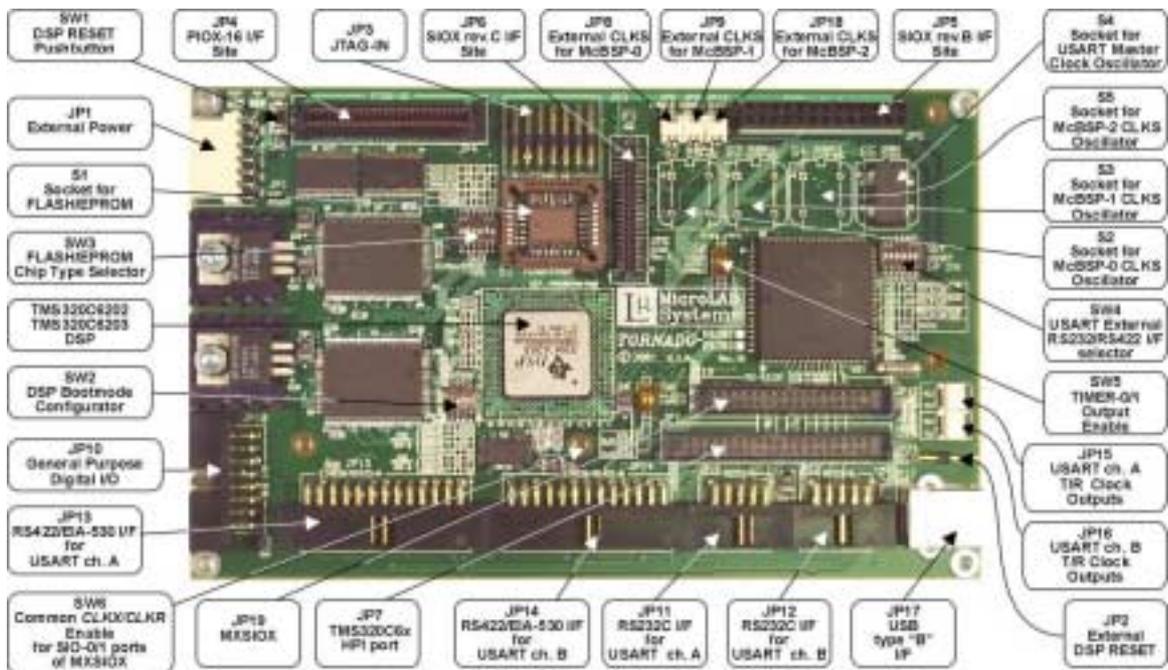
Fig.2-2b. Construction of *TORNADO-E6202/E6203* DSP controllers.
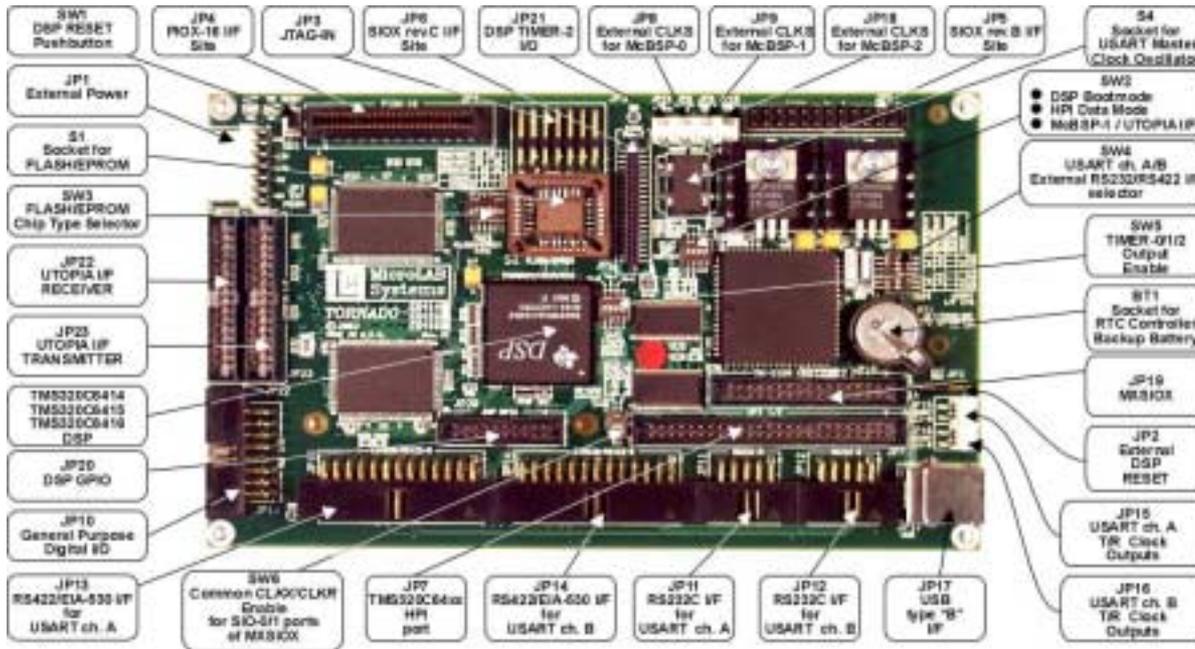
Fig.2-2c.   Construction of *TORNADO-E6414/E6415/E6416* DSP controllers.

TMS320C6x DSP

TORNADO-E6x on-board TMS320C6x DSP is defined by the controller type:
- 1600 MIPS @ 200 MHz 32-bit fixed-point TMS320C6201 DSP at *TORNADO-E62*
- 2000MIPS @ 240 MHz 32-bit fixed-point TMS320C6202 DSP at *TORNADO-E6202*
- 2400 MIPS @ 300 MHz 32-bit fixed-point TMS320C6203 DSP at *TORNADO-E6203*
- 4800 MIPS @ 600 MHz 32-bit fixed-point TMS320C6414/C6415/C6416 DSP at *TORNADO-E6414/E6415/E6416* correspondingly
- 1000 MFLOPS @ 167 MHz 32-bit floating-point TMS320C6701 DSP at *TORNADO-E67*.

All TMS320C6x DSP feature DSP on-chip VelociTI very-long instruction word (VLIW) on-chip architecture, which delivers ultra-high DSP performance. For more details about TMS320C6x DSP refer to the corresponding original TI datasheets and user's guides for TMS320C6x DSP.

Synchronous Burst Static RAM (SBSRAM)

TORNADO-E62xx/E67 DSP controllers provide up to 1Mx32 on-board synchronous burst static RAM (SBSRAM) for TMS320C6x DSP program and data. *TORNADO-E62xx/E67* on-board SBSRAM is mapped to DSP CE-0 EMIF area.

TORNADO-E64xx provide up to 1Mx64 of on-board SBSRAM for DSP program and data. *TORNADO-E64xx* on-board SBSRAM and SDRAM are connected to dedicated 64-bit synchronous EMIF-A bus and is

mapped to CE-0 EMIF-A area. Dedicated 64-bit synchronous EMIF-A bus delivers high SBSRAM/SDRAM bus bandwidth and high DSP performance.

TORNADO-E62/E67 DSP controllers allow simultaneous support of on-board SBSRAM and SDRAM by EMIF of on-board TMS320C6201/C6701 DSP. Number of wait states for DSP-to-SBSRAM access cycles depends upon the speed grades of on-board DSP and SBSRAM chips, and can be set either 0ws or 1ws (contact MicroLAB Systems for SBSRAM wait state details for your *TORNADO-E62/E67* DSP system).

TORNADO-E6202/E6203 DSP controllers do not allow simultaneous support of on-board SBSRAM and SDRAM by EMIF of on-board TMS320C6202/TMS320C6203 DSP. Particular currently active external synchronous memory (either SBSRAM or SDRAM) can be selected by DSP software. *TORNADO-E6202/E6203* DSP controllers always provide 1 ws for DSP-to-SBSRAM access cycles.

TORNADO-E64xx DSP controllers allow simultaneous support of on-board SBSRAM and SDRAM by TMS320C64xx EMIF-A interface. Recommended EMIF-A bus clock is ¼-th of the DSP clock (150MHz), which provides 4ws for DSP-to-SBSRAM access cycles.

Synchronous dynamic RAM (SDRAM)

TORNADO-E62/E67 DSP controllers provide 4Mx32 1ws of on-board synchronous dynamic RAM (SDRAM) for DSP program and data, which is mapped to DSP CE-2 EMIF area. On-board SBSRAM and SDRAM can be simultaneously supported by on-board TMS320C6201/TMS320C6701 DSP of *TORNADO-E62/E67* DSP controllers.

TORNADO-E6202/E6203 DSP controllers provide either 4Mx32 or 8Mx32 1ws of on-board SDRAM for DSP program and data. In case only 4Mx32 SDRAM is installed, then it is mapped into DSP CE-2 EMIF area (default SDRAM bank), whereas in case 8Mx32 SDRAM is installed, then it is splitted to two 4Mx32 SDRAM banks mapped to DSP CE-2 (default SDRAM bank) and CE-0 (SDRAM bank #1) EMIF areas. On-board SBSRAM and SDRAM cannot be simultaneously supported by on-board TMS320C6202/TMS320C6203 DSP of *TORNADO-E6202/E6203* DSP controllers. Particular currently active external synchronous memory (either SBSRAM or SDRAM) can be selected via DSP software.

TORNADO-E64xx DSP controllers provide either 4Mx64 or 16Mx64 of on-board SDRAM for TMS320C6x DSP program and data, which is connected to dedicated 64-bit synchronous EMIF-A bus along with on-board SBSRAM, and is mapped to CE-2 EMIF-A area. Dedicated 64-bit synchronous EMIF-A bus delivers high SBSRAM/SDRAM bus bandwidth and high DSP performance. *TORNADO-E64xx* DSP controllers allow simultaneous support of on-board SBSRAM and SDRAM by TMS320C64xx EMIF-A interface. Recommended EMIF-A bus clock is ¼-th of the DSP clock (150MHz), which provides 4ws for DSP-to-SDRAM access cycles.

FLASH/EPROM Memory

TORNADO-E6x provides up to 1Mx8 of on-board FLASH/EPROM memory for software boot. FLASH memory bank is designed to accommodate a variety of 8-bit FLASH or EPROM memory chip in the PLCC-32 package.

FLASH/EPROM memory bank of *TORNADO-E62xx/E67* DSP controllers is allocated into CE-1 area of DSP EMIF, whereas FLASH/EPROM memory bank of *TORNADO-E64xx* DSP controllers is allocated into CE-1 area of DSP EMIF-B interface.

FLASH/EPROM memory bank of all *TORNADO-E6x* DSP controllers features user selectable write protection facility for data integrity.

Dual-channel USART

TORNADO-E6x features the on-board dual-channel USART (universal synchronous/asynchronous receiver/transmitter) for communication with host computers, terminals, network adapters, or external peripherals.

USART supports industry standard synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) at up to 10 Mbit/s data transfer rate and asynchronous protocol (ASYNC) at up to 2.5 Mbaud independent for each channel.

Each USART channel connects to external equipment via jumper/switch selectable RS232C or RS422/EIA-530 electrical interface.

USB device interface

TORNADO-E6x rev.2A provide on-board 12 Mbit/s USB device interface for communication with external host computers. On-board USB interface connector is the USB type 'B' device connector. USB device controller and external interface meets USB rev.1.1 specifications.

TMS320C6x HPI (host port interface)

TORNADO-E6x delivers access from external host computer to the TMS320C6x DSP on-chip HPI, which allows both boot from host computer and access from host computer to entire TMS320C6x DSP environment with mutual interrupt generation.

TORNADO-E62/E67 DSP controllers feature 16-bit HPI port, which allows generation of bi-directional DSP-to-host interrupt requests via HPI port.

TORNADO-E6202/E6203 DSP controllers feature 32-bit slave HPI port, which does not allow generation of DSP-to-host interrupt request via HPI port.

TORNADO-E64xx DSP controllers provide user selectable 16-bit/32-bit HPI port, which allows generation of bi-directional DSP-to-host interrupt requests via HPI port.

HPI assumes that the HPI memory address must be pre-latched into HPI address register prior HPI data access will be performed. However, the HPI address auto post-incrementing feature is available and simplifies data array upload/download. HPI feature is available only while TMS320C6x DSP is executing the program (not in the reset state).

Real-time clock (RTC) (TORNADO-E64xx only)

TORNADO-E64xx DSP controllers provide on-board real-time clock (RTC) with built-in 2100 year calendar and on-board battery back-up. RTC offers accurate time/day/month/year count, programmable ring comparator and programmable watch-dog timer. RTC provides two programmable interrupt outputs, which can be software configured to generate DSP interrupt on either programmable alarm event or watch-dog timer expiration. RTC also provides 50 bytes of user NvRAM for non-volatile data.

General purpose digital I/O

TORNADO-E6x provide general purpose 8-bit digital I/O, which can be used as external control I/O signals. These digital I/O signals are the part of on-board USART, and allow generation of DSP interrupt on individually programmable high-to-low or low-to-high transitions when programmed as input pins.

DSP on-chip general purpose digital I/O (TORNADO-E64xx only)

TORNADO-E64xx DSP controllers provide optional general purpose 10-bit digital I/O, which is controlled directly by TMS320C64xx DSP on-chip GPIO control registers.

UTOPIA interface (TORNADO-E6415/E6416 only)

TORNADO-E6415/E6415 DSP controllers provide on-board 50MHz 8-bt UTOPIA level 2 slave interface for communication with external telecom equipment. UTOPIA interface is part of on-board TMS320C6415/C6416 DSP and is controlled directly by DSP on-chip UTOPIA control registers.

Serial I/O Expansion Interface (SIOX) sites

TORNADO-E6x on-board SIOX interface sites and comprises of one SIOX rev.B site, one enhanced SIOX rev.C site, and on-board MXSIOX connector (*TORNADO-E6202/E6203/E64xx* only) for connection to external *T/SU-X1* SIOX rev.B mini-extender kit, and shall be used for installation of compatible SIOX rev.B and rev.C DCM.

TORNADO SIOX AD/DA/DIO and application specific DCM include a variety of 'of-the-shelf' DSCM for telecom, speech/fax/modem, audio, and many more applications.

SIOX rev.B site includes signals for two serial ports, timers/IO pins, interrupt request inputs, whereas SIOX rev.C provides optional 8-bit parallel data bus with 6-bit address and data strobes.

On-board MXSIOX connector (*TORNADO-E6202/E6203/E64xx* only) can be used for connection to one external *T/SU-X1* SIOX rev.B mini-extender kit, which can carry one SIOX rev.B DCM, and includes signals for two serial ports, timers/IO pins, and interrupt request inputs.

Parallel I/O Expansion Interface (PIOX-16) site

TORNADO-E6x feature PIOX-16 interface site for installation of high-speed AD/DA/DIO DCM. PIOX-16 interface is allocated into the sub-area of TMS320C6x DSP CE-3 memory area.

PIOX-16 interface comprises of the signals for DSP 16-bit address and 16-bit data buses, data strobes and TMS320C6x DSP on-chip timers/IO pins and interrupts control.

PIOX-16 compatible DCM include a variety of high-speed multichannel AD/DA/DIO modules for high-speed telecom, instrumentation, digital radio and many more applications.

Watch-dog timer (WDT)

TORNADO-E6x provides optional on-board watch-dog timer (WDT) for reliable stand-alone operation. While the DSP is operating properly and in-case the WDT feature is enabled, DSP must send the WDT reset signal every 1.6 sec, otherwise WDT will generate the DSP reset signal in order to restart *TORNADO-E6x*.

DSP Reset Control

The DSP reset signal for *TORNADO-E6x* is generated by the DSP reset controller on the power-on/off conditions, external reset condition, on-board DSP RESET switch condition, on the WDT expiration condition, and on programmable RTC WDT expiration condition (*TORNADO-E64xx* only). Generated DSP reset signal has duration 0.2 sec, whereas the minimum duration of external reset signal is 500ns.

I/O controller

On-board I/O controller (IOC) is implemented using FPGA chip and comprises of a set of configuration and control registers, which are used to configure and control on-board TMS320C6x DSP and external DSP environment. I/O controller also decodes DSP address areas and generates strobes and synchronization signals to the on-board peripherals.

DSP external interrupts and NMI

TORNADO-E62/E67 feature multi-source software configurable DSP *EXT_INT6* and *EXT_INT7* external interrupts. *EXT_INT0* and *EXT_INT1* external interrupts are hardware wired to SIOX/PIOX-16 interrupt requests, and NMI is not used.

TORNADO-E6202/E6203/E64xx DSP controllers feature multi-source software configurable DSP external interrupts and NMI. The interrupt sources comprise of separate SIOX and PIOX-16 interrupts, USART and USB output interrupts, RTC output interrupts (*TORNADO-E64xx* only) and interrupt on WDT expiration event.

Selection of particular interrupt source for each of DSP software configurable external interrupts and NMI is performed by means of the corresponding interrupt selector registers, which are part of the on-board IO controller.

Debugging TMS320C6x DSP Software

TMS320C6x DSP software for *TORNADO-E6x* can be developed and debugged using MicroLAB Systems *MIRAGE-510DX* , *MIRAGE-P510DX* and TI XDS510 JTAG emulators using the industry standard TI C6000 Code Composer Studio IDE.

2.2   TMS320C6x DSP Environment

The *TORNADO-E6x* DSP controllers utilize state of the art TMS320C6x ultra-high performance compatible 32-bit fixed- and floating point DSP from TI:

- 1600 MIPS 32-bit fixed-point TMS320C6201 DSP in *TORNADO-EP62* DSP controller running at 200 MHz
- 2000 MIPS 32-bit fixed-point TMS320C6202 DSP in *TORNADO-E6202* DSP controller running at 250 MHz
- 2400 MIPS 32-bit fixed-point TMS320C6203 DSP in *TORNADO-E6203* DSP controller running at 300 MHz
- 4000 MIPS or 4800 MIPS 32-bit fixed-point TMS320C6414/C6415/C6416 DSP at *TORNADO-E6414/E6415/E6416* DSP controllers correspondingly running at 500 MHz (TMX-grade 'C64xx DSP silicon rev.1) and 600 MHz (TMS-grade 'C64xx DSP) correspondingly

- 1000 MFLOPS 32-bit floating-point TMS320C6701 DSP in *TORNADO-E67* DSP controller running at 167 MHz.

All TMS320C6x DSP feature code compatibility (except for the memory map for *TORNADO-E6414/E6415/E6416* DSP controllers), compatible DSP environment, compatible architecture, and compatible peripherals. The only differences apply to capacity of DSP on-chip RAM, number of DSP on-chip McBSP ports, DSP on-chip HPI port, DSP on-chip UTOPIA interface, DSP on-chip general purpose I/O and external real-time clock (RTC) peripheral.

CAUTION

This manual does not contain description and programming details
for on-board TI TMS320C6x DSP.

For more information refer to original TI datasheets and user's guides for TMS320C6x DSP,
which are supplied in either paper or electronic form together with this manual.

TMS32C6x DSP Endian Mode

TORNADO-E6x DSP controllers have been designed for little endian mode of on-board TMS320C6x DSP only. Big endian mode of on-board TMS320C6x DSP is not supported.

TMS32C6x DSP Bootmode Configurations

The TMS320C6x DSP bootmode configuration is defined by the on-board jumper set J1-1..J1-4 for *TORNADO-E62/E67* DSP controllers (refer to fig.2-2a and fig.A-1a), by the on-board SW2-1..4 switches for *TORNADO-E6202/E6203* DSP controllers (refer to fig.2-2b and fig.A-1b), and by the on-board SW2-1..2 switches for *TORNADO-E64xx* DSP controllers (refer to fig.2-2c and fig.A-1c).

CAUTION

TORNADO-E62xx/E67 DSP controllers support both MAP0 and MAP1 memory map
configurations for on-board TMS320C6x DSP.

Supported TMS320C6x DSP bootmode configurations for all *TORNADO-E6x* DSP controllers are presented in tables 2-1.

Table 2-1a. TMS320C6201/C6701 DSP bootmode configurations for *TORNADO-E62/E67*.

Bootmode ID	jumper J1-4	jumper J1-3	jumper J1-2	jumper J1-1	Description
DSP MAP0 bootmode configurations					
BM#3 (MAP0/SBSRAM/NO-BMODE)	ON	ON	OFF	OFF	Corresponds to TMS320C6x DSP bootmode #3. After DSP reset is released, DSP begins program execution without boot from on-board SBSRAM, which is allocated at EMIF CE-0 area at 00000000H address. DSP is configured to MAP0 memory configuration and automatic selection of ½xCLK SBSRAM at EMIF CE-0 area.
BM#6 (MAP0/X/HPI-BMODE)	ON	OFF	OFF	ON	Corresponds to TMS320C6x DSP bootmode #6. After DSP reset is released, DSP starts with boot via HPI port, and afterthat begins program execution from on-board SBSRAM, which is allocated at EMIF CE-0 area at 00000000H address. DSP is configured to MAP0 memory configuration and default asynchronous memory timings for all EMIF areas. Host can upload data/code to any DSP memory area. Prior uploading data to DSP environment host must configure DSP EMIF CE-0 area via HPI port to run with ½xCLK SBSRAM
BM#11 (MAP0/SBSRAM/ FLASH8-BMODE)	OFF	ON	OFF	OFF	Corresponds to TMS320C6x DSP bootmode #11. After DSP reset is released, DSP reloads 64 Kbytes from on-board 8-bit FLASH/EPROM starting from 00000H FLASH/EPROM address to on-board SBSRAM at 00000000H address, which is allocated at EMIF CE-0 area, and afterthat begins program execution from on-board SBSRAM at 00000000H address. DSP is configured to MAP0 memory configuration and automatic selection of ½xCLK SBSRAM at EMIF CE-0 area.
DSP MAP1 bootmode configurations					
BM#5 (MAP1/X/NO-BMODE)	ON	OFF	ON	OFF	Corresponds to TMS320C6x DSP bootmode #5. After DSP reset is released, DSP begins program execution without boot from DSP on-chip program memory, which is mapped to 00000000H address. DSP is configured to MAP1 memory configuration and default asynchronous memory timings for all EMIF areas. On-board ½xCLK SBSRAM at EMIF CE-0 area is mapped to 00400000H address.

BM#7 (MAP1/X/HPI-BMODE)	ON	OFF	OFF	OFF	Corresponds to TMS320C6x DSP bootmode #7. After DSP reset is released, DSP starts with boot via HPI port, and afterthat begins program execution from DSP on-chip memory, which is mapped to 00000000H address. DSP is configured to MAP1 memory configuration and default asynchronous memory timings for all EMIF areas. On-board ½xCLK SBSRAM at EMIF CE-0 area is mapped to 00400000H address.
BM#13 (MAP1/X/ FLASH8-BMODE)	OFF	OFF	ON	OFF	Corresponds to TMS320C6x DSP bootmode #13. After DSP reset is released, DSP reloads 64 Kbytes from on-board 8-bit FLASH/EPROM starting from 00000H FLASH/EPROM address to DSP on-chip RAM at 00000000H address, and afterthat begins program execution from DSP on-chip memory at 00000000H address. DSP is configured to MAP1 memory configuration and default asynchronous memory timings for all EMIF areas. On-board ½xCLK SBSRAM at EMIF CE-0 area is mapped to 00400000H address.

Note: 1. 'ON' corresponds to installed jumper; 'OFF' corresponds to removed jumper.
2. Other bootmode configurations are reserved and are not recommended for usage.
3. Highlighted configuration corresponds to the factory setting.

Table 2-1b. TMS320C6202/C6203 DSP bootmode configurations for *TORNADO-E6202/E6203*.

Bootmode ID	switch SW2-4	Switch SW2-3	switch SW2-2	switch SW2-1	Description
DSP MAP0 bootmode configurations					
BM#1 (MAP0/SDRAM/ NO-BMODE)	ON	ON	OFF	OFF	Corresponds to TMS320C6x DSP bootmode #1. After DSP reset is released, DSP begins program execution without boot from on-board SDRAM bank #1, which is allocated at EMIF CE-0 area at 00000000H address. DSP is configured to MAP0 memory configuration and automatic selection of SDRAM bank #1 at EMIF CE-0 area. External SDRAM memory is selected via on-board *SYS_CNF_RG* control register. This bootmode configuration shall be used only in case *TORNADO-E6202/E6203* DSP controller has 8Mx32 SDRAM installed.

BM#3 (MAP0/SBSRAM/ NO-BMODE)	ON	ON	OFF	OFF	Corresponds to TMS320C6x DSP bootmode #3. After DSP reset is released, DSP begins program execution without boot from on-board SBSRAM, which is allocated at EMIF CE-0 area at 00000000H address. DSP is configured to MAP0 memory configuration and automatic selection of ½xCLK SBSRAM at EMIF CE-0 area. External SBSRAM memory is selected via on-board *SYS_CNF_RG* control register.
BM#6 (MAP0/X-SBSRAM/ HPI-BMODE)	ON	OFF	OFF	ON	Corresponds to TMS320C6x DSP bootmode #6. After DSP reset is released, DSP starts with boot via HPI port, and afterthat begins program execution without boot from on-board SBSRAM or SDRAM bank #1, which are allocated at EMIF CE-0 area at 00000000H address. DSP is configured to MAP0 memory configuration and default asynchronous memory timings for all EMIF areas. External SBSRAM memory is selected via on-board *SYS_CNF_RG* control register. Prior uploading data to DSP environment host must configure DSP EMIF areas and correspondingly set *SYS_CNF_RG* control register via HPI port to run either with ½xCLK SBSRAM or SDRAM bank #1 upon the customer application.
BM#9 (MAP0/SDRAM/ FLASH8-BMODE)	OFF	ON	ON	OFF	Corresponds to TMS320C6x DSP bootmode #9. After DSP reset is released, DSP reloads 64 Kbytes from on-board 8-bit FLASH/EPROM starting from 00000H FLASH/EPROM address to on-board SDRAM bank #1 at 00000000H address, which is allocated at EMIF CE-0 area, and afterthat begins program execution from on-board SDRAM bank #1 at 00000000H address. DSP is configured to MAP0 memory configuration and automatic selection of SDRAM at EMIF CE-0 area. External SDRAM memory is selected via on-board *SYS_CNF_RG* control register. This bootmode configuration shall be used only in case *TORNADO-E6202/E6203* DSP controller has 8Mx32 SDRAM installed.

BM#11 *(MAP0/SBSRAM/* *FLASH8-BMODE)*	OFF	ON	OFF	OFF	Corresponds to TMS320C6x DSP bootmode #11. After DSP reset is released, DSP reloads 64 Kbytes from on-board 8-bit FLASH/EPROM starting from 00000H FLASH/EPROM address to on-board SBSRAM bank at 00000000H address, which is allocated at EMIF CE-0 area, and afterthat begins program execution without boot from on-board SBSRAM at 00000000H address. DSP is configured to MAP0 memory configuration and automatic selection of ½xCLK SBSRAM at EMIF CE-0 area. External SBSRAM memory is selected via on-board *SYS_CNF_RG* control register.
DSP MAP1 bootmode configurations					
BM#5 *(MAP1/X-SBSRAM/* *NO-BMODE)*	ON	OFF	ON	OFF	Corresponds to TMS320C6x DSP bootmode #5. After DSP reset is released, DSP begins program execution without boot from DSP on-chip program memory, which is mapped to 00000000H address. DSP is configured to MAP1 memory configuration and default asynchronous memory timings for all EMIF areas. External SBSRAM memory is selected via on-board *SYS_CNF_RG* control register. On-board SBSRAM or SDRAM bank #2 at EMIF CE-0 area is mapped to 00400000H address.
BM#7 *(MAP1/X-SBSRAM/* *HPI-BMODE)*	ON	OFF	OFF	OFF	Corresponds to TMS320C6x DSP bootmode #7. After DSP reset is released, DSP starts with boot via HPI port, and afterthat begins program execution from DSP on-chip memory, which is mapped to 00000000H address. DSP is configured to MAP1 memory configuration and default asynchronous memory timings for all EMIF areas. External SBSRAM memory is selected via on-board *SYS_CNF_RG* control register. On-board SBSRAM or SDRAM bank #1 at EMIF CE-0 area is mapped to 00400000H address. In case user application requires to upload data to external DSP memory areas, then host must configure DSP EMIF areas and correspondingly set SYS_CNF_RG control register via HPI port to run either with ½xCLK SBSRAM or SDRAM bank #1 upon the customer application.

BM#13 (MAP1/X-SBSRAM/ FLASH8-BMODE)	OFF	OFF	ON	OFF	Corresponds to TMS320C6x DSP bootmode #13. After DSP reset is released, DSP reloads 64 Kbytes from on-board 8-bit FLASH/EPROM starting from 00000H FLASH/EPROM address to DSP on-chip RAM at 00000000H address, and afterthat begins program execution from DSP on-chip RAM at 00000000H address. DSP is configured to MAP1 memory configuration and default asynchronous memory timings for all EMIF areas. External SBSRAM memory is selected via on-board *SYS_CNF_RG* control register. On-board SBSRAM or SDRAM bank #1 at EMIF CE-0 area is mapped to 00400000H address.

Note: 1. 'ON' corresponds to the 'ON' switch setting; 'OFF' corresponds to the 'OFF' switch setting.
             2. Other bootmode configurations are reserved and are not recommended for usage.
             3. Highlighted configuration corresponds to the factory setting.

Table 2-1c. TMS320C64xx DSP bootmode configurations for *TORNADO-E64xx*.

Bootmode ID	switch SW2-1	switch SW2-2	Description
BM#5 (NO-BMODE)	ON	ON	Corresponds to TMS320C64xx DSP bootmode #0, i.e. no DSP boot. For compatibility with *TORNADO-E62xx/E67* DSP controllers, this TMS320C64xx DSP bootmode for *TORNADO-E64xx* reads back via *BMODE_RG* I/O control register as *BM#5*. After DSP reset is released, DSP begins program execution without boot from DSP on-chip RAM at 00000000H address.
BM#7 (HPI-BMODE)	OFF	ON	Corresponds to TMS320C64xx DSP bootmode #1, i.e. DSP boot via DSP on-chip HPI port. For compatibility with *TORNADO-E62xx/E67* DSP controllers, this TMS320C64xx DSP bootmode for *TORNADO-E64xx* reads back via *BMODE_RG* I/O control register as *BM#7*. After DSP reset is released, DSP starts with boot via HPI port, and afterthat begins program execution without boot from DSP on-chip RAM at 00000000H address. Prior uploading data to DSP external environment host must configure DSP EMIF-A/B areas in accordance with table 2-3.

| BM#13
(FLASH8-BMODE) | ON | OFF | Corresponds to TMS320C64xx DSP bootmode #2, i.e. boot from on-board 8-bit FLASH/EPROM. For compatibility with *TORNADO-E62xx/E67* DSP controllers, this TMS320C64xx DSP bootmode for *TORNADO-E64xx* reads back via *BMODE_RG* I/O control register as *BM#13*.

After DSP reset is released, DSP reloads 1 Kbyte from on-board 8-bit FLASH/EPROM starting from 00000H FLASH/EPROM address to DSP on-chip RAM at 00000000H address, and afterthat begins program execution from 00000000H address. In case user DSP application occupies more than 1 Kbyte, then user must provide optional bootloader, which must be integrated into user code and allocated to be loaded first within 1 Kbyte address area of FLASH/EPROM under TMS320C64xx DSP on-chip EDMA control in 8-bit FLASH/EPROM bootmode in order to load full application code afterthat. |

Note:
1. 'ON' corresponds to the 'ON' switch setting; 'OFF' corresponds to the 'OFF' switch setting.
2. Other bootmode configurations are reserved and are not recommended for usage.
3. Highlighted configuration corresponds to the factory setting.

TORNADO-E62/E67 DSP controllers do not allow read-back of start-up DSP bootmode configuration via DSP software, whereas *TORNADO-E6202/E6203* and *TORNADO-E64xx* DSP controllers provide *BMODE_RG* read-only control register, which can be used to read start-up DSP bootmode code in order to automatically configure base addresses for DSP on-chip program memory, external SBSRAM and FLASH/EPROM memories and in order to perform application specific processing. For more details refer to the corresponding subsection below.

CAUTION

Although original TI documentation specifies TMS320C64xx DSP bootmode ID codes within #0..#2 range, *TORNADO-E64xx* DSP controllers convert original TI bootmode ID codes #0, #1 and #2 for TMS320C64xx DSP to TMS320C62xx/C6701 DSP bootmode ID codes #5, #7 and #13 correspondingly when reading *BMODE_RG* read-only control register.

This delivers compatibility between *TORNADO-E64xx* and *TORNADO-E62xx/E67* DSP controllers and allows to use common TMS320C6x DSP bootmode ID returned via *BMODE_RG* read-only control register for all *TORNADO-E6x* DSP controllers.

On-board reset signal for TMS320C6x DSP, I/O peripherals and I/O control registers

TORNADO-E6x on-board reset controller generates on-board reset signal for on-board TMS320C6x DSP, on-board I/O peripherals and on-board I/O control registers as the logical 'OR' of the following input conditions:
- in case of +5v power on and +5v power off condition
- external active low reset signal is applied via on-board JP2 connector
- external active low reset signal is applied via TMS320C6x DSP HPI port JP7 connector
- on-board RESET pushbutton (SW1) has been pressed
- on-board watch-dog timer (WDT) is enabled via bit *WDT_EN* bit of *WDT_EN_RG* I/O control register and the WDT latency period (1.6 sec typical) has been expired

- *TORNADO-E64xx* only: programmable watch-dog timer of on-board real-time clock (RTC) peripheral is enabled via bit *RTC_WDT_EN* bit of *WDT_EN_RG* I/O control register and programmed WDT-RTC latency period has been expired.

TORNADO-E6x on-board reset signal is generated immediately in case any of the above listed condition goes to the 'true' state. After each of the above listed condition is released to the 'false' state, then on-board reset signal will be released after about 0.2 sec in order to provide minimum duration of *TORNADO-E6x* on-board reset signal about 0.2 sec.

Generated *TORNADO-E6x* on-board reset signal is simultaneously applied to on-board TMS320C6x DSP, all on-board I/O peripherals and all I/O control registers (refer to table 2-2 and to the corresponding subsections below).

TMS320C6x DSP memory map

DSP memory maps for *TORNADO-E62xx/E67* on-board TMS320C62xx/C6701 DSP and for *TORNADO-E64xx* on-board TMS320C64xx DSP significantly differs from each other due to the different memory maps for TMS320C62xx/C6701 and TMS320C64xx DSP.

CAUTION

TMS320C62xx/C6701 DSP applications, which are compiled for *TORNADO-E62xx/E67* DSP controllers and which use onboard SBSRAM, SDRAM, peripherals and control registers, will not run at *TORNADO-E64xx* DSP controllers.

Vice-versa, TMS320C64xx DSP applications, which are compiled for *TORNADO-E64xx* DSP controllers and which use onboard SBSRAM, SDRAM, peripherals and control registers, will not run at *TORNADO-E62xx/E67* DSP controllers.

TORNADO-E62xx/E67 on-board TMS320C62xx/C6701 DSP supports four external memory areas:
- EMIF CE-0 area, which controls on-board 32-bit SBSRAM for *TORNADO-E62/E67* DSP controllers, and shared SBSRAM and optional SDRAM #1 bank for *TORNADO-E6202/E6203* DSP controllers. Selection between SBSRAM and SDRAM memory in EMIF CE-0 area for *TORNADO-E6202/E6203* DSP controllers is performed via bit *XMEM* bit of *SYS_CNF_RG* control register (refer to the corresponding subsection below).
- EMIF CE-1 area, which controls on-board 8-bit FLASH/EPROM
- EMIF CE-2 area, which controls on-board 32-bit SDRAM bank (default SDRAM bank for *TORNADO-E6202/E6203*). SDRAM bank in EMIF CE-2 area for *TORNADO-E6202/E6203* DSP controllers is activated along with optional SDRAM-1 bank via bit *XMEM* of *SYS_CNF_RG* control register (refer to the corresponding subsection below).
- EMIF CE-3 area, which controls on-board control registers and I/O peripherals (USART, USB controller, PIOX-16/SIOX DCM sites, etc).

TORNADO-E64xx on-board TMS320C64xx DSP supports the following four external memory areas:
- EMIF-A CE-0 area, which controls on-board 64-bit SBSRAM
- EMIF-A CE-2 area, which controls on-board 64-bit SDRAM bank

- EMIF-B CE-0 area, which controls on-board control registers and I/O peripherals (USART, USB controller, RTC, PIOX-16/SIOX DCM sites, etc).
- EMIF-B CE-1 area, which controls on-board 8-bit FLASH/EPROM.

Memory maps for *TORNADO-E62xx/E67* on-board TMS320C62xx/C6701 DSP for both MAP0 and MAP1 TMS320C62xx/C6701 DSP memory map configurations are presented in table 2-2a. Memory map for *TORNADO-E64xx* on-board TMS320C64xx DSP is presented in table 2-2b.

CAUTION

TMS320C6x DSP address space for *TORNADO-E6x* DSP controllers is the address space for 8-bit (byte) data words.

16-bit data words are allocated on the x2 DSP address boundaries.

32-bit data words are allocated on x4 DSP address boundaries.

Table 2-2a. TMS320C62xx/C6701 DSP memory map for *TORNADO-E62xx/E67* DSP controllers.

DSP address area	DSP address range (bytes)	valid data bits	value at DSP RESET	access mode	wait states	DSP EMIF area and mode
TMS320C62xx/C6701 DSP on-chip and external memory areas						
SBSRAM	*'C6x DSP MAP0:* 00000000H ..003FFFFFH *'C6x DSP MAP1:* 00400000H ..007FFFFFH	D0..D31	-	r/w	0/1ws [5)] (*TORNADO-E62/E67*) 1ws (*TORNADO-E6202/E6203*)	CE-0 SBSRAM mode
SDRAM bank #1 (*TORNADO-E6202/E6203*)	*'C6x DSP MAP0:* 00000000H ..00FFFFFFH *'C6x DSP MAP1:* 00400000H ..013FFFFFH				1ws	SDRAM mode
FLASH/EPROM	*'C6x DSP MAP0:* 01000000H ..013FFFFFH *'C6x DSP MAP1:* 01400000H ..017FFFFFH	D0..D7	-	r/w	FWS	CE-1 ASYNC ROM mode

DSP on-chip program RAM	01400000H ..0140FFFFH (*TORNADO-E62/E67*) 01400000H ..0143FFFFH (*TORNADO-E6202*) 01400000H ..0145FFFFH (*TORNADO-E6203*)	D0..D31	-	r/w	-	-
DSP on-chip peripheral registers	01800000H ..01FFFFFFH	D0..D31	-	r/w	-	-
SDRAM	02000000H ..02FFFFFFH	D0..D31	-	r/w	1ws	CE-2 SDRAM mode
DSP on-chip data RAM	80000000H ..8000FFFFH (*TORNADO-E62/E67*) 80000000H ..8001FFFFH (*TORNADO-E6202*) 80000000H ..8007FFFFH (*TORNADO-E6203*)	D0..D31	-	r/w	-	-
External peripherals and I/O expansion interfaces						
I/O area: *dual-channel USART*	03000000H ..030000FCH (channel A) 03000100H ..030001FCH (channel B)	D0..D7	-	r/w	70ns (generated by on-board h/w)	CE-3 ASYNC mode
I/O area: *USB controller*	03080000H 0308007CH	D0..D7	-	r/w	70ns (generated by on-board h/w)	
I/O area: *SIOX rev.C parallel interface*	03300000H ..033000FFH	D0..D7	-	r/w	AWS +SX_RDY	
I/O area: *PIOX-16 parallel interface*	033C0000H ..033FFFFFH	D0..D15	-	r/w	AWS +PX_RDY	

External I/O control registers						
I/O area: *WDT_RESET_RG* (WDT reset control register)	03100000H	written data is ignored	-	w	100ns (generated by on-board h/w)	CE-3 ASYNC mode
I/O area: *WDT_EN_RG* (WDT enable control register)	03100004H	D0..D3	0H	r/w	AWS	
I/O area: *DSP_EXT_INT6_SEL_RG* (DSP INT6 source selector control register)	03180000H	D0..D3	0H	r/w	AWS	
I/O area: *DSP_EXT_INT7_SEL_RG* (DSP INT6 source selector control register)	03180004H	D0..D3	2H	r/w	AWS	
I/O area: *DSP_EXT_INT4_SEL_RG* (DSP INT4 source selector control register) (*TORNADO-E6202/E6203*)	03180008H	D0..D3	4H	r/w	AWS	
I/O area: *DSP_EXT_INT5_SEL_RG* (DSP INT5 source selector control register) (*TORNADO-E6202/E6203*)	03180008H	D0..D3	5H	r/w	AWS	
I/O area: *DSP_NMI_SEL_RG* (DSP NMI source selector control register) (*TORNADO-E6202/E6203*)	0318000CH	D0..D3	FH	r/w	AWS	
I/O area: *PXSX_RESET_RG* (PIOX/SIOX reset control register)	03200000H	D0..D3	0H	r/w	AWS	
I/O area: *DEV_ID_RG* (device ID control register) (*TORNADO-E6202/E6203*)	03200004H	D0..D3	[1]	r	AWS	
I/O area: *BMODE_RG* (bootmode control register) (*TORNADO-E6202/E6203*)	03200008H	D0..D3	[1]	r	AWS	

I/O area: *SYS_CNF_RG* *(XMEM_CNF_RG)* (system configuration control register, also known as external memory configuration register) (*TORNADO-E6202/E6203*)	0320000CH	D0..D3	0H/1H [1]	r/w	AWS	

Notes:
1. Refer to the corresponding subsection below for more details.
2. *AWS* denotes number of software programmed wait states for accessing asynchronous TMS320C620x/C6701 DSP EMIF CE-3 area, which is a sum of read/write strobe wait states, read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
3. *FWS* denotes number of software programmed framing wait states for accessing asynchronous DSP EMIF CE-1 area, which is a sum of read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
4. *SX_RDY* and *PX_RDY* denote extra wait states, which can be generated by external hardware ready signals for on-board SIOX-A rev.C site and PIOX/PIOX-16 site. Refer to the corresponding sections later in this chapter for more details about SIOX and PIOX expansion interface sites.
5. Number of programmed wait states (either 0ws or 1ws) for on-board SBSRAM bank of *TORNADO-E62/E67* DSP controllers depends upon the speed grade of particular SBSRAM chips installed. Refer to the corresponding subsection below for more details.
6. Other DSP memory and I/O areas are reserved. Do not use these address areas.
7. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

Table 2-2b. TMS320C64xx DSP memory map for *TORNADO-E64xx* DSP controllers.

DSP address area	DSP address range (bytes)	valid data bits	value at DSP RESET	access mode	wait states	DSP EMIF area and mode
TMS320C64xx DSP on-chip and external memory areas						
DSP on-chip RAM (L2)	00000000H ..000FFFFFH	D0..D31	-	r/w	-	-
DSP on-chip peripheral registers	01800000H ..01B7FFFFH 02000000H ..02000033H	D0..D31	-	r/w	-	-
FLASH/EPROM	64000000H ..641FFFFFH	D0..D7	-	r/w	FWS	EMIF-B CE-1 ASYNC 8-bit ROM mode
SBSRAM	80000000H ..807FFFFFH	D0..D63	-	r/w	4ws [5]	EMIF-A CE-0 64-bit SBSRAM mode

SDRAM	A0000000H ..A7FFFFFFH	D0..D63	-	r/w	4ws [5]	EMIF-A CE-2 64-bit SDRAM mode
External peripherals and I/O expansion interfaces						
I/O area: *dual-channel USART*	60000000H ..6000007EH (channel A) 60000080H ..600000FEH (channel B)	D0..D7	-	r/w	70ns (generated by on-board h/w)	EMIF-B CE-0 16-bit ASYNC mode
I/O area: *USB controller*	60020000H ..6002003EH	D0..D7	-	r/w	70ns (generated by on-board h/w)	
I/O area: *RTC controller*	60040000H ..6004007EH	D0..D7	-	r/w	160ns (generated by on-board h/w)	
I/O area: *SIOX rev.C parallel interface*	60120000H ..6012007FH	D0..D7	-	r/w	AWS *+SX_RDY*	
I/O area: *PIOX-16 parallel interface*	60100000H ..6011FFFFH	D0..D15	-	r/w	AWS *+PX_RDY*	
External I/O control registers						
I/O area: *DSP_EXT_INT4_SEL_RG* (DSP INT4 source selector control register)	60060000H	D0..D3	4H	r/w	AWS	EMIF-B CE-0 16-bit ASYNC mode
I/O area: *DSP_EXT_INT5_SEL_RG* (DSP INT5 source selector control register)	60060002H	D0..D3	5H	r/w	AWS	
I/O area: *DSP_EXT_INT6_SEL_RG* (DSP INT6 source selector control register)	60060004H	D0..D3	0H	r/w	AWS	
I/O area: *DSP_EXT_INT7_SEL_RG* (DSP INT6 source selector control register)	60060006H	D0..D3	2H	r/w	AWS	

I/O area: *DSP_NMI_SEL_RG* (DSP NMI source selector control register)	60060008H	D0..D3	FH	r/w	AWS	
I/O area: *WDT_RESET_RG* (WDT reset control register)	6006000EH	written data is ignored	-	w	100ns (generated by on-board h/w)	
I/O area: *WDT_EN_RG* (WDT enable control register)	60060010H	D0..D3	0H	r/w	AWS	
I/O area: *PXSX_RESET_RG* (PIOX/SIOX reset control register)	60060012H	D0..D3	0H	r/w	AWS	
I/O area: *DEV_ID_RG* (device ID control register)	60060014H	D0..D3	1)	r	AWS	
I/O area: *BMODE_RG* (bootmode control register)	60060016H	D0..D3	1)	r	AWS	
I/O area: *SYS_CNF_RG* (system configuration register)	60060018H	D0..D3	0H/2H 1)	r/w	AWS	
I/O area: *DEV_REV_ID_RG* (device revision ID register)	6006001AH	D0..D3	1)	r/w	AWS	

Notes:
1. Refer to the corresponding subsection below for more details.
2. *AWS* denotes number of software programmed wait states for accessing asynchronous TMS320C64xx DSP EMIF-B CE-0 area, which is a sum of read/write strobe wait states, read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
3. *FWS* denotes number of software programmed framing wait states for accessing asynchronous DSP EMIF CE-1 area, which is a sum of read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
4. *SX_RDY* and *PX_RDY* denote extra wait states, which can be generated by external hardware ready signals for on-board SIOX-A rev.C site and PIOX/PIOX-16 site. Refer to the corresponding sections later in this chapter for more details about SIOX and PIOX expansion interface sites.
5. Number of SBSRAM/SDRAM wait states is defined by EMIF-A interface clock, which is hardware configured to DSPCLK/4. EMIF-A CE-0 and CE-2 secondary control registers shall be configured to set *SNCCLK* bit of these registers to the '0' state in order to synchronize EMIF-A CE-0/CE-2 spaces to EMIF-A ECLKOUT1 clock. Refer to original TI documentation and to the corresponding subsection below for more details.
6. Other DSP memory and I/O areas are reserved. Do not use these address areas.
7. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

> **CAUTION**
>
> *TORNADO-E62xx/E67* on-board peripherals, control registers and PIOX-16 and SIOX rev.C DCM site interfaces are allocated at least significant 8-bit and 16-bit data words of 32-bit data words (UNSIGNED LONG C-type variables) at x4 DSP address boundaries.

> **CAUTION**
>
> *TORNADO-E64xx* on-board peripherals, control registers and SIOX rev.C DCM site interface are allocated at least significant 8-bit data words of 16-bit data words (UNSIGNED SHORT C-type variables) of TMS320C64xx EMIF-B interface at x2 DSP address boundaries.
>
> *TORNADO-E64xx* on-board PIOX-16 DCM site interface is allocated at 16-bit data words (UNSIGNED SHORT C-type variables) of TMS320C64xx EMIF-B interface at x2 DSP address boundaries.

Setting EMIF control registers of TMS320C6x DSP

In order to provide correct operation of *TORNADO-E62xx/E67* on-board hardware, user DSP application for *TORNADO-E62xx/E67* DSP controllers must set TMS320C620x/C6701 DSP on-chip EMIF control registers (*EMIF_GCR, EMIF_CE0_SCR, EMIF_CE1_SCR, EMIF_CE2_SCR, EMIF_CE3_SCR, EMIF_SDRAM_CR, EMIF_SDRAM_TMR*) in accordance with table 2-3a.

Correspondingly, DSP application for *TORNADO-E64xx* DSP controllers must set TMS320C64xx DSP on-chip EMIF control registers (*EMIFA_GCR, EMIFA_CE0_SCR, EMIFA_CE1_SCR, EMIFA_CE2_SCR, EMIFA_CE3_SCR, EMIFA_CE0_SEC, EMIFA_CE1_SEC, EMIFA_CE2_SEC, EMIFA_CE3_SEC, EMIFA_SDRAM_CR, EMIFA_SDRAM_EXT, EMIFA_SDRAM_TMR, EMIFB_GCR, EMIFB_CE0_SCR, EMIFB_CE1_SCR, EMIFB_CE2_SCR, EMIFB_CE3_SCR*) in accordance with table 2-3b.

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CAUTION

Application DSP software must configure TMS320C6x DSP on-chip EMIF control registers in accordance with table 2-3 as early as possible after the program starts.

In case DSP bootmodes via DSP on-chip HPI port (*MAP0/X/HPI-BMODE*, *MAP1/X/HPI-BMODE*, *MAP0/X-SBSRAM/HPI-BMODE*, *MAP1/X-SBSRAM/HPI-BMODE*) are being used (refer to table 2-1), then host computer/controller must configure TMS320C6x DSP on-chip EMIF control registers in accordance with table 2-3 prior uploading data/code to the corresponding external DSP memory areas.

</div>

For more details about TMS320C6x DSP on-chip EMIF control registers refer to original documentation for TI TMS320C6x DSP.

Table 2-3a. Recommended settings for TMS320C620x/C6701 DSP on-chip EMIF control registers for *TORNADO-E62xx/E67* DSP controllers.

TMS320C620x/C6701 DSP on-chip EMIF control register	*TORNADO-E62* (200 MHz DSP clock)	*TORNADO-E67* (167 MHz DSP clock)	*TORNADO-E6202* (250 MHz DSP clock)	*TORNADO-E6203* (300 MHz DSP clock)
EMIF Global Control Register (EMIF_GCR)	0x3078 (for –5, –6, -7.5 and -10 speed grades of installed SBSRAM chips) [1] 1/2x SBSRAM clk (1ws) 1/2x SDRAM clk (1ws) CLKOUT1/CLKOUT2 are enabled 0x307c (for –5 speed grade of installed SBSRAM chips) [1] 1x SBSRAM clk (0ws) 1/2x SDRAM clk (1ws) CLKOUT1/CLKOUT2 are enabled	0x3078 (for –5, –6, -7.5 and -10 speed grades of installed SBSRAM chips) [1] 1/2x SBSRAM clk (1ws) 1/2x SDRAM clk (1ws) CLKOUT1/CLKOUT2 are enabled 0x307c (for –5 and –6 speed grades of installed SBSRAM chips) [1] 1x SBSRAM clk (0ws) [1] 1/2x SDRAM clk (1ws) CLKOUT1/CLKOUT2 are enabled	0x3078 CLKOUT2 is enabled as 1/2x SBSRAM/SDRAM clock	0x3078 CLKOUT2 is enabled as 1/2x SBSRAM/SDRAM clock

EMIF CE-0 Space Control Register (EMIF_CE0_SCR) (controls on-board SBSRAM for TORNADO-E62/E67 and on-board SBSRAM and SDRAM bank #1 for TORNADO-E6202/E6203)	0x40 32-bit SBSRAM mode	0x40 32-bit SBSRAM mode	0x40 32-bit SBSRAM mode (in case external memory is configures as SBSRAM) [2)] 0x30 32-bit SDRAM mode (in case external memory is configures as SDRAM) [2)]	0x40 32-bit SBSRAM mode (in case external memory is configures as SBSRAM) [2)] 0x30 32-bit SDRAM mode (in case external memory is configures as SDRAM) [2)]
EMIF CE-1 Space Control Register (EMIF_CE1_SCR) (controls 8-bit EPROM/FLASH)	0x8638d823 32-bit ASYNC mode r/w strobe: 24 clk (120ns) r/w setup: 8 clk (40ns) r/w hold: 3 clk (15ns)	0x8638d823 32-bit ASYNC mode r/w strobe: 24 clk (144ns) r/w setup: 8 clk (48ns) r/w hold: 3 clk (18ns)	0x87b8de23 32-bit ASYNC mode r/w strobe: 30 clk (120ns) r/w setup: 8 clk (32ns) r/w hold: 3 clk (12ns)	0xc93ce423 32-bit ASYNC mode r/w strobe: 36 clk (110ns) r/w setup: 12 clk (40ns) r/w hold: 3 clk (10ns)
EMIF CE-2 Space Control Register (EMIF_CE2_SCR) (controls on-board SDRAM)	0x30 32-bit SDRAM mode	0x30 32-bit SDRAM mode	0x40 32-bit SBSRAM mode (in case external memory is configures as SBSRAM) [2)] 0x30 32-bit SDRAM mode (in case external memory is configures as SDRAM) [2)]	0x40 32-bit SBSRAM mode (in case external memory is configures as SBSRAM) [2)] 0x30 32-bit SDRAM mode (in case external memory is configures as SDRAM) [2)]
EMIF CE-3 Space Control Register (EMIF_CE3_SCR) (controls external I/O control registers, USART and USB controllers, PIOX-16 site, SIOX-A rev.C site)	0x31b3c623 32-bit ASYNC mode r/w strobe: 6 clk (30ns) r/w setup: 3 clk (15ns) r/w hold: 3 clk (15ns)	0x2162c522 32-bit ASYNC mode r/w strobe: 5 clk (30ns) r/w setup: 2 clk (12ns) r/w hold: 2 clk (12ns)	0x31f3c723 32-bit ASYNC mode r/w strobe: 7 clk (28ns) r/w setup: 3 clk (12ns) r/w hold: 3 clk (12ns)	0x4274c923 32-bit ASYNC mode r/w strobe: 9 clk (29ns) r/w setup: 4 clk (13ns) r/w hold: 3 clk (10ns)
EMIF SDRAM Control Register (EMIF_SDRAM_CR)	0x07339000	0x07338000	0x07339000	0x0733a000
EMIF SDRAM Timing Register (EMIF_SDRAM_TMR)	1000	833	1250	1500

Notes: 1.   Number of programmed wait states (either 0ws or 1ws) for on-board SBSRAM bank of
                  TORNADO-E62/E67 DSP controllers depends upon the speed grade of installed SBSRAM chips.
                  Contact MicroLAB Systems for information about the speed grade of installed SBSRAM chips.
            2.   External DSP memory for *TORNADO-E6202/E6203* DSP controllers can be configured by DSP
                  software as either SBSRAM or SDRAM via bit *XMEM* of *SYS_CNF_RG* control register. Refer to
                  the corresponding subsection below for more details.

Table 2-3b. Recommended settings for TMS320C64xx DSP on-chip EMIF control registers for
TORNADO-E64xx DSP controllers.

TMS320C64x DSP on-chip EMIF control register	TORNADO-E64xx (500 MHz DSP clock (T_{EMIF}=8ns) for TMX-grade 'C64xx silicon rev.1)	TORNADO-E64xx (600 MHz DSP clock (T_{EMIF}=6.6ns) for TMS-grade 'C64xx silicon)
EMIF-A interface control registers		
EMIF-A Global Control Register (EMIFA_GCR)	0x0009277C	0x0009277C
EMIF-A CE-0 Space Control Register (EMIFA_CE0_SCR) (controls on-board SBSRAM)	0x000000e0 64-bit SBSRAM mode	0x000000e0 64-bit SBSRAM mode
EMIF-A CE-0 Space Secondary Control Register (EMIFA_CE0_SEC)	0x00000002	0x00000002
EMIF-A CE-1 Space Control Register (EMIFA_CE1_SCR) (unused, leave as default)	0xffffff03 default 8-bit ASYNC mode	0xffffff03 default 8-bit ASYNC mode
EMIF-A CE-2 Space Control Register (EMIFA_CE2_SCR) (controls on-board SDRAM)	0x000000d0 64-bit SDRAM mode	0x000000d0 64-bit SDRAM mode
EMIF-A CE-2 Space Secondary Control Register (EMIFA_CE2_SEC)	0x00000002	0x00000002
EMIF-A CE-3 Space Control Register (EMIFA_CE3_SCR) (unused, leave as default)	0xffffff03 default 8-bit ASYNC mode	0xffffff03 default 8-bit ASYNC mode
EMIF-A SDRAM Control Register (EMIFA_SDRAM_CR)	0x57117000 (if on-board SDRAM is 4Mx64) 0x63117000 (if on-board SDRAM is 16Mx64)	0x57228000 (if on-board SDRAM is 4Mx64) 0x63228000 (if on-board SDRAM is 16Mx64)
EMIF-A SDRAM Timing Register (EMIFA_SDRAM_TMR)	1952 (if on-board SDRAM is 4Mx64) 976 (if on-board SDRAM is 16Mx64)	2344 (if on-board SDRAM is 4Mx64) 1172 (if on-board SDRAM is 16Mx64)

EMIF-A SDRAM Extension Register *(EMIFA_SDRAM_EXT)*	0x00014D29	0x00014D29
EMIF-B interface control registers		
EMIF-B Global Control Register *(EMIFB_GCR)*	0x0009277C	0x0009277C
EMIF-B CE-0 Space Control Register *(EMIFB_CE0_SCR)* *(controls external I/O control registers, USART,* *USB and RTC controllers, PIOX-16 site, SIOX-A* *rev.C site)*	0x21124411 16-bit ASYNC mode r/w strobe: 4 clk (32ns) r/w setup: 2 clk (16ns) r/w hold: 1 clk (8ns)	0x21524511 16-bit ASYNC mode r/w strobe: 5 clk (33ns) r/w setup: 2 clk (13ns) r/w hold: 1 clk (6ns)
EMIF-B CE-1 Space Control Register *(EMIFB_CE1_SCR)* *(area controls 8-bit EPROM/FLASH)*	0x23524d11 16-bit ASYNC mode r/w strobe:13 clk (104ns) r/w setup: 2 clk (16ns) r/w hold: 1 clk (8ns)	0x24125011 16-bit ASYNC mode r/w strobe:16 clk (105ns) r/w setup: 2 clk (13ns) r/w hold: 1 clk (6ns)
EMIF-B CE-3 Space Control Register *(EMIFB_CE3_SCR)* *(unused, leave as default)*	0xffffff03 default 8-bit ASYNC mode	0xffffff03 default 8-bit ASYNC mode
EMIF-B CE-3 Space Control Register *(EMIFB_CE3_SCR)* *(unused, leave as default)*	0xffffff03 default 8-bit ASYNC mode	0xffffff03 default 8-bit ASYNC mode

Notes: 1.   EMIF-A and EMIF-B interfaces of TMS320C64xx DSP are assumed to run at DSPCLK/4 via corresponding ECLKOUT1 EMIF clock.

SBSRAM and SDRAM memory areas

TORNADO-E6x DSP controllers provide on-board SBSRAM bank for external DSP program/data, which can accommodate 128K/512K/1Mx32 SBSRAM (*TORNADO-E62xx/E67*) or 128K/256K/512K/1Mx64 SBSRAM (*TORNADO-E64xx*). *TORNADO-E62xx/E67* on-board SBSRAM bank is allocated to EMIF CE-0 space of on-board TMS320C620x/C6701 DSP, whereas *TORNADO-E64xx* on0board SBSRAM bank is allocated to EMIF-A CE-0 space of on-board TMS320C64xx DSP.

CAUTION

SBSRAM bank of *TORNADO-E62xx/E67* DSP controllers is allocated to 0x00000000 DSP base address. SBSRAM bank of *TORNADO-E62xx/E67* DSP controllers can't be removed, since TMS320C620x/C6701 DSP starts program execution from 0x00000000 DSP address.

CAUTION

SBSRAM bank of *TORNADO-E64xx* DSP controllers is allocated to 0x80000000 DSP base
address, and therefore is optional for *TORNADO-E64xx* DSP controllers.

TORNADO-E62/E67 DSP controllers provide optional on-board SDRAM bank for external DSP
program/data, which can accommodate 0M/4Mx32 SDRAM capacity and is allocated to EMIF CE-2 space of
on-board TMS320C620x/C6701 DSP.

TORNADO-E6202/E6203 DSP controllers provide two optional on-board SDRAM banks for external DSP
program/data. Each SDRAM bank can accommodate 0M/4Mx32 SDRAM capacity. Default primary SDRAM
bank of *TORNADO-E6202/E6203* DSP controllers is allocated into EMIF CE-2 space of on-board
TMS320C6202/C6203 DSP, whereas secondary SDRAM bank (SDRAM bank #1) and on-board SBSRAM
bank both share common EMIF CE-0 space of on-board TMS320C6202/C6203 DSP.

TORNADO-E64xx DSP controllers provide optional on-board SDRAM bank for external DSP program/data,
which can accommodate 0M/4M/16Mx64 SDRAM capacity and is allocated to EMIF-A CE-2 space of on-board
TMS320C64xx DSP.

CAUTION

TORNADO-E62/E67/E64xx DSP controllers support on-board SBSRAM and SDRAM
simultaneously, i.e. on-board TMS320C6201/TMS320C6701/C64xx DSP can access both
SBSRAM and SDRAM without any EMIF reconfiguration.

TORNADO-E6202/E6203 DSP controllers do not support on-board SBSRAM and SDRAM
simultaneously. On-board TMS320C6202/TMS320C6203 DSP can be configured by DSP
software to access either external SBSRAM or external SDRAM by means of appropriate
configuration of EMIF control registers (table 2-3) and selection of external memory type via
bit *XMEM* of *SYS_CNF_RG* control register (refer to the corresponding subsection below).

CAUTION

TORNADO-E62/E67 on-board SBSRAM bank can be configured by on-board DSP software to run either with 0ws or 1ws depending upon the particular SBSRAM memory chips installed. Number of wait states for accessing on-board SBSRAM can be programmed via *SSCRT* bit of TMS320C6x DSP on-chip EMIF global control register (*EMIF_GCR*) in accordance with table 2-3.

TORNADO-E6202/E6203 on-board SBSRAM bank always run at ½x DSP clock rate and provides 1ws when accessed by on-board DSP.

CAUTION

TORNADO-E62xx/E67 on-board SDRAM bank(s) always run at ½x DSP clock rate and provide(s) 1ws when accessed by on-board DSP.

CAUTION

TORNADO-E64xx on-board SBSRAM and SDRAM banks run at ¼x DSP clock rate and provide 4ws when accessed by on-board DSP.

FLASH/EPROM Area

On-board FLASH/EPROM of *TORNADO-E6x* is allocated into EMIF CE-1 space of TMS320C620x/C6701 DSP for *TORNADO-E62xx/E67* DSP controllers and to into EMIF-B CE-1 space of TMS320C64xx DSP for *TORNADO-E64xx* DSP controllers. FLASH/EPROM bank is designed to store DSP application boot code and/or nonvolatile data.

CAUTION

TORNADO-E6x DSP controllers have been designed to install either 5v-only 128K/512Kx8
FLASH memory chips or 128K..1Mx8 EPROM memory chips in PLCC-32 IC package and
less than 100ns access time into dedicated on-board S1 socket (fig.2-2 and A-1).

Recommended 5v-only FLASH memory chips are available from AMD and other vendors.
Contact MicroLAB Systems for a complete list of compatible FLASH/EPROM memory chip
vendors.

Installation of other FLASH/EPROM memory chips than that specified in table 2-4 may result
in damage of FLASH/EPROM chip and/or of *TORNADO-E6x* hardware.

TORNADO-E6x DSP controllers do not provide on-board facility for programming 8-bit EPROM chips,
whereas 8-bit 5v-only FLASH memory chips can be programmed directly by on-board DSP. The EPROM chip,
however, can be programmed in the external programmer only, and can be used for read-only bootload and data
read purpose in *TORNADO-E6x* DSP controllers.

CAUTION

FLASH programming utilities for AMD 8-bit 5v-only FLASH memory chips for user
TMS320C6x DSP applications are provided with *TORNADO-E6x* DSP controllers.

In case customer is using 8-bit 5v-only FLASH memory chip from the manufacturer other than
the AMD Inc, then he has to follow manufacturer documentation in order to design FLASH
programming utilities.

TORNADO-E62/E67 on-board J3 jumper set and *TORNADO-E6202/E6203/E64xx* on-board SW3 switch
are used to select FLASH/EPROM chip type and to set write protect feature for FLASH memory chip in
accordance with table 2-4.

Table 2-4. FLASH/EPROM chip type selector for *TORNADO-E62/E67*.

FLASH/EPROM chip type in PLCC-32 IC package	J3 jumper set configuration (*TORNADO-E62/E67*) or SW3 switch configuration (*TORNADO-E6202/E6203/E64xx*)					
	J2-1 SW3-1	**J2-2 SW3-2**	**J2-3 SW3-3**	**J2-4 SW3-4**	**J2-5 SW3-5**	**J2-6 SW3-6**
AMD Am29F010 128Kx8 FLASH *AMD Am29F040 512Kx8 FLASH* *with WRITE ENABLE*	OFF	ON	OFF	ON	OFF	OFF
AMD Am29F010 128Kx8 FLASH *AMD Am29F040 512Kx8 FLASH* *with WRITE DISABLE*	OFF	ON	OFF	OFF	ON	OFF
Generic 27C010 128Kx8 EPROM *generic 27C020 256Kx8 EPROM*	OFF	OFF	ON	OFF	ON	OFF
Generic 27C040 512Kx8 EPROM	OFF	OFF	ON	OFF	OFF	ON
Generic 27C080 1Mx8 EPROM	ON	OFF	OFF	OFF	OFF	ON

Notes:.   1. The highlighted configuration corresponds to the factory setting.
2. The recommended access time for the FLASH/EPROM chip is 100ns or less.

CAUTION

TORNADO-E62xx/E67 on-board TMS320C620x/C6701 DSP allocates 8-bit
FLASH/EPROM data words at 32-bit data word boundaries (at x4 DSP base addresses).

TORNADO-E64xx on-board TMS320C64xx DSP allocates 8-bit FLASH/EPROM data
words at 16-bit data word boundaries (at x2 DSP base addresses).

FLASH memory bank provides FLASH memory write protection by means of J3-4 (SW3-4) and J3-5 (SW3-5)
jumpers/switches in order to exclude unauthorized FLASH memory data update.

CAUTION

If J3-5 jumper is removed (SW3-5 switch is set to OFF) and J3-4 jumper is installed (SW3-4
switch is set to ON) while the FLASH memory chip is installed, then the FLASH memory can
be programmed by DSP software.

If J3-5 jumper is installed (SW3-5 switch is set to ON) and J3-4 jumper is removed (SW3-4
switch is set to OFF) while the FLASH memory chip is installed, then write to FLASH
memory is disabled.

I/O peripherals and control registers areas

TMS320C6x DSP environment of *TORNADO-E6x* features asynchronous I/O area, which is allocated into
EMIF CE-3 space of TMS320C620x/C6701 DSP for *TORNADO-E62xx/E67* DSP controllers and into EMIF-
B CE-0 space of TMS320C64xx DSP for *TORNADO-E64xx* DSP controllers, and includes the following on-
board I/O peripherals and I/O control registers (refer to table 2-2):

- *dual-channel USART*, which is used for communication with external computers/peripherals using
  industry-standard serial protocols
- *USB controller*, which is used for communication with external host computer using industry-standard
  USB rev.1.1 protocol
- *RTC controller*, which provides battery backed-up real-time clock, 2100 year calendar, programmable
  alarm and programmable watch-dog timer (*TORNADO-E64xx* only)
- *WDT_CLR_RG* (WDT clear) write-only register and *WDT_EN_RG* (WDT enable) register, which
  are used to control on-board WDT and RTC controller on-chip WDT, and to enable access to RTC
  controller
- *DSP_EXT_INT6_SEL_RG* (DSP external INT6 selector) and *DSP_EXT_INT7_SEL_RG* (DSP
  external INT7 selector) registers, which are used to select interrupt sources for EXT_INT6 and
  EXT_INT7 external interrupt inputs of on-board TMS320C6x DSP
- *DSP_EXT_INT4_SEL_RG* (DSP external INT4 selector), and *DSP_EXT_INT5_SEL_RG* (DSP
  external INT5 selector), and *DSP_NMI_SEL_RG* (DSP NMI selector) registers, which are used to

select interrupt sources for EXT_INT4, EXT_INT5, and NMI external interrupt inputs of on-board TMS320C6202/C6203/C64xx DSP (*TORNADO-E6202/E6203/E64xx* only)

- *DEV_ID_RG* (device ID) and *BMODE_RG* (DSP bootmode) read-only registers, which are used to read device ID and DSP bootmode in TMS320C6202/C6203/C64xx DSP applications (*TORNADO-E6202/E6203/E64xx* only)
- *DEV_REV_ID_RG* (device hardware revision ID) read-only register, which are used to read device revision ID in TMS320C64xx DSP applications (*TORNADO-E64xx* only)
- *SYS_CNF_RG* register, which is used to select external synchronous SBSRAM/SDRAM memory type of *TORNADO-E6202/E6203* DSP controllers and to read external DSP interface type (McBSP-1 or UTOPIA interface) of *TORNADO-E64xx* DSP controllers
- *PXSX_RESET_RG* (PIOX/SIOX reset control) register, which is used control reset signals for on-board SIOX and PIOX-16 DCM sites
- *SIOX rev.C* parallel I/O interface area for compatible DCM
- *PIOX-16* parallel I/O interface area for compatible DCM.

CAUTION

TORNADO-E62xx/E67 on-board external I/O control registers (refer to table 2-2 and to the corresponding subsections below) are allocated to D0..D3 bits of TMS320C620x/C6701 DSP 32-bit data words of DSP EMIF CE-0 area with bits D4..D31 being ignored during write cycles and being undefined during read cycle.

TORNADO-E64xx on-board external I/O control registers (refer to table 2-2 and to the corresponding subsections below) are allocated to D0..D3 bits of TMS320C64xx DSP 16-bit data words of DSP EMIF-B CE-0 area with bits D4..D15 being ignored during write cycles and being undefined during read cycle.

Dual-channel USART

TORNADO-E6x features the on-board dual-channel USART (universal synchronous/asynchronous receiver/transmitter) for communication with host computers, terminals, network adapters, or external peripherals using industry standard serial communication protocols.

USART is based around the SIEMENS SAB 82532 chip and supports popular synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) at up to 10 Mbit/s data transfer rate and industry-standard asynchronous protocol at up to 2.5 Mbaud independent for each channel. USART can generate interrupt to on-board DSP.

Each USART channel connects to external communication equipment via either RS232C or RS422/EIA-530 electrical interface. Selection of particular interface is performed by the on-board jumper sets J3 and J4 for *TORNADO-E62/E67* DSP controllers and on-board SW4 switch for *TORNADO-E6202/E6203/E64xx* DSP controllers.

For more details about USART and external RS232C/RS422 interfaces for USART refer to the corresponding section later in this chapter.

USB interface

TORNADO-E6x DSP controllers provide on-board USB device controller with external USB type 'B' interface connector for communication with external host computers via the industry standard 12 Mbit/s USB protocol.

USB device controller is based around the Lucent Technologies USS-820/USS-825 chip and meets USB rev.1.1 specifications. USB device controller can generate interrupt to on-board DSP. For more details about USB controller and interface refer to the corresponding section later in this chapter.

Real-time clock controller (RTC) of TORNADO-E64xx

TORNADO-E64xx DSP controllers provide on-board real-time clock (RTC) controller, which feature battery back-up real-time clock, 2100 year calendar, programmable alarm and programmable watch-dog timer.

USB device controller is based around the Dallas Semiconductor Inc DS1284 chip. RTC controller can generate two interrupts (INTA and INTB) to on-board DSP: one for programmable watch-dog timer output and one for programmable alarm. For more details about RTC controller refer to the corresponding section later in this chapter.

General purpose digital I/O

All *TORNADO-E6x* DSP controllers provide general purpose 8-bit digital I/O, which can be used as external control I/O signals. These digital I/O signals are the part of on-board USART, and allow generation of DSP interrupt on individually programmable high-to-low or low-to-high transitions when programmed as input pins.

TORNADO-E64xx DSP controllers also provide optional general purpose 10-bit digital I/O, which is controlled directly by TMS320C64xx DSP on-chip GPIO control registers.

For more details about general purpose I/O and TMS320C64xx DSP on-chip general purpose I/O refer to the corresponding section later in this chapter.

Watchdog Timer (WDT) control

TORNADO-E6x provides on-board watchdog timer (WDT) feature, which generates output pulse in case WDT has not been reset by DSP software within the latency period (typically 1.6 sec) since the last WDT reset event. *TORNADO-E6x* DSP software can configure on-board hardware to enable generation of reset signal for on-board DSP and peripherals on the WDT expiration condition in order to increase reliability in embedded environment and to automatically restart on-board DSP and peripherals in case of the DSP idling or DSP software crash.

WDT_EN_RG I/O control register is used to enable DSP reset on the WDT expiration event(s) and to identify between *TORNADO-E62/E67* and *TORNADO-E6202/E6203* DSP controllers.

WDT_EN_RG I/O control register (r/w)

X	0 (r) (TORNADO-E62xx/E67) RTC_WDT_EN (r/w, 0+) (TORNADO-E64xx)	0 (r) (TORNADO-E62xx/E67) RTC_ACCESS_EN (r/w; 0+) (TORNADO-E64xx)	0 (r) (TORNADO-E62/E67) 1 (r) (TORNADO-E6202/E6203/E64xx)	WDT_EN (r/w, 0+)
bit-31...bit-4 (*TORNADO-E62xx/E67*) bit-15...bit-4 (*TORNADO-E64xx*)	bit-3	bit-2	bit-1	bit-0

Table 2-5.   WDT_EN_RG I/O control register.

register bit(s)	access mode	value at DSP reset	Description
WDT_EN	r/w	0	Enable control for generation of reset signal for on-board DSP and peripherals on WDT expiration event. *WDT_EN* =0 corresponds to the WDT disabled, i.e. reset signal for on-board DSP and peripherals can't be generated on WDT expiration event. This is default setting on power on and DSP reset conditions. *WDT_EN* =1 corresponds to the WDT enabled, i.e. reset signal for on-board DSP and peripherals will be generated on WDT expiration event. DSP software must periodically (with the period below 0.8 sec) reset WDT by means of writing to the *WDT_RESET_RG* I/O control register (written data is ignored) in order to exclude automatic generation of reset signal for on-board DSP and peripherals.
RTC_ACCESS_EN (*TORNADO-E64xx* only)	r/w	0	Enable control for access to on-board RTC (real-time clock) controller (*TORNADO-E64xx* only). Software enabled control for RTC controller access provides RTC data integrity and exclude accidental RTC accesses when DSP executes invalid code. *RTC_ACCESS_EN* =0 corresponds to disabled RTC accesses, i.e. all accesses to RTC controller on-chip registers will be ignored and no RTC data will be read or written. This is default setting on power on and DSP reset conditions. *RTC_WDT_EN* =1 corresponds to enabled RTC accesses, i.e. accesses to RTC controller area (refer to table 2-2) will result in access to the RTC controller on-chip registers.

RTC_WDT_EN (TORNADO-E64xx only)	r/w	0	Enable control for generation of reset signal for on-board DSP and peripherals on RTC-WDT (programmable real-time clock WDT) expiration event (*TORNADO-E64xx* only). *RTC_WDT_EN* =0 corresponds to the RTC-WDT disabled, i.e. reset signal for on-board DSP and peripherals can't be generated on RTC-WDT expiration event. This is default setting on power on and DSP reset conditions. *RTC_WDT_EN* =1 corresponds to the RTC-WDT enabled, i.e. reset signal for on-board DSP and peripherals will be generated on RTC-WDT expiration event. DSP software must periodically (with the period below the programmed RTC-WDT period) reset RTC-WDT by means of read/write from/to the RTC registers at 0x0C or 0x0D RTC address in order to exclude automatic generation of reset signal for on-board DSP and peripherals.

Notes: 1. Access modes: r/w – read/write; r – read-only; w – write only.

In case *WDT_EN* bit and/or *RTC_WDT_EN* bit of *WDT_EN_RG* register is set to the '0' state (this state is set as default on the DSP reset condition), then the DSP reset on the WDT and/or RTC-WDT expiration event is disabled, and WDT and/or RTC-WDT output is ignored by on-board reset controller.

In case *WDT_EN* bit and/or *RTC_WDT_EN* bit of *WDT_EN_RG* register flag is set to the '1' state, then the DSP reset on the WDT and/or RTC-WDT expiration event is enabled and the WDT and/or RTC-WDT output will generate the DSP reset signal on WDT and/or RTC-WDT expiration event.

CAUTION

Once WDT is enabled via the *WDT_EN_RG* I/O control register, then the DSP software must periodically reset WDT by means of writing to the *WDT_RESET_RG* I/O control register (refer to table 2-2). Data written to the *WDT_RESET_RG* I/O control register is ignored.

The time period between sequential WDT resets must not exceed 0.8 sec, otherwise the WDT will generate output pulse, which will generate on-board reset signal.

WDT_RESET_RG   I/O control register (w)

x	X	X	x	x
bit-31...bit-4 (*TORNADO-E62xx/E67*) bit-15...bit-4 (*TORNADO-E64xx*)	Bit-3	bit-2	bit-1	bit-0

> **CAUTION**
>
> Once RTC-WDT is enabled via the *RTC_WDT_EN_RG* I/O control register, then the DSP software must periodically reset RTC-WDT by means of read/write from/to the RTC registers at 0x0C or 0x0D RTC address (refer to table 2-2 and to the original RTC datasheet for more details).
>
> The time period between sequential RTC-WDT resets must not exceed programmed RTC-WDT period, otherwise the RTC-WDT will generate output pulse, which will generate on-board reset signal.

RTC_ACCESS_EN bit (D2) of *WDT_EN_RG* register of *TORNADO-E64xx* DSP controllers is used to enable/disable access to on-board RTC controller from DSP application in order to exclude accidental RTC accesses and to increase RTC data integrity. For example, accidental RTC accesses can occur either when DSP boots in *NO-BMODE* and there is no valid DSP code in DSP memory, or in case of DSP malfunction, which can set DSP program counter to invalid area. *RTC_ACCESS_EN* bit defaults to the '0' state on DSP power on and disables access to RTC controller until *RTC_ACCESS_EN* bit will be set to the '1' state by DSP application.

Read-only bit D1 of *WDT_EN_RG* I/O control register of *TORNADO-E62xx/E67* DSP controllers must be used to identify between *TORNADO-E62/E67* and *TORNADO-E6202/E6203* DSP controllers. For more details refer to the corresponding subsection below.

Reset control for SIOX rev.B/C, MXSIOX and PIOX-16 DCM sites

TORNADO-E6x DSP controllers support generation of individual reset signals for on-board SIOX rev.B/C, MXSIOX and PIOX-16 expansion interface sites. This allows correct initialization of installed DCM hardware and synchronization with the DSP software.

Individual reset signals for on-board SIOX rev.B/C, MXSIOX and PIOX-16 DCM sites are controlled via *PXSX_RESET_RG* IOX control register (refer to table 2-2 for addressing details).

PXSX_RESET_RG I/O control register (r/w)

X	0 (r)	SX-B_RESET (r/w, 0+) (TORNADO-E6202/E6203/E64xx) 0 (r) (TORNADO-E62/E67)	SX-A_RESET (r/w, 0+)	PX_RESET (r/w, 0+)
bit-31...bit-4 (*TORNADO-E62xx/E67*) bit-15...bit-4 (*TORNADO-E64xx*)	bit-3	bit-2	bit-1	bit-0

Table 2-6. PXSX_RESET_RG I/O control register.

register bit(s)	access mode	Value at DSP reset	Description
PX_RESET	r/w	0	Controls reset signal for on-board PIOX-16 DCM site. For more details about on-board PIOX-16 DCM site refer to the corresponding section later in this chapter. *PX_RESET* =0 corresponds to active reset signal for PIOX-16 DCM site. This is default setting on power on and DSP reset conditions. *PX_RESET* =1 corresponds to released reset signal for PIOX-16 DCM site.
SX-A_RESET	r/w	0	Controls reset signal for on-board SIOX rev.B and SIOX rev.C I/O DCM sites. Both SIOX rev.B and SIOX rev.C on-board DCM sites share common reset signal. For more details about on-board SIOX DCM sites refer to the corresponding section later in this chapter. *SX-A_RESET* =0 corresponds to active reset signal for both SIOX rev.B and SIOX rev.C DCM sites. This is default setting on power on and DSP reset conditions. *SX-A_RESET* =1 corresponds to released reset signal for both SIOX rev.B and SIOX rev.C DCM sites.
SX-B_RESET	r/w	0	Controls reset signal for on-board MXSIOX connector for connection to external *T/SU-X1* SIOX rev.B mini-extender kit. This bit is valid for *TORNADO-E6202/E6203/E64xx* DSP controllers only with three DSP on-chip McBSP serial ports and does not present for *TORNADO-E62/E67* DSP controllers. For more details about MXSIOX connector and *T/SU-X1* SIOX rev.B mini-extender kit refer to the corresponding section later in this chapter and to Appendix B. *SX-B_RESET* =0 corresponds to active reset signal for on-board MXSIOX connector for connection to external *T/SU-X1* SIOX rev.B mini-extender kit. This is default setting on power on and DSP reset conditions. *SX-A_RESET* =1 corresponds to released reset signal for on-board MXSIOX connector for connection to external *T/SU-X1* SIOX rev.B mini-extender kit.

Notes: 1. Access modes: r/w – read/write; r – read-only; w – write only.

TMS320C6x DSP external interrupt requests

TORNADO-E6x DSP controllers provide multiple on-board interrupt request sources and software configurable TMS320C6x DSP external interrupt request inputs. The number of on-board interrupt request sources and the number of software configurable TMS320C6x DSP external interrupt request inputs is different for different *TORNADO-E6x* DSP controllers (refer to table 2-7).

Table 2-7. TMS320C6x DSP external interrupt request inputs configurations for *TORNADO-E6x*.

TORNADO-E6x DSP controller	on-board interrupt request sources	TMS320C6x DSP external interrupt request inputs				
		NMI	EXT_INT4	EXT_INT5	EXT_INT6	EXT_INT7
TORNADO-E62 *TORNADO-E67*	*IRQ-0..2* interrupt requests from PIOX-16, SIOX rev.B and SIOX rev.C DCM sites. *USART_IRQ* interrupt request from USART. *USB_IRQ* interrupt request from USB controller.	Not used.	On-board wired to *IRQ-0* interrupt request from PIOX-16, SIOX rev.B and SIOX rev.C DCM sites.	On-board wired to *IRQ-1* interrupt request from PIOX-16 and SIOX rev.B DCM sites.	Software configurable via 2-bit *DSP_EXT_INT6_SEL_RG* and *DSP_EXT_INT7_SEL_RG* I/O control registers correspondingly to select from *IRQ-2* interrupt request of PIOX-16 and SIOX rev.B DCM sites, and output interrupt requests from on-board USART and USB controller.	
TORNADO-E6202 *TORNADO-E6203* *TORNADO-E64xx*	*SX_IRQ-0..2* interrupt requests from SIOX rev.B, SIOX rev.C DCM sites and MXSIOX connector. *PX_IRQ-0..3* interrupt requests from PIOX-16 DCM site. *USART_IRQ* interrupt request from USART. *USB_IRQ* interrupt requests from USB controller. *WDT_IRQ* interrupt requests on WDT expiration event *RTC_WDT_IRQ* interrupt requests on RTC WDT expiration event (*TORNADO-E64xx* only). *RTC_ALARM_IRQ* interrupt requests on RTC alarm (*TORNADO-E64xx* only).	Software configurable via 4-bit *DSP_NMI_SEL_RG*, *DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG* and *DSP_EXT_INT7_SEL_RG* I/O control registers correspondingly to select from any of available on-board interrupt request source.				

CAUTION

TORNADO-E62/E67 DSP controllers are designed for *EXT_INT4*...*EXT_INT7* external
interrupt request inputs of TMS320C6x DSP with inverse polarity (active low).

The TMS320C6x DSP on-chip *External Interrupt Polarity Register* (0x019C0008 address in
DSP memory map) must be set to 0x0000000F value for *TORNADO-E62/E67* DSP
controllers in order to support external interrupts requests with inverse polarity.

CAUTION

TORNADO-E6202/E6203/E64xx DSP controllers are designed for *NMI* and
EXT_INT4...*EXT_INT7* external interrupt request inputs of TMS320C6x DSP with positive
polarity (active high).

The TMS320C6x DSP on-chip *External Interrupt Polarity Register* (0x019C0008 address in
DSP memory map) must be set to 0x00000000 value for *TORNADO-E6202/E6203/E64xx*
DSP controllers in order to support external interrupts requests with positive polarity.

CAUTION

Time duration of any active interrupt request signal must be larger than two clock periods of
TORNADO-E6x on-board DSP.

For more information about TMS320C6x interrupts refer to original TI datasheets and user's
guides for TMS320C6x DSP, which are supplied in either paper or electronic form together
with this manual.

CAUTION

TORNADO-E6x on-board USART (Infineon SAB82532) and USB controller (Agere
Systems USS-820/825) chips shall be configured by DSP software to generate active low
output interrupt requests.

> **CAUTION**
>
> *TORNADO-E64xx* on-board RTC (Dallas Semiconductor DS1284) controller chip must be configured by DSP software via RTC on-chip *COMMAND REGISTER* (#B) to generate active low continuous interrupt requests via INTA and INTB interrupt request outputs, and INTA and INTB interrupt request outputs shall be mapped to RTC-WDT and RTC-ALARM output flags correspondingly.

TORNADO-E6x on-board interrupt request source selectors for NMI, EXT_INT4, EXT_INT5, EXT_INT6 and EXT_INT7 external interrupt requests on on-board TMS320C6x DSP can be configured via *DSP_NMI_SEL_RG* (*TORNADO-E6202/E6203/E64xx* only), *DSP_EXT_INT4_SEL_RG* (*TORNADO-E6202/E6203/E64xx* only), *DSP_EXT_INT5_SEL_RG* (*TORNADO-E6202/E6203/E64xx* only), *DSP_EXT_INT6_SEL_RG* and *DSP_EXT_INT7_SEL_RG* I/O control registers correspondingly (refer to table 2-2 for addressing details).

DSP_NMI_SEL_RG I/O control register (r/w)
*(**TORNADO-E6202/E6203/E64xx** only)*

X	NMI_SEL-3 (r/w, 1+)	NMI_SEL-2 (r/w, 1+)	NMI_SEL-1 (r/w, 1+)	NMI_SEL-0 (r/w, 1+)
bit-31...bit-4 (*TORNADO-E62xx/E67*) bit-15...bit-4 (*TORNADO-E64xx*)	bit-3	bit-2	bit-1	bit-0

Default setting for *DSP_NMI_SEL_RG* I/O control register of *TORNADO-E6202/E6203/E64xx* DSP controllers, which is set on the power-on and DSP reset conditions, corresponds to disabled NMI interrupt request input of on-board TMS320C6x DSP.

DSP_EXT_INT4_SEL_RG I/O control register (r/w)
*(**TORNADO-E6202/E6203/E64xx** only)*

X	EXT_INT4_SEL-3 (r/w, 0+)	EXT_INT4_SEL-2 (r/w, 1+)	EXT_INT4_SEL-1 (r/w, 0+)	EXT_INT4_SEL-0 (r/w, 0+)
bit-31...bit-4 (*TORNADO-E62xx/E67*) bit-15...bit-4 (*TORNADO-E64xx*)	bit-3	bit-2	bit-1	bit-0

Default setting for *DSP_EXT_INT4_SEL_RG* I/O control register of *TORNADO-E6202/E6203/E64xx* DSP controllers, which is set on the power-on and DSP reset conditions, corresponds to the SX_IRQ-0 interrupt request from SIOX rev.B and SIOX rev.C DCM sites routed to the EXT_INT4 interrupt request input of on-board TMS320C6x DSP. This provides default compatibility with *TORNADO-E62/E67* DSP controllers.

DSP_EXT_INT5_SEL_RG I/O control register (r/w)
(*TORNADO-E6202/E6203/E64xx* only)

X	EXT_INT5_SEL-3 (r/w, 0+)	EXT_INT5_SEL-2 (r/w, 1+)	EXT_INT5_SEL-1 (r/w, 0+)	EXT_INT5_SEL-0 (r/w, 1+)
bit-31...bit-4 (*TORNADO-E62xx/E67*) bit-15...bit-4 (*TORNADO-E64xx*)	bit-3	bit-2	bit-1	bit-0

Default setting for *DSP_EXT_INT5_SEL_RG* I/O control register of *TORNADO-E6202/E6203/E64xx* DSP controllers, which is set on the power-on and DSP reset conditions, corresponds to the SX_IRQ-1 interrupt request from SIOX rev.B and MXSIOX DCM sites routed to the EXT_INT5 interrupt request input of on-board TMS320C6x DSP. This provides default compatibility with *TORNADO-E62/E67* DSP controllers.

DSP_EXT_INT6_SEL_RG I/O control register (r/w)

X	0 (r) (*TORNADO-E62/E67*) EXT_INT6_SEL-3 (r/w, 0+) (*TORNADO-E6202/E6203/E64xx*)	0 (r) (*TORNADO-E62/E67*) EXT_INT6_SEL-2 (r/w, 1+) (*TORNADO-E6202/E6203/E64xx*)	EXT_INT6_SEL-1 (r/w, 0+)	EXT_INT6_SEL-0 (r/w, 0+)
bit-31...bit-4 (*TORNADO-E62xx/E67*) bit-15...bit-4 (*TORNADO-E64xx*)	bit-3	bit-2	bit-1	bit-0

Default setting for *DSP_EXT_INT6_SEL_RG* I/O control register of *TORNADO-E62/E67* DSP controllers, which is set on the power-on and DSP reset conditions, corresponds to the IRQ-2 interrupt request from SIOX rev.B and PIOX-16 DCM sites routed to the EXT_INT6 interrupt request input of on-board TMS320C6x DSP. Default setting for *DSP_EXT_INT6_SEL_RG* I/O control register of *TORNADO-E6202/E6203/E64xx* DSP controllers, which is set on the power-on and DSP reset conditions, corresponds to the SX_IRQ-2 interrupt request from SIOX rev.B and MXSIOX DCM sites routed to the EXT_INT6 interrupt request input of on-board TMS320C6x DSP.

DSP_EXT_INT7_SEL_RG I/O control register (r/w)

X	0 (r) (*TORNADO-E62/E67*) EXT_INT7_SEL-3 (r/w, 0+) (*TORNADO-E6202/E6203/E64xx*)	0 (r) (*TORNADO-E62/E67*) EXT_INT7_SEL-2 (r/w, 0+) (*TORNADO-E6202/E6203/E64xx*)	EXT_INT7_SEL-1 (r/w, 1+)	EXT_INT7_SEL-0 (r/w, 0+)
bit-31...bit-4 (*TORNADO-E62xx/E67*) bit-15...bit-4 (*TORNADO-E64xx*)	bit-3	Bit-2	bit-1	bit-0

Default setting for *DSP_EXT_INT7_SEL_RG* I/O control register of *TORNADO-E6x* DSP controllers, which is set on the power-on and DSP reset conditions, corresponds to the USART output interrupt request routed to the EXT_INT7 interrupt request input of on-board TMS320C6x DSP.

Available configurations for interrupt request source control registers of *TORNADO-E6x* DSP controllers are presented in table 2-8.

Table 2-8.   DSP_NMI_SEL_RG, DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG and *DSP_EXT_INT7_SEL_RG* I/O control registers.

register bit(s)	access mode	value at DSP reset	Description
{*NMI_SEL-3..0*} (*TORNADO-E6202/E6203*)	r/w	{1,1,1,1}	Select interrupt request source for the corresponding TMS320C6x DSP external interrupt request input.
{*EXT_INT4_SEL-3..0*} (*TORNADO-E6202/E6203*)		{0,1,0,0}	*Common TORNADO-E6x interrupt source configurations:* [0,0,0,0] - *IRQ-2* shared interrupt request from SIOX rev.B DCM site and PIOX-16 DCM site (*TORNADO-E62/E67*), or *SX_IRQ-2* interrupt request from SIOX rev.B DCM site and MXSIOX connector (*TORNADO-E6202/E6203*)
{*EXT_INT5_SEL-3..0*} (*TORNADO-E6202/E6203*)		{0,1,0,1}	[0,0,0,1] - no interrupt request source [0,0,1,0] - *USART_IRQ* USART interrupt request (must be configured as pushed-pulled active low interrupt request output)
{*EXT_INT6_SEL-3..0*}		{0,0,0,0}	[0,0,1,1] - *USB_IRQQ* USB controller interrupt request (must be configured as active low interrupt request output)
{*EXT_INT7_SEL-3..0*}		{0,0,1,0}	*Optional TORNADO-E202/E6203/E64xx only interrupt source configurations:* [0,1,0,0] - *SX_IRQ-0* interrupt request from SIOX rev.B/C DCM sites [0,1,0,1] - *SX_IRQ-1* interrupt request from SIOX rev.B DCM site and MXSIOX connector [1,0,0,0] - *PX_IRQ-0* interrupt request from PIOX-16 DCM site [1,0,0,1] - *PX_IRQ-1* interrupt request from PIOX-16 DCM site [1,0,1,0] - *PX_IRQ-2* interrupt request from PIOX-16 DCM site [1,0,1,1] - *PX_IRQ-3* interrupt request from PIOX-16 DCM site [1,1,0,0] - interrupt on WDT expiration event [1,1,0,1] - interrupt on RTC WDT expiration event (*TORNADO-E64xx* only) [1,1,1,0] - interrupt on RTC alarm (*TORNADO-E64xx* only) [1,1,1,1] - no interrupt request source

Note: 1.   Access modes: r/w – read/write; r – read-only; w – write only.
2.   Not shown configurations are reserved and are not recommended for usage. Setting these configurations will result in missing interrupt source.

Software identification of TORNADO-E6x

TORNADO-E6x DSP controllers product line comprises of a variety of DSP controllers with different DSP performance, DSP on-chip resources and DSP environment configurations. Therefore, software identification of *TORNADO-E6x* DSP controllers is required in order to provide different initialization of DSP EMIF control

registers (refer to table 2-3), different DSP on-chip HPI port control, software support for DSP on-chip floating-point unit, etc.

CAUTION

Generally, due to the code incompatibility between *TORNADO-E62xx/E67* and *TORNADO-E64xx* DSP controllers because of different DSP memory maps for external RAM, peripherals and I/O control registers, software identification of particular DSP controller must be performed inside *TORNADO-E64xx* DSP controllers group and inside *TORNADO-E62xx/E67* DSP controllers group.

Software identification of particular DSP controller within *TORNADO-E62xx/E67* DSP controllers group can be done using the following *TORNADO-E6x* on-board I/O control registers and TMS320C6x DSP on-chip resources in accordance with table 2-9:

- D1 bit of *WDT_EN_RG* I/O control register (refer to the corresponding subsection above)
- *DEV_ID_RG* read-only I/O control register (*TORNADO-E6202/E6203* DSP controllers only), which contains 4-bit device identification code
- *CPU_ID* bit field of TMS320C6x DSP on-chip CSR register (refer to original TI TMS320C6x documentation for more details).

<div align="center">

DEV_ID_RG I/O control register (r)
(TORNADO-E6202/E6203/E64xx only)

</div>

X	DEV_ID_3 (r)	DEV_ID_2 (r)	DEV_ID_1 (r)	DEV_ID_0 (r)
bit-31...bit-4 (*TORNADO-E62xx/E67*) bit-15...bit-4 (*TORNADO-E64xx*)	bit-3	bit-2	bit-1	bit-0

Table 2-9. Software identification of *TORNADO-E62xx/E67* DSP controller.

TORNADO **DSP controller**	**D1 bit of** *WDT_EN_RG* **I/O control register**	**{*DEV_ID_3..DEV_ID_0*} bits of** *DEV_ID_RG* **I/O control register**	*CPU_ID* **bit field (bits 31..24) of TMS320C6x DSP on-chip CSR register**	*REV_ID* **bit field (bits 23..16) of TMS320C6x DSP on-chip CSR register**
TORNADO-E62	0	-	0x00	0x01 0x02
TORNADO-E67	0	-	0x02	0x01 0x02
TORNADO-E6202	1	0x2	0x00	0x02 0x03
TORNADO-E6203	1	0x3	0x00	0x03
TORNADO-E6414	1 (can be ignored)	0x8	0x08	0x0801
TORNADO-E6415	1 (can be ignored)	0x9	0x08	0x0801
TORNADO-E6416	1 (can be ignored)	0xA	0x08	0x0801

Note: 1. *REV_ID* bit field of TMS320C6x DSP on-chip CSR register is optional and can be used to identify revision code of TMS320C6x DSP.

Software identification of *TORNADO-E6x* DSP controller shall begin from analysis of D1 bit of *WDT_EN_RG* I/O control register, which identifies between *TORNADO-E62/E67* and *TORNADO-E6202/E6203* DSP controllers groups. D1 bit of *WDT_EN_RG* register reads as '0' for *TORNADO-E62/E67* DSP controllers and as '1' for *TORNADO-E6202/E6203* DSP controllers. Further identification between *TORNADO-E62* and *TORNADO-E67* DSP controllers can be done by DSP software via *CPU_ID* bit field of TMS320C6x DSP on-chip CSR register, whereas *TORNADO-E6202* and *TORNADO-E6203* DSP controllers can be identified via *DEV_ID_RG* read-only I/O control register, which is available for *TORNADO-E6202/E6203* DSP controllers. If required, user DSP application can also identify optional silicon revision of TMS320C6x DSP via *REV_ID* bit field of DSP on-chip CSR register.

Software identification of particular DSP controller within *TORNADO-E64xx* DSP controllers group can be done using the following *TORNADO-E6x* on-board I/O control registers and TMS320C6x DSP on-chip resources in accordance with table 2-9:

- *DEV_ID_RG* read-only I/O control register, which contains 4-bit device identification code
- *CPU_ID* and *REV_ID* bit fields of TMS320C6x DSP on-chip CSR register (refer to original TI TMS320C6x documentation for more details).

> **CAUTION**
>
> *TORNADO-E6x* on-board TMS320C6x DSP environment does not provide specific hardware resources for identification of the amount of installed SBSRAM and SDRAM.

Firmware revision identification of TORNADO-E64xx

TORNADO-E64xx DSP controllers also allow to identify board firmware revision via DSP software in order to configure DSP software utilities to support different hardware options, which can be added in future board revisions.

Software identification of *TORNADO-E64xx* board firmware revision is performed via *DEV_REV_ID* read-only I/O control register (refer to table 2-2 for addressing details), which provides 4-bit device firmware revision ID code. Device firmware revision ID code must be greater than 0x1 hex value, which corresponds to *TORNADO-E64xx* board rev.1A.

DEV_REV_ID_RG I/O control register (r)
(TORNADO-E64xx only)

X	DEV_REV_ID_3 (r)	DEV_REV_ID_2 (r)	DEV_REV_ID_1 (r)	DEV_REV_ID_0 (r)
bit-15...bit-4 (*TORNADO-E64xx*)	bit-3	bit-2	bit-1	bit-0

BMODE_RG I/O control register for DSP bootmode read-back for TORNADO-E6202/E6203/E64xx

TORNADO-E6202/E6203/E64xx DSP controllers allow to read DSP start-up bootmode code in DSP application software via *BMODE_RG* read-only I/O control register (refer to table 2-2 for addressing details). This allows DSP software to automatically to recognize DSP memory map and to configure DSP environment is required.

BMODE_RG I/O control register (r)
(TORNADO-E6202/E6203/E64xx only)

x	BMODE-3 (r)	BMODE-2 (r)	BMODE-1 (r)	BMODE-0 (r)
bit-31...bit-4 (*TORNADO-E62xx/E67*) bit-15...bit-4 (*TORNADO-E64xx*)	bit-3	bit-2	bit-1	bit-0

> **CAUTION**
>
> *BMODE-0..3* read-only bits of *BMODE_RG* I/O control register of *TORNADO-E6202/E6203* DSP controllers actually contains four least significant bits of TMS320C6x DSP bootmode configuration defined by on-board SW2 switch (refer to table 2-1), which is latched on release of the DSP reset signal, and will not change during DSP is running until new active DSP reset signal will be applied.

CAUTION

Although original TI documentation specifies TMS320C64xx DSP bootmode ID codes within #0..#2 range, *TORNADO-E64xx* DSP controllers convert original TI bootmode ID codes #0, #1 and #2 for TMS320C64xx DSP defined via on-board SW2-1/2 on-board switch to compatible TMS320C62xx/C6701 DSP bootmode ID codes #5, #7 and #13 correspondingly, which are available for read-back via *BMODE_RG* read-only control register.

This delivers compatibility between *TORNADO-E64xx* and *TORNADO-E62xx/E67* DSP controllers and allows to use common TMS320C6x DSP bootmode ID returned via *BMODE_RG* read-only control register for all *TORNADO-E6x* DSP controllers.

BMODE-0..3 read-only bits of *BMODE_RG* I/O control register of *TORNADO-E64xx* DSP controllers are latched on release of the DSP reset signal, and will not change during DSP is running until new active DSP reset signal will be applied.

Table 2-10. BMODE_RG I/O control register for TORNADO-E6202/E6203/E64xx.

register bit(s)	access mode	Description
{BMODE-3..BMODE-0}	r	Returns latched DSP start-up bootmode for *TORNADO-E6202/E6203* as the following (refer to table 2-1 for details about bootmodes configurations): [0,0,0,1] - *TORNADO-E62xx/E67*: DSP MAP0, no boot, SDRAM bank #1 in EMIF CE-0 (*MAP0/SDRAM/NO-BMODE*) [0,0,1,1] - *TORNADO-E62xx/E67*: DSP MAP0, no boot, SBSRAM in EMIF CE-0 (*MAP0/SBSRAM/NO-BMODE*) [0,1,1,0] - *TORNADO-E62xx/E67*: DSP MAP0, boot from HPI, SBSRAM external memory selection (*MAP0/X-SBSRAM/HPI-BMODE*) [0,1,0,1] - *TORNADO-E62xx/E67*: DSP MAP1, no boot, SBSRAM external memory selection (*MAP0/X-SBSRAM/NO-BMODE*); *TORNADO-E64xx*:: no boot (*NO-BMODE*) [0,1,1,1] - *TORNADO-E62xx/E67*: DSP MAP1, boot from HPI, SBSRAM external memory selection (*MAP0/X-SBSRAM/HPI-BMODE*); *TORNADO-E64xx*: boot from HPI (*HPI-BMODE*) [1,0,0,1] - *TORNADO-E62xx/E67*: DSP MAP0, boot from 8-bit FLASH, SDRAM bank #1 in EMIF CE-0 (*MAP0/SDRAM/FLASH8-BMODE*) [1,0,1,1] - *TORNADO-E62xx/E67*: DSP MAP0, boot from 8-bit FLASH, SBSRAM in EMIF CE-0 (*MAP0/SDRAM/FLASH8-BMODE*) [1,1,0,1] - *TORNADO-E62xx/E67*: DSP MAP1, boot from 8-bit FLASH, SBSRAM external memory selection (*MAP0/X-SBSRAM/FLASH8-BMODE*); *TORNADO-E64xx*: boot from 8-bit FLASH (*FLASH8-BMODE*)

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

SYS_CNF_RG system configuration I/O control register of TORNADO-E6202/E6203/E64xx

TORNADO-E6202/E6203/E64xx DSP controllers provide SYS_CNF_RG external I/O control register (refer to table 2-1 for addressing details), which shall be used to select external on-board synchronous memory type (SBSRAM or SDRAM) for *TORNADO-E6202/E6203* DSP controllers and to read-back external DSP communication interface (McBSP-1 or UTOPIA), which has been selected at start-up for *TORNADO-E6415/E6416* DSP controllers.

SYS_CNF_RG I/O control register (r/w)
(TORNADO-E6202/E6203/E64xx only)

X	0	0	0 (r) (TORNADO-E6202/E6203/E6414) MCBSP1_UTOPIA_IF_SEL (r) (TORNADO-E6415/E6416)	XMEM (r/w) (TORNADO-E6202/E6203) 0 (r) (TORNADO-E64xx)
bit-31...bit-4	bit-3	Bit-2	Bit-1	bit-0

Table 2-11. Register bits of *SYS_CNF_RG* I/O control register.

register bits	access mode	value on DSP reset	Description
XMEM *(TORNADO-E6202/E6203 only)*	r/w	1 (*MAP0/SDRAM/NO-BMODE, MAP0/SDRAM/FLASH8-BMODE* DSP bootmode configurations) 0 (all other DSP bootmodes configurations)	Selects external memory type for *TORNADO-E6202/E6203* DSP controllers at TMS320C6202/C6203 DSP EMIF CE-0/CE-2 areas . *XMEM* =0 enables external SBSRAM at TMS320C6202/C6203 DSP EMIF CE-0 area and disables external SDRAM at DSP EMIF CE-0 and CE-2 areas. DSP on-chip EMIF CE-0/CE-2 control registers have to be configured to run with external SBSRAM (table 2-3a). *XMEM* =1 enables external SDRAM at TMS320C6202/C6203 DSP EMIF CE-0/CE-2 areas and disables external SBSRAM at DSP EMIF CE-0 area. DSP on-chip EMIF CE-0/CE-2 control registers have to be configured to run with external SDRAM (table 2-3).
MCBSP1_UTOPIA _IF_SEL *(TORNADO-E64xx only)*	r	0 (*TORNADO-E6414* or SW2-4 is 'ON' to select McBSP-1 serial port I/F for *TORNADO-E6415/E6416*) 1 (SW2-4 is 'OFF' to select UTOPIA I/F for *TORNADO-E6415/E6416*)	Returns TMS320C6415/C6416 DSP external interface type (McBSP-1 serial port or UTOPIA) selected at DSP reset (*TORNADO-E6415/E6416* DSP controllers only) via on-board SW2-4 switch. This bit always reads as '0' for *TORNADO-E6414* controller without UTOPIA interface. *MCBSP1_UTOPIA_IF_SEL* =0 denotes that McBSP-1 serial port interface has been selected via on-board SW2-4 configuration switch (SW2-4 is in the 'ON' position) of *TORNADO-E6415/E6416* DSP controllers. *MCBSP1_UTOPIA_IF_SEL* =1 denotes that 8-bit UTOPIA level 2 slave interface has been selected via on-board SW2-4 configuration switch (SW2-4 is in the 'OFF' position) of *TORNADO-E6415/E6416* DSP controllers.

Note: 1.   Access modes: r/w – read/write; r – read-only; w – write only.

XMEM bit of *SYS_CNF_RG* I/O control register is used for *TORNADO-E6202/E6203* DSP controllers only in order to select external TMS320C6202/C6203 DSP synchronous memory (SBSRAM or SDRAM), which is being currently connected to EMIF CE-0 and CE-2 external memory areas of on-board TMS320C6202/TMS320C6203 DSP. The reason for this selection is due to TMS320C6202/C6203 DSP does not support SBSRAM and SDRAM simultaneously connected to its EMIF. This hardware control selection can be done at run-time via DSP software. Note, that along with setting this bit, user DSP application for *TORNADO-E6202/E6203* DSP controllers must also properly configure DSP on-chip EMIF control registers (refer to table 2-3a) in order to match this setting.

Default read-back state of *XMEM* bit of *SYS_CNF_RG* I/O control register for *TORNADO-E6202/E6203* DSP controllers, which is set on power-on and DSP reset conditions, depends upon the selected DSP bootmode in accordance with table 2-1.

MAP0/SDRAM/NO-BMODE and *MAP0/SDRAM/FLASH8-BMODE* DSP bootmode configurations listed in table 2-1, which assume SDRAM to be automatically configured at EMIF CE-0 area of TMS320C6x DSP, result in default setting of *XMEM* bit to the '1' state. This corresponds to selection of SDRAM external synchronous memory in EMIF CE-0 and CE-2 areas of *TORNADO-E6202/E6203* on-board TMS320C6x DSP.

All other DSP bootmodes for *TORNADO-E6202/E6203* DSP controllers, which are listed in table 2-1 and which assume SBSRAM to be automatically configured at EMIF CE-0 area of TMS320C6x DSP, result in default setting of *XMEM* bit to the '0' state, which corresponds to selection of SBSRAM external synchronous memory in EMIF CE-0 area of *TORNADO-E6202/E6203* on-board TMS320C6x DSP.

MCBSP1_UTOPIA_IF_SEL read-only bit of *SYS_CNF_RG* I/O control register is used for *TORNADO-E6415/E6416* DSP controllers only in order user DSP application can define what particular external TMS320C6415/C6416 DSP on-chip interface (McBSP-1 or UTOPIA) has been selected for communication with external devices and peripherals via *TORNADO-E6415/E6416* on-board connectors. Selection between McBSP-1 and UTOPIA external TMS320C6415/C6416 DSP on-chip interfaces is performed via *TORNADO-E6415/E6416* on-board SW2-4 configuration switch while DSP is in the reset state (refer to the corresponding subsection below and table 2-14). *MCBSP1_UTOPIA_IF_SEL* read-only bit of *SYS_CNF_RG* I/O control register is latched on release of DSP reset signal.

CAUTION

TMS320C6414 DSP at *TORNADO-E6414* DSP controller does not have on-chip UTOPIA interface and uses McBSP-1 serial port only, so *MCBSP1_UTOPIA_IF_SEL* read-only bit of *SYS_CNF_RG* I/O control register always reads as '0' for *TORNADO-E6414* DSP controller.

TMS320C6x DSP on-chip HPI port

TORNADO-E6x DSP controllers offer direct access from host computer/controller to TMS320C6x DSP on-chip 16-bit/32-bit HPI (host port interface) via on-board JP7 connector (refer to fig.2-2 or fig.A-1). This allows to upload/download data/code from/to host computer to/from *TORNADO-E6x* on-board DSP environment (including DSP on-chip memory, on-board memory, I/O peripherals and I/O control registers) using simple asynchronous parallel HPI interface.

TORNADO-E6x on-board HPI port appears as standard TMS320C6201/C6701 16-bit HPI port for *TORNADO-E62/E67* DSP controllers, as the TMS320C6202/C6203 DSP on-chip X-bus configured as 32-bit slave asynchronous HPI port for *TORNADO-E6202/E6203* DSP controllers, and as the user selected either 16-bit or 32-bit HPI port for *TORNADO-E64xx* DSP controllers.

Except for the HPI data bus width difference and HPI register list and format difference, the only important difference between HPI ports of *TORNADO-E62/E67/E64xx* and *TORNADO-E6202/E6203* DSP controllers is that DSP-to-host interrupt generation via HPI port is supported for *TORNADO-E62/E67/E64xx* DSP controllers only due to the different design of TI TMS320C6201/C6701/C64xx and TMS320C6202/C6203 DSP. Also, the minor difference between HPI ports of *TORNADO-E62/E67* and *TORNADO-E6202/E6203/E64xx*

DSP controllers is that HPI port of *TORNADO-E62/E67* DSP controllers supports byte access to HPI registers, whereas HPI port registers of *TORNADO-E6202/E6203/E64xx* DSP controllers can be accessed as full 32-bit and 16-bit data words only.

CAUTION

This manual does not contain description and programming details
for TMS320C6x DSP on-chip HPI port.

For more information refer to original TI datasheets and user's guides for TMS320C6x DSP,
which are supplied in either paper or electronic form together with this manual.

Pinout for on-board HPI connectors for different *TORNADO-E6x* are presented at figure 2-3 and signal descriptions are presented in table 2-12. All signal names for HPI signals correspond to that for the TI TMS320C6x DSP datasheet.
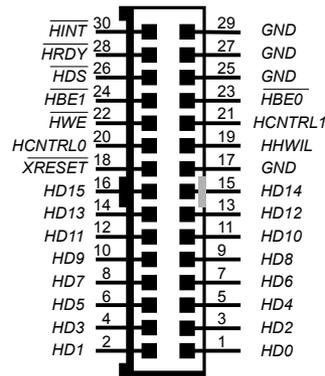
Fig.2-3a. Pinout for HPI port connector of *TORNADO-E62/E67* (top view).
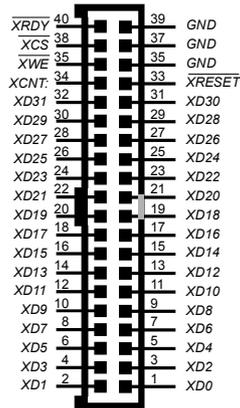
Fig.2-3b. Pinout for HPI port connector of *TORNADO-E6202/E6203* (top view).
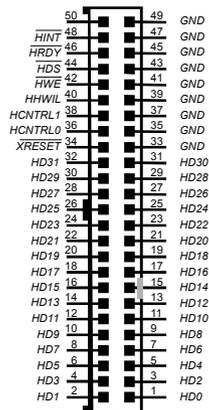
Fig.2-3c. Pinout for HPI port connector of *TORNADO-E64xx* (top view).

CAUTION

TMS320C6201/C6701/C64xx DSP on-chip HPI port for *TORNADO-E62/E67/E64xx* DSP controllers is configured with always active *HCS* and the *HAS* input being connected to the logical '1'.

This corresponds to always enabled *HRDY* output and requires external *HDS* data strobe only for active data synchronization with the *HHWIL/HCNTRL0/HCNTRL1* TMS320C6201/C6701/C64xx DSP on-chip HPI port inputs operating as the host address inputs.

<div style="border:1px solid">

CAUTION

TMS320C6202/C6203 DSP on-chip X-bus is for *TORNADO-E62/E67* DSP controllers is configured as 32-bit slave asynchronous HPI port.

XW/R signal (specified as *XWE* at fig.2-3b) of TMS320C6202/C6203 X-bus of *TORNADO-E6202/C6203* DSP controllers is configured as active low for write cycles.

XBE[0..3] byte enable signals of TMS320C6202/C6203 X-bus do not present at the HPI port connector of *TORNADO-E6202/C6203* DSP controllers and are permanently connected to logical '0' in order to enable HPI data transfers using 32-bit data cycles only.

</div>

<div style="border:1px solid">

CAUTION

Data format (16-bit or 32-bit) for TMS320C64xx DSP on-chip HPI port is selected via *TORNADO-E64xx* on-board SW2-3 configuration switch in accordance with table 2-13.

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Table 2-12a. HPI port connector signals for *TORNADO-E62/E67*.

Signal name	signal type	Description
HD0..HD15	I/O/Z	HPI data bus.
HHWIL HCNTRL0 HCNTRL1	I	HPI register 16-bit half-word selector and register address inputs.
HBE0 HBE1	I	Active low HPI byte enable inputs. These input has on-board pull-up resistor.
HDS	I	Active low data strobe. This input has on-board pull-up resistor.
HR/W	I	HPI data read/write input (active low corresponds to the write cycle). This input has on-board pull-up resistor.
HRDY	O	Active low HPI data ready output.
HINT	O	Active low HPI-to-host interrupt request output.

| XRESET | O | Active low DSP reset input. This signal is not a part of TMS320C6201/C6701 HPI port signal list and is connected to *TORNADO-E62/E67* on-board reset controller. Active low signal at this input enables generation of reset signal for *TORNADO-E62/E67* on-board DSP, I/O peripherals and I/O control registers. Refer to subsection "ON-board reset signal for TMS320C6x DSP, I/O peripherals and I/O control registers" for more details. |
| GND | - | Ground. |

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v TTL signals with *Iout*=1.5mA.

Table 2-12b.   HPI port connector signals for *TORNADO-E6202/E6203*.

Signal name	signal type	Description
XD0..XD31	I/O/Z	X-bus data bus (HPI data bus). All 32-bits have to be transferred in one cycle.
XCNTL	I	HPI register selector address input. This signal selects between host XBD and XBISA register of TMS320C6202/C6203 HPI port. XCNTL=0, access is made to the XBD register. XCNTL=1, access is made to the XBISA register.
XCS	I	Active low data strobe. This input has on-board pull-up resistor.
XWE	I	HPI data read/write input (active low corresponds to the write cycle). This input has on-board pull-up resistor and corresponds to the *XW/R* signal of TMS320C6202/C6203 X-bus.
XRDY	O	Active low HPI data ready output.
XRESET	O	Active low DSP reset input. This signal is not a part of TMS320C6202/C6203 X-bust signal list and is connected to *TORNADO-E6202/E6203* on-board reset controller. Active low signal at this input enables generation of reset signal for *TORNADO-E6202/E6203* on-board DSP, I/O peripherals and I/O control registers. Refer to subsection "ON-board reset signal for TMS320C6x DSP, I/O peripherals and I/O control registers" for more details.
GND	-	Ground.

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v TTL signals with *Iout*=1.5mA.

Table 2-12c.   HPI port connector signals for *TORNADO-E64xx*.

Signal name	signal type	Description
HD0..HD31	I/O/Z	HPI data bus. *HD0..HD15* are used in case HPI is configured in 16-bit mode, whereas *HD0..HD31* are used for 32-bit HPI mode.

HHWIL *HCNTRL0* *HCNTRL1*	I	HPI register 16-bit half-word selector and register address inputs. *HHWIL* input for selection of HPI register 16-bit half-words is used only in case HPI is configured in 16-bit mode.
HDS	I	Active low data strobe. This input has on-board pull-up resistor.
HR/W	I	HPI data read/write input (active low corresponds to the write cycle). This input has on-board pull-up resistor.
HRDY	O	Active low HPI data ready output.
HINT	O	Active low HPI-to-host interrupt request output.
XRESET	O	Active low DSP reset input. This signal is not a part of TMS320C64xx HPI port signal list and is connected to *TORNADO-E64xx* on-board reset controller. Active low signal at this input enables generation of reset signal for *TORNADO-E64xx* on-board DSP, I/O peripherals and I/O control registers. Refer to subsection "ON-board reset signal for TMS320C6x DSP, I/O peripherals and I/O control registers" for more details.
GND	-	Ground.

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
               2. All logical signal levels and load currents correspond to that for 3v/5v TTL signals with *Iout*=1.5mA.

On-board DSP HPI connector is Samtec STMM-115-02-G-D 30-pin 2mm male header for *TORNADO-E62/E67* DSP controllers, Samtec STMM-120-02-G-D 40-pin 2mm male header for *TORNADO-E6202/E6203* DSP controllers, and Samtec STMM-125-02-G-D 50-pin 2mm male header for *TORNADO-E64xx* DSP controllers. The mating parts are Samtec TCSD-15-01-N female plug for 2mm 30-wire flat cable for *TORNADO-E62/E67* DSP controllers, Samtec TCSD-20-01-N female plug for 2mm 40-wire flat cable for *TORNADO-E6202/E6203* DSP controllers, and Samtec TCSD-25-01-N female plug for 2mm 50-wire flat cable for *TORNADO-E64xx* DSP controllers correspondingly, which are included as standard option with *TORNADO-E6x* controllers. Extra HPI connector plugs are available either from Samtec Inc (www.samtec.com) or from MicroLAB Systems upon request.

HPI port of *TORNADO-E64xx* on-board TMS320C64xx DSP can be user selected to operate either in 16-bit or in 32-bit data mode, which delivers outstanding flexibility for connection to external host controller/computer. Selection between 16-bit and 32-bit HPI port data modes for *TORNADO-E64xx* on-board TMS320C64xx DSP is performed via on-board SW2-3 configuration switch while DSP is in the reset state in accordance with table 2-13. Altering of the SW2-3 switch state after DSP has been released from the reset state will have no effect.

Table 2-13. Selection of HPI port data mode for *TORNADO-E64xx* DSP controllers.

SW2-3 switch	Description
ON	TMS320C64xx DSP on-chip HPI port is configured in 16-bit data mode, i.e. 32-bit data shall be read/written to 32-bit HPI registers using two 16-bit half-words (*HD0..HD15*). Selection of 16-bit LSW/MSW is performed via *HHWIL* input of HPI port connector (JP7). This mode provides 100% compatibility for HPI port access with *TORNADO-E62/E67* DSP controllers except for no byte access are allowed to HPI registers of *TORNADO-E64xx* DSP controllers.
OFF	TMS320C64xx DSP on-chip HPI port is configured in 32-bit data mode, i.e. 32-bit data shall be read/written to 32-bit HPI registers using one 32-bit data words (*HD0..HD31*). *HHWIL* input of HPI port connector (JP7) is ignored. No byte access are allowed to HPI registers of *TORNADO-E64xx* DSP controllers.

Note: 1.   Highlighted configuration corresponds to default factory setting.

Selection of TMS320C6415/C6416 external DSP on-chip interface for TORNADO-E6415/E6416

TORNADO-E6415/E6416 DSP controllers provide selection of external TMS320C6415/C6416 DSP on-chip interface (McBSP-1 or UTOPIA) for communication with external devices and peripherals via *TORNADO-E6415/E6416* on-board connectors and DCM sites.

The reason for this selection is that McBSP-1 and UTOPIA external TMS320C6415/C6416 DSP on-chip interfaces share common IC package pins due to the DSP IC package pins lack.

Selection between McBSP-1 and UTOPIA external TMS320C6415/C6416 DSP on-chip interfaces is performed via *TORNADO-E6415/E6416* on-board SW2-4 configuration switch while DSP is in the reset state in accordance with table 2-14. Altering the of SW2-4 switch state after DSP has been released from the reset state will have no effect.

Table 2-14. Selection of TMS320C6415/C6416 external interface for *TORNADO-E6415/E6416* DSP controllers.

SW2-4 switch	Description
ON	TMS320C6415/C6416 DSP on-chip McBSP-1 serial port interface is selected for communication with external devices/peripherals via *TORNADO-E6415/E6416* on-board SIOX rev.B (JP5), SIOX rev.C (JP6) and MXSIOX (JP7) DCM sites.
OFF	TMS320C6415/C6416 DSP on-chip 50MHz 8-bit UTOPIA level 2 slave ATM interface is selected for communication with external devices/peripherals via *TORNADO-E6415/E6416* on-board UTOPIA I/O connectors (JP22 and JP23).

Note: 1.   Highlighted configuration corresponds to default factory setting.

User DSP application for *TORNADO-E6415/E6416* DSP controllers can define which particular external TMS320C6415/C6415 DSP on-chip interface has been selected by reading *MCBSP1_UTOPIA_IF_SEL* read-only bit of *SYS_CNF_RG* I/O control register (refer to the corresponding subsection above and to table 2-11). *MCBSP1_UTOPIA_IF_SEL* read-only bit of *SYS_CNF_RG* I/O control register is latched on release of DSP reset signal and does not change until new DSP reset signal is applied.

UTOPIA interface of TORNADO-E6415/E6416

TORNADO-E6415/E6416 DSP controllers provide 8-bit UTOPIA level 2 slave interface for communication with external ATM master devices at speeds up to 50MHz per direction and user defined cell format up to 64 bytes. UTOPIA interface is the part of TMS320C6415/C6416 DSP on-chip peripherals.

CAUTION

This manual does not contain description and programming details
for TMS320C6415/C6416 DSP on-chip 8-bit UTOPIA level 2 slave ATM interface.

For more information refer to original TI datasheets and user's guides for TMS320C6x DSP,
which are supplied in either paper or electronic form together with this manual.

Before using UTOPIA interface of *TORNADO-E6415/E6416* DSP controllers, it must be enabled via on-board SW2-4 configuration switch in accordance with table 2-14 while DSP is in the reset state. This selection is required because McBSP-1 DSP on-chip serial port and UTOPIA DSP on-chip interface share common DSP IC package pins due to the pins lack (refer to the corresponding subsection above for more details). Change of SW2-4 switch state after DSP has been released from the reset state has no effect.

External UTOPIA ATM master devices shall connect to *TORNADO-E6415/E6416* DSP controllers via on-board JP22 (UTOPIA receiver) and JP23 (UTOPIA transmitter) connectors.

Pinout and signal description for *TORNADO-E6415/E6416* on-board UTOPIA I/O connectors are presented at figure 2-4 and table 2-15. All signal names for UTOPIA receiver and transmitter connector signals correspond to that for the TI TMS320C6415/C6416 DSP datasheet.
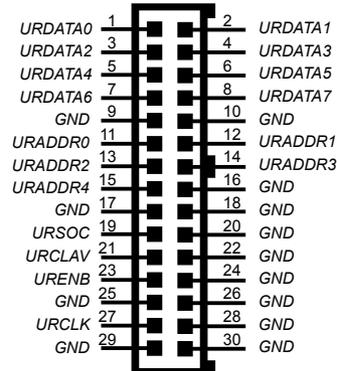
Fig.2-4a. Pinout for UTOPIA receiver connector of *TORNADO-E6415/E6416* (top view).
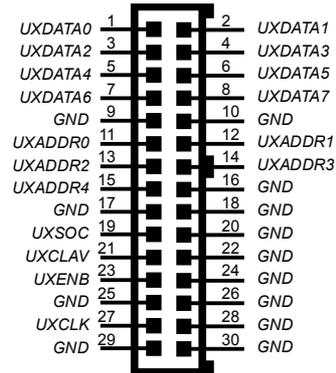
Fig.2-4b.   Pinout for UTOPIA transmitter connector of *TORNADO-E6415/E6416* (top view).

Table 2-15a.   UTOPIA receiver connector signals for *TORNADO-E6415/E6416*.

Signal name	signal type	Description
URDATA[0..7]	I	Active high UTOPIA receiver 8-bit input data.
URADDR[0..4]	I	Active high UTOPIA receiver 5-bit input address.
URSOC	I	Active high UTOPIA receiver start of cell input.
URCLAV	O	Active high UTOPIA receiver cell available output from UTOPIA slave.
URENB	I	Active high UTOPIA receiver enable input.
URCLK	I	Active high UTOPIA receiver clock input.
GND	-	Ground.

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
            2. All logical signal levels and load currents correspond to that for 3v/5v TTL signals with *Iout*=16mA.

Table 2-15b.   UTOPIA transmitter connector signals for *TORNADO-E6415/E6416*.

Signal name	signal type	Description
UXDATA[0..7]	O	Active high UTOPIA transmitter 8-bit input data.
UXADDR[0..4]	I	Active high UTOPIA transmitter 5-bit input address.
UXSOC	O	Active high UTOPIA transmitter start of cell output.

UXCLAV	O	Active high UTOPIA transmitter cell available output from UTOPIA slave.
UXENB	I	Active high UTOPIA transmitter enable input.
UXCLK	I	Active high UTOPIA transmitter clock input.
GND	-	Ground.

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
           2. All logical signal levels and load currents correspond to that for 3v/5v TTL signals with *Iout*=16mA.

CAUTION

All active high/low UTOPIA receiver and transmitter input signals are on-board terminated via pull-down/up 110 Ohm resistors correspondingly, which provides impedance match with 2mm flat cable for connection to external UTOPIA ATM master controller.

TORNADO-E6415/E6416 on-board UTOPIA receiver (JP22) and UTOPIA transmitter (JP23) connectors are Samtec STMM-115-02-G-D 30-pin 2mm male headers. The mating parts are Samtec TCSD-15-01-N female plugs for 2mm 30-wire flat cable, which are included as standard option with *TORNADO-E6415/E6416* controllers. Extra UTOPIA receiver/transmitter connector plugs are available either from Samtec Inc (www.samtec.com) or from MicroLAB Systems upon request.

Generating DSP-to-Host Interrupt Request for TORNADO-E62/E67/E64xx

TORNADO-E62/E67/E64xx DSP controllers supports generation of DSP-to-host interrupt request from the on-board TMS320C6x DSP to host computer via HPI port (*HINT* signal at the HPI port connector JP5) in order to synchronize between program execution in host and on-board DSP environments.

Writing logical '1' by the DSP software to the *HINT* bit of TMS320C6201/C6701/C64xx DSP on-chip HPIC register will result in generation of low level *HINT* signal at the HPI port connector JP5. This signal level is active for generation of DSP-to-host interrupt request.

Processing interrupt request from host computer

All *TORNADO-E6x* DSP controllers supports processing of host-to-DSP interrupt request from host computer to TMS320C6x DSP via HPI port in order to synchronize between the program execution in host and on-board DSP environments.

Writing of logical '1' by host software to the *DSPINT* bit (host-to-DSP interrupt via HPI) of TMS320C6201/C6701/C64xx DSP on-chip HPIC register for *TORNADO-E62/E67/E64xx* DSP controllers and to the *DSPINT* bit of TMS320C6202/C6203 DSP on-chip XBISA register for *TORNADO-E6202/E6203* DSP controllers will result in generation *HPIINT* on-chip interrupt request for TMS320C6x DSP.

In order to set *DSPINT* interrupt request to DSP, host software must write 0x03030303 hex value to TMS320C6201/C6701/C64xx DSP on-chip HPIC register for *TORNADO-E62/E67/E64xx* DSP controllers and must perform logical 'OR' of the 0x00000001 hex value with the contents of TMS320C6202/C6203 DSP on-chip XBISA register for *TORNADO-E6202/E6203* DSP controllers.

Application DSP software for the TMS320C6x DSP must provide correct processing of *HPIINT* interrupt request in accordance with software requirements.

TMS320C6x DSP on-chip timers

TORNADO-E62xx/E67 on-board TMS320C620x/C6701 DSP provides two DSP on-chip timers (TM0 and TM1), whereas *TORNADO-E64xx* on-board TMS320C64xx DSP provides three DSP on-chip timers (TM0, TM1 and TM2).

All timers of *TORNADO-E6x* on-board TMS320C6x DSP are used for external timer or general purpose I/O and are externally available as either the corresponding timer input-only or timer output-only (fig.2-5), which can be also used as general purpose I/O correspondingly.
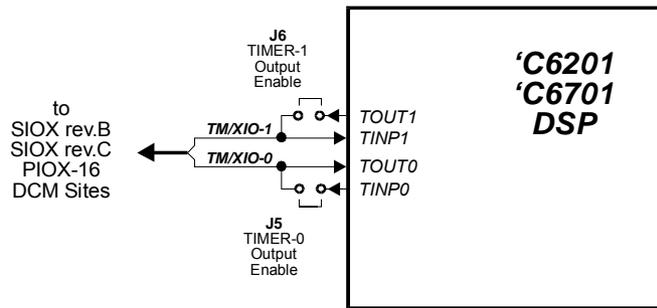

*Fig. 2-5a.* Connection diagram for DSP on-chip timers for *TORNADO-E62/E67*.
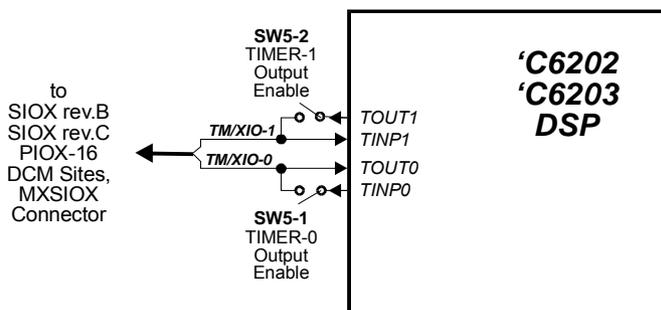
Fig. 2-5b. Connection diagram for DSP on-chip timers for *TORNADO-E6202/E6203*.
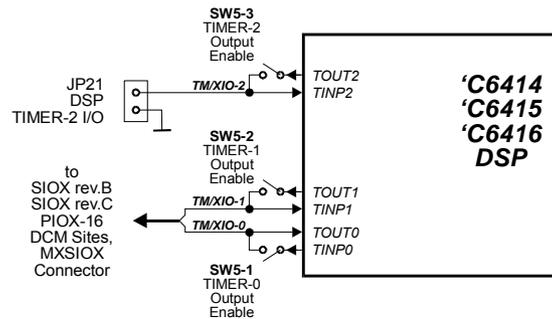
Fig. 2-5c. Connection diagram for DSP on-chip timers for *TORNADO-E64xx*.

Selection between timer input and timer output modes is performed via the corresponding on-board jumpers J5 and J6 (*TORNADO-E62/E67*) and on-board switches SW5-1 and SW5-2 (*TORNADO-E6202/E6203/E64xx*) and SW5-3 (*TORNADO-E64xx* only). When jumper is not installed, or switch is in the 'OFF' state, then the corresponding external *TM/XIO-n* signal is connected to the *TINPn* input of the corresponding DSP on-chip timer #n (n=0..2), which corresponds to timer input-only or general purpose input mode. In case jumper is installed, or switch is in the 'ON' state, then the corresponding external *TM/XIO-n* signal is connected to both *TINPn* input and *TOUTn* output of the corresponding DSP on-chip timer #n (n=0..2) , which corresponds to timer output-only or general purpose output mode.

Note, that the software configuration of TMS320C6x DSP on-chip timer pins must match configuration of the corresponding on-board J5/J6 jumpers (*TORNADO-E62/E67*) and SW5 switches (*TORNADO-E6202/E6203/E64xx*), and it is not possible to dynamically reconfigure these pins at run-time via DSP software from timer/input-only to timer/output-only and vise-versa.

All *TORNADO-E6x* on-board external *TM/XIO-n* timer I/O signals are CMOS/TTL 3v/5v compatible I/O signals and provide I_L=1.6mA.

DSP on-chip timer-0 (TM0) and timer-1 (TM1) of *TORNADO-E6x* on-board DSP are routed directly to on-board PIOX-16 and SIOX rev.B/C DCM site headers and to on-board MXSIOX connector. I/O control signals for these TM0 and TM1 DSP on-chip timers appear as the corresponding timer/XIO signals of on-board PIOX-16 and SIOX rev.B/C DCM site headers and on-board MXSIOX connectors. Refer to the corresponding sections below in this chapter for more details.

DSP on-chip timer-2 (TM2) of *TORNADO-E64xx* on-board DSP is routed directly to on-board JP21 edge connector. Pinout for TMS320C64xx DSP on-chip timer-2 I/O connector (JP21) is presented at figure 2-6. *TORNADO-E64xx* on-board JP21 TM2 I/O connector is the industry standard 0.05" 2-pin male header from Molex (www.molex.com). The mating plugs are available from upon request from MicroLAB Systems.
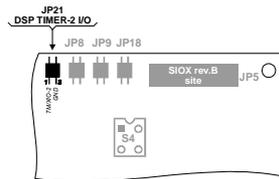
Fig. 2-6. Pinout of TMS320C64xx DSP on-chip timer-2 I/O for *TORNADO-E64xx* (top view).

PIOX-16 DCM site

TORNADO-E6x DSP controllers provide on-board JP4 PIOX-16 (16-bit parallel I/O expansion interface) DCM site header (refer to figure 2-2 and A-1) for compatible high-speed AD/DA/DIO DCM.

PIOX-16 area of *TORNADO-E62xx/E67* DSP controllers is mapped directly to the address space of on-board TMS320C620x/C6701 DSP and PIOX-16 interface data words occupy least significant 16-bit words of 64Kx32 I/O sub-area of DSP EMIF CE-3 area (refer to table 2-2 for addressing details).

PIOX-16 area of *TORNADO-E64xx* DSP controllers is mapped directly to the address space of on-board TMS320C64xx DSP and PIOX-16 interface data words occupy 64Kx16 I/O sub-area of DSP EMIF-B CE-0 area (refer to table 2-2 for addressing details).

PIOX-16 site comprises of the TMS320C6x DSP 16-bit data and 16-bit address buses, data strobes, timer/IO pins, external interrupt requests, dedicated reset signal and ±5v/±12v power supply lines. For details about PIOX-16 site refer to the corresponding section later in this chapter.

SIOX rev.B DCM site

TORNADO-E6x provides on-board JP5 SIOX (serial I/O expansion interface) rev.B DCM site header (refer to figure 2-2 and A-1) for compatible *TORNADO* SIOX rev.B AD/DA/DIO DCM.

SIOX rev.B site comprises of two serial ports, timer/IO pins, external interrupt requests, dedicated reset signal and ±5v/±12v power supply lines. For details about SIOX rev.B site refer to the corresponding section later in this chapter.

SIOX rev.C enhanced DCM site

TORNADO-E6x also provides on-board JP6 SIOX rev.C DCM site header (refer to figure 2-2 and A-1) for compatible *TORNADO* SIOX rev.C AD/DA/DIO DCM.

SIOX rev.C is an enhanced version of SIOX rev.B DCM site and comprises of two serial ports, timer/IO pins, external interrupt request, 8-bit DSP parallel data bus, 6-bit DSP address lines, parallel data strobes, dedicated reset signal and +5v/±12v power supply lines.

SIOX rev.C 8-bit parallel data words of *TORNADO-E62xx/E67* DSP controllers occupy least significant bytes of 64x32 I/O sub-area of DSP EMIF CE-3 area (refer to table 2-2 for addressing details).

SIOX rev.C 8-bit parallel data words of *TORNADO-E64xx* DSP controllers occupy least significant bytes of 64x162 I/O sub-area of DSP EMIF-B CE-0 area (refer to table 2-2 for addressing details).

For details about SIOX rev.C site refer to the corresponding section later in this chapter.

MXSIOX connector for external T/SU-X1 SIOX rev.B mini-extender kit for TORNADO-E6202/E6203/E64xx

TORNADO-E6202/E6203/E64xx DSP controllers with on-board TMS320C6202/C6203/C64xx DSP, which feature three DSP on-chip McBSP serial ports, provide on-board JP19 MXSIOX connector (refer to figure 2-2 and A-1) for connection to external *T/SU-X1* SIOX rev.B mini-extender kit, which can carry one compatible *TORNADO* SIOX rev.B AD/DA/DIO DCM.

MXSIOX connector comprises of signals for two serial ports, timer/IO pins, external interrupt requests, dedicated reset signal and +5v/±12v power supply lines.

For more details about MXSIOX connector refer to the corresponding section later in this chapter and to Appendix B.

External reset input connector

TORNADO-E6x on-board JP2 external reset input connector (refer to figures 2-2 and A-1) can be used in order to apply active low external reset signal (*XRESET*).

Pinout for *TORNADO-E6x* on-board JP2 external reset input connector is presented at figures 2-7. *XRESET* input is on-board pulled-up and is 3v/5v TTL compatible digital input.
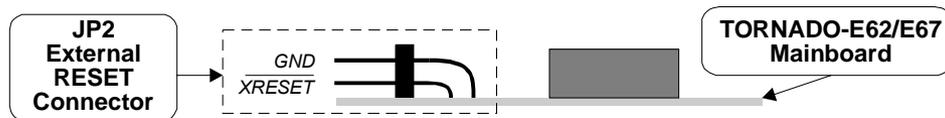
*Fig. 2-7a.* Pinout of external reset input connector for *TORNADO-E62/E67* (side view.
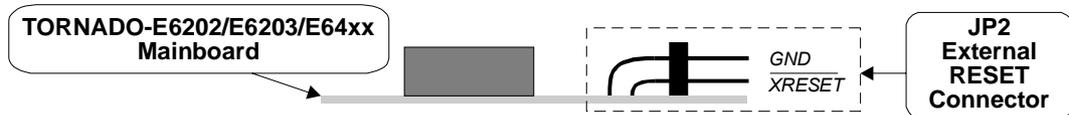

Fig. 2-7b. Pinout of external reset input connector for *TORNADO-E6202/E6203/E64xx* (side view).

TORNADO-E6x on-board JP2 external reset input connector is the industry standard 2-pin 0.1" pitch dual-row right-angle male header. Compatible 2-pin female plug is available from a variety of vendors including AMP, Molex, etc..

External Power Connector

External power connector (JP1) for *TORNADO-E6x* (refer to fig.2-2 and fig.A-1) comprises of the ±5v and ±12v power lines.

CAUTION

Only +5v external power supply input is required for operation of on-board *TORNADO-E6x* hardware.

-5v and ±12v external power supply inputs are directly wired to on-board PIOX-16 and SIOX rev.B/C DCM sites and MXSIOX connector (*TORNADO-E6202/E6203/E64xx*) and are not used by *TORNADO-E6x* on-board hardware. If neither of PIOX-16, SIOX rev.B/C DCM is installed or external SIOX rev.B mini-extender is connected via on-board MXSIOX connected, then -5v and ±12v external power supply inputs can be left unconnected.

```
GND
GND
+12v
-12v
-5v
+5v
+5v
```
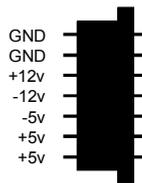
Fig. 2-8. Pinout of external power input connector for *TORNADO-E6x* (front view).

External power connector for *TORNADO-E6x* is the industry standard 7-pin 0.1" pitch single-row right-angle male power header, which is available from a variety of vendors including AMP, Molex, etc. One piece of the mating power plug is included as the standard option with *TORNADO-E6x*. Extra power plugs are available from ether from MicroLAB Systems upon request, or from AMP, Molex and other manufacturers.

2.3   Parallel I/O Expansion Interface Site (PIOX-16)

TORNADO-E6x DSP controller architecture provides expansion of the on-board I/O resources using 16-bit parallel I/O expansion (PIOX-16) interface site for compatible DCM, which must be installed above the *TORNADO-E6x* mainboard (refer to fig.1-1, fig.1-2 and fig.2-9).

A variety of available 'of-the-shelf' *TORNADO* PIOX-16 DCM comprises of AD/DA/DIO, application-specific and DSP coprocessor DCM for real time multi-channel high-speed telecom, instrumentation, industrial, digital radio, etc signal processing applications.

Description

TORNADO-E6x on-board PIOX-16 DCM interface site comprises 16-bit DSP data bus, 16-bit DSP address bus, data strobes, timer/IO pins, interrupt request inputs, dedicated reset signal, and power supply lines. PIOX-16 DCM interface site supports 16-bit data transfer cycles only.

Installation of PIOX-16 DCM onto TORNADO-E6x

Figure 2-9 shows installation of PIOX-16 DCM onto *TORNADO-E6x* DSP controller.
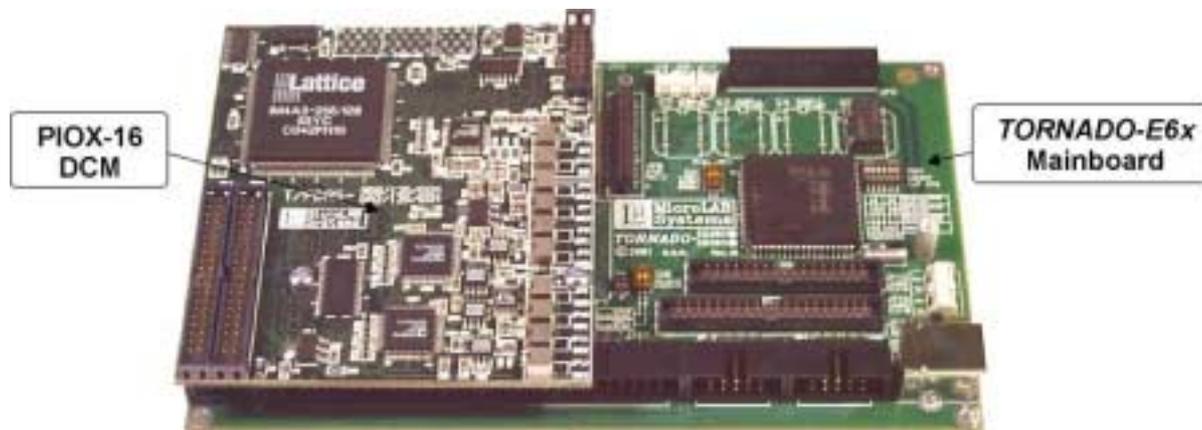
Fig.2-9.   Installation of PIOX-16 DCM onto *TORNADO-E6x* mainboard.

Accessing PIOX-16 interface from DSP software

TORNADO-E6x on-board PIOX-16 DCM interface can be accessed by on-board TMS320C6x DSP when addressing the corresponding external DSP memory area (refer to table 2-2 for addressing details).

CAUTION

For *TORNADO-E62xx/E67* DSP controllers, PIOX-16 interface data words are allocated as least significant 16-bit data words (bits D0..D15) of 32-bit data words of 64Kx32 sub-area of TMS320C62xx/C6701 DSP EMIF CE-3 area.

For *TORNADO-E62xx/E67* DSP controllers, PIOX-16 interface data can be accessed using 16-bit and 32-bit DSP external data access cycles.

For *TORNADO-E62xx/E67* DSP controllers, the most significant D16..D31 data bits are ignored when writing to PIOX-16 interface and are undefined when reading from PIOX-16 interface.

CAUTION

For *TORNADO-E64xx* DSP controllers, PIOX-16 interface data words are allocated as 16-bit data words (bits D0..D15) of 64Kx16 sub-area of TMS320C64xx DSP EMIF-B CE-0 area.

For *TORNADO-E64xx* DSP controllers, PIOX-16 interface data can be accessed using 16-bit DSP external data access cycles only.

CAUTION

TMS320C6x DSP on-chip EMIF Control Registers shall be configured in accordance with table 2-3 in order to meet requirements of *TORNADO-E6x* hardware for PIOX-16 interface.

PIOX-16 connector pinout and signals specification

On-board PIOX-16 interface connector signal specification and pinout are generally identical for all *TORNADO* DSP systems and controllers, and can differ in the number/designation of interrupt request pins and/or timer/IO pins control. The following are the only differences for PIOX-16 interface connectors for *TORNADO-E6x* DSP controllers:

- *TORNADO-E62/E67* DSP controllers have three on-board common interrupt request inputs (*IRQ-0...IRQ-2*), which are shared by all on-board SIOX rev.B/C and PIOX-16 DCM sites (refer to section "TMS320C6x DSP Environment" earlier in this chapter)
- *TORNADO-E6202/E6203* DSP controllers have four dedicated interrupt request inputs for PIOX-16 DCM site (*PX_IRQ-0...PX_IRQ-3*), which are connected to on-board DSP interrupt source selectors for each of DSP external interrupt request inputs (refer to section "TMS320C6x DSP Environment" earlier in this chapter) PIOX-16 DCM site interrupts are not shared with SIOX rev.B/C DCM site interrupts for *TORNADO-E6202/E6203* DSP controllers.

TORNADO-E6x on-board PIOX-16 interface connector p/n is DHB-RB50-S13NN, which is a high-density 50-pin DHB-series dual-row female connector with 0.05" pin pitch from Fujikura-DDK Ltd (www.ddkconnectors.com). Compatible PIOX-16 plug is DHB-PK50-S13NN, which are available upon request from MicroLAB Systems for design custom PIOX-16 DCM.

PIOX-16 interface connector pinout is presented at fig. 2-10, whereas signal specifications is listed in table 2-16.
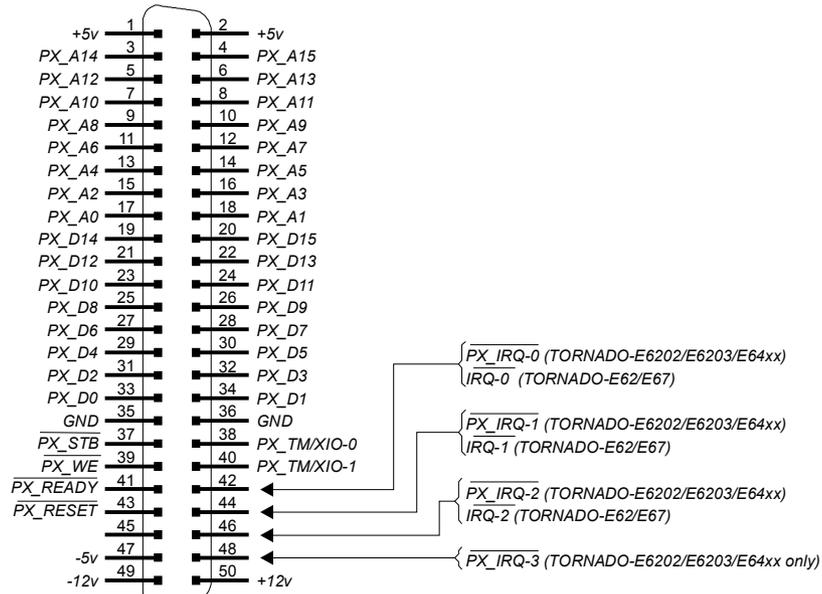
Fig.2-10. PIOX-16 DCM site connector pinout (top view).

Table 2-16. Signal description for PIOX-16 DCM site connector.

Signal name	signal type	Description
PX_A[0..15]	O	PIOX-16 address bus, which is connected to A2..A17 address bus of on-board TMS320C620x/C6701 DSP for *TORNADO-E62xx/E67* DSP and to EMIF-B A1..A16 address bus of on-board TMS320C64xx DSP for *TORNADO-E64xx* DSP controllers.
PX_D[0..15]	I/O	PIOX-16 data bus, which is connected to D0..D15 data bus of on-board TMS320C620x/C6701 DSP for *TORNADO-E62xx/E67* DSP controllers and to EMIF-B D0..D15 data bus of on-board TMS320C64xx DSP for *TORNADO-E64xx* DSP controllers.
$\overline{PX\_STB}$	O	Active low PIOX-16 data transfer strobe.
$\overline{PX\_WE}$	O	Active low PIOX-16 write enable signal.
$\overline{PX\_READY}$	I	Active low pulled-up PIOX-16 data ready signal. This signal must be generated by installed PIOX-16 DCM in order to terminate current data transfer cycle and meet timing requirements of memory and I/O devices used in particular PIOX-16 module.

PX_TM/XIO-0 *PX_TM/XIO-1*	I/O/Z	Timer or I/O pins, which are connected to the corresponding TMS320C6x DSP on-chip timer pins (TOUT0/TINP0 and TOUT1/TINP1) (refer to fig.2-1). Each of these pins can be used as timer input, timer output, or general purpose I/O pin (refer to fig.2-5 and TI TMS320C6x documentation for more details).
$\overline{PX\_RESET}$	O	Active low reset signal for on-board PIOX-16 interface site, which is the output state of *PX_RESET* bit of *PXSX_RESET_RG* I/O control register (refer to table 2-2 and section 2.2 for more details).
$\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, $\overline{IRQ\text{-}2}$ (*TORNADO-E62/E67*) *or* $\overline{PX\_IRQ\text{-}0}$, $\overline{PX\_IRQ\text{-}1}$ $\overline{PX\_IRQ\text{-}2}$ $\overline{PX\_IRQ\text{-}3}$ (*TORNADO-E6202/E6203/E64xx*)	I	Active low pulled-up external interrupt requests from PIOX-16 DCM site. If enabled, DSP interrupts are generated on the falling edge of these interrupt request inputs. *TORNADO-E62/E67* DSP controllers use three $\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, and $\overline{IRQ\text{-}2}$ PIOX-16 interrupt request inputs only, which are shared with the corresponding interrupt request inputs of on-board SIOX rev.B/C DCM sites. $\overline{IRQ\text{-}0}$ and $\overline{IRQ\text{-}1}$ are connected directly to *EXT INT4* and *EXT INT5* external interrupt requests of TMS320C6201/C6701 DSP. $\overline{IRQ\text{-}2}$ can be configured by DSP software to connect to any of *EXT_INT6* and *EXT_INT7* external interrupt requests of TMS320C6x DSP (refer to section 2-2 and tables 2-7 and 2-8 for more details). *TORNADO-E6202/E6203/E64xx* DSP controllers are using four dedicated $\overline{PX\_IRQ\text{-}0}$, $\overline{PX\_IRQ\text{-}1}$, $\overline{PX\_IRQ\text{-}2}$, and $\overline{PX\_IRQ\text{-}3}$ PIOX-16 interrupt request inputs, which are not shared with interrupt requests of on-board SIOX rev.B/C DCM sites ($\overline{SX\_IRQ\text{-}0}$, $\overline{SX\_IRQ\text{-}1}$, and $\overline{SX\_IRQ\text{-}2}$), and can be configured by DSP software to connect to any of *EXT_INT4..7* and *NMI* external interrupt requests of TMS320C6202/C6203/C64xx DSP (refer to section 2-2 and tables 2-7 and 2-8 for more details).
GND		Ground.
+5v		+5v power (from on-board JP1 power input connector).
+12v		+12v power (from on-board JP1 power input connector).
-5v		-5v power (from on-board JP1 power input connector).
-12v		-12v power (from on-board JP1 power input connector).

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v CMOS/TTL signals.

PIOX-16 data transfer cycle format

PIOX-16 interface site supports 16-bit data transfer cycles only, and, therefore PIOX-16 connector does not contain the cycle format definition signals.

Data transfer timing for PIOX-16

PIOX-16 interface data transfer timing is presented at fig.2-11. This data transfer timing is known as MOTO mode and assumes usage of data strobe signal and write enable signal.

CAUTION

Data transfer acknowledgement is provided by installed PIOX-16 DCM by means of asynchronous *PX_READY* signal.

In case TMS320C6x DSP performs access to PIOX-16 interface while PIOX-16 DCM is not installed, then this results in missing *PX_READY* signal and infinite wait condition for *TORNADO-E6x* on-board TMS320C6x DSP.
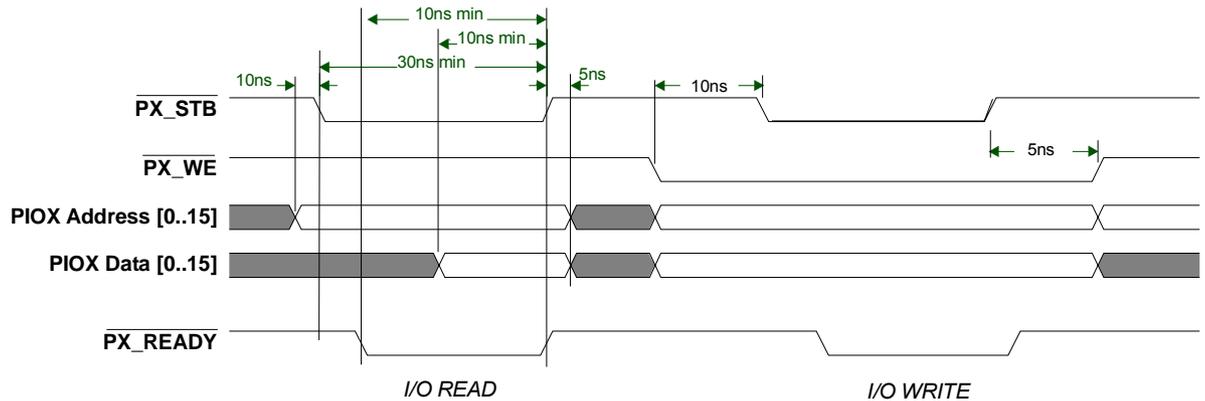
Fig.2-11. Timing diagram for PIOX-16 data transfer cycle.

Timer/IO pins

PX_TM/XIO-0 and *PX_TM/XIO-1* timer/ IO pins of *TORNADO-E6x* on-board PIOX-16 DCM site are connected to *TOUT0/TINP0* and *TOUT1/TINP1* pins of on-board TMS320C6x DSP and can be configured as either input-only or output-only via on-board jumpers J5 and J6 (*TORNADO-E62/E67*) and on-board switches SW5-1 and SW5-2 (*TORNADO-E6202/E6203/E64xx*).

Generating Reset Signal for PIOX/PIOX-16 Site

TORNADO-E6x provide individual reset signal for PIOX-16 site, which is controlled by *PX_RESET* bit of *PXSX_RESET_RG* I/O control register (refer to table 2-2 and section 2.2 for more details). This allows correct initialization of installed PIOX-16 DCM hardware and DSP software controlled synchronization with host *TORNADO-E6x* DSP software.

Physical dimensions for PIOX-16 DCM

Physical dimensions for PIOX-16 DCM are presented at fig.2-12. This information is intended for those *TORNADO-E6x* customers, who need to design customized PIOX-16 DCM.
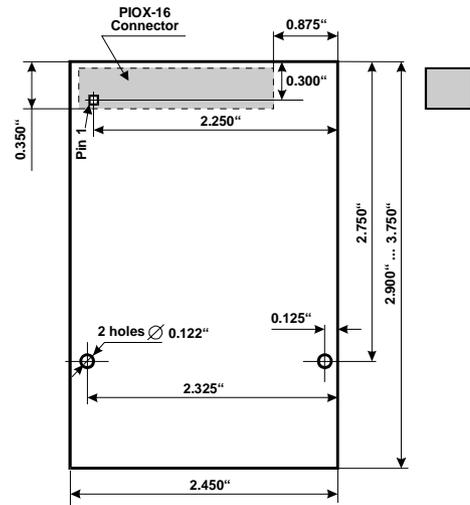
PIOX-16 connector: DDK DHB-Px50

Fig.2-12.   Physical dimensions for PIOX-16 DCM.

2.4   Serial I/O Expansion Interface Sites (SIOX)

TORNADO-E6x DSP controllers provide several on-board SIOX (serial I/O expansion) DCM sites (refer to figures 1-2, 2-2 and A-1), which are designed to carry *TORNADO* SIOX compatible DCM:

A variety of 'of-the-shelf' *TORNADO* SIOX DCM comprise from AD/DA/DIO and application specific I/O coprocessors DCM for telecommunication, speech/fax/modem and audio signal processing, industrial and instrumentation applications, and many more.

Description

TORNADO-E6x DSP controllers provide three different types of on-board SIOX DCM sites (fig.2-13):
- SIOX-A rev.B DCM site (JP5), which comprises of signals for two serial ports (SIO-0 and SIO-1), two timer/IO pins (*SX_TM/XIO-0* and *SX_TM/XIO-1*), external interrupts request inputs (*IRQ-0, IRQ-1, and IRQ-2* for *TORNADO-E62/E67* and *SX_IRQ-0, SX_IRQ-1* and *SX_IRQ-2* for *TORNADO-E6202/E6203/E64xx*), dedicated SIOX-A rev.B/C reset signal, and power supply lines
- enhanced SIOX rev.C DCM site (JP6), which comprises of signals for two serial ports (SIO-0 and SIO-1), two timer/IO pins (*SX_TM/XIO-0* and *SX_TM/XIO-1*), external interrupts request input (*IRQ-0* for *TORNADO-E62/E67* and *SX_IRQ-0* for *TORNADO-E6202/E6203/E64xx*), dedicated SIOX-A rev.B/C reset signal, 8-bit parallel data bus, 6-bit address bus, parallel data bus strobes, and power supply lines
- MXSIOX connector (JP19) (*TORNADO-E6202/E6203/E64xx* only) for connection to external *T/SU-X1* SIOX rev.B mini-extender kit (refer to Appendix B), which can carry one SIOX rev.B DCM. MXSIOX connector site comprises of signals for two serial ports (SIO-0 and SIO-1), two timer/IO pins (*SX_TM/XIO-0* and *SX_TM/XIO-1*), external interrupts request inputs (*SX_IRQ-1* and *SX_IRQ-2*), dedicated SIOX-B rev.B/C reset signal, and power supply lines.
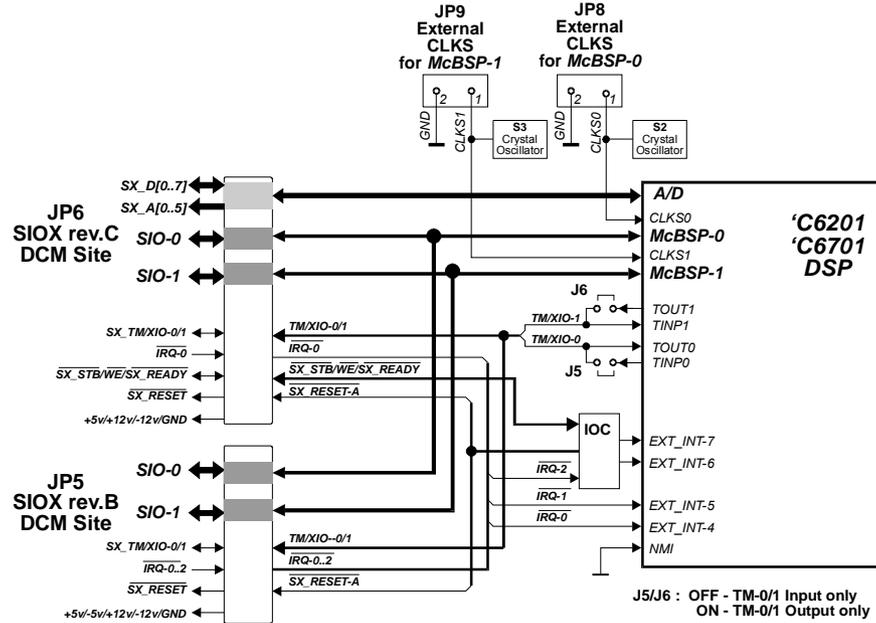
Fig.2-13a. SIOX sites connection diagram for *TORNADO-E62/E67*.
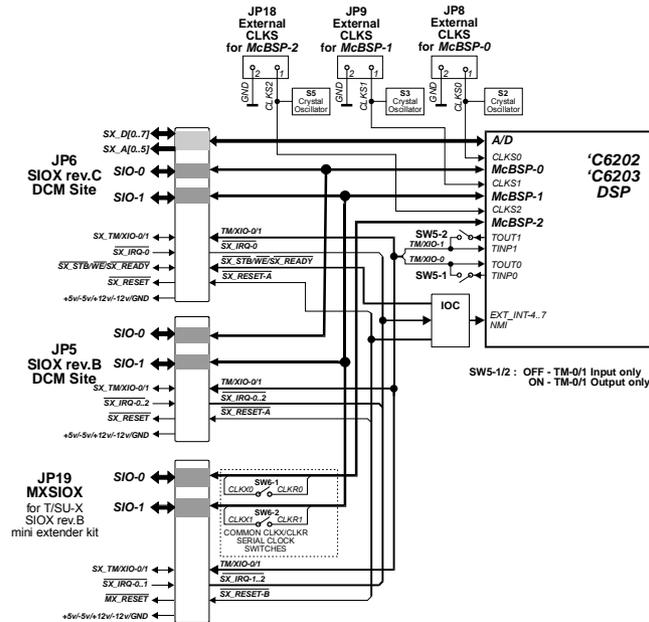
Fig.2-13b. SIOX sites connection diagram for *TORNADO-E6202/E6203*.
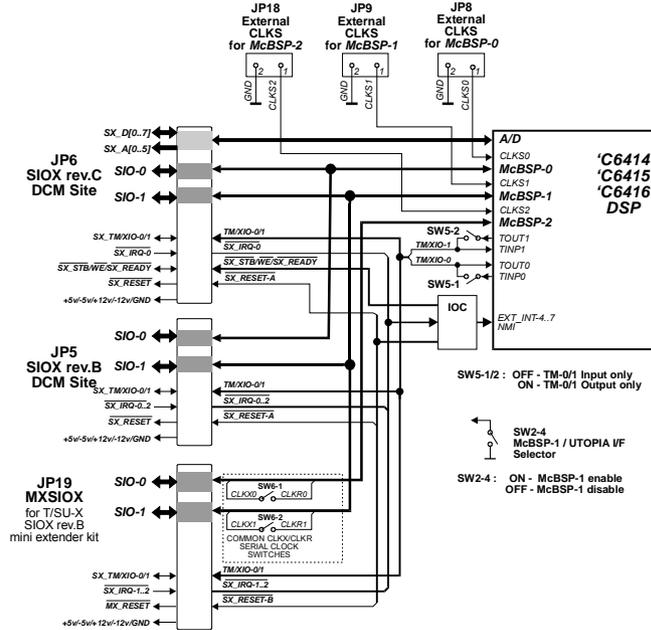
Fig.2-13c. SIOX sites connection diagram for *TORNADO-E64xx*.

CAUTION

SIO-0 and SIO-1 ports of SIOX rev.B and rev.C sites of all *TORNADO-E6x* DSP controllers are connected to TMS320C6x DSP on-chip McBSP-0 and McBSP-1 serial ports correspondingly.

CAUTION

SIO-0 and SIO-1 ports of MXSIOX site of *TORNADO-E6202/E6203/E64xx* DSP controllers are connected to TMS320C6x DSP on-chip McBSP-2 and McBSP-1 serial ports correspondingly.

TORNADO-E6202/E6203/E64xx on-board MXSIOX connector is also supplied with on-board SW6-1 and SW6-2 switches, which are used to set common serial clock for transmitter/receiver of MXSIOX SIO-0 and SIO-1 ports correspondingly. This is required to compensate long line effects for serial clock distribution over long *T/SU-X1/XC* connector cable for high serial clock frequencies. Refer to the corresponding subsection below and Appendix B for more details.

CAUTION

In case TMS320C6415/C6416 DSP on-chip McBSP-1 port is used for DSP application via *TORNADO-E6415/E6416* on-board SIOX rev.B/C DCM sites or external SIOX rev.B mini-extender kit connected via MXSIOX on-board connector, then McBSP-1 port must be enabled via *TORNADO-E6415/E6416* on-board SW2-4 switch (refer to section 2-2 and table 2-14 for more details).

Maximum throughoutput of SIO-0/1 serial ports of SIOX DCM sites is 200 Mbit/s for *TORNADO-E62* DSP controllers, 250 Mbit/s for *TORNADO-E6202* DSP controllers, 300 Mbit/s for *TORNADO-E6203* DSP controllers, 600 Mbit/s for *TORNADO-E64xx* DSP controllers, and 167 Mbit/s for *TORNADO-E67* DSP controllers. Refer to original TI documentation for more details about programming TMS320C6x DSP on-chip McBSP serial ports.

Timer/IO pins

SX_TM/XIO-0 and *SX_TM/XIO-1* timer/ IO pins of *TORNADO-E6x* on-board SIOX sites are connected to *TOUT0/TINP0* and *TOUT1/TINP1* pins of on-board TMS320C6x DSP and shall be configured to be either input-only or output-only via on-board jumpers J5 and J6 (*TORNADO-E62/E67*) and on-board switches SW5-1 and SW5-2 (*TORNADO-E6202/E6203/E64xx*).

Maximum clock frequency for timer/IO pins (*SX_TM/XIO-0* and *SX_TM/XIO-1*), in case these TMS320C6x DSP timer I/O pins are configured as timer pins, is 50 MHz for *TORNADO-E62* DSP controllers, 62.5 MHz for *TORNADO-E6202* DSP controllers, 75 MHz for *TORNADO-E6203* DSP controllers, 125 MHz or 150 MHz for *TORNADO-E64xx* DSP controllers, and 41.75 MHz for *TORNADO-E67* DSP controllers. Refer to original TI documentation for more details about programming TMS320C6x DSP on-chip timers.

Installation of SIOX DCM onto TORNADO-E6x mainboard

SIOX rev.B and SIOX rev.C DCM can plug directly into *TORNADO-E6x* on-board SIOX rev.B DCM site (JP5) and SIOX rev.C DCM site (JP6) correspondingly. External analog and digital I/O signals for installed SIOX rev.B/C DCM shall be connected by means of SIOX on-module I/O connector.

CAUTION

TORNADO-E6x on-board area for SIOX rev.B DCM is shared with the on-board area for SIOX rev.C DCM. Either SIOX rev.B DCM or SIOX rev.C can be installed onto *TORNADO-E6x* DSP controller mainboard.

TORNADO-E6202/E6203/E64xx on-board MXSIOX connector (JP19) is used for connection to external *T/SU-X1* SIOX rev.B mini-extender kit via *T/SU-X1/XC* flat cable. *T/SU-X1* SIOX rev.B mini-extender can be used for installation of one SIOX rev.B DCM.

Figure 2-14 shows installation examples of different SIOX DCM into the corresponding DCM sites on *TORNADO-E6x* mainboard.

Fig.2-14a. TORNADO-E6x mainboard with installed SIOX rev.B DCM.
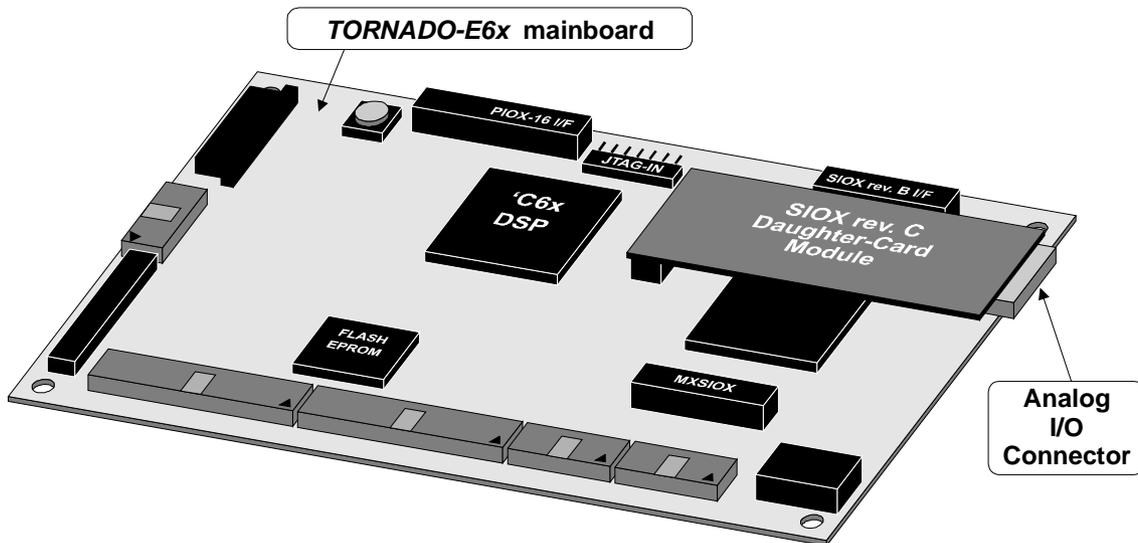
Fig.2-14b. TORNADO-E6x mainboard with installed SIOX rev.C DCM.
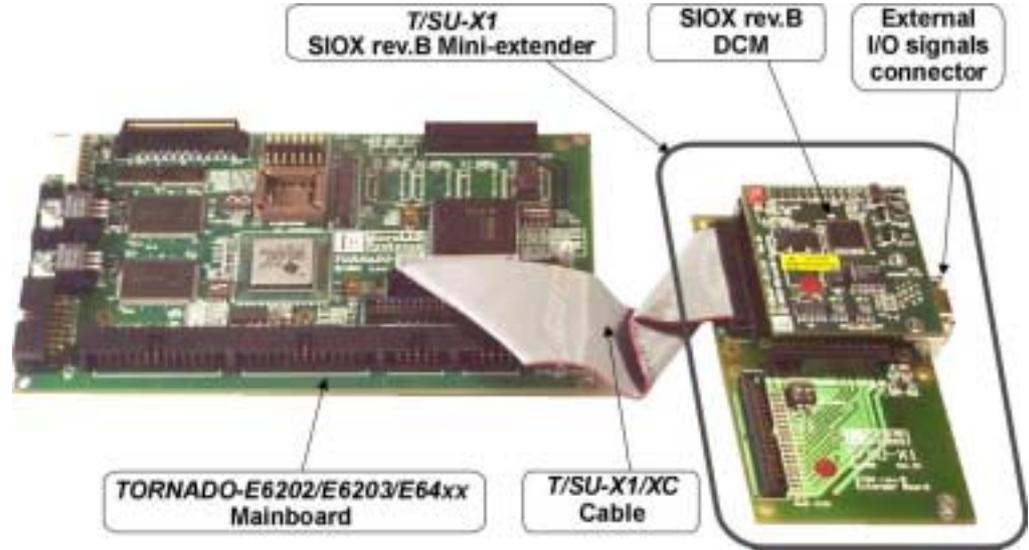
Fig.2-14c. TORNADO-E6202/E6203/E64xx mainboard with external *T/SU-X1* mini-extender with installed SIOX rev.B DCM.

SIOX rev.B site connector

TORNADO-E6x on-board SIOX rev.B DCM site connector (JP5) is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. Mating plug is the industry standard 26-pin dual-row male header with 0.1"x0.1" pin pattern, which is available from virtually all connector manufacturers.

SIOX rev.B DCM site connector pinout is shown at figure 2-15 and signal specifications are presented in table 2-17.
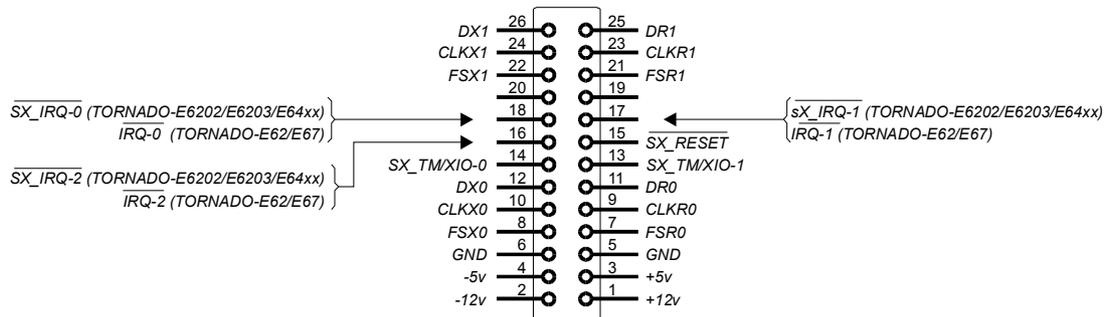
Fig.2-15. SIOX rev.B DCM site connector pinout (top view).

Table 2-17.   Signal description for SIOX rev.B DCM site connector.

SIOX signal name	signal type	description
SIO-0 port control		
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX site. For SIOX site of *TORNADO-E6x* DSP controllers these signals correspond to the TMS320C6x DSP on-chip McBSP-0 serial port transmitter and are wired directly to its pins.
DR0 FSR0 CLKR0	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX site. For SIOX site of *TORNADO-E6x* DSP controllers these signals correspond to the TMS320C6x DSP on-chip McBSP-0 serial port receiver and are wired directly to its pins.
SIO-1 port control		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX site. For SIOX site of *TORNADO-E6x* DSP controllers these signals correspond to the TMS320C6x DSP on-chip McBSP-1 serial port transmitter and are wired directly to its pins.
DR1 FSR1 CLKR1	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX site. For SIOX site of *TORNADO-E6x* DSP controllers these signals correspond to the TMS320C6x DSP on-chip McBSP-1 serial port receiver and are wired directly to its pins.
Timers, Reset and Interrupt Requests		
SX_TM/XIO-0 SX_TM/XIO-1	I/O/Z	SIOX timer or I/O pins, which are connected to the corresponding TMS320C6x DSP on-chip timer pins (TOUT0/TINP0 and TOUT1/TINP1) (refer to fig.2-1). Each of these pins can be used as timer input, timer output, or general purpose I/O pin (refer to fig.2-5 and TI TMS320C6x documentation for more details).
$\overline{SX\_RESET}$	O	Active low reset signal for on-board SIOX rev.B/C DCM sites, which is controlled via *SX-A_RESET* bit of *PXSX_RESET_RG* I/O control register (refer to table 2-2 and section 2.2 for more details).

$\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, $\overline{IRQ\text{-}2}$ (TORNADO-E62/E67) or $\overline{SX\_IRQ\text{-}0}$, $\overline{SX\_IRQ\text{-}1}$ $\overline{SX\_IRQ\text{-}2}$ (TORNADO-E6202/E6203/E64xx)	I	Active low pulled-up external interrupt requests from SIOX rev.B/C DCM sites and MXSIOX connector. If enabled, DSP interrupts are generated on the falling edge of these interrupt request inputs. *TORNADO-E62/E67* DSP controllers use $\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, and $\overline{IRQ\text{-}2}$ interrupt request inputs from SIOX rev.B/C DCM sites, which are shared with the corresponding interrupt request inputs of on-board PIOX-16 DCM site. $\overline{IRQ\text{-}0}$ and $\overline{IRQ\text{-}1}$ are connected directly to *EXT_INT4* and *EXT_INT5* external interrupt requests of TMS320C6x DSP. $\overline{IRQ\text{-}2}$ can be configured by DSP software to connect to any of *EXT_INT6* and *EXT_INT7* external interrupt requests of TMS320C6201/C6701 DSP (refer to section 2-2 and tables 2-7 and 2-8 for more details). *TORNADO-E6202/E6203/E64xx* DSP controllers feature dedicated $\overline{SX\_IRQ\text{-}0}$, $\overline{SX\_IRQ\text{-}1}$, and $\overline{SX\_IRQ\text{-}2}$ interrupt request inputs from SIOX rev.B/C and MXSIOX DCM sites, which are not shared with interrupt requests of on-board PIOX-16 DCM site ($\overline{PX\_IRQ\text{-}0}$, $\overline{PX\_IRQ\text{-}1}$, $\overline{PX\_IRQ\text{-}2}$, and $\overline{PX\_IRQ\text{-}3}$), and can be configured by DSP software to connect to any of *EXT_INT4..7* and *NMI* external interrupt requests of TMS320C6202/C6203/C64xx DSP (refer to section 2-2 and tables 2-7 and 2-8 for more details).
Power Supplies		
GND		Ground.
+5v		+5v power (from on-board JP1 power input connector).
+12v		+12v power (from on-board JP1 power input connector).
-5v		-5v power (from on-board JP1 power input connector).
-12v		-12v power (from on-board JP1 power input connector).

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
1. All logical signal levels and load currents correspond to that for 3v/5v CMOS/TTL signals.

SIOX rev.C site connector

TORNADO-E6x on-board SIOX rev.C DCM site connector (JP6) is a high-density dual-row 40-pin female header with 0.05"x0.05" pin pattern from Samtec Inc (www.samtec.com). Compatible SIOX rev.C plugs (Samtec p/n TFM-120-22-S-D-LC) for design of custom SIOX rev.B DCM are available from MicroLAB Systems upon request.

SIOX rev.C DCM site connector pinout is shown at figure 2-16 and signal specifications are presented in table 2-18.
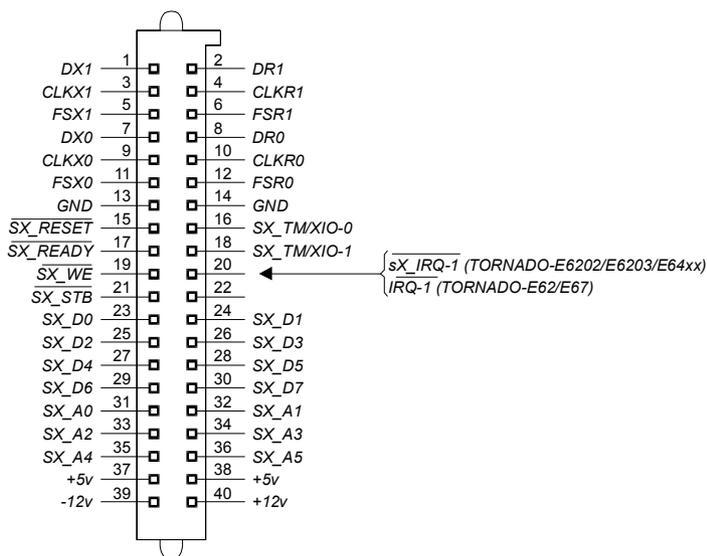
Fig.2-16.   SIOX rev.C DCM site connector pinout (top view).

Table 2-18.   Signal description for SIOX rev.C DCM site connector.

SIOX rev.B connector pin	signal type	description
SIO-0 port control		
DX0 FSX0 CLKX0	O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX site. For SIOX site of *TORNADO-E6x* DSP controllers these signals correspond to the TMS320C6x DSP on-chip McBSP-0 serial port transmitter and are wired directly to its pins.
DR0 FSR0 CLKR0	I I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX site. For SIOX site of *TORNADO-E6x* DSP controllers these signals correspond to the TMS320C6x DSP on-chip McBSP-0 serial port receiver and are wired directly to its pins.
SIO-1 port control		
DX1 FSX1 CLKX1	O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX site. For SIOX site of *TORNADO-E6x* DSP controllers these signals correspond to the TMS320C6x DSP on-chip McBSP-1 serial port transmitter and are wired directly to its pins.
DR1 FSR1 CLKR1	I I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX site. For SIOX site of *TORNADO-E6x* DSP controllers these signals correspond to the TMS320C6x DSP on-chip McBSP-1 serial port receiver and are wired directly to its pins.

DSP Timers, Reset and Interrupt Requests		
SX_TM/XIO-0 *SX_TM/XIO-1*	I/O/Z	SIOX timer or I/O pins, which are connected to the corresponding TMS320C6x DSP on-chip timer pins (TOUT0/TINP0 and TOUT1/TINP1) (refer to fig.2-1). Each of these pins can be used as timer input, timer output, or general purpose I/O pin (refer to fig.2-5 and TI TMS320C6x documentation for more details).
$\overline{SX\_RESET}$	O	Active low reset signal for on-board SIOX rev.B/C DCM sites, which is controlled via *SX-A_RESET* bit of *PXSX_RESET_RG* I/O control register (refer to table 2-2 and section 2.2 for more details).
$\overline{IRQ\text{-}0}$ (TORNADO-E62/E67) $\overline{SX\_IRQ\text{-}0}$ (TORNADO-E6202/E6203/E64xx)	I	Active low pulled-up external interrupt request input from SIOX rev.B/C DCM sites. If enabled, DSP interrupt is generated on the falling edge of this interrupt request input. *TORNADO-E62/E67* DSP controllers use $\overline{IRQ\text{-}0}$ interrupt request inputs from SIOX rev.B/C DCM sites, which is shared with the corresponding interrupt request input of on-board PIOX-16 DCM site. $\overline{IRQ\text{-}0}$ is connected directly to *EXT_INT4* external interrupt request of TMS320C6201/C6701 DSP (refer to section 2-2 and tables 2-7 and 2-8 for more details). *TORNADO-E6202/E6203/E64xx* DSP controllers feature dedicated $\overline{SX\_IRQ\text{-}0}$ interrupt request input from SIOX rev.B/C DCM site, which is not shared with interrupt requests of on-board PIOX-16 DCM site ($\overline{PX\_IRQ\text{-}0}$, $\overline{PX\_IRQ\text{-}1}$, $\overline{PX\_IRQ\text{-}2}$, and $\overline{PX\_IRQ\text{-}3}$), and can be configured by DSP software to connect to any of *EXT_INT4..7* and *NMI* external interrupt requests of TMS320C6202/C6203/C64xx DSP (refer to section 2-2 and tables 2-7 and 2-8 for more details).
Parallel Data Bus		
SX_A[0..5]	O	SIOX rev.C interface parallel address bus, which is connected to A2..A7 address bus of on-board TMS320C620x/C6701 DSP for *TORNADO-E62xx/E67* DSP and to EMIF-B A1..A6 address bus of on-board TMS320C64xx DSP for *TORNADO-E64xx* DSP controllers.
SX_D[0..7]	I/O	SIOX rev.C interface parallel data bus, which is connected to D0..D7 data bus of on-board TMS320C620x/C6701 DSP for *TORNADO-E62xx/E67* DSP controllers and to EMIF-B D0..D7 data bus of on-board TMS320C64xx DSP for *TORNADO-E64xx* DSP controllers.
$\overline{SX\_STB}$	O	Active low data SIOX rev.C interface data transfer strobe, which is generated when *TORNADO-E6x* on-board CU when DSP performs access to the SIOX rev.C sub-area of EMIF CE-3 address area in accordance with table 2-2.
$\overline{SX\_WE}$	O	Active low write enable signal.
$\overline{SX\_READY}$	I	Active low pulled-up SIOX rev.C parallel data ready signal. This signal must be generated by installed SIOX rev.C DCM in order to terminate current data transfer cycle and meet timing requirements of memory and I/O devices used in particular SIOX rev.C module.

Power Supplies		
GND		Ground.
+5v		+5v power (from on-board JP1 power input connector).
+12v		+12v power (from on-board JP1 power input connector).
-12v		-12v power (from on-board JP1 power input connector).

Note: 1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
          2. All logical signal levels and load currents correspond to that for 3v/5v CMOS/TTL logic.

MXSIOX connector pinout and signal description for TORNADO-E6202/E6203

MXSIOX connector (JP19) can be used for connection to external *T/SU-X1* SIOX rev.B DCM mini-extender kit (refer to Appendix B) and is available for *TORNADO-E6202/E6203/E64xx* DSP controllers only with TMS320C6202/C6203/C64xx DSP, which provides three DSP on-chip McBSP ports. *T/SU-X1* SIOX rev.B DCM mini-extender kit can be used for installation of one SIOX rev.B DCM, therefore signal specifications for MXSIOX connector are the same as that for SIOX rev.B DCM site.

TORNADO-E6202/E6203/E64xx on-board MXSIOX connector 34-pin dual-row 2mm guarded male headers from Samtec Inc (www.samtec.com). Compatible MXSIOX plug (Samtec p/n TCSD-17-01-N) comes standard with *T/SU-X1/XC* SIOX rev.B mini-extender connection cables (refer to Appendix B for more details), whereas optional MXSIOX plugs for 2mm flat cables are available either from Samtec Inc or from MicroLAB Systems upon request.

Connector pinout for *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector is shown at figure 2-14 and signal specifications are presented in table 2-19.

|			
GND	34	33	DX1
GND	32	31	CLKX1
GND	30	29	FSX1
GND	28	27	DR1
GND	26	25	CLKR1
GND	24	23	FSR1
GND	22	21	DX0
GND	20	19	CLKX0
GND	18	17	FSX0
GND	16	15	DR0
GND	14	13	CLKR0
GND	12	11	FSR0
+5v	10	9	SX_TM/XIO-1
+5v	8	7	SX_TM/XIO-0
+12v	6	5	MX_RESET
-5v	4	3	SX_IRQ-2
-12v	2	1	SX_IRQ-1
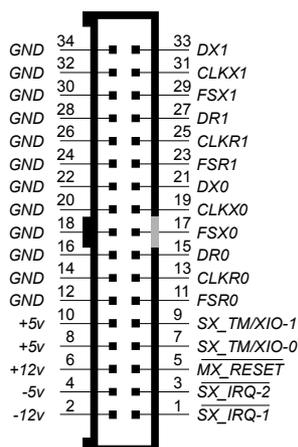
Fig.2-17. Pinout for *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector (top view).

Table 2-19. Signal description for *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector.

SIOX rev.B interface signal	signal type	Description
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port. For MXSIOX connector of *TORNADO-E6202/E6203/E64xx* DSP controllers these signals correspond to the TMS320C6202/C6203/C64xx DSP on-chip McBSP-2 serial port transmitter.
DR0 FSR0 CLKR0	I I I	Data, frame synchronization and serial clock signals for receiver of SIO-0 port. For MXSIOX connector of *TORNADO-E6202/E6203/E64xx* DSP controllers these signals correspond to the TMS320C6202/C6203/C64xx DSP on-chip McBSP-2 serial port receiver.
SIO-1 port control		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port. For MXSIOX connector of *TORNADO-E6202/E6203/E64xx* DSP controllers these signals correspond to the TMS320C6202/C6203/C64xx DSP on-chip McBSP-1 serial port transmitter.
DR1 FSR1 CLKR1	I I/O I	Data, frame synchronization and serial clock signals for receiver of SIO-1 port. For MXSIOX connector of *TORNADO-E6202/E6203/E64xx* DSP controllers these signals correspond to the TMS320C6202/C6203/C64xx DSP on-chip McBSP-1 serial port receiver.
Timer/IO, Reset and Interrupt Requests		
SX_TM/XIO-0 SX_TM/XIO-1	I/O	Timer or I/O pins, which are connected to the corresponding TMS320C6x DSP on-chip timer pins (TOUT0/TINP0 and TOUT1/TINP1) (refer to fig.2-1). Each of these pins can be used as timer input, timer output, or general purpose I/O pin (refer to fig.2-5 and TI TMS320C6x documentation for more details).
$\overline{MX\_RESET}$	O	Active low reset signal for on-board MXSIOX connector, which is controlled via *SX-B_RESET* bit of *PXSX_RESET_RG* I/O control register (refer to table 2-6 and section 2.2 for more details).
$\overline{SX\_IRQ\text{-}1}$ $\overline{SX\_IRQ\text{-}2}$	I	Active low pulled-up external interrupt requests from SIOX rev.B/C DCM sites and MXSIOX connector. If enabled, DSP interrupts are generated on the falling edge of these interrupt request inputs. *TORNADO-E6202/E6203/E64xx* DSP controllers connect $\overline{SX\_IRQ\text{-}1}$ and $\overline{SX\_IRQ\text{-}2}$ interrupt request inputs of MXSIOX connector to the corresponding dedicated interrupt request inputs of SIOX rev.B/C DCM sites. $\overline{SX\_IRQ\text{-}1}$ and $\overline{SX\_IRQ\text{-}2}$ interrupt request inputs can be configured by DSP software to connect to any of the *EXT_INT4..7* and *NMI* external interrupt requests of on-board TMS320C6202/C6203/C64xx DSP (refer to section 2-2 and tables 2-7 and 2-8 for more details).

Power Supplies		
GND		Ground.
+5v		+5v power (from on-board JP1 power input connector).
+12v		+12v power (from on-board JP1 power input connector).
-5v		-5v power (from on-board JP1 power input connector).
-12v		-12v power (from on-board JP1 power input connector).

Note: 1.   Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
          2.   All logical signal levels and load currents correspond to that for 3v/5v CMOS signals.

Maximum serial clock frequency for MXSIOX connector and T/SU-X1 SIOX rev.B mini-extender kit for TORNADO-E6202/E6203/E64xx

Although maximum theoretical output serial clock frequency for McBSP serial ports of *TORNADO-E6x* DSP controllers is 250 MHz for *TORNADO-E6202* DSP controllers, 300 MHz *TORNADO-E6203* for DSP controllers, and either 500 MHz or 600 MHz for *TORNADO-E64xx* for DSP controllers, actual maximum serial clock frequency for SIO-0/1 serial ports of MXSIOX connector is limited by the length of connection cables, which are used for connection to external *T/SU-X1* SIOX rev.B mini-extender, and particular by serial clock distribution configuration for installed SIOX rev.B DCM.

CAUTION

In case standard 10" long (0.25m) cable is used for connection of external *T/SU-X1* SIOX rev.B mini-extender to *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector, and the corresponding *TORNADO-E6202/E6203/E64xx* on-board SW6-1 and SW6-2 common serial clock enable switches are set to the 'OFF' state (refer to the corresponding subsection below for more details) , then the recommended maximum serial clock frequency for CLKX/CLKR signals for SIO-0/1 serial ports of MXSIOX connector is 33 MHz.

CAUTION

In case standard 10" long (0.25m) cable is used for connection of external *T/SU-X1* SIOX
rev.B mini-extender to *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector, and
the corresponding *TORNADO-E6202/E6203/E64xx* on-board SW6-1 and SW6-2 common
serial clock enable switches are set to the 'ON' state (refer to the corresponding subsection
below for more details) , then the recommended maximum serial clock frequency for
CLKX/CLKR signals for SIO-0/1 serial ports of MXSIOX connector is 20 MHz.

Common CLKX/CLKR serial clock enable control for MXSIOX connector for TORNADO-E6202/E6203/E64xx

TORNADO-E6202/E6203/E64xx DSP controllers with on-board MXSIOX connector provide on-board SW6-1 and SW6-2 common CLKX/CLKR serial clock enable switches (refer to figures 2-2, 2-13b, 2-13c and A-1) for each of SIO-0 and SIO-1 MXSIOX serial ports correspondingly.

Table 2-20 presents available settings for on-board SW6-1 and SW6-2 common CLKX/CLKR serial clock enable switches for MXSIOX SIO-0 and SIO-1 serial ports.

Table 2-20a. Common serial clock enable switches settings for SIO-0 port of MXSIOX connector at *TORNADO-E6202/E6203/E64xx* DSP controllers.

SW6-1 switch	Description
OFF	Transmitter serial clock (CLKX) and receiver serial clock (CLKR) are disconnected for SIO-0 port of *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector.
ON	Transmitter serial clock (CLKX) and receiver serial clock (CLKR) are connected for SIO-0 port of *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector. This setting corresponds to reduced serial clock frequency and data transfer speed.

Note: 1.   Highlighted configuration corresponds to default factory setting.

Table 2-20b. Common serial clock enable switches settings for SIO-1 port of MXSIOX connector at *TORNADO-E6202/E6203/E64xx* DSP controllers.

SW6-2 switch	Description
OFF	Transmitter serial clock (CLKX) and receiver serial clock (CLKR) are disconnected for SIO-1 port of *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector.
ON	Transmitter serial clock (CLKX) and receiver serial clock (CLKR) are connected for SIO-1 port of *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector. This setting corresponds to reduced serial clock frequency and data transfer speed.

Note: 1.   Highlighted configuration corresponds to default factory setting.

CAUTION

TORNADO-E6202/E6203/E64xx on-board SW6-1 and SW6-2 common serial clock enable switches for MXSIOX connector shall be used in conjunction with *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switches (SW1 and SW2) in accordance with general guidelines provided in Appendix B of this manual and below in this subsection.

TORNADO-E6202/E6203/E64xx on-board SW6-1 and SW6-2 common serial clock enable switches for MXSIOX connector and *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) enable switches are used to compensate 'long-line' effect of serial clock signals distribution over connection flat cable between *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector and *T/SU-X1* SIOX rev.B mini-extender, which occurs due to the 'long-line wave nature' of connection flat cable.

Although the 'long-line' compensation resistors are being used for all MXSIOX SIO-0/1 serial port control signals (frame synchronization pulse, serial clock and serial data) at both *TORNADO-E6202/E6203/E64xx* DSP controller and *T/SU-X1* SIOX rev.B mini-extender boards in order to exclude signal reflection, a 'long-line' non-compensation for serial clock signals can still occur in case installed SIOX rev.B DCM is using common shorted serial clock for transmitter and receiver of SIO port (many SIOX rev.B DCM actually use this in order to simplify design). Note, that this problem does not occur with SIO port frame synchronization and serial data signals, since these signals always use dedicated lines of SIOX interface and can't be connected together.

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CAUTION

In case installed SIOX rev.B DCM, which is installed onto external T/SU-X1 SIOX rev.B mini-extender kit connected to *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector, has been designed without on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and each serial clock is using its dedicated pins, then the corresponding *TORNADO-E6202/E6203/E64xx* on-board common CLKX/CLKR serial clock enable switch (SW6-1 or SW6-2) must be set to 'OFF' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'ON'.

In case installed SIOX rev.B DCM, which is installed onto external T/SU-X1 SIOX rev.B mini-extender kit connected to *TORNADO-E6202/E6203/E64xx* on-board MXSIOX connector, has been designed with on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and both serial clocks are using shared pins, then the corresponding *TORNADO-E6202/E6203/E64xx* on-board common CLKX/CLKR serial clock enable switch (SW6-1 or SW6-2) must be set to 'ON' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'OFF'.

</div>

For more information about external *T/SU-X1* SIOX rev.B mini-extenders refer to Appendix B later in this manual.

External clocks for TMS320C6x DSP on-chip McBSP serial ports

TORNADO-E6x DSP controllers allow connection of external clock sources to the DSP on-chip McBSP serial ports. These clocks are known as CLKS-0, CLKS-1 and CLKS-2 (*TORNADO-E6202/E6203/E64xx* only) signals in accordance with TI TMS320C6x McBSP serial port specifications and correspond to TMS320C6x DSP on-chip McBSP-0, McBSP-1 and McBSP-2 (*TORNADO-E6202/E6203/E64xx* only) serial ports. External CLKS-0/1/2 clocks facility for the DSP on-chip McBSP-0/1/2 serial ports delivers outstanding flexibility in generation of virtually any data transfer frequency for the McBSP-0/1/2 serial ports in order to meet requirements of any application.

External clock source signals CLKS-0/1/2 for each of the McBSP-0/1/2 serial ports can be connected independently and are available from the following external sources:

- from external clock signals via JP8 on-board connector (for McBSP-0 serial port), JP9 on-board connector (for McBSP-1 serial port) and JP18 on-board connector (*TORNADO-E6202/E6203/E64xx* only, for McBSP-2 serial port) (refer to fig.2-2, 2-10, 2-18 and A-1)
- from on-board user installed 5v TTL/CMOS crystal oscillators (*TORNADO-E62xx/E67* only) in DIP-4 package and 0.3"x0.3" pin pattern (example: Epson SG-531 crystal oscillators), which can be installed into on-board S2 socket (for McBSP-0 serial port), on-board S3 socket (for McBSP-1 serial port), and on-board S5 socket (*TORNADO-E6202/E6203* only, for McBSP-2 serial port) (refer to fig.2-2, 2-13b, 2-18 and A-1).

Location and pinout for on-board JP8/JP9/JP18 connectors and on-board S2/S3/S5 oscillators sockets (*TORNADO-E62xx/E67* only) are shown at figure 2-18.
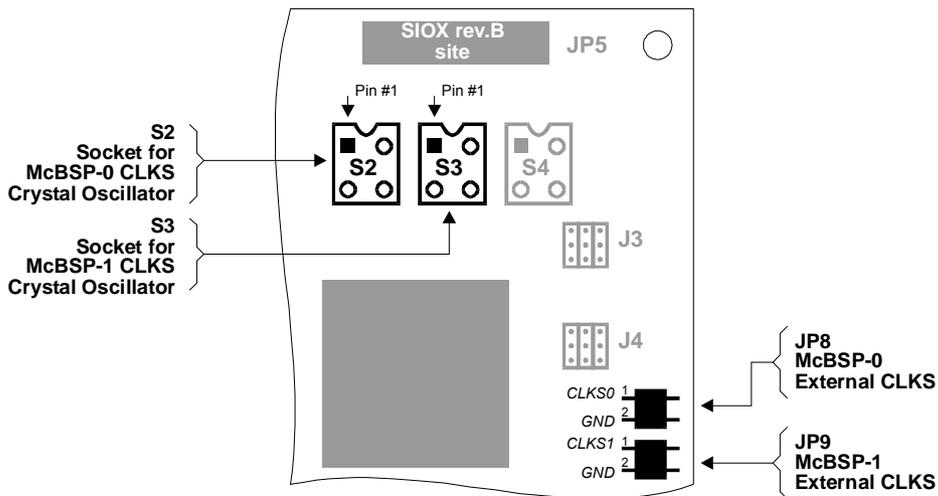
Fig. 2-18a.   McBSP-0/McBSP-1 External Clock Connectors and Crystal Oscillator Sites for
*TORNADO-E62/E67*.
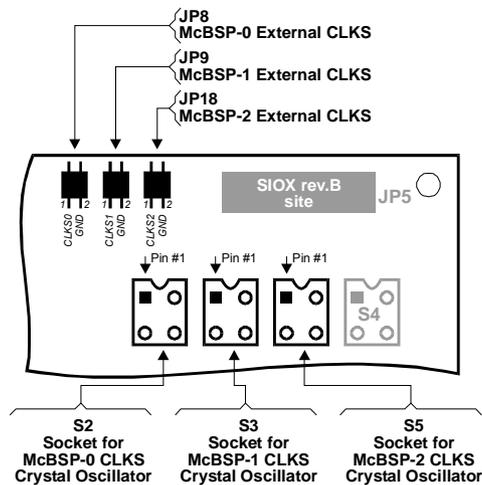
Fig. 2-18b.   McBSP-0/McBSP-1/McBSP-2 External Clock Connectors and Crystal Oscillator Sites for
*TORNADO-E6202/E6203*.
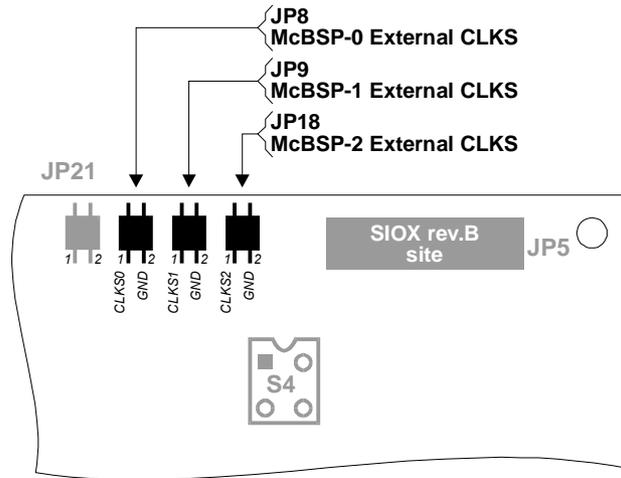
Fig. 2-18c. McBSP-0/McBSP-1/McBSP-2 External Clock Connectors for *TORNADO-E64xx*.

Selection of the CLKS-0/1/2 external source clock as the source clock for the McBSP-0/1/2 instead of DSP clock can be done by means of programming the DSP on-chip McBSP-0/1/2 control registers. Refer to original TI TMS320C6x documentation for getting more information on programming the McBSP serial ports.

Generating Reset Signal for SIOX DCM Sites and MXSIOX connector

TORNADO-E6x provide individual reset signal for on-board SIOX rev.B/C sites and on-bard MXSIOX connector, which is controlled by *SX-A_RESET* and *SX-B_RESET* bits of *PXSX_RESET_RG* I/O control register (refer to table 2-2 and section 2.2 for more details). *SX-A_RESET* bit of *PXSX_RESET_RG* I/O control register controls common reset signal for on-board SIOX rev.B/C sites, whereas *SX-B_RESET* bit of *PXSX_RESET_RG* I/O control register controls individual reset signal of MXSIOX connector (*TORNADO-E6202/E6203/E64xx* only).

Dedicated reset signals for on-board SIOX rev.B/C DCM sites and MXSIOX connector allows correct initialization of installed SIOX DCM hardware and correct synchronization with host *TORNADO-E6x* DSP software.

Accessing parallel data bus of SIOX rev.C interface from DSP software

8-bit parallel data bus of *TORNADO-E6x* on-board SIOX rev.C DCM interface can be accessed by on-board TMS320C6x DSP when addressing the corresponding external DSP memory area (refer to table 2-2 for addressing details).

CAUTION

For *TORNADO-E62xx/E67* DSP controllers, SIOX rev.C interface parallel data words are allocated as least significant bytes (bits D0..D7) of 32-bit data words of 64Kx32 sub-area of TMS320C62xx/C6701 DSP EMIF CE-3 area.

For *TORNADO-E62xx/E67* DSP controllers, SIOX rev.C interface parallel data words can be accessed using 8-bit, 16-bit and 32-bit DSP external data access cycles.

For *TORNADO-E62xx/E67* DSP controllers, the most significant D8..D31 data bits are ignored when writing to parallel data bus SIOX rev.C interface and are undefined when reading from parallel data bus SIOX rev.C interface.

CAUTION

For *TORNADO-E64xx* DSP controllers, SIOX rev.C interface parallel data words are allocated as least significant bytes (bits D0..D7) of 16-bit data words of 64Kx16 sub-area of TMS320C64xx DSP EMIF-B CE-0 area.

For *TORNADO-E64xx* DSP controllers, SIOX rev.C interface parallel data words can be accessed using 8-bit and 16-bit DSP external data access cycles.

For *TORNADO-E64xx* DSP controllers, the most significant D8..D15 data bits are ignored when writing to parallel data bus SIOX rev.C interface and are undefined when reading from parallel data bus SIOX rev.C interface.

CAUTION

TMS320C6x DSP on-chip EMIF Control Registers shall be configured in accordance with table 2-3 in order to meet requirements of *TORNADO-E6x* hardware for SIOX rev.C interface.

Parallel Data Transfer Timing for SIOX rev.C Site

Timing diagram for parallel data transfer via SIOX rev.C DCM site is presented at fig.2-19. This data transfer timing is known as the industry standard MOTO mode and assumes usage of data strobe signal and write enable signal.

> **CAUTION**
>
> Data transfer acknowledgement via parallel data bus of SIOX rev.C DCM interface is provided by installed SIOX rev.C DCM by means of asynchronous *SX_READY* signal.
>
> In case TMS320C6x DSP performs access to parallel data bus of SIOX rev.C -16 DCM interface while SIOX rev.C DCM is either not installed or does not utilize parallel data bus, then this results in missing *SX_READY* signal and infinite wait condition for *TORNADO-E6x* on-board TMS320C6x DSP.
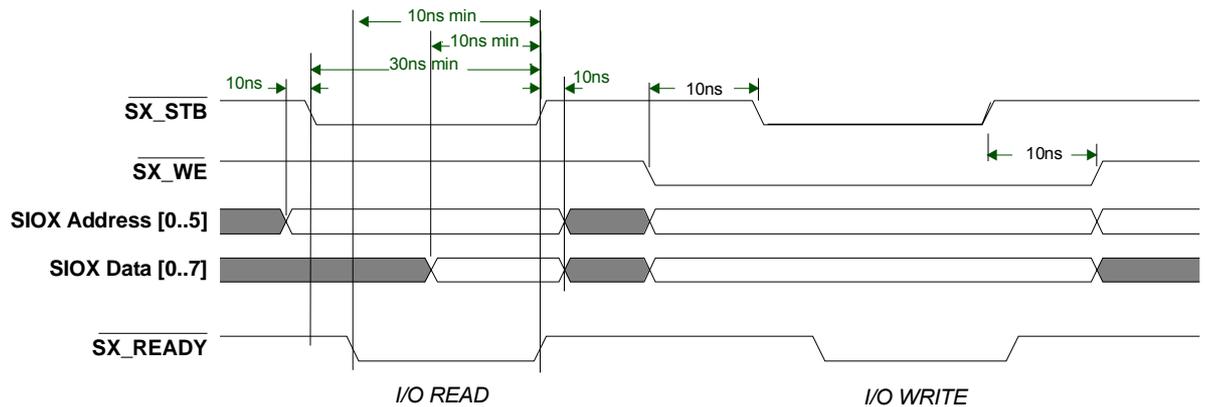
Fig.2-19. Timing diagram for parallel data transfer via SIOX rev.C DCM site.

Physical dimensions for SIOX DCM

Physical dimensions for SIOX rev.B and SIOX rev.C DCM are presented at fig.2-20. This information might be useful for those *TORNADO* customers, who need to design custom SIOX DCM.
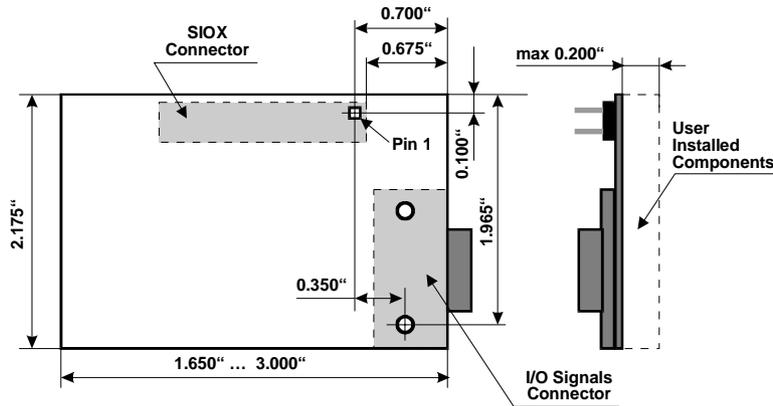
SIOX connector: 20-pin or 26-pin straight dual-row mail header
(0.025" Sq.,   0.1"x0.1" pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.2-20a.   Physical dimensions for SIOX rev.B DCM.
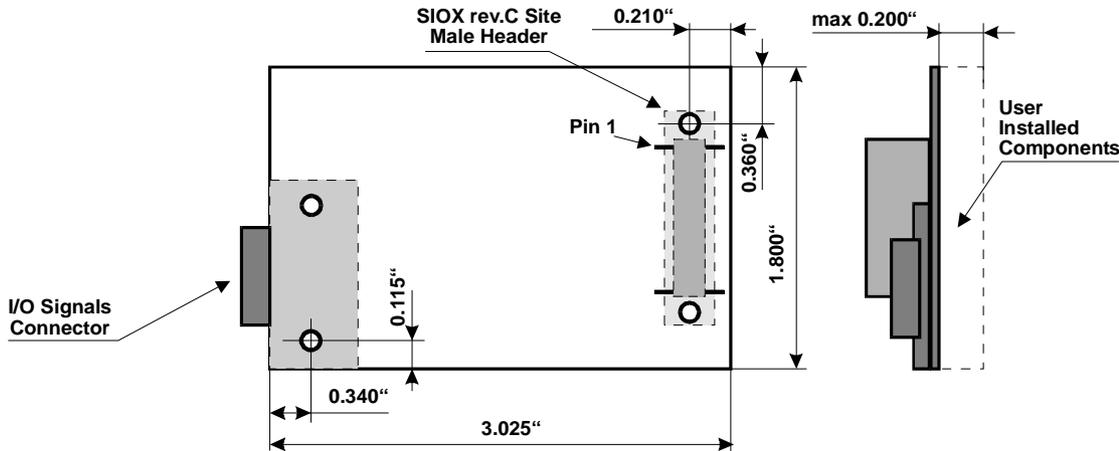
SIOX rev.C Site Male Header: SAMTEC TFM-120-22-S-D-LC

Recommended connector for Analog I/O: DDK DHA-RC26-R122N

Fig.2-20b.   Physical dimensions for SIOX rev.C DCM.

2.5   Dual-channel USART

TORNADO-E6x features the on-board dual-channel USART (universal synchronous/asynchronous receiver/transmitter) for communication with host computers, terminals, network adapters, or external peripherals using industry standard serial communication protocols.

TORNADO-E6x on-board dual-channel USART is the Infineon SAB 82532 chip (www.infineon.com), which supports industry standard synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) at up to 10 Mbit/s data transfer rate and the industry-standard asynchronous protocol (ASYNC) at up to 2.5 Mbaud. Protocol selection is performed independent for each channel.

Each channel of USART connects to external communication equipment via either RS232C or RS422/EIA-530 electrical interface. Selection of particular interface is performed by the on-board jumpers. RS232C interface provides communication at up to 115 kBaud and the RS422/EIA-530 interface provides up to 10 Mbit/s of data transfer rate. Transmitter and received clock outputs are also available via on-board connectors for external equipment, which might need to synchronize its data I/O rate to the USART clock.

USART also provides 8-bit of general purpose digital I/O (*DIO-0..7*), which is available via on-board JP10 connector. For details about on-board general purpose digital I/O refer to the corresponding section later in this chapter.

CAUTION

This databook does not contain detail information for architecture and programming of Infineon SAB 82532 USART.

For details about Infineon SAB 82532 USART refer to original manufacturer documentation, which is supplied in either electronic or paper form together with *TORNADO-E6x* board.

USART register set

SAB 82532 USART register set comprises of 128 8-bit registers totally for on-chip channels "A" and "B". SAB 82532 chip is extremely flexible programmable device with build-in FIFO for each of communication channel, PLL and system configuration registers.

USART is allocated in the EMIF CE-3 I/O area of on-board TMS320C6x DSP (refer to table 2-2). USART features 8-bit data bus, which is connected to the lowest significant byte of 32-bit DSP data bus. Therefore, the 8-bit USART registers are allocated at the x4 byte boundaries of 32-bit DSP data words.

USART-to-DSP interrupt

USART can generate interrupt request (*USART_IRQ*) to on-board TMS320C6x DSP via *EXT_INT6* and *EXT_INT7* external interrupt request inputs in accordance with the setting of *DSP_EXT_INT6_SEL_RG* and *DSP_EXT_INT6_SEL_RG* I/O control registers of *TORNADO-E6x* DSP controllers (refer to section 2.2 and tables 2-2 and 2-7 for more details). *TORNADO-E6202/E6203/E64xx* DSP controllers also allow to route USART interrupt request to *EXT_INT4*, *EXT_INT5* and *NMI* external interrupt requests of on-board TMS320C6x DSP, which are controlled via *DSP_EXT_INT4_SEL_RG*, *DSP_EXT_INT5_SEL_RG* and *DSP_NMI_SEL_RG* I/O control registers.

USART_IRQ interrupt is internal logical OR from many interrupt sources inside USART including the interrupt requests from parallel digital I/O port.

<div style="border: 2px solid black; padding: 10px;">

CAUTION

The interrupt request output of the SAB 82532 USART chip must be configured by the DSP software as "pushed-pulled" "active-low" output (refer to Infineon SAB 82532 USART documentation for how to configure the interrupt request output).

</div>

USART-hardware reset

USART hardware reset is performed simultaneously with the hardware reset for *TORNADO-E6x* board, and is actually the hardware reset signal for on-board TMS320C6x DSP, on-board I/O peripherals and I/O control registers.

Configuring external interfaces for USART

Each channel of USART connects to external devices via either RS232C or RS422/EIA-530 on-bard electrical interfaces.

Selection of electrical interface channel for channel 'A' of USART is performed by the on-board J3 jumpers set for *TORNADO-E62/E67* DSP controllers and by the on-board SW4-1..3 switches for *TORNADO-E6202/E6203/E64xx* DSP controllers in accordance with tables 2-21a and 2-21b.

Table 2-21a.   Configuration of external interfaces for channel "A" of USART for *TORNADO-E62/E67*.

Interface	interface connector on *TORNADO-E62/E67* board	jumper J3-A	jumper J3-B	jumper J3-C
RS422/EIA-530 (transmitter clock is generated by the USART on-chip clock generator and does not appear at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP13	2-3	1-2	2-3
RS422/EIA-530 (external transmitter clock is used from pins CLKX+/CLKX- RS422/EIA-530 connector)	JP13	2-3	1-2	1-2
RS422/EIA-530 (transmitter clock is generated by the USART on-chip clock generator and appears at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP13	2-3	2-3	2-3
RS232C	JP11	1-2	1-2	2-3

Notes: 1. The highlighted configuration corresponds to the factory settings.

Table 2-21b. Configuration of external interfaces for channel "A" of USART for *TORNADO-E6202/E6203/E64xx*.

Interface	interface connector on *TORNADO-E6202/E6203/E64xx* board	switch SW4-1	switch SW4-2	switch SW4-3
RS422/EIA-530 (transmitter clock is generated by the USART on-chip clock generator and does not appear at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP13	OFF	ON	OFF
RS422/EIA-530 (external transmitter clock is used from pins CLKX+/CLKX- RS422/EIA-530 connector)	JP13	OFF	ON	ON
RS422/EIA-530 (transmitter clock is generated by the USART on-chip clock generator and appears at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP13	OFF	OFF	OFF
RS232C	JP11	ON	ON	OFF

Notes: 1. Highlighted configuration corresponds to the factory settings.

Selection of electrical interface channel for channel 'B' of USART is performed by the on-board J4 jumpers set for *TORNADO-E62/E67* DSP controllers and by the on-board SW4-4..6 switches for *TORNADO-E6202/E6203/E64xx* DSP controllers in accordance with tables 2-22a and 2-22b.

Table 2-22a.   Configuration of external interfaces for channel "B" of USART for
TORNADO-E62/E67.

Interface	interface connector on *TORNADO-E62/E67* board	Jumper J4-A	jumper J4-B	jumper J4-C
RS422/EIA-530 (transmitter clock is generated by the USART on-chip clock generator and does not appear at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP14	2-3	1-2	2-3
RS422/EIA-530 (external transmitter clock is used from pins CLKX+/CLKX- RS422/EIA-530 connector)	JP14	2-3	1-2	1-2
RS422/EIA-530 (transmitter clock is generated by the USART on-chip clock generator and appears at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP14	2-3	2-3	2-3
RS232C	JP12	1-2	1-2	2-3

Notes: 1. The highlighted configuration corresponds to the factory settings.

Table 2-22b. Configuration of external interfaces for channel "B" of USART for *TORNADO-E6202/E6203/E64xx*.

Interface	interface connector on *TORNADO-E6202/E6203/E64xx* board	switch SW4-1	switch SW4-2	switch SW4-3
RS422/EIA-530 (transmitter clock is generated by the USART on-chip clock generator and does not appear at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP14	OFF	ON	OFF
RS422/EIA-530 (external transmitter clock is used from pins CLKX+/CLKX- RS422/EIA-530 connector)	JP14	OFF	ON	ON
RS422/EIA-530 (transmitter clock is generated by the USART on-chip clock generator and appears at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP14	OFF	OFF	OFF
RS232C	JP12	ON	ON	OFF

Notes: 1. Highlighted configuration corresponds to the factory settings.

RS232C interface connectors

RS232C interface assumes the single-ended bipolar I/O signals, provides communication at up to 115 kBaud and is designed for ASYNC asynchronous protocol of USART. RS232C interface is an industry standard interface for communication with personal computers, computer peripherals, industrial control devices, etc.

Pinout for *TORNADO-E6x* on-board RS232C interface connectors is presented at figure 2-21.
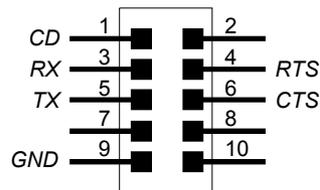
Fig. 2-21. RS232C interface connectors pinout for *TORNADO-E6x* (front view).

RS422/EIA-530 interface connectors

RS422/EIA-530 interface assumes differential unipolar I/O signals with 110 Ohm line terminators, provides communication at up to 10 Mbit/s, and is designed for all synchronous protocols. RS422/EIA-530 interface can be also used with ASYNC asynchronous protocol of USART delivering up to the 2.5 Mbaud of data transfer rate, however this solution is not standard. The RS422/EIA-530 interface is an industry standard electrical interface for communication with network equipment, high-speed computer peripherals, etc.

Pinout for *TORNADO-E6x* on-board RS422/EIA-530 interface connectors is presented at figure 2-22.
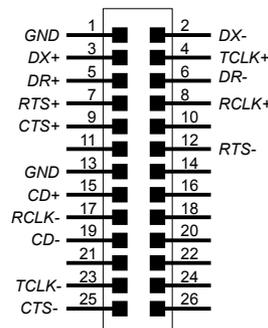
Fig. 2-22. RS422/EIA-530 interface connectors pinout for *TORNADO-E6x* (front view).

USART master source clock

TORNADO-E6x DSP controllers allow user to change frequency of USART master clock by means of simple replacement of crystal oscillator installed into on-board S4 socket (refer to fig.2-1, 2-2, 2-23 and A1).

USART master clock replacement feature makes *TORNADO-E6x* DSP controllers an extremely flexible tool and allows to set virtually any USART clock frequency value in order to meet any user application, which requires communication with external computers/peripherals at specific communication rates.

CAUTION

Maximum USART master clock frequency for *TORNADO-E6x* DSP controllers
is 10 MHz.

TORNADO-E6x DSP controllers are shipped from factory with default 1.8432 MHz USART master clock oscillator installed into on-board S4 socket. Different frequency value within the 1..10 MHz range for factory installed on-board USART master clock oscillator is available upon request from MicroLAB Systems.
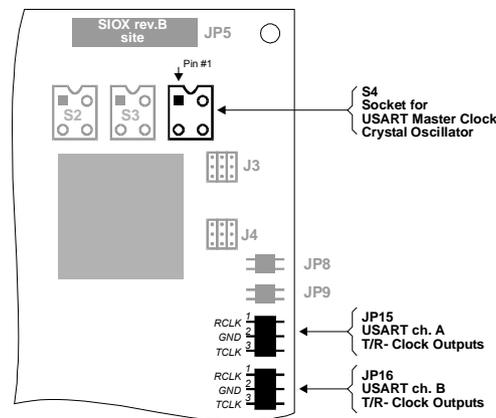
Fig. 2-23a. USART master clock oscillator site and transmitter/receiver clock output connectors for *TORNADO-E62/E67*.
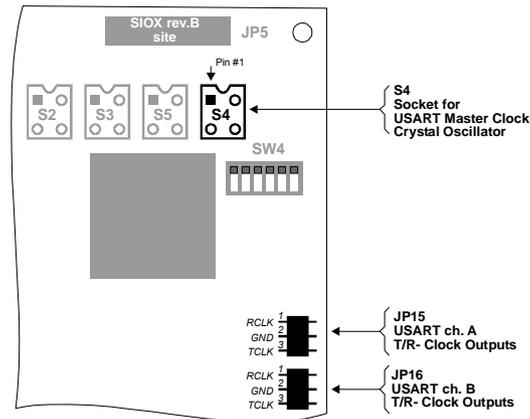
Fig. 2-23b.   USART master clock oscillator site and transmitter/receiver clock output connectors for
TORNADO-E6202/E6203.
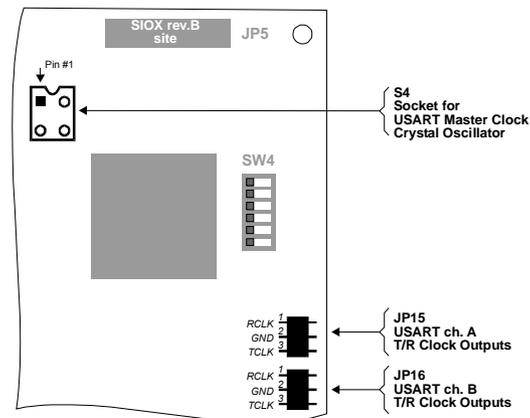
Fig. 2-23c.   USART master clock oscillator site and transmitter/receiver clock output connectors for
TORNADO-E64xx.

TORNADO-E6x on-board S4 socket for USART master clock oscillator allows to install 5v TTL/CMOS crystal oscillators in DIP-4 package and 0.3"x0.3" pin pattern (example: Epson SG-531 crystal oscillators). Pinout for S4 socket is shown at figures 2-23.

USART transmitter/receiver output clocks

TORNADO-E6x provides optional on-board USART transmitter/receiver clocks output connectors separately for each of USART channels "A" and "B" (JP15 and JP16 on-board connectors correspondingly at fig.2-2, 2-23 and A-1) in order to allow external AD/DA or I/O equipment to synchronize its data sampling clock with

USART transmitter and receiver clocks. This feature is useful, for example, for satellite modems, which provide external synchronous communication from one side and AD/DA from the other side.

TORNADO-E6x on-board connectors for USART transmitter/receiver clock outputs are the industry standard 0.05" 3-pin male headers from Molex (www.molex.com). The mating plugs are available upon request from MicroLAB Systems. Pinout for on-board USART transmitter/receiver clock output connectors is shown at fig 2-23. The output USART transmitter/receiver clock signals are 5v CMOS/TTL compatible.

2.6 General Purpose I/O

All *TORNADO-E6x* DSP controllers provide 8-bit of general purpose digital I/O signals (*DIO-0..7*), which are wired to on-board JP10 connector (refer to fig.2-2 and fig.A-1). *TORNADO-E64xx* DSP controllers also add extra 10-bit of DSP general purpose digital I/O signals (*DSP_GPIO-0/3/8..15*), which are wired to on-board JP20 connector (refer to fig.2-2c and fig.A-1).

General purpose digital I/O is useful for interfacing to external sensors, switches, etc and for generation of local control signals in a variety of applications.

General purpose I/O connectors

Pinout for JP10 general purpose I/O connector and for JP20 DSP general purpose I/O connector (*TORNADO-E64xx* only) are presented at fig.2-24.
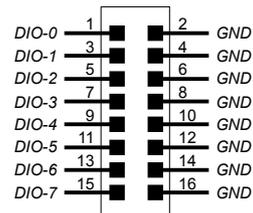
Fig.2-24a. Pinout for JP10 general purpose I/O connector for *TORNADO-E6x* (front view).
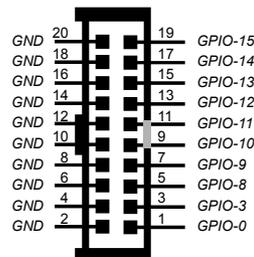

Fig.2-24b. Pinout for JP20 DSP general purpose I/O connector for *TORNADO-E64xx* (top view).

TORNADO-E6x on-board JP10 general purpose I/O connector is the industry-standard 16-pin 0.1"x0.1" guarded male headers. The mating 16-pin 0.1"x0.1" flat cable female plugs and solder ed-in female headers are available from a variety of manufacturers (AMP, Molex, 3M, etc).

TORNADO-E64xx on-board JP20 DSP general purpose I/O connector is Samtec STMM-110-02-G-D 30-pin 2mm guarded male headers. The mating parts are Samtec TCSD-10-01-N female plugs for 2mm 20-wire flat cable, which are included as standard option with *TORNADO-E64xx* DSP controllers. Extra DSP general purpose I/O plugs are available either from Samtec Inc (www.samtec.com) or from MicroLAB Systems upon request.

DIO-0..7 general purpose I/O

DIO-0..7 general purpose digital I/O signals present in all *TORNADO-E6x* DSP controllers and are available via on-board JP10 connector. *DIO-0..7* signals are programmable I/O pins of the on-board SAB 82532 USART.

> **CAUTION**
>
> For details about Infineon SAB 82532 USART on-chip general purpose I/O refer to original manufacturer documentation, which is supplied in either electronic or paper form together with *TORNADO-E6x* board.

DIO-0..7 general purpose digital I/O signals are TTL 5v compatible signals with I_{OL}=2mA and I_{OH}=0.4mA load current.

Each of the *DIO-0..7* general purpose digital I/O lines allows individual programming of direction and masking of USART interrupt, which might be generated on the user programmable input signal edge.

DSP_GPIO-0/3/8..15 DSP general purpose I/O (TORNADO-E64xx only)

DSP_GPIO-0/3/8..15 DSP general purpose digital I/O signals are available in *TORNADO-E64xx* DSP controllers only via on-board JP20 connector. *DSP_GPIO-0/3/8..15* signals are actually the corresponding general purpose I/O pins of TMS320C64xx DSP, which are controlled via TMS320C64xx DSP on-chip GPEN, GPDIR, GPVAL, GPDL, GPDH, GPHM, GPLM, GPGC, and GPPOL registers.

> **CAUTION**
>
> For details about TMS320C64xx DSP on-chip general purpose I/O pins refer to original TI TMS320C6x DSP documentation, which is supplied in either electronic or paper form together with *TORNADO-E6x* board.

> **CAUTION**
>
> *TORNADO-64xx* on-board TMS320C64xx DSP provide only *DSP_GPIO-0*, *DSP_GPIO-3*, and *DSP_GPIO-8..15* DSP on-chip general purpose I/O signals available for external I/O via on-board JP20 connector.
>
> Other TMS320C64xx DSP on-chip general purpose I/O are reserved and shall not be configured as general purpose I/O pins via TMS320C64xx DSP on-chip GPEN register.

DSP_GPIO-0/3/8..15 DSP general purpose I/O signals are TTL 3v/5v compatible signals with I_L=3.2mA load current.

DSP_GPIO-0/3/8..15 DSP general purpose I/O signals can be used for general purpose I/O, generation of DSP interrupt, and EDMA events.

2.7 USB Device Interface

TORNADO-E6x features the on-board 12 Mbit/s USB device interface for communication with host computers.

USB device interface is based around the Agere Systems (www.agere.com) USS-820/USS-825 chip and supports the industry USB protocol at up to 12 Mbit/s data transfer rate. On-board USB connector (JP17) is the USB type 'B' device connector. USB device controller and external interface meets USB rev.1.1 specifications.

> **CAUTION**
>
> The on-board USS-820/USS-825 USB device controller is sourced from 12 MHz clock, which allows full-speed 12 Mbit/s communication over the USB bus.

USB interface connector

TORNADO-E6x on-board USB device connector is the industry standard USB type 'B' receptacle with pinout presented ate figure 2-25. The mating plug is the USB device plug available on all host-to-device USB cables.
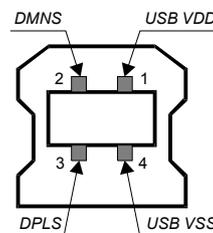

Fig. 2-25. Pinout of USB device connector for *TORNADO-E6x* (front view).

Accessing USB controller from DSP software

For *TORNADO-E62xx/E67* DSP controllers, USB device controller is allocated in the sub-area of EMIF CE-3 I/O area of the on-board TMS320C6x DSP (refer to table 2-2). USB device controller features 8-bit data bus, which is connected to the lowest significant byte of 32-bit DSP data bus. Therefore, the 8-bit USB controller on-chip registers are allocated at the x4 byte boundaries of 32-bit DSP data.

For *TORNADO-E64xx* DSP controllers, USB device controller is allocated in the sub-area of EMIF-B CE-0 I/O area of the on-board TMS320C6x DSP (refer to table 2-2). USB device controller features 8-bit data bus, which is connected to the lowest significant byte of 16-bit EMIF-B DSP data bus. Therefore, the 8-bit USB controller on-chip registers are allocated at the x2 byte boundaries of 16-bit EMIF-B DSP data words.

USB register set

USS-820/USS-825 USB device controller register set comprises of 32 8-bit registers. USS-820/USS-825 USB controller is extremely flexible programmable device with build-in programmable FIFO for transmitter and receiver, dual-packet support, support for 16 USB endpoints, integrated USB transceivers, and many more features.

CAUTION

For details about Agere Systems USS-820/USS-825 USB device controller refer to original manufacturer documentation, which is supplied in either electronic or paper form together with *TORNADO-E6x* board.

CAUTION

The DPPU output pin of on-board USS-820/USS-825 USB device controller is connected to the on-board hardware, which allows simulation of the USB device disconnect.

In order to activate presence of the USS-820/USS-825 USB device controller on host USB bus, the DPPU output must be set to logical '1' value via the DPEN bit of MCSR register of USS-820/USS-825 USB device controller.

USB-to-DSP interrupt

USB controller can generate interrupt request (*USB_IRQ*) to on-board TMS320C6x DSP via *EXT_INT6* and *EXT_INT7* external interrupt request inputs in accordance with the setting of *DSP_EXT_INT6_SEL_RG* and *DSP_EXT_INT6_SEL_RG* I/O control registers of *TORNADO-E6x* DSP controllers (refer to section 2.2 and tables 2-2 and 2-7 for more details). *TORNADO-E6202/E6203/E64xx* DSP controllers also allow to route USB controller interrupt request to *EXT_INT4*, *EXT_INT5* and *NMI* external interrupt requests of on-board TMS320C6x DSP, which are controlled via *DSP_EXT_INT4_SEL_RG*, *DSP_EXT_INT5_SEL_RG* and *DSP_NMI_SEL_RG* I/O control registers.

The USB controller interrupt is internal logical OR from many interrupt sources inside USART including the interrupt requests from parallel digital I/O port.

CAUTION

The interrupt request output of the Agere Systems USS-820/USS-825 USB device controller chip must be configured by the DSP software as "active-low" output (refer to USS-820/USS-825 USB controller documentation for how to configure the interrupt request output).

Hardware reset for USB controller

Hardware reset for USB controller is performed simultaneously with the hardware reset for *TORNADO-E6x* board, and is actually the hardware reset signal for on-board TMS320C6x DSP, on-board I/O peripherals and I/O control registers.

2.8   Real-time Clock (RTC) Controller of *TORNADO-E64xx*

TORNADO-E64xx DSP controllers provide on-board real-time clock (RTC) controller with battery back-up clock, '2100 year calendar, programmable alarm and WDT features, and user NvRAM. RTC can be used in those DSP applications, which require accurate time-of-day, date and year keeping, programmable alarm events, short system restore latency using WDT after probable system crash, and non-volatile RAM for run-time application parameters and variables.

TORNADO-E64xx on-board RTC controller is based around the Dallas Semiconductor (www.dalsemi.com) DS1284 timekeeper chip with external backup battery.

RTC power backup battery

TORNADO-E64xx DSP controllers provide on-board BT1 socket (fig.2-26, fig.2-2c and A-1c) for external RTC power backup battery, which is used to automatically write protect internal RTC contents and keep real-time clock running in case on-board +5v power will get out of tolerance.
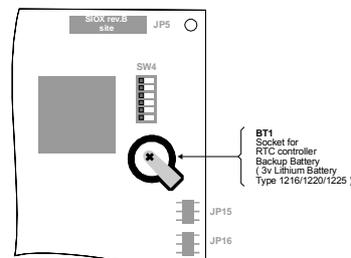

Fig.2-26.   RTC controller power backup battery socket at *TORNADO-E64xx* board.

TORNADO-E64xx DSP controllers have been designed to use 3V lithium battery (type 1216, 1228, or 1225) as external RTC power backup battery, which plugs directly into on-board BT1 socket. Typically, new Duracell 3V lithium type 1216 battery will safely maintain RTC on-chip data within 2..3 years.

> **CAUTION**
>
> Installation of other than 3V lithium battery type 1216/1228/1225 is prohibited and can result in damage of *TORNADO-E64xx* on-board hardware.

Accessing RTC controller from DSP software

TORNADO-E64xx on-board RTC controller is allocated in the sub-area of EMIF-B CE-0 I/O area of the on-board TMS320C6x DSP (refer to table 2-2). RTC device controller features 8-bit data bus, which is connected to the lowest significant byte of 16-bit EMIF-B DSP data bus. Therefore, the 8-bit RTC controller on-chip registers are allocated at the x2 byte boundaries of 16-bit EMIF-B DSP data words.

TORNADO-E64xx DSP controller provides software controlled on-board hardware resources, which are used to enable/disable access to on-board RTC controller in order to exclude accidental RTC accesses and to increase RTC data integrity. For example, accidental RTC accesses can occur either when DSP boots in *NO-BMODE* and there is no valid DSP code in DSP memory, or in case of DSP malfunction, which can set DSP program counter to invalid area. *RTC_ACCESS_EN* bit of *WDT_EN_RG* register of *TORNADO-E64xx* DSP controllers is used to enable/disable access to on-board RTC controller from DSP application. *RTC_ACCESS_EN* bit defaults to the '0' state on DSP power on and disables access to RTC controller until *RTC_ACCESS_EN* bit will be set to the '1' state by DSP application.

RTC register set

DS1284 RTC controller register set comprises of 64 8-bit registers, which includes registers for clock, calendar, alarm programming, WDT programming, device control, and 50 bytes of user NvRAM.

> **CAUTION**
>
> For details about Dallas Semiconductor DS1284 RTC controller refer to original manufacturer documentation for DS1286 RTC controller, which is supplied in either electronic or paper form together with *TORNADO-E6x* board.

RTC clock oscillator control

DS1284 RTC controller allows to enable/disable RTC controller on-chip clock oscillator in order to start/stop real-time clock and to reduce power consumption from backup battery.

RTC controller on-chip clock oscillator is controlled via EOSC bit (D7) of register #9. When this bit is set to the '0' state, then RTC clock oscillator is enabled and real-time clock data and calendar are updated. When this bit is set to the '1' state, then RTC clock is disabled, and real-time clock data and calendar are not updated, however,

in this case RTC controller consumes significantly lower power from backup battery when *TORNADO-E64xx* DSP controller power is off.

CAUTION

TORNADO-E64xx DSP controller is shipped with RTC controller on-chip clock oscillator disabled (bit EOSC of register #9 is set to the '1' state).

RTC-to-DSP interrupts

TORNADO-E64xx on-board DS1284 RTC controller can generate two interrupt requests (*INTA* and *INTB*) to on-board TMS320C64xx DSP from two RTC controller on-chip interrupt request sources (programmable alarm event and on expiration of programmable WDT), which can be software configured to appear at any of the interrupt request outputs via RTC controller on-chip command register (register #B)

CAUTION

TORNADO-E64xx on-board hardware requires that DS1284 RTC controller must be configured by TMS320C64xx DSP software to provide WDT expiration flag at active low *INTA* interrupt request output and programmable alarm flag at active low *INTB* interrupt request output.

This can be obtained by setting *IPSW*, *IBH/LO* and *PU/LVL* bits of DS1284 RTC controller on-chip *COMMAND REGISTER* (register #B) to the '0' state.

After DS1284 RTC controller has been be correctly configured by TMS320C64xx DSP software, then *RTC_WDT_IRQ* (interrupt request on WDT expiration event via RTC controller *INTA* output) and *RTC_ALARM_IRQ* (interrupt request on alarm event via RTC controller *INTB* output) interrupt request outputs of RTC controller can be software configured by TMS320C64xx DSP software to be routed any of the DSP *EXT_INT4*, *EXT_INT5*, *EXT_INT6*, *EXT_INT7*, and *NMI* external interrupt requests of on-board TMS320C6x DSP, which are controlled via *DSP_EXT_INT4_SEL_RG*, *DSP_EXT_INT5_SEL_RG*, *DSP_EXT_INT6_SEL_RG*, *DSP_EXT_INT7_SEL_RG* and *DSP_NMI_SEL_RG* I/O control registers (refer to section 2.2 and tables 2-2 and 2-7 for more details).

Generating board reset on programmable RTC WDT expiration event

TORNADO-E64xx on-board hardware can be software configured by TMS320C64xx DSP software via *WDT_EN_RG* I/O control register (refer to section 2.2 and table 2-5) to generate board reset signal on RTC WDT expiration event. This is performed by means of routing of *RTC_WDT_IRQ* (interrupt request on WDT expiration event via RTC controller *INTA* output) interrupt request output of RTC controller to the input of on-board reset controller.

Instead of *TORNADO-E64xx* on-board WDT, which features WDT latency period typically 1.6sec, RTC controller on-chip WDT can be programmed to generate WDT expiration event within 0.01sec..99.99sec with

resolution 0.01sec, which is important for DSP applications with reduced system restore latency after probably system crash.

2.9   Emulation Tools for *TORNADO-E6x*

TORNADO-E6x uses scan-path emulation technique for the on-board TMS320C6x DSP in order to debug resident TMS320C6x DSP environment and software.

Compatible scan-path emulation tools include MicroLAB Systems *MIRAGE-510DX*, *MIRAGE-P510D* or TI XDS510 and XDS560 universal JTAG emulators, which connect directly to the on-board JTAG-IN connector (JP3).

2.10   Software Development Tools

TMS320C6x DSP is an industry standard DSP and are supported by a variety of software development tools from multiple 3rd party vendors.

Compilers and Debuggers

Software development for *TORNADO-E6x* DSP controllers is supported by TI C6000 Code Composer Studio Compiler Tools (www.ti.com), which include C6000 DSP Optimizing C Compiler and Assembly Language Tools.

Compatible JTAG emulators include TI XDS510 JTAG emulator for ISA-bus, TI XDS560 emulator for PCI-bus, MicroLAB Systems *MIRAGE-510DX* dual-/single-channel JTAG emulator for ISA-bus, and MicroLAB Systems *MIRAGE-P510D* dual-single-channel JTAG emulator for PCI-bus. All JTAG emulators run under TI C6000 Code Composer Studio Debug tools.

Hypersignal RIDE Visual DSP Algorithm Development and Simulation Tool

TORNADO-E6x DSP controllers are supported by DSP algorithm development tools from Hyperception Inc (www.hyperception.com), which include Hypersignal Block Diagram, RIDE and Code Generator. Hypersignal RIDE is the visual real-time integrated DSP algorithm development and simulation environment for Windows, and allows design entry using high-level function blocks (FIR, FFT, math, etc).

Real-time Multitasking Operating Systems (RTOS)

TORNADO-E6x DSP controllers are supported by multiple RTOS that provide multitasking capabilities:
- *DSP/BIOS* from Texas Instruments Inc (www.ti.com), which is the part of TI C6000 Code Composer Studio Compiler/Debug tools. *DSP/BIOS* is redesigned version of former SPOX RTOS from Spectron Microsystems Inc, which has been acquired by TI.
- *VIRTUOSO* from Wind River Systems Inc (www.wrs.com), which is an industry standard high-performance RTOS and provides full feature multitasking support. *VIRTUOSO* RTOS has been originally designed by Eonic Systems (Belgium) company, which has been acquired by Wind River Systems.

- *NUCLEUS PLUS* from Mentor Graphics Inc (www.mentor.com) is an industry standard single-processor high-performance RTOS and provides full feature multitasking support. It features low cost and comes standard with source codes. Available options include *NUCLEUS FILE* MS-DOS compatible file system (can be easily ported onto any floppy and hard-disk controller running under the DSP control), *NUCLEUS NET* IP/UDP protocol stack (can be easily ported onto any network adapter running under the DSP control), *NUCLEUS SHELL* and *DBUG+* system-level debuggers (can be easily ported onto to display run-time system information at any remote terminal), and many more options, which also come in source codes. *NUCLEUS PLUS* RTOS has been originally designed by Accelerated Technology Inc, which has been acquired by Mentor Graphics Inc.

Application Software Tools for TORNADO-E6x

Application specific tools for *TORNADO-E6x* DSP controller include a variety of function libraries for DSP, math, vector, image, etc computation, as well as function libraries for vocoder/fax/modem applications and audio multimedia.

Chapter 3. Installation and Configuration

This chapter includes instructions for installation of *TORNADO-E6x* DSP controller.

3.1   Applying the power

The power to *TORNADO-E6x* controller should apply via on-board JP1 connector (refer to fig.A-1). For proper operation the board requires +5v power only, whereas optional -5v and ±12v power inputs are routed to the on-board SIOX and PIOX-16 daughter-card sites.

3.2   Installation of FLASH/EPROM chip

Installation of FLASH/EPROM chip (refer to fig.2-2 and fig.A-1) into the *TORNADO-E6x* on-board S1 socket must be performed while the board power is off.

CAUTION

TORNADO-E6x on-board S1 socket is designed to carry the FLASH 5v-only 128K..512Kx8 chips or EPROM 128K..1Mx8 chips in the PLCC-32 IC package.

Installation of FLASH/EPROM chip other than that specified in table 2-4 may result in damage of FLASH/EPROM chip and/or of *TORNADO-E6x* hardware.

CAUTION

You have to set the on-board J2 jumper (*TORNADO-E62/E67*) and switch SW3 (*TORNADO-E6202/E6203E64xx*) in accordance with table 2-4 in order to meet the installed FLASH/EPROM chip type.

Installation of FLASH/EPROM chip

In order to FLASH/EPROM into the *TORNADO-E6x* on-board S1 socket recommendations below (refer to fig. 3-1):

- switch off the power for *TORNADO-E6x* DSP controller
- take FLASH/EPROM chip by your fingers in such way that its front (labeling) surface is turned at you
- adjust FLASH /EPROM chip to be parallel to surface of the *TORNADO-E6x* on-board S1 PLCC-32 socket

- orient FLASH/EPROM chip in such way, that the key corner of its PLCC-32 package would match the corresponding corner of *TORNADO-E6x* on-board S1 socket
- safely insert FLASH/EPROM chip into the *TORNADO-E6x* on-board S1 socket
- safely plug and fix FLASH/EPROM chip in the *TORNADO-E6x* on-board S1 socket
- configure J2 jumper (*TORNADO-E62/E67*) and switch SW3 (*TORNADO-E6202/E6203/E64xx*) in accordance with table 2-4 to meet the installed FLASH/EPROM chip type
- switch on the power for *TORNADO-E6x* DSP controller.
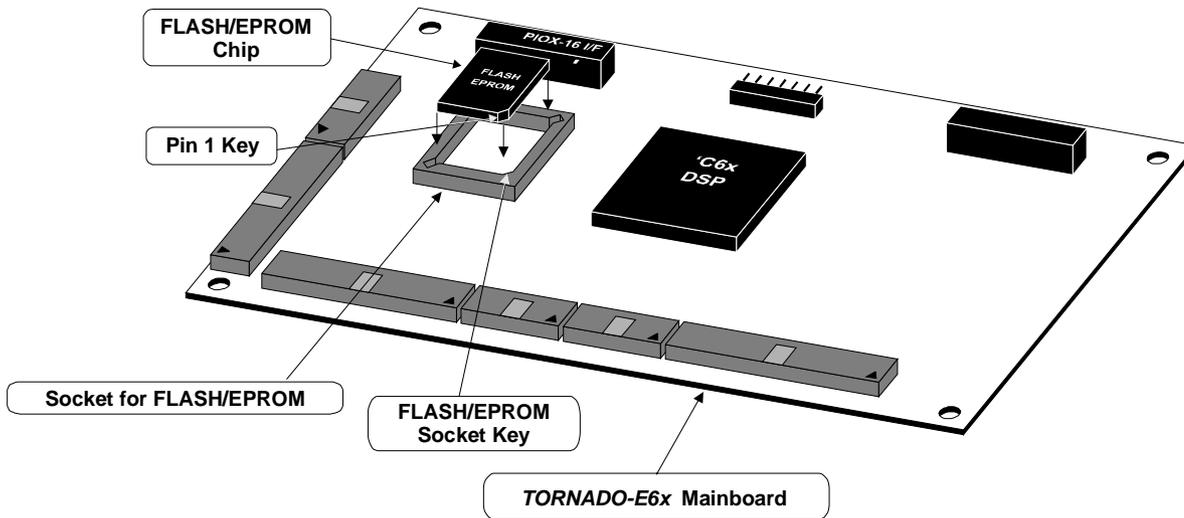
Fig.3-1.   Installation of FLASH/EPROM chip onto *TORNADO-E6x*.

3.3   Configuring *TORNADO-E6x* board

Generally, the following configuration procedure must be performed prior applying power to *TORNADO-E6x* DSP controller for the first time (refer to fig.A-1 for on-board jumpers, switches and connectors list):

- set TMS320C6x DSP bootmode configuration (jumper J1 for *TORNADO-E62/E67* and switch SW2 for *TORNADO-E6202/E6203/E64xx*) in accordance with table 2-1
- *TORNADO-E64xx* board only: if required, set TMS320C64xx DSP on-chip HPI port 16-bit or 32-bit data format using switch SW2-3 in accordance with table 2-13
- *TORNADO-E6415/E6416* boards only: if required, select TMS320C6415/C6416 DSP on-chip external communication interface (McBSP-1 or UTOPIA) using switch SW2-4 in accordance with table 2-14
- *TORNADO-E64xx*: if required, install or change RTC controller power backup battery in BT1 on-board socket in order to ensure that RTC controller has valid backup power and real-time clock is running (refer to section 2.8 and fig.2-26)
- if required, install FLASH/EPROM chip and set jumper J2 (*TORNADO-E62/E67*) and switch SW3 (*TORNADO-E6202/E6203/E64xx*) in accordance with the FLASH/EPROM chip type

- if required, select appropriate RS232 or RS422/EIA-530 interface for USART channels #A and #B and configure configuration jumpers J3/J4 (*TORNADO-E62/E67*) and switch SW4 (*TORNADO-E6202/E6203/E64xx*) in accordance with tables 2-21 and 2-22
- if required, configure J5 and J6 jumpers (*TORNADO-E62/E67*) and switches SW5-1/SW5-2 (*TORNADO-E6202/E6203/E64xx*) in accordance with required modes for SIOX/PIOX-16 timer/IO pins (timer/input-only or timer/output-only) for on-board TMS320C6x DSP (refer to fig.2-5)
- *TORNADO-E64xx* board only: if required, configure SW5-3 in accordance with required mode for TMS320C64xx DSP on-chip timer-2 I/O (timer/input-only or timer/output-only), which is available via on-board JP21 connector (refer to fig.2-5c)
- connect external power supply via JP1 external power connector and keep external power supply off
- if required, plug-in RS232C or RS422/EIA-530 cables into on-board JP11..JP14 connectors (refer to fig. 2-21 and 2-22)
- if required, plug-in external general purpose I/O cable into on-board JP10 connector (refer to fig. 2-24a)
- *TORNADO-E64xx* board only: if required, plug-in external DSP general purpose I/O cable into on-board JP20 connector (refer to fig. 2-24b)
- if required, connect USB type 'B' cable plug of USB cable into the on-board USB device connector (JP17)
- if required, install SIOX and/or PIOX-16 DCM(s) and configure installed DCMs in accordance with provided manuals
- *TORNADO-E6202/E6203/E64xx* only: if required, connect external *T/SU-X1* SIOX rev.B mini-extender kit to on-board MXSIOX connector (section 2.4, Appendix B, figure 2-17), install SIOX rev.B DCM onto *T/SU-X1* mini-extender board, and configure installed SIOX DCM in accordance with provided documentation. Configure *TORNADO-E6202/E6203/E64xx* on-board SW6-1 and SW6-2 common serial clock enable switches in accordance with recommendations in section 2.4, table 2-20 and Appendix B.
- *TORNADO-E62xx/E67* only: if required, install CLKS crystal oscillators for McBSP-0/1/2 serial ports into on-board S2/S3/S4 sockets or connect external CLKS signals to on-board JP8/JP9/JP18 connectors (refer to fig.2-18)
- *TORNADO-E64xx* only: if required, connect external CLKS signals to on-board JP8/JP9/JP18 connectors (refer to fig.2-18)
- if required, connect HPI port cable to on-board JP7 connector
- *TORNADO-E6415/E6416* only: if required, connect UTOPIA port cables to on-board JP22 and JP23 connectors (refer to section 2.2 and fig.2-4)
- if required, connect JTAG emulator cable to on-board JP3 JTAG-IN connector
- switch on external power supply in order to apply power to *TORNADO-E6x* DSP controller via JP1 external power connector.

Appendix A. Board Layout and Physical Dimensions

This Appendix includes a summarized description for the *TORNADO-E6x* on-board configuration jumpers, connectors, sockets and switches, and provides detail mechanical dimensions for *TORNADO-E6x* boards.

A.1 *TORNADO-E6x* boards layout

Board layouts for *TORNADO-E6x* DSP controller boards including on-board configuration jumpers, switches, connectors and LED indicators, are presented at fig.A-1.
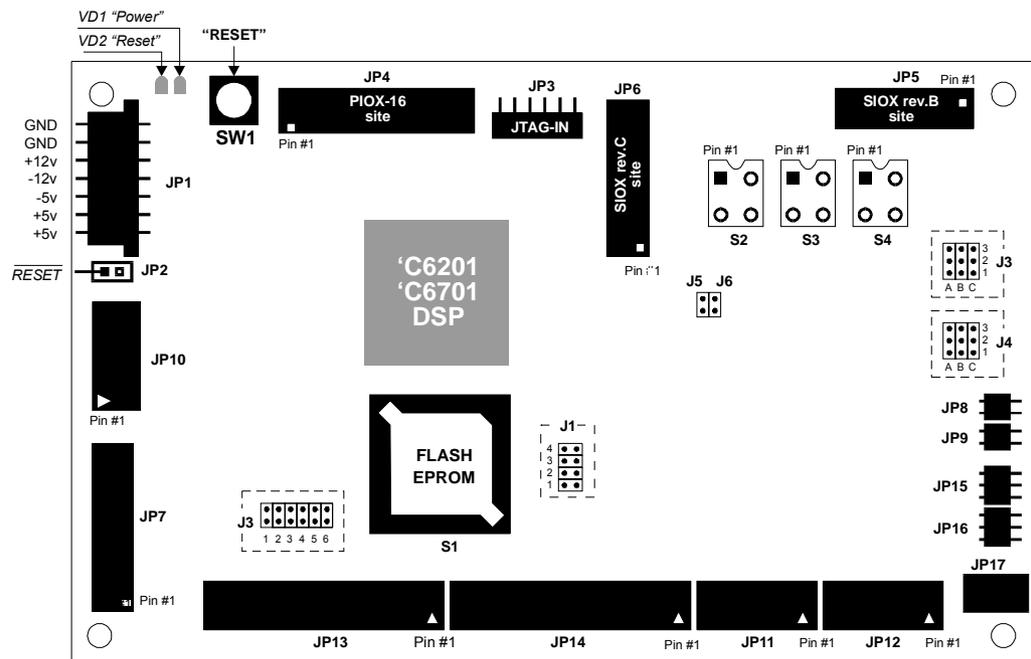
Fig.A-1a. On-board layout for *TORNADO-E62/E67*.
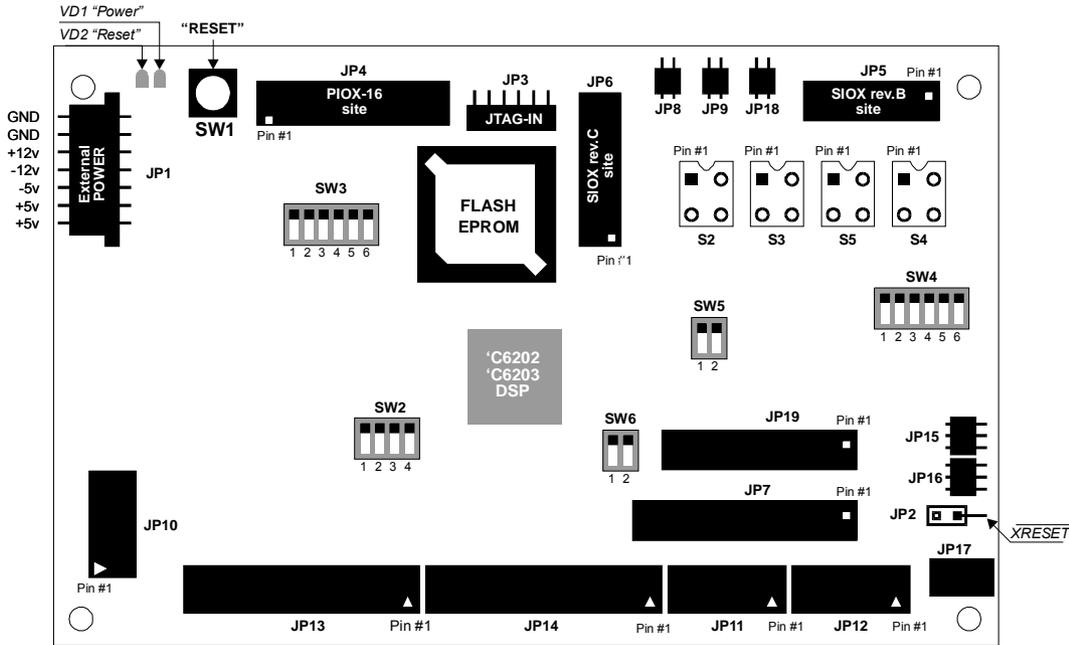
Fig.A-1b. On-board layout for *TORNADO-E6202/E6203*.
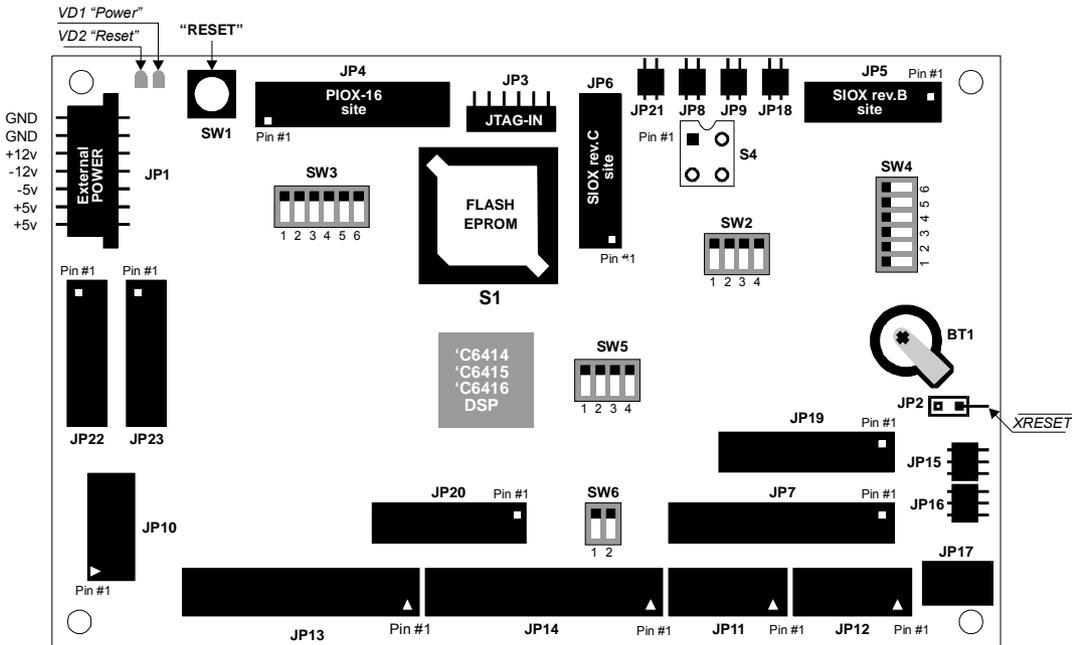
Fig.A-1c. On-board layout for *TORNADO-E64xx*.

A.2   On-board Configuration Jumpers for *TORNADO-E62/E67*

List of on-board configuration jumpers for *TORNADO-E6x* DSP controllers is presented in table A-1. Note, that *TORNADO-E6202/E6203/E64xx* DSP controllers do not have on-board configuration jumpers and are using configuration switches instead.

Table A-1. On-board configuration jumpers for *TORNADO-E62/E67*.

jumper ID	jumper function description	reference information
J1 (J1-1..J1-4)	TMS320C6x DSP Bootmode configuration.	Section 2.2; table 2-1.
J2 (J2-1..J2-6)	FLASH/EPROM chip type selector.	Sections 2.2 and 3.2; table 2-4.
J3	External RS232C/RS422 interface selector for USART channel "A".	Section 2.5 ; table 2-20a
J4	External RS232C/RS422 interface selector for USART channel "B".	Section 2.5 ; table 2-21a
J5	DSP Timer-0 output enable. DSP Timer-0 I/O is available via SIOX/PIOX-16 daughter-card sites.	Sections 2.2, 2.3 and 2.4; fig.2-5a
J6	DSP Timer-1 output enable. DSP Timer-1 I/O is available via SIOX/PIOX-16 daughter-card sites.	Sections 2.2, 2.3 and 2.4; fig.2-5a

A.3   On-board Connectors

List of on-board connectors for *TORNADO-E6x* DSP controllers is presented in table A-2.

Table A-2. On-board connectors and headers for *TORNADO-E6x*.

connector ID	connector function description	reference information
JP1	External power connector.	Sections 2.1 and 3-1.
JP2	External DSP Reset connector.	Section 2.2.
JP3	JTAG-IN connector	Section 2.9

JP4	PIOX-16 expansion interface site header.	Section 2.3; fig.2-10; table 2-16
JP5	SIOX rev.B expansion interface site header.	Section 2.4; fig.2-15; table 2-17
JP6	SIOX rev.C expansion interface site header.	Section 2.4; fig.2-16, table 2-18
JP7	TMS320C6x HPI port connector.	Section 2.2; fig.2-3; table 2-12
JP8 JP9	Connectors for external clock (CLKS) for McBSP-0/1 ports of TMS320C6x DSP.	Section 2.5; fig.2-18
JP10	General purpose digital I/O connector.	Section 2.6; fig.2-24a
JP11 JP12	RS232C interface connectors for channels "A" and "B" of USART.	Section 2.5; fig.2-21
JP13 JP14	RS422/EIA-530 interface connectors for channels "A" and "B" of USART.	Section 2.5; fig.2-2
JP15 JP16	USART Transmitter/receiver clock outputs for channels "A" and "B" of USART.	Section 2.5; fig.2-23
JP17	USB device connector.	Section 2.7; fig.2-25
JP18 (*TORNADO-E6202/E6203/E64xx*)	Connector for external clock (CLKS) for McBSP-2 port of TMS320C6202/C6203/C64xx DSP.	Section 2.5; fig.2-18
JP19 (*TORNADO-E6202/E6203/E64xx*)	MXSIOX connector.	Section 2.4; fig.2-17; table 2-19
JP20 (*TORNADO- E64xx*)	DSP general purpose I/O connector.	Section 2.6; fig.2-24b
JP21 (*TORNADO- E64xx*)	TMS320C64xx DSP timer-2 I/O connector.	Section 2.2; fig.2-5c and 2-6
JP22 (*TORNADO- E64xx*)	UTOPIA receiver connector.	Section 2.2; fig.2-4a
JP23 (*TORNADO- E64xx*)	UTOPIA transmitter connector.	Section 2.2; fig.2-4b

A.4   On-board Sockets

List of on-board sockets for *TORNADO-E6x* DSP controllers is presented in table A-3.

Table A-3.   On-board sockets for *TORNADO-E6x*.

socket ID	socket function	reference information
S1	PLCC-32 socket for FLASH/EPROM chip.	Sections 2.2 and 3-2.
S2 *S3* *(TORNADO-E62xx/E67)*	DIP-4 (0.3"x0.3") sockets for 5V crystal oscillators (example: EPSON (SG-531) for external clock (CLKS) for McBSP-0/1 ports of *TORNADO-E62/E67* on-board TMS320C6x DSP.	Section 2.2; fig. 2-18
S4	DIP-4 (0.3"x0.3") socket for 5V crystal oscillator (example: EPSON SG-531) for USART master source clock.	Section 2.5; fig.2-20
S5 *(TORNADO-E6202/E6203)*	DIP-4 (0.3"x0.3") socket for 5V crystal oscillator (example: EPSON (SG-531) for external clock (CLKS) for McBSP-2 ports of *TORNADO-E6202/E6203* on-board TMS320C6202/C6203 DSP.	Section 2.4; fig.2-18b
BT1 *(TORNADO-E64xx)*	RTC controller power backup battery socket for 3V lithium type 1216/1220/1225 battery.	Section 2.8; fig.2-26

A.5   On-board Switches

List of on-board switches for *TORNADO-E6x* DSP controllers is presented in table A-4.

Table A-4.   On-board switches for *TORNADO-E6x*.

switch ID	switch function	reference information
SW1	DSP reset pushbutton.	Section 2.2.
SW2-1..4 *(TORNADO-E6202/E6203)* *SW2-1..2* *(TORNADO-E64xx)*	TMS320C6202/C6203/C64xx DSP Bootmode configuration.	Section 2.2; table 2-1.
SW2-3 *(TORNADO-E64xx)*	TMS320C64xx DSP HPI port data mode (16-bit or 32-bit).	Section 2.2; table 2-13.

SW2-4 (TORNADO-E6415/E6416)	TMS320C6415/C6416 DSP external data communication interface (McBSP-1 or UTOPIA).	Section 2.2; table 2-14.
SW3-1..6 (TORNADO-E6202/E6203/E64xx)	FLASH/EPROM chip type selector.	Sections 2.2 and 3.2; table 2-4.
SW4-1..6 (TORNADO-E6202/E6203/E64xx)	External RS232C/RS422 interface selector for USART channels "A" and "B".	Section 2.5 ; tables 2-21 and 2-22
SW5-1..2 (TORNADO-E6202/E6203/E64xx)	DSP on-chip timer-0 and timer-1 output enable. DSP Timer-0/1 I/O is available via SIOX/PIOX-16/MXSIOX daughter-card sites.	Sections 2.2, 2.3 and 2.4; fig.2-5
SW5-3 (TORNADO- E64xx)	TMS320C64xx DSP on-chip timer-2 output enable. DSP Timer-2 I/O is available via JP21 connector.	Sections 2.2, 2.3 and 2.4; fig.2-5
SW6-1..2 (TORNADO-E6202/E6203/E64xx)	Common serial clock enable for SIO-0 and SIO-1 serial ports of on-board MXSIOX connector.	Section 2.4, Appendix B tables 2-20

A.6   On-board LED indicators

On-board LED indicators for *TORNADO-E6x* DSP controllers are listed in table A-5.

Table A-5. On-board LED indicators for *TORNADO-E6x*.

LED	LED function description
VD1	Board power indicator (GREEN).
VD2	DSP reset indicator (RED).

A.7   Physical Dimensions for *TORNADO-E6x* Mainboard

Detail mainboard dimensions for *TORNADO-E6x* DSP controllers including physical positions for all mounting holes and daughter-card site header is presented at fig.A-2. More details including positions of on-board edge connectors is available from MicroLAB Systems upon request.
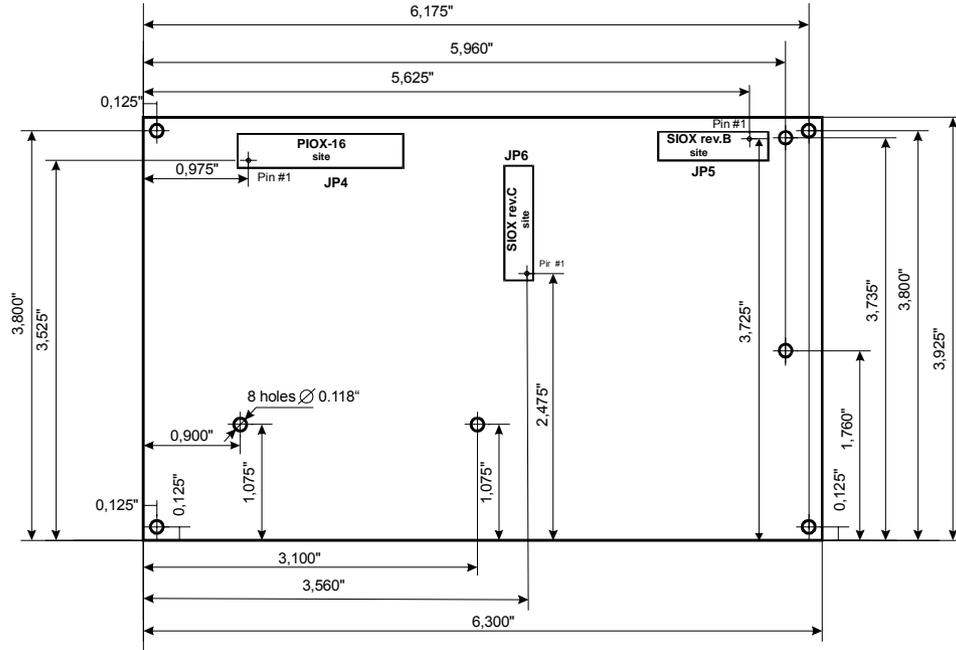
Fig.A-2. Physical dimensions for *TORNADO-E6x* DSP controller mainboard.

Appendix B.   *T/SU-X1* SIOX rev.B Mini-Extender Kit

This appendix contains description for *T/SU-X1* external SIOX rev.B mini-extender kit, which can be used to connect external SIOX rev.B AD/DA/DIO and application specific DCM to *TORNADO* DSP controllers and coprocessors, which provide on-board compatible connector for connection to external *T/SU-X1* SIOX rev.B mini-extenders.

B.1   General Description

T/SU-X1 SIOX rev.B mini-extender kit is normally provided as dual SIOX rev.B mini-extender kit (fig.B-1), which comprises of the following components:

- two identical *T/SU-X1* SIOX rev.B mini-extender carrier boards
- PC chassis mounting bracket
- two *T/SU-X1/XC* 10" (0.25m) long connection cables.
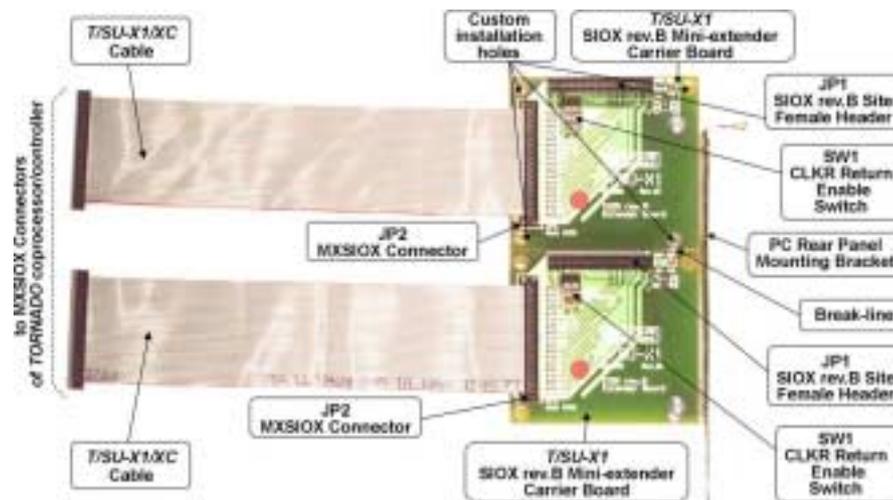
Fig.B-1.   Dual *T/SU-X1* SIOX rev.B mini-extender with mounting bracket and connection cables.

Each *T/SU-X1* SIOX rev.B mini-extender carrier board provides on-board site for one full-size SIOX rev.B DCM (fig.B-2), which can be either fixed to the *T/SU-X1*carrier board via optional spacers, or screwed to the mounting bracket.
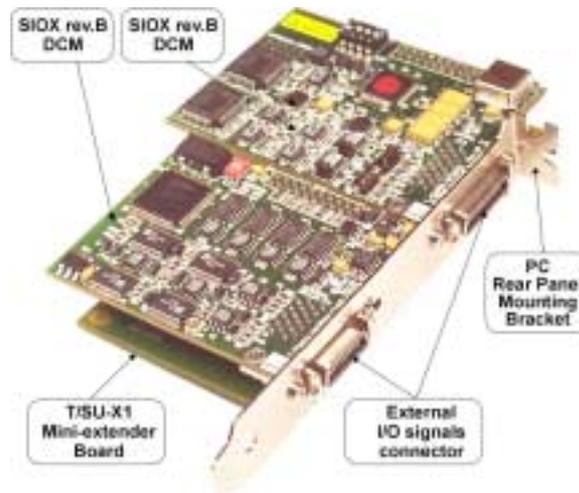
Fig.B-2.   Dual *T/SU-X1* SIOX rev.B mini-extender with two installed SIOX rev.B DCM.

connection of T/SU-X1 SIOX rev.B mini-extender to host TORNADO DSP controllers and coprocessors

T/SU-X1 SIOX rev.B mini-extender connects to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* 10" (0.25m) long connection cable (fig.B-3), which connects to the MXSIOX connectors on the *T/SU-X1* SIOX rev.B mini-extender on one side and to with the corresponding MXSIOX matching connector host *TORNADO* DSP controller/coprocessor.
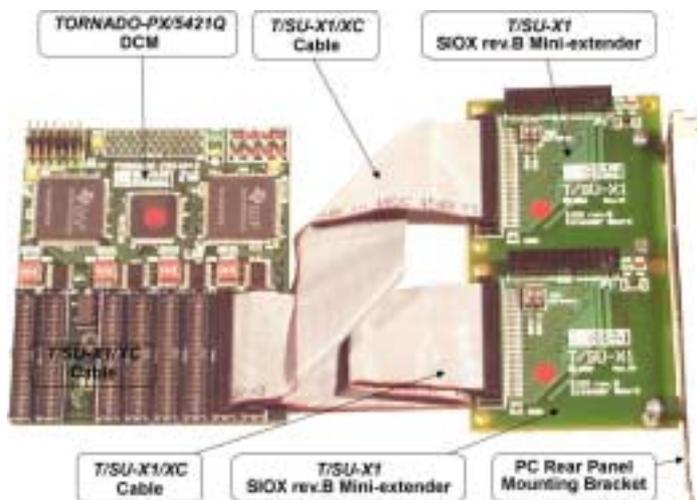
Fig.B-3.   Connection of dual *T/SU-X1* SIOX rev.B mini-extender to host *TORNADO-PX5421Q* PIOX-16 DSP coprocessor DCM.

installation

Dual *T/SU-X1* SIOX rev.B mini-extender can either mount at the rear panel of PC using installed mounting bracket, or can be hand-broken into two identical *T/SU-X1* SIOX rev.B mini-extenders using on-board perforated broke line (fig.B-1).

Single *T/SU-X1* SIOX rev.B mini-extender, which appears as the broken half of dual *T/SU-X1* SIOX rev.B mini-extender, can be installed into the embedded custom chassis environment.

physical dimensions

Figure B-4 provides physical dimensions for single *T/SU-X1* SIOX rev.B mini-extender and positions for all installation holes and connectors.
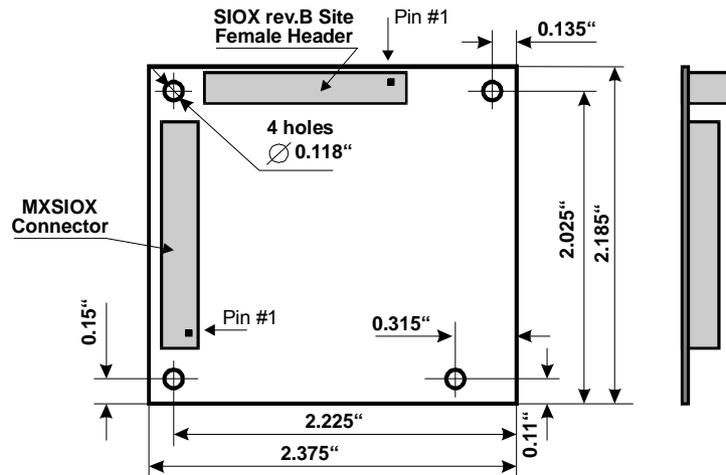
Fig.B-4.   Physical dimensions of *T/SU-X1* SIOX rev.B mini-extender.

B.2   Technical Specifications

The following are technical specifications for *T/SU-X1* SIOX rev.B mini-extenders.

Parameter description	*parameter value*
number of SIO ports	2
number of TM/XIO I/O lines	2
number of external interrupt request inputs (*XIRQ*)	2
number of SIOX reset signals (*RESET*)	1

maximum serial clock frequency for transmitter/receiver of SIO ports	50 MHz
power supply outputs	±5v, ±12v
optional features	LED indicators for power and SIOX reset control
	CLKR0/CLKR1 serial receiver clock enable switches
Dimensions	2.16"x2.36" (55x60 mm)
length of *T/SU-X1/XC* extender cable	10" (0.25m)

B.3   Technical Description

Figure B-5 presents block diagram of *T/SU-X1* SIOX rev.B mini-extender kit.
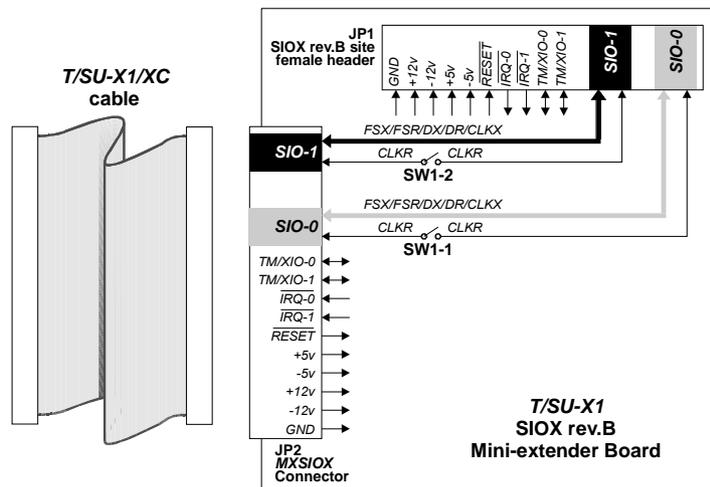
Fig.B-5.   Block diagram of *T/SU-X1* SIOX rev.B mini-extender.

T/SU-X1 SIOX rev.B mini-extender carrier board

T/SU-X1 SIOX rev.B mini-extender carrier board comprises of the following components:
- SIOX rev.B site header (JP1)
- MXSIOX connector (JP2) for connection to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* connection cable
- on-board SW1 switch, which is used to enable serial receiver clock (CLKR) for each serial port.

T/SU-X1 on-board JP1 SIOX rev.B site header and JP2 MXSIOX connector for connection to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* connection cable comprise of the signals for two serial ports (SIO-0 and SIO-1), two timer/IO lines (*TM/XIO-0/1*), two external interrupt request inputs (*IRQ-0/1*), SIOX interface reset control output (*RESET*), and host ±5V/±12V power supply lines.

Pinout information for JP1 SIOX rev.B site header and JP2 MXSIOX connector is provided in the corresponding subsections below and figures B-6 and B-5 correspondingly. Common signal description is provided in table B-1.

T/SU-X1 on-board SW1 switch shall be used in conjunction with host *TORNADO* DSP coprocessor/controller on-board common serial clock enable switches in order to enable return of receiver' serial clock for each of two serial ports of SIOX interface to host *TORNADO* DSP coprocessor/controller depending upon the type of installed SIOX rev.B DCM. Refer to the corresponding subsection below for more details.

MXSIOX connector pinout and signal description

T/SU-X1 on-board MXSIOX connector is used for connection to host *TORNADO* DSP coprocessor/controller via *T/SU-X1/XC* connection cable.

MXSIOX connector is Samtec 34-pin dual-row 2mm guarded male header. Although MXSIOX plugs come standard with *T/SU-X1/XC* SIOX rev.B mini-extender connection cables, optional MXSIOX plugs for 2mm flat cables are available from MicroLAB Systems upon request.

MXSIOX connector pinout is presented at fig.B-6, whereas signal description is provided in table B-1.
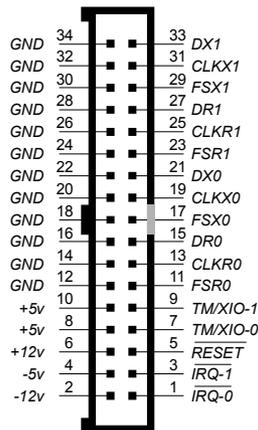
Fig.B-6. Pinout for *T/SU-X1* SIOX rev.B mini-extender on-board MXSIOX connector (top view).

Table B-1. Signal description for *T/SU-X1* SIOX rev.B mini-extender on-board MXSIOX connector.

SIOX rev.B interface signal	signal type	Description
SIO-0 port control		
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port, which connect to the transmitter control signals for SIO-0 serial port.
DR0 FSR0 CLKR0	I I I	Data, frame synchronization and serial clock signals for receiver of SIO-0 port, which connect to the receiver control signals for SIO-0 serial port.
SIO-1 port control		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port, which connect to the transmitter control signals for SIO-1 serial port.
DR1 FSR1 CLKR1	I I/O I	Data, frame synchronization and serial clock signals for receiver of SIO-1 port, which connect to the receiver control signals for SIO-2 serial port.
Timers/IO, DSP Reset and Interrupt Requests		
TM/XIO-0 TM/XIO-1	I/O	Timer/IO pins.
$\overline{RESET}$	O	Active low SIOX reset output pin.
$\overline{IRQ\text{-}0}$ $\overline{IRQ\text{-}1}$	I	Active low external interrupt request inputs. Active DSP core' external interrupt requests are generated on the falling edge (1→0) of $\overline{IRQ\text{-}0}$ and $\overline{IRQ\text{-}1}$.. inputs.
Power Supplies		
GND		Ground.
+5v		+5v power supply.
+12v		+12v power supply.
-5v		-5v power supply.
-12v		-12v power supply.

Note: 1.   Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
                   3.   All logical signal levels and load currents correspond to that for 3v/5v CMOS signals.

SIOX rev.B site header

T/SU-X1 on-board SIOX rev.B site header with two serial ports is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM must be the industry standard either 26-pin 0.1"x0.1"male header (in case both SIO-0 and SIO-1 serial ports are used on SIOX plugged-in DCM) or 20-pin 0.1"x0.1"male header (in case only SIO-0 serial port is used on SIOX plugged-in DCM).

SIOX rev.B site connector pinout with two serial ports is shown at fig.B-7 and signal specifications are listed in table B-1.
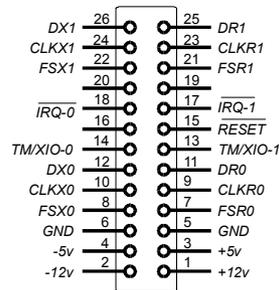
Fig.B-7. SIOX rev.B connector pinout (top view).

Signal levels for SIOX interface signals of T/SU-X1 SIOX rev.B mini-extender is defined by host *TORNADO* DSP coprocessor/controller and correspond to that for the CMOS/TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

<div style="border:1px solid black; padding:1em;">

CAUTION

Some *TORNADO* boards provide SIOX interface signal levels for CMOS/TTL only, whereas other *TORNADO* boards provide SIOX interface signal levels universal for both 3V TTL and standard 5V TTL. Refer to documentation for your particular *TORNADO* board for information about SIOX interface signal levels.

</div>

T/SU-X1/XC mini-extender connection cable

T/SU-X1 SIOX rev.B mini-extender carrier board connects to host *TORNADO* DSP coprocessor/controller via *T/SU-X1/XC* 10" (0.25m) long 34-pin 2mm flat cable.

T/SU-X1/XC mini-extender connection cable plugs to MXSIOX connector of *T/SU-X1* SIOX rev.B mini-extender carrier board on one side and to MXSIOX connector of host *TORNADO* DSP coprocessor/controller on the other side (fig.B-3).

on-board receiver serial clock return enable switches

T/SU-X1 SIOX rev.B mini-extender carrier board provides on-board SW1-1 and SW1-2 switches in order to enable return of SIO-0 and SIO-1 receiver serial clock (CLKR0 and CLKR1 correspondingly) SIOX interface to host *TORNADO* DSP coprocessor/controller depending upon the type of installed SIOX rev.B DCM.

T/SU-X1 SIOX rev.B mini-extender on-board SW1-1 and SW1-2 switches shall be used in conjunction with host *TORNADO* DSP coprocessor/controller on-board common serial clock enable switches using general recommendations below.

Host *TORNADO* DSP coprocessor/controller provides on-board common CLKX/CLKR serial clock enable switches for each of serial ports of MXSIOX connectors.

CAUTION

In case on-board common serial clock enable switch of host *TORNADO* DSP coprocessor/controller is set to 'ON', then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are connected together on-board.

In case on-board common serial clock enable switch of host *TORNADO* DSP coprocessor/controller is set to 'OFF', then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are disconnected on-board.

Background for usage on-board common CLKX/CLKR serial clock enable switches of host *TORNADO* DSP coprocessor/controller and *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKR) return enable switches is the 'long-line' compensation issue for serial clock signals distribution over connection flat cable between host *TORNADO* DSP coprocessor/controller on-board MXSIOX connector and *T/SU-X1* SIOX rev.B mini-extender due to the 'long-line wave nature' of connection flat cable.

Although the 'long-line' compensation resistors are being used for control signals for serial ports at both host *TORNADO* DSP coprocessor/controller and *T/SU-X1* SIOX rev.B mini-extender boards in order to exclude signal reflection, a 'long-line' non-compensation for serial clock signals can still occur in case installed SIOX rev.B DCM is using common shorted serial clock for transmitter and receiver of SIO port (many SIOX rev.B DCM actually use this in order to simplify design). Note, that this problem does not occur with SIO port frame synchronization and serial data signals, since these signals always use dedicated lines of SIOX interface and can't be connected together.

CAUTION

In case installed SIOX rev.B DCM has been designed without on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and each serial clock is using its dedicated pins, then the corresponding host *TORNADO* DSP coprocessor/controller on-board common CLKX/CLKR serial clock enable switch must be set to 'OFF' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'ON'.

In case installed SIOX rev.B DCM has been designed with on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and both serial clocks are using shared pins, then the corresponding host *TORNADO* DSP coprocessor/controller on-board common CLKX/CLKR serial clock enable switch must be set to 'ON' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'OFF'.

LED indicators

T/SU-X1 SIOX rev.B carrier board also provides two on-board LED indicators for host power (V1) and for SIOX reset state (V2).

B.4   Physical Dimensions for SIOX DCM

Physical dimensions for SIOX DCM are presented at fig.B-8. This information is intended for those customers, who need to design customized SIOX DCMs.
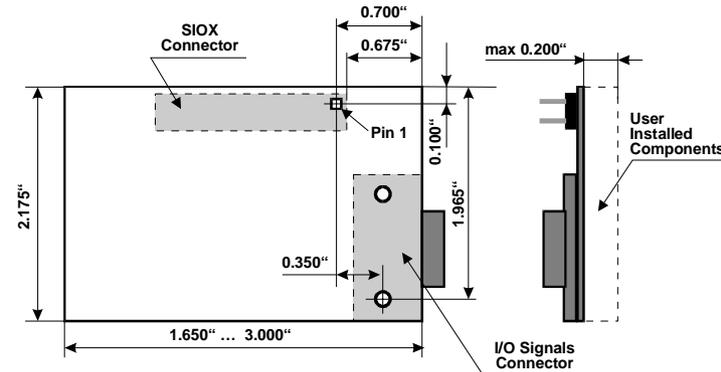
SIOX connector: 20-pin or 26-pin straight dual-row mail header
(0.025" Sq., 0.1"x0.1" pattern)
Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.B-8.   Physical dimensions for SIOX DCM.

Appendix C.   Glossary of Terms

This Glossary contains definition for terms and other synchronism, which are most often used along in this manual.

A

B

bootmode
> TMS320C6x DSP start-up procedure, which corresponds to either no load of DSP application code to DSP environment (no boot procedure), or to the loading of application code to TS320C6x DSP environment from either on-board FLASH/EPROM, or HPI port. Refer to section 2.2 and original TI documentation for more details.

BMODE_RG
> I/O control read-only register, which contains information about DSP start-up bootmode (*TORNADO-E6202/E6203/E64xx* only). Refer to section 2.2 for more details.

C

CLKX, CLKR
> Serial clock for transmitter and receiver of TMS320C6x DSP on-chip McBSP serial ports. Refer to section 2.4 and Appendix B for more details.

D

DCM
> Daughter-card module.

DEV_ID_RG
> I/O control read-only register, which contains information about *TORNADO- E6202/E6203/E64xx* device ID code. Refer to section 2.2 for more details.

DEV_REV_ID_RG
> I/O control read-only register, which contains information about *TORNADO-E64xx* board firmware revision ID code. Refer to section 2.2 for more details.

DSP

On-board TI TMS320C6x Digital Signal Processor. Refer to sections 2.1 and 2.2 for more details.

DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG,
DSP_EXT_INT7_SEL_RG, DSP_NMI_SEL_RG
> I/O control registers, which are used to configure on-board interrupt request source for TMS320C6x DSP external interrupt request inputs (*EXT_INT4..7* and *NMI*). Refer to section 2.2 for more details.

DSPINT
> Host-to-DSP interrupt request via TMS320C6x DSP on-chip HPI port. Refer to section 2.2 for more details.

DX, DR
> Serial data for transmitter and receiver of TMS320C6x DSP on-chip McBSP serial ports. Refer to section 2.4 and Appendix B for more details.

E

EPROM
> Electrically programmable read-only memory chip, which can be used to store application boot code or non-volatile data. 8-bit EPROM chip in PLCC-32 IC package can be installed into *TORNADO-E6x* on-board S1 socket.. Refer to section 2.2 for more details.

F

FLASH
> Electrically programmable and electrical erasable read/write memory chip, which can be used to store application boot code or non-volatile data. 8-bit 5v-only FLASH chip in PLCC-32 IC package can be installed into *TORNADO-E6x* on-board S1 socket.. Refer to section 2.2 for more details.

FSX, FSR
> Frame synchronization for transmitter and receiver of TMS320C6x DSP on-chip McBSP serial ports. Refer to section 2.4 and Appendix B for more details.

G

H

HINT

DSP-to-host interrupt request via TMS320C6x DSP on-chip HPI port. Refer to section 2.2 for more details.

HPI

TMS320C6x DSP on-chip host port interface, which is used to access DSP environment (memory, peripherals, registers, etc) from host controller. Refer to section 2.2 for more details.

I

I/O control registers

A set of control registers, which is mapped to EMIF CE-3 area of *TORNADO-E6x* on-board TMS320C6x DSP. Refer to section 2.2 for more details.

J

JTAG

Joint Test Action Group interface, which is a part of the TMS320C2xx/VC33/C4x/C5x/ C54x/C6x/C8x DSP on-chip hardware, and is used to debug *TORNADO-E6x* on-board TMS320C6x DSP software using external JTAG emulators (TI XDS510 and MicroLAB' *MIRAGE-510DX*, *MIRAGE-P510D*, *UECMX*). Refer to section 2.8 for more details.

JTAG-IN

On-board input connector, which is used for connection to external JTAG emulator. Refer to section 2.8 and Appendix A for more details.

K

L

LED

Light emitting diode indicator. Refer to Appendix A for more details.

M

McBSP

TMS320C6x DSP on-chip serial ports. Refer to sections 2.2 and 2.4 for more details.

MXSIOX

On-board connector for external *T/SU-X1* SIOX rev.B mini-extender (*TORNADO-E6202/E6203/E64xx* only). Refer to section 2.4 and Appendix B for more details.

N

O

P

PIOX-16

16-bit Parallel I/O eXpansion interface site for compatible daughter-card modules (DCM) at *TORNADO* PC plug-in DSP systems and DSP controllers. *TORNADO-E6x* provides one on-board PIOX-16 DCM site. Refer to section 2.3 for more details.

Pod

Electronic device, which connects external JTAG emulator with *TORNADO-E6x* on-board JTAG-IN connector for uploading and debugging of TMS320C6x DSP software.

PX_IRQ-0, PX_IRQ-1, PX_IRQ-2, PX_IRQ-3

Interrupt requests from PIOX-16 DCM site. Refer to sections 2.2 and 2.3 for more details.

PX_RESET

Reset control bit of *PXSX_RESET_RG* I/O control register for PIOX-16 DCM site. Refer to sections 2.2 and 2.3 for more details.

PXSX_RESET_RG

I/O control register, which is used to control reset signals for on-board SIOX rev.B/C DCM sites, PIOX-16 DCM site, and for MXSIOX connector. Refer to section 2.2 for more details.

Q

R

RS232C external interface

External electrical interfaces for each channel of on-board USART chip, which provides up to 115 kBaud data transfer rate and is typically used in case the corresponding USART channel is

configured for ASYNCH protocol in order to connect to external host computer or peripherals. RS232C external interface is selected via on-board J3/J4 jumpers (*TORNADO-E62/E67*) or SW4 switch (*TORNADO-E6202/E6203/E64xx*). Refer to section 2.5 and original Infineon documentation for more details.

RS422/EIA-530 external interface

External electrical interfaces for each channel of on-board USART chip, which provides up to 10 Mbit/s data transfer rate and is typically used in case the corresponding USART channel is configured for either of HDLC/X.25, SDLC, MONOSYNC, BISYNC synchronous protocols in order to connect to external network, or high-speed peripherals or host computers. RS232C external interface is selected via on-board J3/J4 jumpers (*TORNADO-E62/E67*) or SW4 switch (*TORNADO-E6202/E6203/E64xx*). Refer to section 2.5 and original Infineon documentation for more details.

RTC

Battery back-up real-time clock controller (DS1284), which is available at *TORNADO-E64xx* DSP controllers only. Refer to section 2.8 and original Dallas Semiconductor documentation for more details.

RTC_ALARM_IRQ

Interrupt request on software programmable RTC controller on-chip alarm, which is available at *TORNADO-E64xx* DSP controllers only. Refer to section 2.8 and original Dallas Semiconductor documentation for more details.

RTC_WDT_IRQ

Interrupt request on software programmable RTC controller on-chip watch-dog timer expiration event, which is available at *TORNADO-E64xx* DSP controllers only. Refer to section 2.8 and original Dallas Semiconductor documentation for more details.

S

SIOX rev.B

Serial I/O eXpansion interface site revision B for compatible daughter-card modules (DCM) at *TORNADO* DSP systems, controllers, and SIOX extenders. Refer to sections 2.2 and 2.4, and Appendix B for more details.

SIOX rev.C

Enhanced serial I/O eXpansion interface site revision C for compatible daughter-card modules (DCM) at *TORNADO* DSP systems and controllers. Refer to section 2.4 for more details.

SX-A_RESET, SX-B_RESET

Reset control bits of *PXSX_RESET_RG* I/O control register for on-board SIOX rev.B/C DCM site and MXSIOX connector. Refer to sections 2.2 and 2.3 for more details.

SX_IRQ-0, SX_IRQ-1, SX_IRQ-2

External interrupt request inputs from *TORNADO-E6x* on-board SIOX rev.B DCM site, SIOX rev.C DCM site and MXSIOX connector. Refer to section 2.4 for more details.

T

T/SU-X1

External SIOX rev.B mini-extender, which can carry one SIOX rev.B DCM and connect to *TORNADO-E6x* on-board MXSIOX connector. Refer to section 2.4 and Appendix B for more details.

T/SU-X1/XC

Extender connector cable, which is used to connect external SIOX rev.B mini-extender and *TORNADO-E6x* on-board MXSIOX connector. Refer to section 2.4 and Appendix B for more details.

TM/XIO-0/1

Timer/IO pins of on-board SIOX rev.B/C DCM sites, PIOX-16 DCM site and MXSIOX connector. Refer to section 2.2 for more details.

U

USART

Universal synchronous asynchronous receiver transmitter interface chip, which is the Infineon SAB82532 ECC2 chip on *TORNADO-E* DSP controllers. Refer to section 2.5 and original Infineon documentation for more details.

USART_IRQ

Interrupt request from on-board USART chip. Refer to sections 2.2 and 2.5, and original Infineon documentation for more details.

USB device controller

Universal serial bus (USB) device controller chip, which is the Agere Systems either USS-820 or USS-825 chip on *TORNADO-E* DSP controllers. Refer to section 2.7 and original Agere Systems documentation for more details.

USB_IRQ

Interrupt request from on-board USB device controller. Refer to sections 2.2 and 2.7, and original Agere Systems documentation for more details.

UTOPIA

TMS320C6415/C6416 DSP on-chip communication controller, which meets slave level 2 Universal Test and Operation Interface for ATM specification and is available at *TORNADO-E6415/E6416* DSP controllers only. Refer to section 2.2 and original TI documentation for more details.

V

W

WDT
Watchdog timer. Refer to section 2.2 for more details.

WDT_EN_RG
I/O control register, which is used to enable reset of *TORNADO-E6x* on-bard DSP and peripherals on WDT expiration condition. Refer to section 2.2 for more details.

WDT_RESET_RG
I/O control write-only register, which is used to reset WDT. Refer to section 2.2 for more details.

X

XMEM
Bit of *SYS_CNF_RG* I/O control register, which is used to select external synchronous memory type (SBSRAM or SDRAM) for *TORNADO-E6202/E6203* DSP controllers. Refer to section 2.2 for more details.

SYS_CNF_RG
I/O control register, which is used to select external synchronous memory type (SBSRAM or SDRAM) for *TORNADO-E6202/E6203* DSP controllers and to read system start-up configuration for *TORNADO-E64xx* DSP controllers. Refer to section 2.2 for more details.

Y

Z