

# ***TORNADO-E64xx***

## ***F/W rev.1A-1 and rev.1A-2***

Stand-alone DSP Controllers with  
Ultra-High Performance 32-bit Fixed-/Floating-Point TMS320C6xxx DSP

### ***Addendum to***

### ***TORNADO-E6x User's Guide rev.4A***

covers:  
TORNADO-E62/E67 rev.2A  
TORNADO-E6202/E6203 rev.1B  
TORNADO-E6414/E6415/E6416 rev.1A, rev.1A-1, rev.1A-2

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## About this Document

This document contains addendum to *TORNADO-E6x* User's Guide rev.4A and describes the firmware updates rev.1A-1 and rev.1A-2 for *TORNADO-E6414/E6415/E6416* boards rev.1A.

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# Chapter 1. Introduction

This chapter contains general description for most recent updates to *TORNADO-E6x* stand-alone DSP controller boards, which have been introduced after release of the latest *TORNADO-E6x* User's Guide (rev.4A) and which are not covered by that document.

## 1.1 Revision History

The updates to *TORNADO-E6x* stand-alone DSP controllers product line, which have been introduced after release of the latest *TORNADO-E6x* User's Guide and which are not covered by that document, are applicable to *TORNADO-E64xx* (*TORNADO-E6414/E6415/E6416*) boards only and include new firmware updates rev.1A-1 and rev.1A-2 for these boards.

### NOTE

There have been no updates introduced for *TORNADO-E62/E67/E6202/E6203* boards.

The *TORNADO-E64xx* rev.1A boards with new firmware rev.1A-1 and rev.1A-2 can be visually recognized by means of the attached label with the corresponding ether 'F/W rev.1A-1' or 'F/W rev.1A-2' text on it. Instead, the *TORNADO-E64xx* rev.1A boards with initial firmware rev.1A do not have such a label.

Also, user DSP application can recognize the firmware rev.1A-1 and rev.1A-2 by means of reading the *DEV\_REV\_ID\_RG* I/O control register from the DSP environment as it described later in this document.

## 1.2 Software Compatibility Issues

User DSP application software, which has been designed for initial firmware rev.1A of *TORNADO-E64xx* boards, generally does not need any modifications in order to run at the *TORNADO-E64xx* boards with firmware rev.1A-1 and rev.1A-2. The only requirement is to recompile a user DSP application with the new updated release of *TORNADO-E6x* DSP software utilities (rev.4D), which come standard with all *TORNADO-E6x* boards.

However, in case user DSP application for initial firmware rev.1A of *TORNADO-E64xx* boards has been designed without DSP software utilities for *TORNADO-E6x* boards, which come standard with these boards, then the minor modifications are required in order to comply with firmware rev.1A-1 and rev.1A-2 of *TORNADO-E64xx* boards and apply to the initialization procedure for the TMS320C64xx DSP on-chip EMIF control registers as it is described later in this document.

**NOTE**

In order to stay up-to-date with the latest firmware modification and to minimize the software design efforts, it is recommended that user DSP applications for *TORNADO-E6x* boards are being designed using the latest release of *TORNADO-E6x* DSP software utilities, which come standard with all *TORNADO-E6x* boards and which are available from MicroLAB Systems FTP-site.

Extra DSP software modifications, which may be required, apply to the timing issues (DSP on-chip timers programming, software loop delays, etc) in case the TMS320C64xx DSP chip with increased DSP clock frequency is used in new *TORNADO-E64xx* boards (either 600 MHz, or 720 MHz, or 1 GHz).

There are no backward software compatibility problems known when running user DSP application designed for firmware rev.1A-1 and rev.1A-2 of *TORNADO-E64xx* boards at the *TORNADO-E64xx* boards with initial firmware rev.1A in case user DSP application has been designed using the latest release of *TORNADO-E6x* DSP software utilities. However, this requires clear understanding of all update details, which are described below in this document.



## Chapter 2. System Architecture and Construction

This chapter contains detail description for the new features available in the new firmware revisions of *TORNADO-E64xx* boards.

### 2.1 New features available in the firmware rev.1A-1 and rev.1A-2 for *TORNADO-E64xx* boards rev.1A

The following is a detail list of hardware updates for the firmware rev.1A-1 and rev.1A-2 of *TORNADO-E64xx* boards rev.1A against initial firmware rev.1A:

- The TMS320C64xx DSP memory map has been updated to include new *DSP\_CLK\_ID\_RG* and *XMEM\_LEN\_ID\_RG* external I/O control registers. Refer to [section 2.2](#) later in this chapter for more details.
- The DSP EMIF-A clock is external and is supplied as 125 MHz and 133 MHz for firmware rev.1A-1 and rev.1A-2 correspondingly. This allows to increase the SBSRAM/SDRAM data transfer performance by 25% and 33% correspondingly if compared to *TORNADO-E64xx* boards with 600 MHz DSP and initial firmware rev.1A. This modification requires the corresponding updates for the settings of the DSP on-chip EMIF-A control registers as it is described in [section 2.3](#) later in this chapter.
- The DSP EMIF-B clock is external and is supplied as 125 MHz and 133 MHz for firmware rev.1A-1 and rev.1A-2 correspondingly. This allows to increase the I/O control register read/write performance by 25% and 33% correspondingly if compared to *TORNADO-E64xx* boards with 600 MHz DSP and initial firmware rev.1A. This modification requires the corresponding updates for the settings of the DSP on-chip EMIF-B control registers as it is described in [section 2.3](#) later in this chapter.
- The *DEV\_REV\_ID\_RG* read-only I/O control register from the DSP environment reads as 2H and 3H for firmware rev.1A-1 and rev.1A-2 correspondingly in order the DSP application could recognize the firmware revision and to perform applicable actions as required. Refer to [section 2.4](#) later in this chapter for more details.
- New *DSP\_CLK\_ID\_RG* read-only I/O control register is added in the firmware rev.1A-1 and rev.1A-2, which returns the ID code for the DSP clock frequency (600 MHz, 720 MHz and 1 GHz). Given that, a user DSP application may now correctly handle all applicable timing issues (programming of the DSP on-chip timers, software loop delays, etc) and will therefore appear compatible with all speed grades of on-board TMS320C64xx DSP. Refer to [section 2.5](#) later in this chapter for more details.
- New *XMEM\_LEN\_ID\_RG* read-only I/O control register is added in the firmware rev.1A-1 and rev.1A-2, which returns the ID codes for the on-board SBSRAM capacity (none, 128Kx32, 256Kx32, and 512Kx32) and for the on-board SDRAM capacity (none, 4Mx64, 16Mx64). Given that, a user DSP application may now easily detect the on-board SBSRAM/SDRAM capacity in order to correspondingly configure the DSP on-chip EMIF-A SDRAM control registers and to correspondingly set the DSP application environment variables for external memory pools, etc. Refer to [section 2.6](#) later in this chapter for more details.

The corresponding sections below provide details about all new features and/or the corresponding update information applicable to the new firmware revisions of *TORNADO-E64xx* boards.

## 2.2 Updated TMS320C64xx DSP memory map

In firmware rev.1A-1 and rev.A-2, the DSP memory map for *TORNADO-E64xx* DSP controllers have been updated to include new *DSP\_CLK\_ID\_RG* and *XMEM\_LEN\_ID\_RG* read-only external I/O control registers as it is shown below in the updated table [2-2b].

*Table [2-2b]. TMS320C64xx DSP memory map for TORNADO-E64xx DSP controllers (firmware rev.1A, rev.1A-1, and rev.1A-2).*

DSP address area	DSP address range (bytes)	valid data bits	access mode	wait states	DSP EMIF area and mode
<b><i>TMS320C64xx DSP on-chip and external memory areas</i></b>					
DSP on-chip RAM (L2)	00000000H ..000FFFFFFH	D0..D31	r/w	-	-
DSP on-chip peripheral registers	01800000H ..01B7FFFFH  02000000H ..02000033H	D0..D31	r/w	-	-
FLASH/EPROM	64000000H ..641FFFFFFH	D0..D7	r/w	FWS	EMIF-B CE-1  8-bit ASYNC mode
SBSRAM	80000000H ..807FFFFFFH	D0..D63	r/w	4ws <sup>5)</sup>	EMIF-A CE-0  64-bit SBSRAM mode
SDRAM	A0000000H ..A7FFFFFFH	D0..D63	r/w	4ws <sup>5)</sup>	EMIF-A CE-2  64-bit SDRAM mode
<b><i>External peripherals and I/O expansion interfaces</i></b>					
I/O area: <i>dual-channel USART</i>	60000000H ..6000007EH (channel A)  60000080H ..600000FEH (channel B)	D0..D7	r/w	70ns (generated by on-board h/w)	EMIF-B CE-0  16-bit ASYNC mode

I/O area: <i>USB controller</i>	60020000H ..6002003EH	D0..D7	r/w	70ns (generated by on-board h/w)	
I/O area: <i>RTC controller</i>	60040000H ..6004007EH	D0..D7	r/w	160ns (generated by on-board h/w)	
I/O area: <i>SIOX rev.C parallel interface</i>	60120000H ..6012007FH	D0..D7	r/w	AWS + <i>SX_RDY</i>	
I/O area: <i>PIOX-16 parallel interface</i>	60100000H ..6011FFFFH	D0..D15	r/w	AWS + <i>PX_RDY</i>	
<i>External I/O control registers</i>					
I/O area: <i>DSP_EXT_INT4_SEL_RG</i> (DSP INT4 source selector control register)	60060000H	D0..D3	r/w	AWS	EMIF-B CE-0  16-bit ASYNC mode
I/O area: <i>DSP_EXT_INT5_SEL_RG</i> (DSP INT5 source selector control register)	60060002H	D0..D3	r/w	AWS	
I/O area: <i>DSP_EXT_INT6_SEL_RG</i> (DSP INT6 source selector control register)	60060004H	D0..D3	r/w	AWS	
I/O area: <i>DSP_EXT_INT7_SEL_RG</i> (DSP INT6 source selector control register)	60060006H	D0..D3	r/w	AWS	
I/O area: <i>DSP_NMI_SEL_RG</i> (DSP NMI source selector control register)	60060008H	D0..D3	r/w	AWS	
I/O area: <i>WDT_RESET_RG</i> (WDT reset control register)	6006000EH	written data is ignored	w	100ns (generated by on-board h/w)	
I/O area: <i>WDT_EN_RG</i> (WDT enable control register)	60060010H	D0..D3	r/w	AWS	

I/O area: <i>PXSX_RESET_RG</i> (PIOX/SIOX reset control register)	60060012H	D0..D3	r/w	AWS	
I/O area: <i>DEV_ID_RG</i> (device ID control register)	60060014H	D0..D3	r	AWS	
I/O area: <i>BMODE_RG</i> (bootmode control register)	60060016H	D0..D3	r	AWS	
I/O area: <i>SYS_CNF_RG</i> (system configuration register)	60060018H	D0..D3	r/w	AWS	
I/O area: <i>DEV_REV_ID_RG</i> (device revision ID register)	6006001AH	D0..D3	r/w	AWS	
I/O area: <a href="#"><i>XMEM_LEN_ID_RG</i></a> (external memory capacity ID register, f/w rev.1A-1 and rev.1A-2 only)	6006001CH	D0..D3	r/w	AWS	
I/O area: <a href="#"><i>DSP_CLK_ID_RG</i></a> (DSP clock ID register, f/w rev.1A-1 and rev.1A-2 only)	6006001EH	D0..D3	r/w	AWS	

- Notes:
1. *AWS* denotes number of software programmed wait states for accessing asynchronous TMS320C64xx DSP EMIF-B CE-0 area, which is a sum of read/write strobe wait states, read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
  2. *FWS* denotes number of software programmed framing wait states for accessing asynchronous DSP EMIF CE-1 area, which is a sum of read/write setup wait states and read/write hold wait states. Refer to the corresponding subsection below for more details.
  3. *SX\_RDY* and *PX\_RDY* denote extra wait states, which can be generated by external hardware ready signals for on-board SIOX-A rev.C site and PIOX/PIOX-16 site. Refer to the corresponding sections later in this chapter for more details about SIOX and PIOX expansion interface sites.
  4. Number of SBSRAM/SDRAM wait states is defined by EMIF-A interface clock, which is hardware configured to DSPCLK/4. EMIF-A CE-0 and CE-2 secondary control registers shall be configured to set *SNCCCLK* bit of these registers to the '0' state in order to synchronize EMIF-A CE-0/CE-2 spaces to EMIF-A ECLKOUT1 clock. Refer to original TI documentation and to the corresponding subsection below for more details.
  5. Other DSP memory and I/O areas are reserved. Do not use these address areas.
  6. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

## 2.3 Updated settings for the TMS320C64xx DSP on-chip EMIF control registers

The TMS320C64xx DSP on-chip EMIF-A/B control registers are set upon the *TORNADO-E64xx* board firmware revision and the DSP clock frequency (for initial firmware rev.1A only) as it is listed below in the updated table [2-3b].

*Table [2-3b]. Recommended settings for TMS320C64xx DSP on-chip EMIF control registers for TORNADO-E64xx DSP controllers (firmware rev.1A, rev.1A-1, and rev.1A-2).*

<b>TMS320C64x DSP on-chip EMIF control register</b>	<b><i>TORNADO-E64xx f/w rev.1A</i></b> (500 MHz DSP clock, TMX-grade silicon, 125MHz EMIF-A/B clock)	<b><i>TORNADO-E64xx f/w rev.1A</i></b> (600 MHz DSP clock, 100MHz EMIF-A/B clock)	<b><i>TORNADO-E64xx f/w rev.1A-1</i></b> (600/720/1000 MHz DSP clock, 125MHz EMIF-A/B clock)	<b><i>TORNADO-E64xx f/w rev.1A-2</i></b> (600/720/1000 MHz DSP clock, 133MHz EMIF-A/B clock)
<b>EMIF-A interface control registers</b>				
<i>EMIF-A Global Control Register (EMIFA_GCR)</i>	0x0009277C	0x0009277C	0x0009277C	0x0009277C
<i>EMIF-A CE-0 Space Control Register (EMIFA_CE0_SCR) (controls on-board SBSRAM)</i>	0x000000e0 64-bit SBSRAM mode	0x000000e0 64-bit SBSRAM mode	0x000000e0 64-bit SBSRAM mode	0x000000e0 64-bit SBSRAM mode
<i>EMIF-A CE-0 Space Secondary Control Register (EMIFA_CE0_SEC)</i>	0x00000002	0x00000002	0x00000002	0x00000002
<i>EMIF-A CE-1 Space Control Register (EMIFA_CE1_SCR) (unused, leave as default)</i>	0xfffff03 default 8-bit ASYNC mode	0xfffff03 default 8-bit ASYNC mode	0xfffff03 default 8-bit ASYNC mode	0xfffff03 default 8-bit ASYNC mode
<i>EMIF-A CE-2 Space Control Register (EMIFA_CE2_SCR) (controls on-board SDRAM)</i>	0x000000d0 64-bit SDRAM mode	0x000000d0 64-bit SDRAM mode	0x000000d0 64-bit SDRAM mode	0x000000d0 64-bit SDRAM mode
<i>EMIF-A CE-2 Space Secondary Control Register (EMIFA_CE2_SEC)</i>	0x00000002	0x00000002	0x00000002	0x00000002

<i>EMIF-A CE-3 Space Control Register (EMIFA_CE3_SCR) (unused, leave as default)</i>	0xffffffff03 default 8-bit ASYNC mode	0xffffffff03 default 8-bit ASYNC mode	0xffffffff03 default 8-bit ASYNC mode	0xffffffff03 default 8-bit ASYNC mode
<i>EMIF-A SDRAM Control Register (EMIFA_SDRAM_CR)</i>	0x57117000 (if on-board SDRAM is 4Mx64)  0x63117000 (if on-board SDRAM is 16Mx64)	0x57115000 (if on-board SDRAM is 4Mx64)  0x63115000 (if on-board SDRAM is 16Mx64)	0x57117000 (if on-board SDRAM is 4Mx64)  0x63117000 (if on-board SDRAM is 16Mx64)	0x57117000 (if on-board SDRAM is 4Mx64)  0x63117000 (if on-board SDRAM is 16Mx64)
<i>EMIF-A SDRAM Timing Register (EMIFA_SDRAM_TMR)</i>	1952 (if on-board SDRAM is 4Mx64)  976 (if on-board SDRAM is 16Mx64)	1562 (if on-board SDRAM is 4Mx64)  781 (if on-board SDRAM is 16Mx64)	1952 (if on-board SDRAM is 4Mx64)  976 (if on-board SDRAM is 16Mx64)	282 (if on-board SDRAM is 4Mx64)  1041 (if on-board SDRAM is 16Mx64)
<i>EMIF-A SDRAM Extension Register (EMIFA_SDRAM_EXT)</i>	0x00014D29	0x00014D29	0x00014D29	0x00014D29
<b>EMIF-B interface control registers</b>				
<i>EMIF-B Global Control Register (EMIFB_GCR)</i>	0x0001207c	0x0001207c	0x0001207c	0x0001207c
<i>EMIF-B CE-0 Space Control Register (EMIFB_CE0_SCR)</i>  (controls external I/O control registers, USART, USB and RTC controllers, PIOX-16 site, SIOX-A rev.C site)	0x21124411  16-bit ASYNC mode strobe: 4 clk (32ns) setup: 2 clk (16ns) hold: 1 clk (8ns)	0x20d24311  16-bit ASYNC mode strobe: 3 clk (30ns) setup: 2 clk (20ns) hold: 1 clk (10ns)	0x21124411  16-bit ASYNC mode strobe: 4 clk (32ns) setup: 2 clk (16ns) hold: 1 clk (8ns)	0x21224412  16-bit ASYNC mode strobe: 4 clk (30ns) setup: 2 clk (15ns) hold: 1 clk (7.5ns)
<i>EMIF-B CE-1 Space Control Register (EMIFB_CE1_SCR)</i>  (area controls 8-bit EPROM/FLASH)	0x23524d01  8-bit ASYNC mode strobe:13 clk (104ns) setup: 2 clk (16ns) hold: 1 clk (8ns)	0x22924a01  8-bit ASYNC mode strobe:10 clk (100ns) setup: 2 clk (20ns) hold: 1 clk (10ns)	0x23524d01  8-bit ASYNC mode strobe:13 clk (104ns) setup: 2 clk (16ns) hold: 1 clk (8ns)	0x23d24e01  8-bit ASYNC mode strobe:14 clk (100ns) setup: 2 clk (15ns) hold: 1 clk (7.5ns)
<i>EMIF-B CE-3 Space Control Register (EMIFB_CE3_SCR) (unused, leave as default)</i>	0xffffffff03 default 8-bit ASYNC mode	0xffffffff03 default 8-bit ASYNC mode	0xffffffff03 default 8-bit ASYNC mode	0xffffffff03 default 8-bit ASYNC mode

<i>EMIF-B CE-3 Space Control Register (EMIFB_CE3_SCR) (unused, leave as default)</i>	0xfffff03 default 8-bit ASYNC mode	0xfffff03 default 8-bit ASYNC mode	0xfffff03 default 8-bit ASYNC mode	0xfffff03 default 8-bit ASYNC mode
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Notes: 1. EMIF-A and EMIF-B interfaces of TMS320C64xx DSP are assumed to run at DSPCLK/4 for *TORNADO-E64xx* f/w rev.1A with 500 MHz TMX-grade DSP, at DSPCLK/6 for *TORNADO-E64xx* f/w rev.1A with 600 MHz DSP, and at external 125MHz and 133MHz clock for *TORNADO-E64xx* f/w rev.1A-1 and rev.1A-2 correspondingly.

## 2.4 Updated *DEV\_REV\_ID\_RG* I/O control register

*TORNADO-E64xx* boards provide the *DEV\_REV\_ID\_RG* read-only I/O control register, which returns a 4-bit device firmware revision ID code.

***DEV\_REV\_ID\_RG* I/O control register (r)**  
(*TORNADO-E64xx* only)

X	<i>DEV_REV_ID_3</i> (r)	<i>DEV_REV_ID_2</i> (r)	<i>DEV_REV_ID_1</i> (r)	<i>DEV_REV_ID_0</i> (r)
bit-15...bit-4 ( <i>TORNADO-E64xx</i> )	bit-3	bit-2	bit-1	bit-0

Table 2-X1 below provides a list of firmware revision ID codes available for *TORNADO-E64xx* boards.

**Table 2-X1.** Firmware revision ID codes available via the *DEV\_REV\_ID\_RG* I/O control register of *TORNADO-E64xx* boards.

register bit(s)	Access mode	Description
{ <i>DEV_REV_ID_3..0</i> }	R	<p>Returns a firmware revision ID code.</p> <p>{<i>DEV_REV_ID_3..0</i>} = {0,0,0,1} setting corresponds to initial firmware rev.1A of <i>TORNADO-E64xx</i> boards with 500MHz TMX-grade DSP (125MHz EMIF-A/B clock frequency) and 600MHz DSP (100MHz EMIF-A/B clock frequency).</p> <p>{<i>DEV_REV_ID_3..0</i>} = {0,0,1,0} setting corresponds to the firmware rev.1A-1 of <i>TORNADO-E64xx</i> boards with 600/720/1000MHz DSP (125MHz EMIF-A/B clock frequency).</p> <p>{<i>DEV_REV_ID_3..0</i>} = {0,0,1,1} setting corresponds to the firmware rev.1A-2 of <i>TORNADO-E64xx</i> boards with 600/720/1000MHz DSP (133MHz EMIF-A/B clock frequency).</p> <p>Other {<i>DEV_REV_ID_3..0</i>} codes are reserved for future expansion.</p>

2.5 New *DSP\_CLK\_ID\_RG* I/O control register for f/w rev.1A-1 and rev.1A-2

*TORNADO-E64xx* boards with firmware rev.1A-1 and rev.1A-2 provide new *DSP\_CLK\_ID\_RG* read-only I/O control register, which returns a 2-bit DSP clock frequency ID code.

*DSP\_CLK\_ID\_RG* I/O control register (r)  
(*TORNADO-E64xx* only with f/w rev.1A-1 and rev.1A-2)

X	0	0	<i>DSP_CLK_FREQ_ID-1</i> (r)	<i>DSP_CLK_FREQ_ID-0</i> (r)
bit-15...bit-4 ( <i>TORNADO-E64xx</i> )	bit-3	bit-2	bit-1	bit-0

The DSP clock frequency ID code is used to identify the DSP clock frequency and to correspondingly adjust the timing parameters of a user DSP application (programming of the DSP on-chip timers, software loop delays, programming the bit rate frequency of DSP on-chip McBSP ports, etc) and thus making an application compatible with all speed grades of TMS320C64xx DSP used in *TORNADO-E64xx* boards.

NOTE

The *DSP\_CLK\_ID\_RG* read-only I/O control register is not available in *TORNADO-E64xx* boards with initial firmware rev.1A.

Table 2-X2 below provides a list of DSP clock frequency ID codes available for the firmware rev.1A-1 and rev.1A-2 of *TORNADO-E64xx* boards.

Table 2-X2. DSP clock frequency ID codes available via the *DSP\_CLK\_ID\_RG* I/O control register of *TORNADO-E64xx* boards with f/w rev.1A-1 and rev.1A-2.

register bit(s)	access mode	Description
{ <i>DSP_CLK_FREQ_ID-1..0</i> }	r	Returns a DSP clock frequency ID code.  { <i>DSP_CLK_FREQ_ID-1..0</i> } = {0,0} setting corresponds to the 600MHz speed grade of TMS320C64xx DSP.  { <i>DSP_CLK_FREQ_ID-1..0</i> } = {0,1} setting corresponds to the 720MHz speed grade of TMS320C64xx DSP.  { <i>DSP_CLK_FREQ_ID-1..0</i> } = {1,0} setting corresponds to the 1GHz speed grade of TMS320C64xx DSP.  { <i>DSP_CLK_FREQ_ID-1..0</i> } = {1,1} setting is reserved.



Although the *DSP\_CLK\_ID\_RG* read-only I/O control register was not available in *TORNADO-E64xx* boards with initial firmware rev.1A, there is a simple way to identify the DSP clock frequency for firmware rev.1A from the DSP software using the TMS320C64xx DSP on-chip silicon revision ID register.

The *TORNADO-E64xx* boards with initial firmware rev.1A have been manufactured using either 500MHz TMX-grade silicon revision 1.0 TMS320C64xx DSP or 600MHz TMS-grade silicon revision 1.03 DSP. The *DSP silicon revision* for TMS320C64xx DSP is identified via bits #16..19 of 32-bit DSP on-chip register at a memory address 0x01B00200, which return the 0001B binary value for 600MHz TMS320C64xx silicon revision 1.03. Any other value (typically 0000B) returned by these bits correspond to the 500MHz TMX-grade silicon revision 1.0 DSP for *TORNADO-E64xx* boards with firmware rev.1A.

## 2.6 New *XMEM\_LEN\_ID\_RG* I/O control register for f/w rev.1A-1 and rev.1A-2

*TORNADO-E64xx* boards with firmware rev.1A-1 and rev.1A-2 provide new *XMEM\_LEN\_ID\_RG* read-only I/O control register, which returns the ID codes for on-board SBSRAM and SDRAM memory capacities.

***XMEM\_LEN\_ID\_RG* I/O control register (r)**  
(*TORNADO-E64xx* only with f/w rev.1A-1 and rev.1A-2)

X	<i>SDRAM_LEN_ID-1</i> (r)	<i>SDRAM_LEN_ID-0</i> (r)	<i>SBSRAM_LEN_ID-1</i> (r)	<i>SBSRAM_LEN_ID-0</i> (r)
bit-15...bit-4 ( <i>TORNADO-E64xx</i> )	bit-3	bit-2	bit-1	bit-0

The SBSRAM/SDRAM capacity ID codes are used to identify on-board DSP external memory capacity in order to correspondingly configure the DSP on-chip EMIF-A SDRAM control registers and to correspondingly set the DSP application environment variables for external memory pools, etc.

### NOTE

The *XMEM\_LEN\_ID\_RG* read-only I/O control register is not available in *TORNADO-E64xx* boards with initial firmware rev.1A.

Table 2-X3 below provides a list of SBSRAM/SDRAM capacity ID codes available for the firmware rev.1A-1 and rev.1A-2 of *TORNADO-E64xx* boards.

Table 2-X3. SBSRAM/SDRAM capacity ID codes available via the *XMEM\_LEN\_ID\_RG* I/O control register of *TORNADO-E64xx* boards with f/w rev.1A-1 and rev.1A-2.

register bit(s)	access mode	Description
{ <i>SBSRAM_LEN_ID-1..0</i> }	r	<p>Returns a capacity ID code for on-board SBSRAM memory bank.</p> <p>{<i>SBSRAM_LEN_ID-1..0</i>} = {0,0} setting corresponds to no SBSRAM memory installed.</p> <p>{<i>SBSRAM_LEN_ID-1..0</i>} = {0,1} setting corresponds to the 128Kx64 SBSRAM memory installed.</p> <p>{<i>SBSRAM_LEN_ID-1..0</i>} = {1,0} setting corresponds to the 256Kx64 SBSRAM memory installed.</p> <p>{<i>SBSRAM_LEN_ID-1..0</i>} = {1,1} setting corresponds to the 512Kx64 SBSRAM memory installed.</p>
{ <i>SDRAM_LEN_ID-1..0</i> }	r	<p>Returns a capacity ID code for on-board SDRAM memory bank.</p> <p>{<i>SDRAM_LEN_ID-1..0</i>} = {0,0} setting corresponds to no SDRAM memory installed.</p> <p>{<i>SDRAM_LEN_ID-1..0</i>} = {0,1} setting corresponds to the 4Mx64 SDRAM memory installed.</p> <p>{<i>SDRAM_LEN_ID-1..0</i>} = {1,0} setting corresponds to the 16Mx64 SDRAM memory installed.</p> <p>{<i>SDRAM_LEN_ID-1..0</i>} = {1,1} setting is reserved.</p>