

TORNADO-E54x

Stand-alone DSP Controllers with 16-bit Fixed-Point TMS320C54x DSP

User's Guide

covers:
TORNADO-E548/E549/E5402/
E5409/E5410/E5416 rev.2A

MicroLAB Systems Ltd

59a Beskudnikovsky blvd, 127486, Moscow, RUSSIA

phone/fax: +7-(095)-485-6332 WWW: <http://www.mlabsys.com> Email: info@mlabsys.com

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About this Document

This user's guide contains description for **TORNADO-E54x** (**TORNADO-E548/E549/E5402/E5409/E5410/E5416**) rev.2A stand-alone digital signal processing (DSP) controllers with high performance 16-bit fixed-point TMS320C54x DSP (TMS320LC548, TMS320VC549, TMS320VC5402, TMS320VC5409, TMS320VC5410, TMS320VC5416) from Texas Instruments Inc (TI).

1. **TMS320C54x, TMS320LC54x, TMS320VC54x Fixed-point DSP.** Texas Instruments Inc, SPRS039B, 1998.
2. **TMS320C5402 Fixed-point DSP.** Texas Instruments Inc, SPRS079C, 1998.
3. **TMS320C5410 Fixed-point DSP.** Texas Instruments Inc, SPRS075D, 2000.
4. **TMS320C5409 Fixed-point DSP.** Texas Instruments Inc, SPRS082B, 1999.
5. **TMS320C5416 Fixed-point DSP.** Texas Instruments Inc, SPRS095E, 2000.
6. **TMS320C54x. CPU and Peripherals. Reference Guide.** Texas Instruments Inc, SPRU131F, 2000.
7. **TMS320C54x DSP Reference Set. Volume 5: Enhanced Peripherals.** Texas Instruments Inc, SPRU302, 1999.
8. **TMS320C5000 DSP Family Functional Overview.** Texas Instruments Inc, SPRU307, 1999.

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Chapter 1. Introduction

This chapter contains general description for *TORNADO-E54x* stand-alone DSP controllers product line, which comprises of *TORNADO-E548/E549/E5402/E5409/E5410/E5416* DSP controllers.

CAUTION

TORNADO-E54x stand-alone DSP controllers are designed to accommodate 16-bit fixed-point TMS320C54x DSP (TMS320LC548, TMS320VC549, TMS320VC5402, TMS320VC5409, TMS320VC5410, TMS320VC5416) from Texas Instruments Inc (TI). The particular DSP installed specifies the final name of *TORNADO-E54x* DSP controller, i.e. *TORNADO-E548/E549/E5402/E5409/E5410/E5416*.

Hereafter in this document the '*TORNADO-E54x*' denotes that the supplied information is applicable to all *TORNADO-E54x* DSP controllers, which are comprised of *TORNADO-E548/E549/E5402/E5409/E5410/E5416* DSP controllers.

Should information be a product specific, then the name of the corresponding product (*TORNADO-E548/E549/E5402/E5409/E5410/E5416*) will be highlighted.

1.1 General Information

TORNADO-E54x (fig.1-1) are high performance 16-bit fixed-point DSP controllers for stand-alone DSP applications. *TORNADO-E54x* DSP controllers meet industry standard 3U form-factor and feature flexible modular system construction with daughter-card modules (DCM) in order to meet requirements for multiple applications while keeping a cost to a minimum.

CAUTION

System architecture and construction of *TORNADO-E54x* DSP controllers are compatible with that for *TORNADO-E* DSP controllers product line, and the only difference implies to the DSP type and on-board memory capacity.



Fig.1-1. TORNADO-E54x DSP controller.

Overview

TORNADO-E54x DSP controllers are based around TI 16-bit fixed-point TMS320C54x DSP (TMS320LC548, TMS320VC549, TMS320VC5402, TMS320VC5409, TMS320VC5410, or TMS320VC5416) with maximum DSP performance up to 160 MIPS.

On-board memory comprises of 128Kx16 program SRAM, 128Kx16 data SRAM, and of optional 1Mx8 FLASH/EPROM for boot code and non-volatile data.

TORNADO-E54x DSP controllers offer extensive set of on-board interfaces for communication with external host computers and peripherals:

- dual-channel 10Mbit/s USART (universal synchronous/asynchronous receiver/transmitter) with and external RS232C/RS422 interfaces allows direct connections to host computers, networks, and peripherals using industry standard HDLC/SDLC/BISYNC/MONOSYNC synchronous and ASYNC asynchronous protocols.
- 12 Mbit/s USB rev.1.1 slave interface allows easy connection to host computers and can be used for fast bulk data transfers
- TMS320C54x DSP on-chip 8-bit HPI port allows access to DSP on-chip memory and DSP boot from any host controller/computer using simple parallel 8-bit interface.

TMS320C54x DSP can start either in microprocessor mode without boot, or in microcontroller mode with boot from either on-board FLASH/EPROM or DSP HPI port.

A set of on-board peripherals also include general purpose 8-bit parallel digital I/O for local system control, watchdog timer, and a set of configuration and control registers.

external real-time I/O

TORNADO-E54x DSP controller has been designed with modular construction in mind and provides several on-board I/O expansion facilities for installation of DCM. This allows quick system configuration using 'of-the-shelf' DCM in order to meet customer application requirements.

At first, on-board SIOX (serial I/O expansion) rev.B and SIOX rev.C sites allows installation of one SIOX rev.B/C DCM. A variety of ‘of-the-shelf’ **TORNADO** SIOX rev.B/C DCM comprises of AD/DA/DIO and application specific DCM for real-time telecom, speech/fax/modem, audio, instrumentation, industrial, digital radio, etc signal processing applications.

AT second, on-board MXSIOX connector allows connection to external **T/SU-X1** SIOX rev.B mini-extender kit, which can be used for installation of one SIOX rev.B DCM. This facility is available for **TORNADO-E548/E549/E5409/E5410/E5416** DSP controllers only with three DSP on-chip BSP/TDM or McBSP serial ports.

Finally, one site for **TORNADO** parallel I/O expansion (PIOX-16) DCM can be used for installation of one PIOX-16 DCM. A variety of ‘of-the-shelf’ **TORNADO** PIOX-16 DCM comprises of AD/DA/DIO, application-specific and DSP coprocessor DCM for real time multi-channel high-speed telecom, instrumentation, industrial, digital radio, etc signal processing applications.

Figure 1-2 illustrates installation of different DCM at **TORNADO-E54x** DSP controller board and connection of external **T/SU-X1** SIOX rev.B mini-extender kit with one SIOX rev.B DCM.

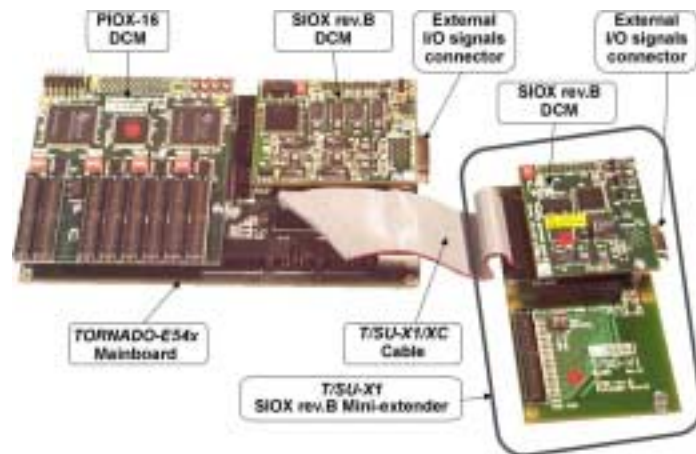


Fig.1-2. **TORNADO-E54x** DSP controller with installed SIOX rev.B and PIOX-16 DCM and **T/SU-X1** external SIOX rev.B mini-extender kit with one SIOX rev.B DCM installed.

Applications

TORNADO-E54x stand-alone DSP controllers have been designed for general purpose embedded and stand-alone DSP applications with communication with external host computers/peripherals and real-time signal I/O. The following are only few of many applications for **TORNADO-E54x** DSP controllers:

- *fax/modem communication*
- *vocoders and speech signal processing*
- *computer telephony and IP telephony*
- *networking*
- *audio and acoustics signal processing*
- *multimedia*
- *radars*

- digital radio
- instrumentation and industrial
- evaluation and education
- many more ...

1.2 Technical Specification

The following are the technical specifications for *TORNADO-E54x* DSP controllers.

<u>Parameter description</u>	<u>parameter value</u>
power supply voltages	+5V for <i>TORNADO-E54x</i> board, optional -5V and ± 12 V for SIOX/PIOX-16 DCM
power consumption	+5V@1.0A (t=+20°C)
board dimensions	3U (100x160 mm)
operating temperature	+0°C..+55°C
maximum DSP performance	80 MIPS (<i>TORNADO-E548/E5409</i>) 100 MIPS (<i>TORNADO-E549/5402/5410</i>) 160 MIPS (<i>TORNADO-E5416</i>)
on-board DSP input clock (CLKIN) frequency	80 MHz (<i>TORNADO-E548/E5409</i>) 100 MHz (<i>TORNADO-E549/5410</i>) 50 MHz (<i>TORNADO-E5402</i>) 32 MHz (<i>TORNADO-E5416</i>)
TMS320C54x DSP bootmodes	<i>microprocessor mode</i> with no boot <i>microcontroller mode</i> : boot from 8-bit FLASH/EPROM boot from HPI
I/O expansion interfaces	- one site for SIOX rev.B DCM, - one site for SIOX rev.C DCM, - <i>TORNADO-E548/E549/E5409/E5410/E5416</i> : one on-board MXSIOX connector for connection to external SIOX rev.B mini- extender kit (<i>T/SU-X1</i>), which can carry one SIOX rev.B DCM - one site for PIOX-16 DCM.
I/O signal level for I/O expansion interfaces (SIOX rev.B, SIOX rev.C, MXSIOX, PIOX-16)	3v/5v TTL

on-board memory:

external program SRAM area	128Kx16 (2 pages of 64Kx16 each), 1ws
external data SRAM area	<i>TORNADO-E548/E549/E5409/E5410/E5416:</i> 128Kx16 (4 pages of 32Kx16 each), 1ws <i>TORNADO-E5402:</i> 128Kx16 (2 pages of 64Kx16 each), 1ws
FLASH/EPROM memory capacity	128K..1Mx8 (Ta=100ns) with write-protection feature

watchdog timer (WDT) and reset controller:

WDT latency period	1.6 sec typical
duration of external reset input signal	>500 ns
duration of the output DSP reset signal	0.2 sec typ

on-board parallel digital I/O

8 bits
(I/O signal levels: 5v TTL)

on-board USART (universal synchronous/asynchronous receiver/transmitter):

number of channels	2
supported protocols for each channel	<i>synchronous:</i> HDLC/X.25, SDLC, MONOSYNC, BISYNC <i>asynchronous:</i> ASYNC
external electrical interfaces for each channel	RS232C or RS422 (EIA-530 pinout)
maximum data transfer speed for synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) and external RS422 interface	10 Mbit/s
maximum data transfer speed for asynchronous protocol (ASYNC) and external RS232C interface	115 kBaud
maximum data transfer speed for asynchronous protocol (ASYNC) and external RS422 interface	2.5 MBaud
maximum frequency of on-board USART master clock oscillator (socket S2)	10 MHz
I/O signal levels for external T/R clock outputs	5v TTL

on-board HPI interface

TMS320C54x 8-bit HPI port
(I/O signal levels: 3v/5v TTL)

on-board USB interface

12 Mbit/s USB device interface, meets USB specs rev.1.1, USB type B connector pinout

external RESET input:

active low signal duration	>2uS
input signal level	3v/5v TTL
I/O signal level for JTAG interface	3v/5v TTL

Chapter 2. System Architecture and Construction

This chapter contains description for *TORNADO-E54x* system architecture, construction, host interfaces, and I/O expansion facilities.

2.1 *TORNADO-E54x* System Architecture

System architecture and construction for *TORNADO-E54x* DSP controllers are presented at figures 2-1 and 2-2 correspondingly.

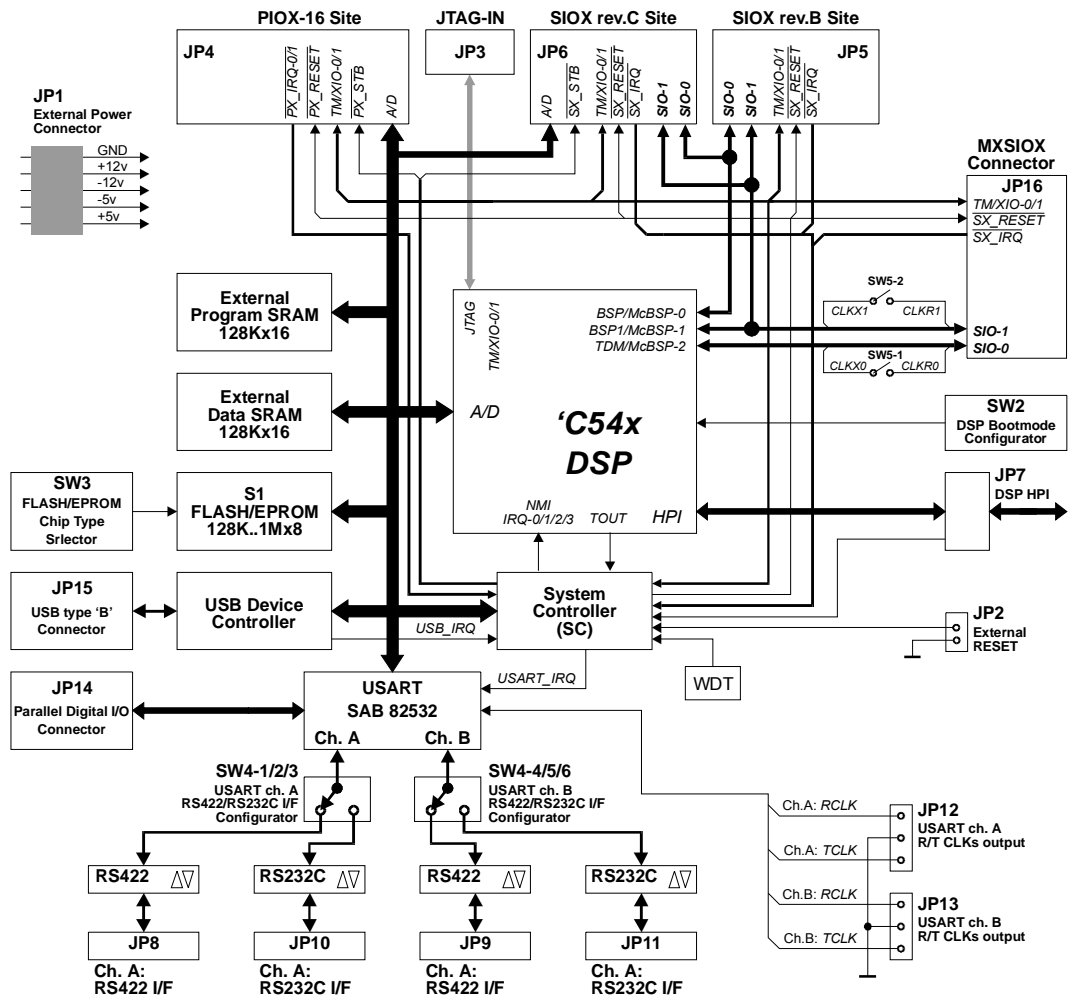


Fig.2-1. Block diagram of *TORNADO-E54x* DSP controller.

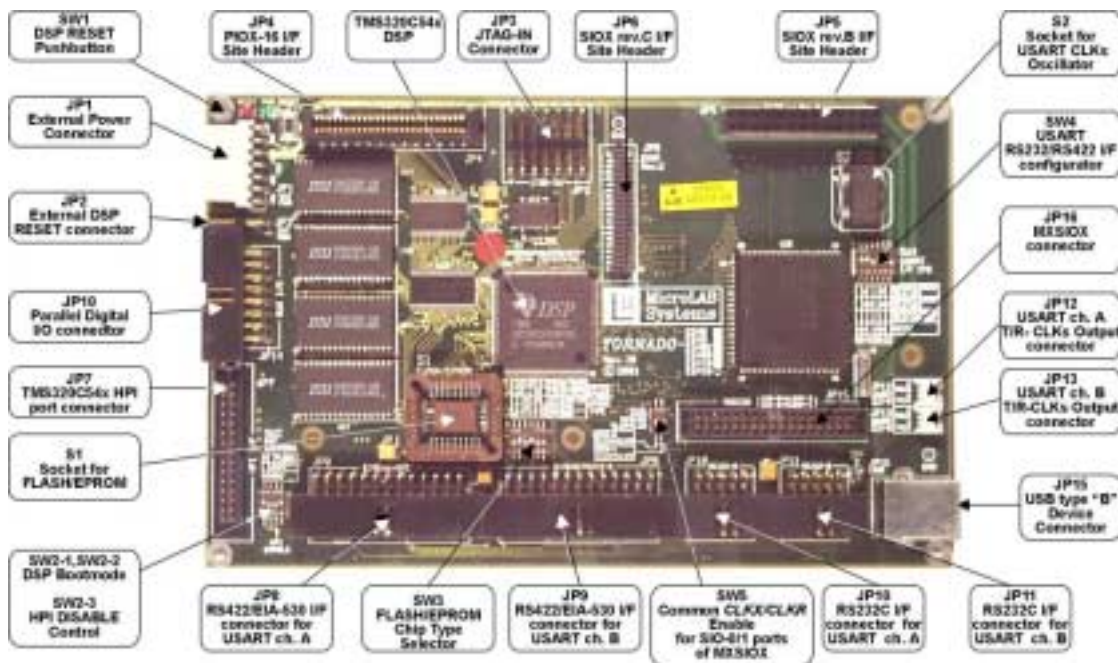


Fig.2-2. Construction of TORNADO-E54x DSP controller.

TORNADO-E54x DSP controller comprises of the following components:

- 16-bit fixed-point TMS320C54x DSP (TMS320LC548, TMS320VC549, TMS320VC5402, TMS320VC5409, TMS320VC5410, TMS320VC5416) running at up to 160MHz depending upon the DSP installed
- 128Kx16 of on-board program static RAM (SRAM) and 128Kx16 of on-board data SRAM
- up to 1Mx8 of on-board FLASH/EPROM
- dual-channel multi-protocol 10Mbit/s USART (universal synchronous/asynchronous receiver/transmitter), which supports HDLC/X.25, SDLC, MONOSYNC, BISYNC, ASYNC protocols
- interface multiplexer (UIF-MUX) for each of USART channel, which connects either to 115 kBaud RS232C or 10 Mbit/s RS422/EIA-530 interfaces
- 8-bit parallel digital I/O controller (as the part of USART) with individual polarity and mask for generation of DSP interrupt generation
- 12 Mbit/s USB device controller and JP15 USB type B connector
- JP7 connector for external connection to TMS320C54x DSP HPI port
- TORNADO serial I/O expansion (SIOX) rev.B and rev.C interface sites (JP5 and JP6) for installation of the corresponding DCM
- MXSIOX connector (JP16) for connection to one external T/SU-X1 SIOX rev.B mini-extender kit, which can carry one SIOX rev.B DCM
- TORNADO parallel I/O expansion (PIOX-16) interface site (JP4) for installation of the corresponding DCM
- watch-dog timer (WDT)
- system controller (SC)

- DSP reset controller (RC) and external RESET connector (JP2)
- JTAG-IN connector (JP3) for connection to external JTAG emulator
- external power connector (JP1)

TMS320C54x DSP

TORNADO-54x DSP controllers have been designed to accommodate different compatible high-performance 16-bit fixed point TMS320C54x DSP with the only differences applied to DSP performance, amount of DSP on-chip memory and a set of DSP on-chip peripherals:

- 80MIPS TMS320LC548 DSP in **TORNADO-E548**
- 100MIPS TMS320VC549 DSP in **TORNADO-E549**
- 100MIPS TMS320VC5402 DSP in **TORNADO-E5402**
- 80MIPS TMS320VC5409 DSP in **TORNADO-E5409**
- 100MIPS TMS320VC5410 DSP in **TORNADO-E5410**
- 160MIPS TMS320VC5416 DSP in **TORNADO-E5416**.

TMS320C54x DSP can start either in microprocessor mode without boot, or in microcontroller mode with boot from either on-board FLASH/EPROM or DSP HPI port.

Static RAM (SRAM) for Program and Data

TORNADO-E54x DSP controllers provides on-board 256Kx16 static RAM (SRAM) for TMS320C54x DSP, which comprises of 128Kx16 DSP external program SRAM and 128Kx16 DSP external data SRAM areas.

On-board 128Kx16 program SRAM is directly mapped into DSP program memory space (two 64Kx16 memory pages #0 and #1) and on-board TMS320C54x DSP can directly access this memory using extended program memory addressing capabilities.

On-board 128Kx16 data SRAM is organized as the multi-page memory with on-board extended data memory addressing hardware (via extended data memory page register *XDMP_RG*), which is used to switch between these data memory pages from the DSP software. On-board DSP external data SRAM organization differs for different **TORNADO-E54x** DSP systems as the following:

- on-board 128Kx16 external data SRAM for **TORNADO-E548/E549/E5409/E5410/E5416** is organized as four pages of 32Kx16 each with each page being mapped into the DSP off-chip data memory address space of TMS320LC548/VC549/VC5409/VC5410/VC5416 DSP
- on-board 128Kx16 external data SRAM for **TORNADO-E5402** is organized as two pages of 64Kx16 each with each page mapped into the upper 48Kx16 DSP off-chip data memory address space of TMS320VC5402 DSP.

FLASH/EPROM Memory

TORNADO-E54x provides up to 1Mx8 of on-board FLASH/EPROM memory for DSP boot code and non-volatile data memory. FLASH/EPROM memory bank is designed to accommodate a variety of FLASH or EPROM memory chip in the PLCC-32 package.

On-board FLASH/EPROM memory is allocated into DSP external data memory area and can be selected alternatively to on-board external data SRAM using on-board extended data memory page register *XDMP_RG*.

Dual-channel USART

TORNADO-E54x features the on-board dual-channel USART (universal synchronous/asynchronous receiver/transmitter) for communication with host computers, terminals, network adapters, or external peripherals.

USART supports industry standard synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) at up to 10 Mbit/s data transfer rate, and industry standard asynchronous protocol (ASYNC) at up to 2.5 MBaud independently for each channel.

Each USART channel connects to external equipment via on-board configurable RS232C or RS422/EIA-530 electrical interface.

USB device interface

TORNADO-E54x rev.2A provides the on-board 12 Mbit/s USB device interface for communication with external host computers. On-board USB interface connector is the USB type 'B' device connector. USB device controller and external interface meets USB rev.1.1 specifications.

TMS320C54x HPI (host port interface)

TORNADO-E54x DSP controller offers access from external host computer to TMS320C54x DSP on-chip 8-bit HPI port, which allows access from to DSP on-chip memory, mutual interrupt generation, and to perform HPI boot procedure.

HPI assumes that the HPI memory address must be pre-latched into HPI address register prior HPI data access will be performed. However, the HPI address auto post-incrementing feature is available and simplifies data array upload/download.

Parallel digital I/O

TORNADO-E54x provides general purpose 8-bit parallel digital I/O, which might be used as external control I/O signals. These digital I/O signals are the part of on-board USART, and allow generation of DSP interrupt on individually programmable high-to-low or low-to-high transitions when programmed as input pins.

TORNADO-E5402/E5409/E5416 DSP controllers also allows to use 8-bit data lines of TMS320C54x DSP on-chip port as general purpose I/O pins in case DSP on-chip HPI port feature is disabled. This increases total number of general purpose I/O pins for **TORNADO-E5402/E5409/E5416** DSP controllers to 16 pins.

Serial I/O Expansion Interface (SIOX) sites

TORNADO-E54x on-board SIOX interface sites and comprises of one SIOX rev.B site, one enhanced SIOX rev.C site, and on-board MXSIOX connector (**TORNADO-E548/E549/E5409/E5410/E5416** only) for connection to external **T/SU-X1** SIOX rev.B mini-extender kit, and shall be used for installation of compatible SIOX rev.B and rev.C DCM.

TORNADO SIOX AD/DA/DIO and application specific DCM include a variety of 'of-the-shelf' DSCM for telecom, speech/fax/modem, audio, and many more applications.

SIOX rev.B site includes signals for two TMS320C54x DSP on-chip McBSP serial ports, two timers/IO pins, and three dedicated SIOX interrupt request inputs, whereas SIOX rev.C provides optional 8-bit parallel data bus with 6-bit address and data strobes.

On-board MXSIOX connector (*TORNADO-E548/E549/E5409/E5410/E5416* only) can be used for connection to one external *T/SU-X1* SIOX rev.B mini-extender kit, which can carry one SIOX rev.B DCM, and includes signals for two TMS320C54x DSP on-chip McBSP serial ports, two timers/IO pins, and two dedicated SIOX interrupt request inputs.

Parallel I/O Expansion Interface (PIOX-16) site

TORNADO-E54x feature PIOX-16 interface site for installation of high-speed AD/DA/DIO DCM. PIOX-16 interface is allocated into TMS320C54x DSP external I/O area.

PIOX-16 interface comprises of the signals for DSP 16-bit address and 16-bit data buses, data strobes, two timer/IO pins and two dedicated PIOX-16 interrupt request inputs.

PIOX-16 compatible DCM include a variety of high-speed multi-channel AD/DA/DIO modules for high-speed telecom, instrumentation, digital radio and many more applications.

Watch-dog timer (WDT)

TORNADO-E54x provides optional on-board watch-dog timer (WDT) for reliable stand-alone operation. While the DSP is operating properly and in-case the WDT feature is enabled, DSP must send the WDT reset signal every 1.6 sec, otherwise WDT will generate the DSP reset signal in order to restart *TORNADO-E54x*.

DSP Reset Control

The DSP reset signal for *TORNADO-E54x* is generated by the DSP reset controller (RC) on the power-on/off conditions, external reset condition, on-board DSP reset switch condition and on the WDT expiration condition. Generated DSP reset signal has duration 0.2 sec, whereas the minimum duration of external reset signal is 500ns.

System controller (SC)

On-board system controller (SC) is implemented using FPGA chip and comprises of a set of configuration and control registers, which are used to configure and control on-board TMS320C54x DSP and external DSP environment.

Debugging TMS320C54x DSP Software

TMS320C54x DSP software for *TORNADO-E54x* DSP controllers can be developed and debugged using TI C5000 Code Composer Studio tools using TI XDS510 and MicroLAB' *MIRAGE-510DX* JTAG emulators.

2.2 TMS320C54x DSP Environment

TORNADO-E54x DSP controllers are based around the state of the art TMS320C54x high-performance 16-bit fixed point DSP from TI, which can be used for DSP operation, for communication with external host computers

and peripherals via on-board communication interfaces, and for real-time signal I/O and control via on-board general purpose I/O and on-board I/O expansion sites with installed DCM.

TMS320C54x DSP

TORNADO-54x DSP controllers have been designed to accommodate different compatible high-performance 16-bit fixed point TMS320C54x DSP with the only differences applied to DSP performance, amount of DSP on-chip memory and a set of DSP on-chip peripherals:

- 80MIPS TMS320LC548 DSP in **TORNADO-E548** with DSP on-chip 32Kx16 RAM, three BSP/TDM serial ports, one timer and 8-bit HPI port
- 100MIPS TMS320VC549 DSP in **TORNADO-E549** with DSP on-chip 32Kx16 RAM, three BSP/TDM serial ports, one timer and 8-bit HPI port
- 100MIPS TMS320VC5402 DSP in **TORNADO-E5402** with DSP on-chip 16Kx16 RAM, two McBSP serial ports, two timers and enhanced 8-bit HPI8 port
- 80MIPS TMS320VC5409 DSP in **TORNADO-E5409** with DSP on-chip 32Kx16 RAM, three McBSP serial ports, one timer, and enhanced 8-bit HPI8 port
- 100MIPS TMS320VC5410 DSP in **TORNADO-E5410** with DSP on-chip 64Kx16 RAM, three McBSP serial ports, one timer, and enhanced 8-bit HPI8 port
- 160MIPS TMS320VC5416 DSP in **TORNADO-E5416** with DSP on-chip 256Kx16 RAM, three McBSP serial ports, one timer, and enhanced 8-bit HPI8 port.

CAUTION

This manual does not contain description and programming details for on-board TI TMS320C54x DSP.

For more information refer to original TI datasheets and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TMS320C54x DSP Bootmode Configurations

The TMS320C54x DSP bootmode configuration is defined by on-board SW2-1 and SW2-2 switches (refer to fig.2-2 and fig.A-1). Supported bootmode configurations are presented in table 2-1.

Table 2-1. TMS320C54x DSP Bootmode Configurations for TORNADO-E54x.

Bootmode	switch SW2-2	switch SW2-1	description
<i>MP/NO-BMODE (Microprocessor mode, no boot)</i>	ON	ON	<p><i>Corresponds to DSP Microprocessor (MP) start-up mode without boot process.</i></p> <p><i>After DSP reset will be released, DSP will fetch the reset vector from address 0FF80H of on-board DSP external program SRAM.</i></p> <p><i>Page #0 of on-board data SRAM page #0 will be mapped to external DSP data memory area via on-board XDMP_RG control register after release of DSP reset signal.</i></p> <p><i>TMS320C54x DSP OVLY bit is set to '0', i.e. on-board external DSP program SRAM will be mapped into lower DSP program memory space.</i></p>
<i>MC/FLASH8-BMODE (Microcontroller mode, boot from 8-bit FLASH/EPROM)</i>	OFF	ON	<p><i>Corresponds to DSP Microcontroller (MC) start-up mode and boot from the on-board 8-bit FLASH/EPROM page #0 starting at DSP data memory address 8000H.</i></p> <p><i>After DSP reset will be released, DSP will run on-chip bootloader and initialize parallel boot from 8-bit ROM. User boot code must either completely fit into page #0 of on-board FLASH/EPROM, or must contain valid entry code at page #0 to application specific bootloader, which will move extended DSP code to external program memory.</i></p> <p><i>Page #0 of on-board FLASH/EPROM memory will be mapped to external DSP data memory area via on-board XDMP_RG control register after release of DSP reset signal.</i></p> <p><i>TMS320C54x DSP OVLY bit is set to '1' by DSP on-chip bootloader, i.e. DSP on-chip memory will be mapped into lower DSP program memory space.</i></p>

MC/HPI-BMODE (Microcontroller mode, boot from HPI)	ON	OFF	<p>Corresponds to DSP Microcontroller (MC) start-up mode and boot from DSP on-chip HPI port.</p> <p>After DSP reset will be released, DSP will run on-chip bootloader and initialize HPI bootmode. Depending upon the particular TMS320C54x DSP chip installed, external host computer/controller must upload DSP code via DSP on-chip HPI port either before release of DSP reset signal (TMS320LC548/TMS320VC549/TMS320VC5410), or after release of DSP reset signal with further write of address for code entry point to specific DSP on-chip memory location (TMS320VC5402/TMS320VC5409/TMS320VC5416). Refer to original TI TMS320C54x DSP documentation for more details.</p> <p>Page #0 of on-board data SRAM page #0 will be mapped to external DSP data memory area via on-board XDMP_RG control register after release of DSP reset signal.</p> <p>TMS320C54x DSP OVLY bit is set to '1' by DSP on-chip bootloader, i.e. DSP on-chip memory will be mapped into lower DSP program memory space.</p>
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- Notes:
1. 'ON' corresponds to switched-on setting of on-board switch; 'OFF' corresponds to the switched-off setting of on-board switch.
 2. Other bootmode configurations are reserved and are not recommended for usage.
 3. Highlighted configuration corresponds to the factory setting.

On-board TMS320C54x DSP can be configured to start either in *microprocessor mode* without boot (**MP/NO-BMODE** bootmode in accordance with table 2-1), or in *microcontroller mode* with boot from either on-board 8-b FLASH/EPROM memory (**MC/FLASH8-BMODE** bootmode in accordance with table 2-1), or from DSP on-chip HPI port (**MP/HPI-BMODE** bootmode in accordance with table 2-1).

MP/NO-BMODE bootmode corresponds to DSP microprocessor start-up mode without boot process, and is useful for DSP code development and debugging, when multiple DSP restarts are required. DSP reset vector mapped to 0FF80H address of the on-board external DSP program SRAM. Page #0 of on-board data SRAM page #0 is mapped to external DSP data memory area via on-board XDMP_RG control register after release of DSP reset signal. TMS320C54x DSP OVLY bit is set to '0', i.e. on-board external DSP program SRAM will be mapped into lower DSP program memory space.

MC/FLASH8-BMODE DSP bootmode configuration corresponds to DSP microcontroller start-up mode with boot from on-board 8-bit FLASH/EPROM page #0, which is allocated to the DSP data memory address area 8000H..FFFFH. Page #0 of on-board FLASH/EPROM memory is mapped to external DSP data memory area via on-board XDMP_RG control register after release of DSP reset signal. TMS320C54x DSP OVLY bit is set to '1' by DSP on-chip bootloader, i.e. DSP on-chip memory will be mapped into lower DSP program memory space.

CAUTION

Application boot code must be allocated into the FLASH/EPROM page #0, since this is the FLASH/EPROM memory page, which is selected during FLASH/EPROM boot procedure.

In case user application boot code exceeds the FLASH/EPROM memory page limits (32KB) and must be loaded into on-board external DSP program SRAM, then user application must provide the start-up kernel of boot code at FLASH/EPROM page #0, which must be initialized after the boot of FLASH/EPROM page #0. This start-up kernel must load FLASH/EPROM pages #1..#3 into the DSP on-chip memory depending upon the user application.

MC/HPI-BMODE DSP bootmode configuration corresponds to DSP microcontroller start-up mode with boot via DSP on-chip HPI port. Page #0 of on-board data SRAM page #0 will be mapped to external DSP data memory area via on-board *XDMP_RG* control register after release of DSP reset signal. TMS320C54x DSP OVLY bit is set to '1' by DSP on-chip bootloader, i.e. DSP on-chip memory will be mapped into lower DSP program memory space.

CAUTION

Different TMS320C54x DSP chips, which can be used in *TORNADO-E54x* DSP controllers, feature different HPI boot sequence.

Depending upon the particular TMS320C54x DSP, external host computer/controller must upload DSP code via DSP on-chip HPI port either before release of DSP reset signal, or after release of DSP reset signal with further write of address for code entry point to specific DSP on-chip memory location.

For *TORNADO-E548/E549/E5410* the application DSP code must be uploaded via DSP on-chip HPI port before release of DSP reset signal, and after DSP reset signal has been released, then DSP bootloader will start DSP code from specific DSP on-chip memory location (0x01000 for *TORNADO-E548/E549* and 0x2000 for *TORNADO-E5410*).

For *TORNADO-E5402/E5409/E5416* the application DSP code must be uploaded via DSP on-chip HPI port after release of DSP reset signal. Once the host has finished loading the boot code, it must perform additional writes to specific data memory addresses (0x0007F for *TORNADO-E5402*, and 0x0007E/0x0007F for *TORNADO-E5416*) in order to set the entry point (start address) of the loaded code and to notify DSP on-chip bootloader about finish of code upload. ***The entry point of the loaded code must be a non-zero number.*** For *TORNADO-E5416* the word at address 0x0007Eh must contain the extended address (XPC) of the entry point (addresses A22–A16), whereas the word at address 0x0007Fh contains the lower 16-bits (PC) of the entry point (address A15–A0).

Refer to original TI TMS320C54x DSP documentation for more details about HPI boot procedure for particular TMS320C54x DSP, which is installed in your *TORNADO-E54x* DSP controller.

Compiling TMS320C54x DSP applications for bootloading from 8-bit FLASH/EPROM memory

It is important to note that in case of bootloading from *TORNADO-E54x* on-board 8-bit FLASH/EPROM memory, data contents of 8-bit FLASH/EPROM for *TORNADO-E54x* DSP controllers must meet format of 8-bit ROM boot table for DSP on-chip bootloader for TMS320LC548, TMS320VC549, TMS320VC5402, TMS320VC5409, TMS320VC5410, and TMS320VC5416 DSP, which all require ROM/PARALLEL boot tables in extended addressing format.

In order to provide compatibility with TI C5000 Code Composer Hex Conversion Utility (HEX500.EXE), which creates ROM files in TMS320C54x DSP on-chip bootloader format, user C/Assembler DSP applications for *TORNADO-E54x* DSP controllers shall be compiled with either '-v548' or '-v549' command line options:

```
CL500 <file> -v549 <other CLI500.EXE command-line options>
ASM500 <file> -v549 <other ASM500.EXE command-line options>
```

Both '-v548' and '-v549' command line options for TI C5000 Code Composer CL500.EXE compiler command line shell and ASM500.EXE assembler compiler to force HEX500.EXE conversion utility to generate ROM/PARALLEL boot table using extended addressing format.

For more information refer *TORNADO-E54x* software demo samples and to original TI datasheets and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TMS320C54x DSP reset control

Reset signal for *TORNADO-E54x* on-board TMS320C54x DSP and peripherals is generated by on-board reset controller (RC) on any of the following conditions:

- in case of power-on and power off condition (the power is controlled by built-in power supervisory circuit)
- on-board SW1 reset pushbutton (refer to figures 2-2 and A-1) is pressed
- external active low reset signal is applied at *XRESET* input pin of on-board JP2 external reset connector (refer to figures 2-2, 2-5 and A-1)
- external active low reset signal is applied at *XRESET* input pin of on-board JP7 HPI interface connector (refer to figures 2-2, 2-4 and A-1, and to the corresponding subsection below)
- on-board watchdog timer (WDT) has expired, in case WDT is enabled via *WDT_EN_RG* IOX control register (refer to tables 2-3 and 2-5, and the corresponding subsection below) while DSP is released from the reset state.

Duration of generated reset signal for on-board TMS320C54x DSP and peripherals is at least 0.2 sec after release of any of the above conditions.

Note, that the last of the above listed conditions must be used in order to increase system operation reliability and to exclude system idling. Once DSP application has enabled WDT via *WDT_EN_RG* IOX control register, then it must periodically reset WDT (with the period about 0.8 sec) via DSP software by means of writing to the *WDT_RESET_RG* IOX control register, otherwise WDT will generate restart signal for on-board reset controller, which will restart DSP and all on-board peripherals. This will result in system restart in case it idles while WDT is enabled. For more details about WDT control refer to the corresponding subsection below.

Programming TMS320C54x DSP on-chip wait state and PLL control registers

In order to provide correct operation of *TORNADO-E54x* on-board hardware and to benefit of full performance of TMS320C54x on-board DSP, be sure to program TMS320C54x on-chip wait state control registers and PLL control registers in your TMS320C54x DSP software in accordance with table 2-2.

Table 2-2. Programming TMS320C54x DSP on-chip wait state control and PLL control registers.

Board	DSP source clock (CLKIN)	DSP internal clock	DSP PLL mode	DSP external bus clock (CLKOUT)	Data, which must be programmed to DSP on-chip wait state control and PLL control registers			
					SWWSR (@0x0028)	SWCR (@0x002B)	BSCR (@0x0029)	CLKMD (@0x0058)
TORNADO-E548	80 MHz	80 MHz	x1	80 MHz	0x2209 @DSRAM 0x2409 @FLASH	-	0x8800	0xF7F7
TORNADO-E549	100 MHz	100 MHz	x1	100 MHz	0x2209 @DSRAM 0x2409 @FLASH	0x0000	0x8800	0xF7F7
TORNADO-E5402	50 MHz	100 MHz	x2	100 MHz	0x2249 @DSRAM 0x2489 @FLASH	0x0000	0xC800	0x17F7
TORNADO-E5409	80 MHz	80 MHz	x1	80 MHz	0x2209 @DSRAM 0x2409 @FLASH	0x0000	0x8800	0xF7F7
TORNADO-E5410	100 MHz	100 MHz	x1	100 MHz	0x2209 @DSRAM 0x2409 @FLASH	0x0000	0x8800	0xF7F7
TORNADO-E5416	32 MHz	160 MHz	x5	80 MHz	0x2209 @DSRAM 0x2409 @FLASH	0x0000	0xA000	0x47F7

Notes: 1. @DSRAM denotes SWWSR register contents in case external data memory is configured as SRAM via XDMP_RG external I/O control register; @FLASH denotes SWWSR register contents in case external data memory is configured as FLASH/EPROM via XDMP_RG external I/O control register.

CAUTION

For more information about TMS320C54x DSP on-chip wait state control and PLL control registers refer to original TI datasheets and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TMS320C54x DSP memory and I/O map

TORNADO-E54x on-board TMS320C54x DSP address area comprises of program memory, data memory and I/O areas. Table 2-3 specifies the DSP memory and I/O maps, and the corresponding access wait states.

Table 2-3. TMS320C54x DSP memory and I/O map.

address area of TMS320C54x DSP	value at DSP RESET	access mode	address range (in 16-bit words)	access time/WS
TMS320C54x DSP on-chip and external memory areas				
DSP on-chip PROGRAM memory <i>(refer to TMS320C54x DSP datasheets for more details)</i>	-	r/w	<i>TORNADO-E5402:</i> 0000H...3FFFFH and aliases at pages #1..#N @PROG with OVLY=1 <i>TORNADO-</i> <i>E548/E549/E5409/E5410/E5416:</i> 0000H...7FFFFH and aliases at pages #1..#N @PROG with OVLY=1 <i>TORNADO-E5410/E5416:</i> 18000H...1FFFFH @PROG for MC/FLASH8-BMODE or MC/HPI-BMODE <i>TORNADO-E5416:</i> 28000H...2FFFFH 38000H...3FFFFH @PROG for MC/FLASH8-BMODE or MC/HPI-BMODE	0ws

<p>external PROGRAM SRAM memory</p> <p><i>(refer to TMS320C54x DSP datasheets for more details)</i></p>	-	r/w	<p><i>TORNADO-E5402:</i> <u>page #0</u>: 4000H...FFFFH <u>page #1</u>: 14000H...1FFFFH @PROG with OVLY=1</p> <p><u>page #0</u>: 0080H...FFFFH <u>page #1</u>: 10080H...1FFFFH @PROG with OVLY=0</p> <p><i>TORNADO-E548/E549/E5409:</i> <u>page #0</u>: 8000H...FFFFH <u>page #1</u>: 18000H...1FFFFH @PROG with OVLY=1</p> <p><u>page #0</u>: 0080H...FFFFH <u>page #1</u>: 10080H...1FFFFH @PROG with OVLY=0</p> <p><i>TORNADO-E5410/E5416:</i> <u>page #0</u>: 8000H...FFFFH <u>page #1</u>: 18000H...1FFFFH @PROG with OVLY=1 for MP/NO-BMODE</p> <p><u>page #0</u>: 0080H...FFFFH <u>page #1</u>: 10080H...1FFFFH @PROG with OVLY=0 for MP/NO-BMODE</p> <p><i>TORNADO-E5410:</i> <u>page #0</u>: 8000H...BFFFFH <u>page #0/alias</u>: 28000H...2FFFFH <u>page #1</u>: 38000H...3FFFFH @PROG with OVLY=1 for MC/FLASH8-BMODE or MC/HPI-BMODE</p> <p><u>page #0</u>: 0080H...BFFFFH <u>page #1</u>: 10000H...17FFFFH <u>page #0/alias</u>: 20000H...2FFFFH <u>page #1/alias</u>: 30000H...3FFFFH @PROG with OVLY=0 for MC/FLASH8-BMODE or MC/HPI-BMODE</p> <p><i>TORNADO-E5416:</i> <u>page #0</u>: 8000H...BFFFFH <u>page #0/alias</u>: 48000H...4FFFFH <u>page #1</u>: 58000H...5FFFFH @PROG with OVLY=1 for MC/FLASH8-BMODE or MC/HPI-BMODE</p> <p><u>page #0</u>: 0080H...BFFFFH <u>page #1</u>: 10000H...17FFFFH <u>page #0/alias</u>: 20000H...27FFFFH <u>page #1/alias</u>: 30000H...37FFFFH @PROG with OVLY=0 for MC/FLASH8-BMODE or MC/HPI-BMODE</p>	1ws
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DSP on-chip DATA memory <i>(refer to TMS320C54x DSP datasheets for more details)</i>	-	r/w	TORNADO-E5402: 0000H...3FFFFH @DATA TORNADO-E548/E549/E5409/E5410/E5416: 0000H...7FFFFH @DATA TORNADO-E5410/E5416: 8000H...FFFFFH @DATA with DROM=1	0ws
external DATA SRAM memory <i>(refer to TMS320C54x DSP datasheets for more details)</i>	-	r/w	TORNADO-E5402: <u>page #0:</u> 4000H..FFFFFH @DATA with XDMP_RG=0x00 <u>page #1:</u> 4000H..FFFFFH @DATA with XDMP_RG=0x01 TORNADO-E548/E549/E5409 and TORNADO-E5410/E5416 with DROM=0: <u>page #0:</u> 8000H..FFFFFH @DATA with XDMP_RG=0x00 <u>page #1:</u> 8000H..FFFFFH @DATA with XDMP_RG=0x01 <u>page #2:</u> 8000H..FFFFFH @DATA with XDMP_RG=0x02 <u>page #3:</u> 8000H..FFFFFH @DATA with XDMP_RG=0x03	1ws (on-board data SRAM is enabled via XDMP_RG register)
external DATA FLASH/EPROM memory <i>(refer to TMS320C54x DSP datasheets for more details)</i>	-	r/w	TORNADO-E548/E549/E5402/E5409 and TORNADO-E5410/E5416 with DROM=0: <u>pages #0..#31:</u> 8000H..FFFFFH @DATA with XDMP_RG=0x80..0x9F	Ta=120ns (WS are controlled via on-board h/w, on-board FLASH is enabled via XDMP_RG register)
external I/O (IOX) peripherals and parallel I/O interfaces				
IOX area: <i>dual-channel USART controller registers</i>	-	r/w	0000H..007FH @I/O with XF=1 (bits D0..D7 only)	Ta=70ns (WS are controlled via on-board h/w)
IOX area: <i>USB controller registers</i>	-	r/w	2000H..2001FH @I/O with XF=1 (bits D0..D7 only)	Ta=74ns (WS are controlled via on-board h/w)

IOX area: SIOX rev.C interface	-	r/w	6000H..6003FH @I/O with XF=1 (bits D0..D7 only)	Ta=(50ns + SX_RDY) (min WS are controlled via on-board h/w)
IOX area: PIOX-16 interface	-	r/w	0000H..FFFFH @I/O with XF=0	Ta=(50ns + PX_RDY) (min WS are controlled via on-board h/w)
external I/O (IOX) Control Registers area				
IOX area: WDT_RESET_RG register (WDT reset)	-	w	4000H @I/O with XF=1 (data ignored)	Ta=100ns (WS are controlled via on-board h/w)
IOX area: XDMP_RG register (external data memory page selector)	00H @ MP/NO-BMODE and MC/HPI- BMODE bootmodes 80H @ MC/FLASH8- BMODE bootmode	r/w	8000H @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: XIO_DATA_RG register (PIOX-16/SIOX TM/XIO pins I/O data)	00H	r/w	8001H @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: XIO_DIR_RG register (PIOX-16/SIOX TM/XIO pins direction control)	00H	r/w	8002H @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: XIO_CNF_RG register (PIOX-16/SIOX TM/XIO pins configuration control)	00H	r/w	8003H @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: PX SX_RESET_RG register (PIOX-16/SIOX I/O expansion sites reset control)	00H	r/w	8006H @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: WDT_EN_RG register (WDT enable control)	00H	r/w	8007H @I/O with XF=1 (bits D0..D7 only)	2ws

IOX area: <i>MIRQ0_SEL_RG</i> register (DSP INT-0 source selector)	00H	r/w	A000H @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: <i>MIRQ1_SEL_RG</i> register (DSP INT-1 source selector)	00H	r/w	A001H @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: <i>MIRQ2_SEL_RG</i> register (DSP INT-2 source selector)	00H	r/w	A002H @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: <i>MIRQ3_SEL_RG</i> register (DSP INT-3 source selector)	00H	r/w	A003H @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: <i>MNMI_SEL_RG</i> register (DSP NMI source selector)	00H	r/w	A004H @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: <i>DEV_ID_RG</i> register (device ID and revision ID)	(refer to the corresponding subsection below)	r	FFFDH @I/O with XF=1 (bits D0..D7 only)	2ws
IOX area: <i>SYS_STAT_RG</i> register (DSP bootmode and HPI enable status)	(refer to the corresponding subsection below)	r	FFFEH @I/O with XF=1 (bits D0..D7 only)	2ws

- Notes:**
1. @PROG denotes PROGRAM memory DSP area; @DATA denotes DATA memory DSP area, @IO denotes I/O DSP area.
 2. The DROM bit of DSP on-chip PMST register must be set to DROM=0 value (default value on DSP reset) in order to enable access to DSP external on-board DPRAM/FLASH memory.
 3. The XF denotes XF bit of DSP on-chip ST1 register.
 4. OVLY bit of DSP on-chip PMST register must be set to OVLY=1 value in order to map low PROGRAM memory to DSP on-chip DARAM memory.
 5. *Ta* denotes access time.
 6. *WS* denote number of wait states.
 7. *SX_RDY* and *PX_RDY* denote await for the '1' state of ready signal for SIOX rev.C and PIOX-16 I/F correspondingly.
 8. Access modes: *r* - read only, *w* - write only, *r/w* - read/write.

TMS320C54x DSP on-chip program and data memory areas

TMS320C54x DSP on-chip program and memory areas vary upon the particular DSP chip type installed onto **TORNADO-E54x** DSP controller. DSP on-chip memory is always accessed at maximum DSP speed without wait states.

For more information refer to table 2-3 and to original TI datasheets and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TMS320C54x DSP external program SRAM

TORNADO-E54x on-board DSP external program memory area comprises of two 64Kx16 SRAM memory pages.

CAUTION

External program SRAM mapping into DSP program memory address space depends upon the DSP bootmode, upon the state of OVLY bit of DSP on-chip PMST register, and upon the particular DSP chip type installed onto *TORNADO-E54x* DSP controller.

For more information refer to table 2-3 and to original TI datasheets and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TORNADO-E54x on-board TMS320C54x DSP can access on-board 128Kx16 external program SRAM with one wait state.

CAUTION

One wait state for access to external SRAM and peripherals means $\frac{1}{2}$ of maximum DSP speed for all *TORNADO-E54x* DSP controllers except for *TORNADO-E5416* DSP controller.

One wait state for access to external SRAM and peripherals means $\frac{1}{4}$ of maximum DSP speed for *TORNADO-E5416* DSP controller since DSP external bus clock (CLKOUT) for *TORNADO-E5416* DSP controller must be software configured to $\frac{1}{2}$ of DSP internal clock via DSP on-chip BSCR register.

TMS320C54x DSP external data memory area

TORNADO-E54x on-board DSP external data memory area can be configured as either on-board 128Kx16 data SRAM, or on-board 128K..1Mx8 FLASH/EPROM.

TORNADO-E54x DSP controllers are using extended data memory addressing concept in order to access different on-board data memories (SRAM and FLASH/EPROM) as external data memories for TMS320C54x DSP with external memory capacity, which exceeds built-in addressing capabilities of TMS320C54x DSP. Extended data memory addressing for *TORNADO-E54x* on-board DSP is controlled via *XDMP_RG* IOX control register (refer to tables 2-3 and 2-11, and to the corresponding subsection below).

CAUTION

Particular address mapping for DSP external data memory address space depends upon the particular DSP chip type installed onto *TORNADO-E54x* DSP controller, and upon the state of DROM bit of DSP on-chip PMST register for *TORNADO-E5410/E5416* DSP controllers.

For more information refer to figure 2-3, table 2-11 and to original TI datasheets and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

Figure 2-3 shows extended data memory addressing concept when accessing external data SRAM and FLASH/EPROM memories for different *TORNADO-E54x* DSP controllers using *XDMP_RG* IOX control register.

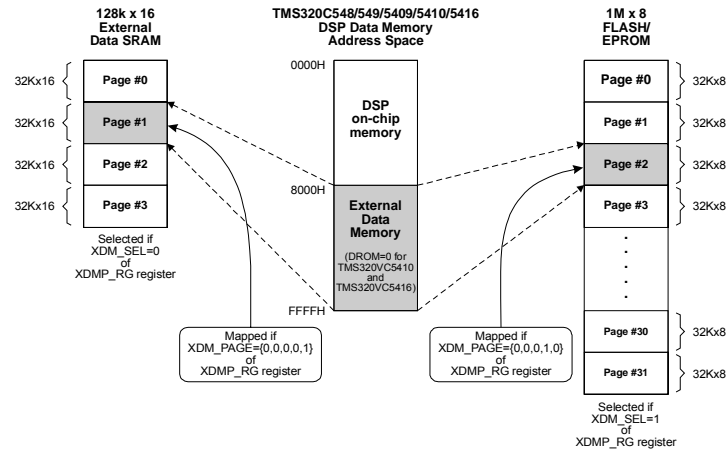


Fig.2-3a. Extended external data memory addressing for *TORNADO-E548/E549/E5409/E5410/E5416* DSP controllers.

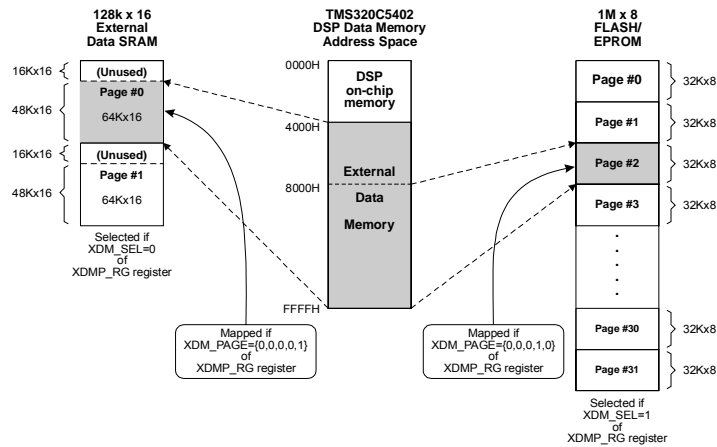


Fig.2-3b. Extended external data memory addressing for *TORNADO-E5402* DSP controller.

Selection between external data SRAM and FLASH/EPROM memories as external TMS320C54x DSP memory is performed at run-time by DSP software via bit *XDM_SEL* of *XDMP_RG* IOX control register, whereas {*XDM_PAGE-0...4*} bits of *XDMP_RG* IOX control register must be used to select a particular data memory page of either external data SRAM or FLASH/EPROM memory, which will be mapped to DSP external data memory address space.

On-board data SRAM as TMS320C54x DSP external data memory

TORNADO-E54x on-board 128Kx16 data SRAM is selected as DSP external program memory in case bit *XDM_SEL* of on-board *XDMP_RG* IOX control register is set to the '0' state (refer to the figure 2-3 and table 2-11). This is default setting on DSP reset conditions for *MP/NO-BMODE* and *MC/HPI-BMODE* DSP bootmodes (refer to table 2-1 for more details).

TORNADO-E54x on-board DSP external data SRAM appears as four overlapped 32Kx16 SRAM memory pages for *TORNADO-E548/E549/E5409/E5410/E5416* DSP controllers and as two overlapped 64Kx16 SRAM memory pages for *TORNADO-E5402* DSP controllers. Particular data SRAM memory page, which is mapped into DSP external data memory area, is selected via bits D0..D1 of *XDMP_RG* IOX control register for *TORNADO-E548/E549/E5409/E5410/E5416* DSP controllers and by bit D0 for *TORNADO-E5402* DSP controllers.

CAUTION

Particular address mapping of external data SRAM into DSP external data memory address space depends upon the particular DSP chip type installed onto *TORNADO-E54x* DSP controller, and upon the state of DROM bit of DSP on-chip PMST register for *TORNADO-E5410/E5416* DSP controllers (figure 2-3).

For more information refer to original TI datasheets and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

TORNADO-E54x on-board TMS320C54x DSP can access on-board 128Kx16 external data SRAM with one wait state.

CAUTION

One wait state for access to external SRAM and peripherals means $\frac{1}{2}$ of maximum DSP speed for all *TORNADO-E54x* DSP controllers except for *TORNADO-E5416* DSP controller.

One wait state for access to external SRAM and peripherals means $\frac{1}{4}$ of maximum DSP speed for *TORNADO-E5416* DSP controller since DSP external bus clock (CLKOUT) for *TORNADO-E5416* DSP controller must be software configured to $\frac{1}{2}$ of DSP internal clock via DSP on-chip BSCR register.

On-board FLASH/EPROM as TMS320C54x DSP external data memory

FLASH/EPROM memory can be used to store non-volatile data and/or for DSP boot. 8-bit FLASH boot code from FLASH memory page #0 is reloaded into DSP on-chip memory during *MC/FLASH8-BMODE* bootmode.

TORNADO-E54x DSP controllers allow installation of either 5v-only 128K..512Kx8 FLASH or 128K..1Mx8 EPROM chip with access time below 100ns and in the PLCC-32 IC package into the *TORNADO-E54x* on-board dedicated S1 socket (refer to figures 2-2 and A-1).

CAUTION

TORNADO-E54x on-board S1 socket is designed to carry the FLASH 5v-only 128K..512Kx8 chips or EPROM 128K..1Mx8 chips in the PLCC-32 IC package.

Installation of other FLASH/EPROM chip than that specified in table 2-3 may result in damage of FLASH/EPROM chip and/or of the *TORNADO-E54x* hardware.

CAUTION

MicroLAB Systems highly recommends that AMD (www.amd.com) 5v only 128Kx8 Am29F010B-55JC (or -70JC, or -90JC) FLASH chips and 512Kx8 Am29F040B-70JC (or -90JC) FLASH chips in PLCC-32 IC package are used as 8-bit FLASH memory chips for *TORNADO-E54x* DSP controllers. These FLASH chips have proved to meet industry standards and have demonstrated best reliability and data integrity parameters when evaluated with *TORNADO-E54x* DSP controllers.

There is no preferences for any particular manufacturer for EPROM/ROM chips, which can be used with *TORNADO-E54x* DSP controllers.

The on-board SW3 switch set (switches SW3-1..SW3-6) is used to select the particular FLASH/EPROM chip type installed and to enable/disable write protect feature for the FLASH chip. Supported FLASH/EPROM chips are presented in table 2-4.

Table 2-4. FLASH/EPROM chip type selector.

FLASH/EPROM chip type in PLCC-32 IC package	SW3 jumper setting					
	SW3-1	SW3-2	SW3-3	SW3-4	SW3-5	SW3-6
<i>Am29F010</i> <i>128Kx8 FLASH</i> <i>Am29F040</i> <i>512Kx8 FLASH</i> <i>with</i> <i>WRITE ENABLE</i>	OFF	ON	OFF	ON	OFF	OFF
<i>Am29F010</i> <i>128Kx8 FLASH</i> <i>Am29F040</i> <i>512Kx8 FLASH</i> <i>with</i> <i>WRITE DISABLE</i>	OFF	ON	OFF	OFF	ON	OFF
<i>27C010</i> <i>128Kx8 EPROM</i> <i>27C020</i> <i>256Kx8 EPROM</i>	OFF	OFF	ON	OFF	ON	OFF
<i>27C040</i> <i>512Kx8 EPROM</i>	OFF	OFF	ON	OFF	OFF	ON
<i>27C080</i> <i>1Mx8 EPROM</i>	ON	OFF	OFF	OFF	OFF	ON

Notes:.

1. The highlighted configuration corresponds to the factory setting.
2. The recommended access time for the FLASH/EPROM chip is 100ns or less.

TORNADO-E54x on-board FLASH/EPROM memory is selected as DSP external program memory in case bit **XDM_SEL** of on-board **XDMP_RG** IOX control register is set to the '1' state (refer to the figure 2-3 and table 2-11). This is default setting on DSP reset condition for **MC/FLASH8-BMODE** DSP bootmode (refer to table 2-1 for more details).

CAUTION

TORNADO-E54x on-board DSP allocates 8-bit FLASH/EPROM memory into least significant data byte (bits D0..D7) of DSP data word with most significant data byte (bits D8..D15) left undefined.

TORNADO-E54x on-board FLASH/EPROM data memory bank appears as set of 32 overlapped 32Kx8 memory pages, which are mapped to TMS320C54x DSP external memory address area 0x8000..0xFFFF. Particular data SRAM memory page, which is mapped into DSP external data memory area, is selected via bits D0..D4 of *XDMP_RG* IOX control register.

CAUTION

Once on-board FLASH/EPROM memory has been selected as external DSP data memory via bit *XDM_SEL* of *XDMP_RG* IOX control register, then *TORNADO-E548/E549/E5402/E5409* on-board DSP can access external FLASH/EPROM memory any time it performs data access to 0x8000...0xFFFF external data memory area.

However, *TORNADO-E5410/E5416* DSP controllers requires that bit DROM of DSP on-chip PMST register must be also set to the '0' state in order to allow access to external FLASH/EPROM memory.

FLASH memory bank provides FLASH memory write protection in order to exclude unauthorized FLASH memory data update and to provide integrity of FLASH memory contents.

CAUTION

If SW3-5 switch is set to the 'OFF' state and SW3-4 switch is set to 'ON' while the FLASH memory chip is installed into on-board S1 socket, then the FLASH memory can be programmed by the DSP software.

If SW3-5 switch is set to the 'ON' state and SW3-4 switch is set to 'OFF' while the FLASH memory chip is installed into on-board S1 socket, then writing to FLASH memory is disabled.

For more information about programming FLASH memory refer to original manufacturer datasheet for particular installed FLASH memory chip.

CAUTION

In case AMD Am29F010B or Am29F040B FLASH memory chips are being used with *TORNADO-E54x* DSP controller, then *TORNADO-E54x* supplied flash programming DSP software utilities and demo samples can be used in order to auto-detect and to program FLASH memory directly from DSP software.

CAUTION

EPROM chip can be programmed in the external programmer only, and can be used for read-only software boot purpose in *TORNADO-E54x* DSP controllers.

external I/O (IOX) area

TMS320C54x DSP external I/O (IOX) area for *TORNADO-E54x* DSP controllers (refer to table 2-3) is allocated into DSP I/O address space and includes the following on-board peripherals and control registers:

- dual-channel USART area
- USB device controller area
- IOX Control Registers area
- SIOX rev.C interface area for compatible DCM
- PIOX-16 interface area for compatible DCM.

CAUTION

TORNADO-E54x on-board DSP access to on-board USART, USB, SIOX rev.C interface and IOX control registers areas must be performed with DSP XF flag set to '1'.

TORNADO-E54x on-board DSP access to on-board PIOX-16 interface area must be performed with DSP XF flag set to '0'.

TMS320C54x DSP XF flag is controlled via DSP on-chip ST1 status/control register. For more details refer to original TI datasheets and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

CAUTION

In case user TMS320C54x DSP application for *TORNADO-E54x* DSP controller requires run-time dynamic switching of the output state for DSP XF flag along with DSP access to IOX area , then possible delays shall be taken into account due to the TMS320C54x DSP pipelined architecture.

Dual-channel USART

TORNADO-E54x on-board dual-channel USART (universal synchronous/asynchronous receiver/transmitter) can be used for communication with host computers, terminals, network adapters, or external peripherals using industry standard serial communication protocols.

USART is based around the SIEMENS SAB 82532 chip and supports popular synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) at up to 10 Mbit/s data transfer rate and industry-standard asynchronous protocol at up to 2.5 MBaud independent for each channel. USART can generate interrupt to on-board DSP.

Each USART channel connects to external communication equipment via either RS232C or RS422/EIA-530 electrical interface. Selection of particular interface is performed by the on-board switch SW4.

CAUTION

USART on-chip registers are allocated directly into external I/O address space of TMS320C54x DSP (refer to table 2-3) and can be accessed via DSP I/O read/write instructions in case DSP XF flag is set to the '1' state.

For more details about USART and external RS232C/RS422 interfaces for USART refer to the corresponding section later in this chapter.

USB interface

TORNADO-E54x on-board USB device controller with external USB type 'B' interface connector can be used for communication to external host computers via the industry standard 12 Mbit/s USB protocol.

USB device controller is based around the Lucent Technologies USS-820/USS-825 chip and meets USB rev.1.1 specifications. USB device controller can generate interrupt to on-board DSP.

CAUTION

On-chip registers of USB device controller are allocated directly into external I/O address space of TMS320C54x DSP (refer to table 2-3) and can be accessed via DSP I/O read/write instructions in case DSP XF flag is set to the '1' state.

For more details about USB device controller and interface refer to the corresponding section later in this chapter.

IOX control registers area

TORNADO-E54x on-board external I/O (IOX) control registers area comprises of a set of control registers, which shall be used in order to configure on-board TMS320C54x DSP environment and to generate control signals to on-board peripherals.

CAUTION

IOX control registers are mapped to TMS320C54x DSP external I/O address area (refer to table 2-3) and can be accessed via DSP I/O read/write instructions in case DSP XF flag is set to the '1' state.

The following is the list of IOX control registers (for more details refer to table 2-3 and to the corresponding subsections below):

- *WDT_EN_RG* and *WDT_RESET_RG* registers, which are used to control on-board watchdog timer (WDT)
- *PXSX_RESET_RG* register, which is used to control reset signals for on-board PIOX-16 and SIOX rev.B/C I/O expansion interface sites for DCM, and the reset signal for on-board MXSIOX connector for external *T/SU-X1* SIOX rev.B mini-extender kit
- *XIO_DATA_RG*, *XIO_DIR_RG* and *XIO_CNF_RG* registers, which are used to configure and control timer/IO TM/XIO-0/1 pins for PIOX/SIOX I/O expansion interface sites
- *MIRQ0_SEL_RG*, *MIRQ1_SEL_RG*, *MIRQ2_SEL_RG*, *MIRQ3_SEL_RG* and *MNMI_SEL_RG*, which are used to configure source select multiplexers for DSP external interrupt request inputs (*INT0..INT3* and *NMI*)
- *XDMP_RG* register, which is used to select external DSP data memory type (SRAM or FLASH/EPROM) and to set external data memory page
- *DEV_ID_RG* register, which is used to read device ID and revision ID in order to identify *TORNADO-E54x* board via DSP software
- *SYS_STAT_RG* register, which is used to read latched DSP start-up configuration via DSP software.

CAUTION

IOX control registers have 8-bit data format and are allocated to the least significant byte (bits D0..D7) of DSP data word. Most significant byte (bits D8..D15) is ignored when writing to IOX control registers and is returned undefined when reading from IOX control registers.

watchdog timer (WDT) control

TORNADO-E54x provides on-board watchdog timer (WDT), which generates output pulse in case WDT has not been reset by DSP software within the WDT latency period (typically 0.8 sec) since the last WDT reset event. *TORNADO-E54x* DSP software can configure on-board hardware to enable generation of reset signal for on-board DSP and peripherals on the WDT expiration condition in order to increase reliability in embedded environment and to automatically restart on-board DSP and peripherals in case of the DSP idling or DSP software crash.

Generation of reset signal for *TORNADO-E54x* on-board DSP and peripherals on the WDT expiration event is enabled by the *WDT_EN* bit of *WDT_EN_RG* IOX register (refer to table 2-3 for addressing details).

***WDT_EN_RG* IOX control register (r/w)**

X	0 (r)	0 (r)	0 (r)	0 (r)	0 (r)	0 (r)	0 (r)	WDT_EN (r/w, 0+)
bit-15...bit-8	bit-7	Bit-6	Bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-5. *WDT_EN_RG* IOX control register.

register bit(s)	access mode	value at DSP reset	Description
<i>WDT_EN</i>	r/w	0	<p>Enable control for generation of reset signal for on-board DSP and peripherals on WDT expiration event.</p> <p><i>WDT_EN</i> =0 corresponds to the WDT disabled, i.e. reset signal for on-board DSP and peripherals can't be generated on WDT expiration event. This is default setting on power on and DSP reset conditions.</p> <p><i>WDT_EN</i> =1 corresponds to the WDT enabled, i.e. reset signal for on-board DSP and peripherals will be generated on WDT expiration event. DSP software must periodically (with the period below 0.8 sec) reset WDT by means of writing to the <i>WDT_RESET_RG</i> IOX control register (written data is ignored) in order to exclude automatic generation of reset signal for on-board DSP and peripherals.</p>

Notes: 1. Access modes: r/w – read/write; r – read-only; w – write only.

In case WDT is enabled b n-board DSP software via setting bit *WDT_EN* bit of *WDT_EN_RG* IOX control register to the '1' state, then DSP software must periodically write (with the period below 0.8 sec) to the *WDT_RESET_RG* IOX control register (refer to table 2-3 for addressing details) in order to reset WDT. When writing to *WDT_RESET_RG* IOX control register, written data is ignored, and WDT is reset.

WDT_RESET_RG IOX control register (w)

X	X	X	X	X	X	X	X	X
bit-15...bit-8	bit-7	Bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

TM/XIO-0/1 timer/I/O pins control for PIOX-16/SIOX/MXSIOX I/O expansion interface sites

TM/XIO-0 and *TM/XIO-1* timer/I/O pins are used in PIOX-16, SIOX rev.B/C and MXSIOX on-board I/O expansion interface site connectors in order to provide either DSP timer outputs or general purpose I/O to installed DCM (refer to the corresponding sections later in this chapter). Each of *TM/XIO-0/1* pins can be independently configured as either timer, or general purpose I/O pin.

TM/XIO-0 and *TM/XIO-1* timer/I/O pins are configured and controlled via the following IOX control registers (refer to table 2-3 for addressing details):

- *XIO_CNF_RG* IOX control register, which is used to configure *TM/XIO-0/1* timer/I/O pins as either timer output or general purpose I/O pins (each pin is configure independently)
- *XIO_DIR_RG* IOX control register, which is used to configure *TM/XIO-0/1* pins as either general purpose input or general purpose output pins, in case *TM/XIO-0/1* pins have been configured as general purpose I/O pins via *XIO_CNF_RG* IOX control register (each pin is configure independently)
- *XIO_DATA_RG* IOX control register, which is used to write output data and read current status of *TM/XIO-0/1* pins, in case *TM/XIO-0/1* pins have been configured as general purpose I/O pins *XIO_CNF_RG* IOX control register (each pin is configure independently).

XIO_CNF_RG IOX control register must be used in order to configure *TM/XIO-0/1* timer/I/O pins as either timer output or general purpose I/O pins.

XIO_CNF_RG IOX control register (r/w)

x	0 (r)	0 (r)	0 (r)	0 (r)	0 (r)	0 (r)	<i>TM/XIO-1_CNF</i> (r/w, 0+) (TORNADO-E5402 with HPI port disabled) 0 (r) (TORNADO-E5402 with HPI port enabled, and TORNADO-E548/E549/E5409/E5410/E5416)	<i>TM/XIO-0_CNF</i> (r/w, 0+)
bits-15..8	Bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-6. *XIO_CNF_RG* IOX control register.

register bit(s)	access mode	value at DSP reset	Description
<i>TM/XIO-0_CNF</i>	r/w	0	<p>Configures <i>TM/XIO-0</i> timer/IO pin.</p> <p><i>TM/XIO-0_CNF</i> =0 corresponds to the <i>TM/XIO-0</i> pin configured as general purpose I/O pin. Particular I/O configuration and data I/O value shall be set via <i>XIO-0_DIR</i> bit of <i>XIO_DIR_RG</i> IOX control register and <i>XIO-0_DATA</i> bit of <i>XIO_DATA_RG</i> IOX control register. This is default setting on power on and DSP reset conditions.</p> <p><i>TM/XIO-0_CNF</i> =1 corresponds to the <i>TM/XIO-0</i> pin configured as TMS320C54x DSP on-chip TOUT timer output pin. Settings of <i>XIO-0_DIR</i> bit of <i>XIO_DIR_RG</i> IOX control register and <i>XIO-0_DATA</i> bit of <i>XIO_DATA_RG</i> IOX control register are ignored. Refer to original TI documentation for more details about programming TMS320C54x DSP on-chip timer.</p>
<i>TM/XIO-1_CNF</i>	r/w	0	<p>Configures <i>TM/XIO-1</i> timer/IO pin for <i>TORNADO-E5402</i> DSP controller with HPI disabled during DSP start-up via on-board SW2-3 switch (refer to the corresponding subsection below). Otherwise, this bit can't be set via DSP software and always reads as '0'.</p> <p><i>TM/XIO-1_CNF</i> =0 corresponds to the <i>TM/XIO-1</i> pin configured as general purpose I/O pin. Particular I/O configuration and data I/O value shall be set via <i>XIO-1_DIR</i> bit of <i>XIO_DIR_RG</i> IOX control register and <i>XIO-1_DATA</i> bit of <i>XIO_DATA_RG</i> IOX control register. This is default setting on power on and DSP reset conditions for <i>TORNADO-E5402</i> DSP controller with HPI disabled via SW2-3 on-board switch during DSP start-up (refer to the corresponding subsection below) and is hardware forced setting for <i>TORNADO-E548/E549/E5409/E5410/E5416</i> DSP controllers.</p> <p><i>TM/XIO-1_CNF</i> =1 setting can be configured for <i>TORNADO-E5402</i> DSP controller only with HPI disabled during DSP start-up via on-board SW2-3 switch (refer to the corresponding subsection below), and corresponds to the <i>TM/XIO-1</i> pin configured as TMS320C5402 DSP on-chip TOUT1 timer #1 output pin. TMS320VC5402 DSP on-chip timer #1 output (TOUT1) must be enabled via bit TOUT1 of DSP on-chip GPCR register. Settings of <i>XIO-1_DIR</i> bit of <i>XIO_DIR_RG</i> IOX control register and <i>XIO-1_DATA</i> bit of <i>XIO_DATA_RG</i> IOX control register are ignored. Refer to original TI documentation for more details about programming TMS320C5402 DSP on-chip timer #1 output.</p>

Notes: 1. Access modes: r/w – read/write; r – read-only; w – write only.

XIO_DIR_RG IOX control register must be used in order to configure *TM/XIO-0/1* timer/IO pins as either general purpose input or general purpose output pins in case *TM/XIO-0/1* pins have been configured as general purpose I/O pins via *XIO_CNF_RG* IOX control register.

XIO_DIR_RG IOX control register (r/w)

X	0 (r)	0 (r)	0 (r)	0 (r)	0 (r)	0 (r)	XIO-1_DIR (r/w, 0+)	XIO-0_DIR (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-7. XIO_DIR_RG IOX control register.

register bit(s)	access mode	value at DSP reset	Description
XIO-0_DIR	r/w	0	<p>Configures direction of <i>TM/XIO-0</i> IO pin as either general purpose input or general purpose output pin in case <i>TM/XIO-0</i> pin has been configured as general purpose I/O pins via bit <i>TM/XIO-0_CNF</i> of <i>XIO_CNF_RG</i> IOX control register (refer to table 2-6).</p> <p><i>XIO-0_DIR</i> =0 corresponds to the <i>TM/XIO-0</i> pin configured as general purpose input pin. <i>TM/XIO-0</i> bit of <i>XIO_CNF_RG</i> IOX control register must be set to '0' in order to configure <i>TM/XIO-0</i> pin as general purpose I/O pin (refer to table 2-6). Current input state of <i>TM/XIO-0</i> input pin can be read via bit <i>XIO-0_DATA</i> of <i>XIO_DATA_RG</i> IOX control register (refer to table 2-8). This is default setting on power on and DSP reset conditions.</p> <p><i>XIO-0_DIR</i> =1 corresponds to the <i>TM/XIO-0</i> pin configured as general purpose output pin. <i>TM/XIO-0</i> bit of <i>XIO_CNF_RG</i> IOX control register must be set to '0' in order to configure <i>TM/XIO-0</i> pin as general purpose I/O pin (refer to table 2-6). Current output state of <i>TM/XIO-0</i> input pin can be set via bit <i>XIO-0_DATA</i> of <i>XIO_DATA_RG</i> IOX control register (refer to table 2-8).</p>
XIO-1_DIR	r/w	0	<p>Configures direction of <i>TM/XIO-1</i> IO pin as either general purpose input or general purpose output pin in case <i>TM/XIO-1</i> pin has been configured as general purpose I/O pins via bit <i>TM/XIO-1_CNF</i> of <i>XIO_CNF_RG</i> IOX control register (refer to table 2-6).</p> <p><i>XIO-1_DIR</i> =0 corresponds to the <i>TM/XIO-1</i> pin configured as general purpose input pin. <i>TM/XIO-1</i> bit of <i>XIO_CNF_RG</i> IOX control register must be set to '0' in order to configure <i>TM/XIO-1</i> pin as general purpose I/O pin (refer to table 2-6). Current input state of <i>TM/XIO-1</i> input pin can be read via bit <i>XIO-1_DATA</i> of <i>XIO_DATA_RG</i> IOX control register (refer to table 2-8). This is default setting on power on and DSP reset conditions.</p> <p><i>XIO-1_DIR</i> =1 corresponds to the <i>TM/XIO-1</i> pin configured as general purpose output pin. <i>TM/XIO-1</i> bit of <i>XIO_CNF_RG</i> IOX control register must be set to '0' in order to configure <i>TM/XIO-1</i> pin as general purpose I/O pin (refer to table 2-6). Current output state of <i>TM/XIO-1</i> input pin can be set via bit <i>XIO-1_DATA</i> of <i>XIO_DATA_RG</i> IOX control register (refer to table 2-8).</p>

Notes: 1. Access modes: r/w – read/write; r – read-only; w – write only.

XIO_DATA_RG IOX control register must be used in order to write output state and read current state for *TM/XIO-0/1* timer/IO pins in case they have been configured as general purpose I/O pins via *XIO_CNF_RG* IOX control register.

***XIO_DATA_RG* IOX control register (r/w)**

x	0 (r)	0 (r)	0 (r)	0 (r)	0 (r)	0 (r)	<i>XIO-1_DATA</i> (r/w, 0+)	<i>XIO-0_DATA</i> (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-8. *XIO_DATA_RG* IOX control register.

register bit(s)	access mode	value at DSP reset	Description
<i>XIO-0_DATA</i>	r/w	- (r) 0 (w)	<p>Sets output state and returns current state of <i>TM/XIO-0</i> IO pin in case <i>TM/XIO-0</i> pin has been configured as general purpose I/O pins via bit <i>TM/XIO-0_CNF</i> of <i>XIO_CNF_RG</i> IOX control register (refer to table 2-6).</p> <p><i>XIO-0_DATA</i>=0 during write operation corresponds to the '0' output state of <i>TM/XIO-0</i> pin, in case it has been configured as general purpose output pin via bit <i>XIO-0_DIR</i> of <i>XIO_DIR_RG</i> IOX control register (refer to table 2-7). <i>XIO-0_DATA</i>=0 during read operation corresponds to the '0' current I/O state of <i>TM/XIO-0</i> pin not regarding whether it has been configured as general purpose output or input pin via bit <i>XIO-0_DIR</i> of <i>XIO_DIR_RG</i> IOX control register. In case <i>TM/XIO-0</i> pin is configured as general purpose input pin, then writes to bit <i>XIO-0_DATA</i> will be ignored, however data written will be stored upon <i>TM/XIO-0</i> pin will be configured as general purpose output pin. <i>TM/XIO-0</i> bit of <i>XIO_CNF_RG</i> IOX control register must be set to '0' in order to configure <i>TM/XIO-0</i> pin as general purpose I/O pin (refer to table 2-6). This is default write setting on power on and DSP reset conditions.</p> <p><i>XIO-0_DATA</i>=1 during write operation corresponds to the '1' output state of <i>TM/XIO-0</i> pin, in case it has been configured as general purpose output pin via bit <i>XIO-0_DIR</i> of <i>XIO_DIR_RG</i> IOX control register (refer to table 2-7). <i>XIO-0_DATA</i>=1 during read operation corresponds to the '1' current I/O state of <i>TM/XIO-0</i> pin not regarding whether it has been configured as general purpose output or input pin via bit <i>XIO-0_DIR</i> of <i>XIO_DIR_RG</i> IOX control register. In case <i>TM/XIO-0</i> pin is configured as general purpose input pin, then writes to bit <i>XIO-0_DATA</i> will be ignored, however data written will be stored upon <i>TM/XIO-0</i> pin will be configured as general purpose output pin. <i>TM/XIO-0</i> bit of <i>XIO_CNF_RG</i> IOX control register must be set to '0' in order to configure <i>TM/XIO-0</i> pin as general purpose I/O pin (refer to table 2-6).</p>

<i>XIO-1_DATA</i>	r/w	<p>- (r)</p> <p>0 (w)</p>	<p>Sets output state and returns current state of <i>TM/XIO-1</i> IO pin in case <i>TM/XIO-1</i> pin has been configured as general purpose I/O pins via bit <i>TM/XIO-1_CNF</i> of <i>XIO_CNF_RG</i> IOX control register (refer to table 2-6).</p> <p><i>XIO-1_DATA</i>=0 during write operation corresponds to the '0' output state of <i>TM/XIO-1</i> pin, in case it has been configured as general purpose output pin via bit <i>XIO-1_DIR</i> of <i>XIO_DIR_RG</i> IOX control register (refer to table 2-7). <i>XIO-1_DATA</i>=0 during read operation corresponds to the '0' current I/O state of <i>TM/XIO-1</i> pin not regarding whether it has been configured as general purpose output or input pin via bit <i>XIO-1_DIR</i> of <i>XIO_DIR_RG</i> IOX control register. In case <i>TM/XIO-1</i> pin is configured as general purpose input pin, then writes to bit <i>XIO-1_DATA</i> will be ignored, however data written will be stored upon <i>TM/XIO-1</i> pin will be configured as general purpose output pin. <i>TM/XIO-1</i> bit of <i>XIO_CNF_RG</i> IOX control register must be set to '0' in order to configure <i>TM/XIO-1</i> pin as general purpose I/O pin (refer to table 2-6). This is default write setting on power on and DSP reset conditions.</p> <p><i>XIO-1_DATA</i>=1 during write operation corresponds to the '1' output state of <i>TM/XIO-1</i> pin, in case it has been configured as general purpose output pin via bit <i>XIO-1_DIR</i> of <i>XIO_DIR_RG</i> IOX control register (refer to table 2-7). <i>XIO-1_DATA</i>=1 during read operation corresponds to the '1' current I/O state of <i>TM/XIO-1</i> pin not regarding whether it has been configured as general purpose output or input pin via bit <i>XIO-1_DIR</i> of <i>XIO_DIR_RG</i> IOX control register. In case <i>TM/XIO-1</i> pin is configured as general purpose input pin, then writes to bit <i>XIO-1_DATA</i> will be ignored, however data written will be stored upon <i>TM/XIO-1</i> pin will be configured as general purpose output pin. <i>TM/XIO-1</i> bit of <i>XIO_CNF_RG</i> IOX control register must be set to '0' in order to configure <i>TM/XIO-1</i> pin as general purpose I/O pin (refer to table 2-6).</p>
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Notes: 1. Access modes: r/w – read/write; r – read-only; w – write only.

reset signals control for SIOX rev.B/C, MXSIOX and PIOX-16 expansion interface sites

TORNADO-E54x DSP controllers support generation of individual reset signals for on-board SIOX rev.B/C, MXSIOX and PIOX-16 expansion interface sites. This allows correct initialization of installed DCM hardware and synchronization with the DSP software.

Individual reset signals for on-board SIOX rev.B/C, MXSIOX and PIOX-16 DCM sites are controlled via **PXSX_RESET_RG** IOX control register (refer to table 2-3 for addressing details).

PXSX_RESET_RG IOX control register (r/w)

X	0 (r)	0 (r)	0 (r)	0 (r)	0 (r)	<p>SX-B_RESET (r/w, 0+) (TORNADO-E548/E549/E5409/E5410/E5416)</p> <p>0 (r) (TORNADO-E5402)</p>	SX-A_RESET (r/w, 0+)	PX_RESET (r/w, 0+)
bit-15...bit-8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-9. *PXSX_RESET_RG* IOX control register.

register bit(s)	access mode	value at DSP reset	Description
<i>PX_RESET</i>	r/w	0	<p>Controls reset signal for on-board PIOX-16 DCM site. For more details about on-board PIOX-16 DCM site refer to the corresponding section later in this chapter.</p> <p><i>PIOX16_RESET</i> =0 corresponds to active reset signal for PIOX-16 DCM site. This is default setting on power on and DSP reset conditions.</p> <p><i>PIOX16_RESET</i> =1 corresponds to released reset signal for PIOX-16 DCM site.</p>
<i>SX-A_RESET</i>	r/w	0	<p>Controls reset signal for on-board SIOX rev.B and SIOX rev.C I/O DCM sites. Both SIOX rev.B and SIOX rev.C on-board DCM sites share common reset signal. For more details about on-board SIOX DCM sites refer to the corresponding section later in this chapter.</p> <p><i>SIOX-A_RESET</i> =0 corresponds to active reset signal for both SIOX rev.B and SIOX rev.C DCM sites. This is default setting on power on and DSP reset conditions.</p> <p><i>SIOX-A_RESET</i> =1 corresponds to released reset signal for both SIOX rev.B and SIOX rev.C DCM sites.</p>
<i>SX-B_RESET</i>	r/w	0	<p>Controls reset signal for on-board MXSIOX connector for connection to external <i>T/SU-X1</i> SIOX rev.B mini-extender kit. This bit is valid for <i>TORNADO-E548/E549/E509/E5410/E5416</i> DSP controllers only with three DSP on-chip BSP/TDM/McBSP serial ports and does not present for <i>TORNADO-E5402</i> DSP controller. For more details about MXSIOX connector and <i>T/SU-X1</i> SIOX rev.B mini-extender kit refer to the corresponding section later in this chapter and to Appendix B.</p> <p><i>SIOX-B_RESET</i> =0 corresponds to active reset signal for on-board MXSIOX connector for connection to external <i>T/SU-X1</i> SIOX rev.B mini-extender kit. This is default setting on power on and DSP reset conditions.</p> <p><i>SIOX-A_RESET</i> =1 corresponds to released reset signal for on-board MXSIOX connector for connection to external <i>T/SU-X1</i> SIOX rev.B mini-extender kit.</p>

Notes: 1. Access modes: r/w – read/write; r – read-only; w – write only.

TMS320C54x DSP external interrupt requests

TORNADO-E54x DSP controllers provide software configurable selectors of interrupt request source for each of TMS320C54x DSP external interrupt requests (INT0..3 and NMI). This delivers flexible DSP software controlled mapping of multiple on-board interrupt sources to a limited number of external DSP reset inputs.

Each of TMS320C54x DSP external interrupt requests (INT0..3 and NMI) can be configured to generate the corresponding DSP interrupt request from the following *TORNADO-E54x* on-board interrupt request sources:

- *SX_IRQ-0*, *SX_IRQ-1*, *SX_IRQ-2* interrupt requests from on-board SIOX rev.B, SIOX rev.C DCM sites and MXSIOX connector for external *T/SU-X1* SIOX rev.B mini-extender kit (refer to the corresponding section later in this chapter for more details)
- *PX_IRQ-0*, *PX_IRQ-1* interrupt requests from on-board PIOX-16 DCM site (refer to the corresponding section later in this chapter for more details)
- USART interrupt request output
- USB device controller interrupt request output
- WDT expiration condition.

CAUTION

Time duration of active interrupt request signal must be larger than two periods of external bus clock (CLKOUT) of *TORNADO-E54x* on-board DSP.

For more information about TMS320C54x interrupts refer to original TI datasheets and user's guides for TMS320C54x DSP, which are supplied in either paper or electronic form together with this manual.

CAUTION

TORNADO-E54x on-board USART (Infineon SAB82532) and USB controller (Agere Systems USS-820/825) chips shall be configured by DSP software to generate active low output interrupt requests.

TORNADO-E54x on-board interrupt request source selectors for INT0, INT1, INT2, INT3 and NMI TMS320C54x DSP external interrupt requests can be configured via *MIRQ0_SEL_RG*, *MIRQ1_SEL_RG*, *MIRQ2_SEL_RG*, *MIRQ3_SEL_RG* and *MNMI_SEL_RG* IOX control registers correspondingly (refer to table 2-3 for addressing details).

***MIRQ0_SEL_RG* IOX control register (r/w)**

X	0 (r)	0 (r)	0 (r)	0 (r)	<i>MIRQ0_SEL-3</i> (r/w, 0+)	<i>MIRQ0_SEL-2</i> (r/w, 0+)	<i>MIRQ0_SEL-1</i> (r/w, 0+)	<i>MIRQ0_SEL-0</i> (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

MIRQ1_SEL_RG IOX control register (r/w)

X	0 (r)	0 (r)	0 (r)	0 (r)	MIRQ1_SEL-3 (r/w, 0+)	MIRQ1_SEL-2 (r/w, 0+)	MIRQ1_SEL-1 (r/w, 0+)	MIRQ1_SEL-0 (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

MIRQ2_SEL_RG IOX control register (r/w)

X	0 (r)	0 (r)	0 (r)	0 (r)	MIRQ2_SEL-3 (r/w, 0+)	MIRQ2_SEL-2 (r/w, 0+)	MIRQ2_SEL-1 (r/w, 0+)	MIRQ2_SEL-0 (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

MIRQ3_SEL_RG IOX control register (r/w)

X	0 (r)	0 (r)	0 (r)	0 (r)	MIRQ3_SEL-3 (r/w, 0+)	MIRQ3_SEL-2 (r/w, 0+)	MIRQ3_SEL-1 (r/w, 0+)	MIRQ3_SEL-0 (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

MNMI_SEL_RG IOX control register (r/w)

X	0 (r)	0 (r)	0 (r)	0 (r)	MNMI_SEL-3 (r/w, 0+)	MNMI_SEL-2 (r/w, 0+)	MNMI_SEL-1 (r/w, 0+)	MNMI_SEL-0 (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-10. *MIRQ0_SEL_RG, MIRQ1_SEL_RG, MIRQ2_SEL_RG, MIRQ3_SEL_RG and MNMI_SEL_RG* IOX control registers.

register bit(s)	access mode	value at DSP reset	description
{ <i>MIRQ0_SEL-3..0</i> } { <i>MIRQ1_SEL-3..0</i> } { <i>MIRQ2_SEL-3..0</i> } { <i>MIRQ2_SEL-3..0</i> } { <i>MNMI_SEL-3..0</i> }	r/w	{0,0,0,0}	Select interrupt request source for the corresponding TMS320C54x DSP external interrupt request input. The following valid configurations are available: [0,0,0,0] - no interrupt request source (default setting on DSP reset condition) [0,0,0,1] - <i>USART_IRQ</i> USART interrupt request (must be configured as pushed-pulled active low interrupt request output) [0,0,1,0] - <i>USB_IRQQ</i> USB controller interrupt request (must be configured as active low interrupt request output) [0,0,1,1] - interrupt on WDT expiration event [0,1,0,0] - <i>SX_IRQ-0</i> interrupt request from SIOX rev.B/C DCM sites [0,1,0,1] - <i>SX_IRQ-1</i> interrupt request from SIOX rev.B DCM site and MXSIOX connector [0,1,1,0] - <i>SX_IRQ-2</i> interrupt request from SIOX rev.B DCM site and MXSIOX connector [0,1,1,1] - <i>PX_IRQ-0</i> interrupt request from PIOX-16 DCM site [1,0,0,0] - <i>PX_IRQ-1</i> interrupt request from PIOX-16 DCM site. Not shown configurations are reserved and are not recommended for usage.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

XDMP_RG IOX control register for DSP external data memory control

XDMP_RG IOX control register (refer to table 2-3 for addressing details) must be used by on-board TMS320C54x DSP software in order to select memory type for DSP external data memory area (data SRAM or FLASH/EPROM), and to select particular data memory page of either data SRAM or FLASH/EPROM memory, which will be mapped to DSP external data memory address space (refer to figure 2-3 and to the corresponding subsections earlier).

XDMP_RG IOX control register (r/w)

x	<i>XDM_SEL</i> (r/w)	0 (r)	0 (r)	<i>XDM_PAGE-4</i> (r/w, 0+)	<i>XDM_PAGE-3</i> (r/w, 0+)	<i>XDM_PAGE-2</i> (r/w, 0+)	<i>XDM_PAGE-1</i> (r/w, 0+)	<i>XDM_PAGE-0</i> (r/w, 0+)
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-11. XDMP_RG IOX register.

register bit(s)	access mode	value at DSP reset	Description
<i>XDMP_SEL</i>	r/w	0 (for <i>MP/NO-BMODE</i> <i>MC/HPI-BMODE</i> bootmodes) 1 (for <i>MC/FLASH8-BMODE</i> bootmode)	Defines on-board memory type (external data SRAM or FLASH/EPROM), which is selected as external data memory for on-board TMS320C54x DSP. TMS320VC5410 and TMS320VC5416 DSP of <i>TORNADO-E5410/E5416</i> DSP controllers correspondingly also require that bit DROM of DSP on-chip PMST register must be set to the DROM=0 state. <i>XDMP_SEL</i> =0 corresponds to on-board external data SRAM is selected as external data memory. This is default setting for <i>MP/NO-BMODE</i> and <i>MC/HPI-BMODE</i> bootmodes. <i>XDMP_SEL</i> =1 corresponds to on-board FLASH/EPROM is selected as external data memory. This is default setting for <i>MC/FLASH8I-BMODE</i> bootmode.
{ <i>XDM_PAGE-4..0</i> }	r/w	{0,0,0,0,0}	Selects particular external data memory page of selected on-board external data memory, which is mapped to the DSP external data memory address space. TMS320VC5410 and TMS320VC5416 DSP of <i>TORNADO-E5410/E5416</i> DSP controllers correspondingly also require that bit DROM of DSP on-chip PMST register must be set to the DROM=0 state. Number of external data memory pages varies upon the TMS320C54x DSP type (refer to figure 2-3 and original TI documentation for more details) and capacity of installed FLASH/EPROM chip.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DEV_ID_RG IOX control register for software identification of TORNADO-E54x DSP controllers

On-board DSP software of *TORNADO-E54x* DSP controllers can read DSP controller type (device ID) and revision code (revision ID) via read-only *DEV_ID_RG* IOX control register (refer to table 2-3 for addressing details). This allows DSP software to automatically configure DSP environment and DSP on-chip wait state control and PLL control registers upon the particular DSP installed.

DEV_ID_RG IOX control register (r)

x	0 (r)	<i>REV_ID-2</i> (r)	<i>REV_ID-1</i> (r)	<i>REV_ID-0</i> (r)	0 (r)	<i>DEV_ID-2</i> (r)	<i>DEV_ID-1</i> (r)	<i>DEV_ID-0</i> (r)
bit-15...bit-8	Bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-12. DEV_ID_RG IOX control register.

register bit(s)	access mode	Description
{DEV_ID-2..0}	r	Returns device ID code for TORNADO-E54x DSP controllers as the following: [0,0,1] - TORNADO-E548 [0,1,0] - TORNADO-E549 [0,1,1] - TORNADO-E5402 [1,0,0] - TORNADO-E5409 [1,0,1] - TORNADO-E5410 [1,1,0] - TORNADO-E5416 Unlisted device ID codes are reserved.
{REV_ID-2..0}	r	Returns hardware revision ID code for TORNADO-E54x DSP controllers as the following: [0,0,1] - revision 1 Unlisted revision ID codes are reserved.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

SYS_STAT_RG IOX control register for information about DSP start-up mode

On-board DSP software of *TORNADO-E54x* DSP controllers can read latched DSP start-up boot mode and HPI enable status information via read-only *SYS_STAT_RG* IOX control register (refer to table 2-3 for addressing details). This allows DSP software to automatically configure DSP environment and to recognize DSP memory map.

SYS_STAT_RG IOX control register (r)

x	0 (r)	0 (r)	0 (r)	0 (r)	HPI_ENABLE (r) (TORNADO-E5402/E5409/E5416) 1 (r) (TORNADO-E548/E549/E5410)	0 (r)	BMODE-1 (r)	BMODE-0 (r)
bit-15...bit-8	Bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

CAUTION

BMODE-0, *BMODE-1* and *HPI_ENABLE* read-only bits of *SYS_STAT_RG* IOX control register are latched on release of DSP reset signal and will not change during DSP is running until new active DSP reset signal will be applied.

Table 2-13. *SYS_STAT_RG* IOX control register.

register bit(s)	access mode	Description
{ <i>BMODE-1</i> , <i>BMODE-0</i> }	r	<p>Returns latched DSP start-up bootmode as the following (refer to table 2-1 for details about bootmodes configurations):</p> <ul style="list-style-type: none"> [0,0] - DSP microprocessor mode, no boot (<i>MP/NO-BMODE</i>) [0,1] - DSP microcontroller mode, boot from 8-bit FLASH/EPROM (<i>MC/FLASH8-BMODE</i>) [1,0] - DSP microcontroller mode, boot from DSP on-chip HPI port (<i>MC/HPI-BMODE</i>) [1,1] - reserved, currently corresponds to DSP microprocessor mode, no boot (<i>MP/NO-BMODE</i>).
<i>HPI_ENABLE</i>	r	<p>Returns latched HPI enable status for <i>TORNADO-E5402/E5409/E5416</i> DSP controllers with DSP on-chip enhanced HPI8 port, which is defined by on-board SW2-3 switch (refer to the corresponding subsection later in this chapter and Appendix A). <i>TORNADO-E5402/E5409/E5416</i> DSP controllers always read this bit as '1'.</p> <p><i>HPI_ENABLE=0</i> corresponds to disabled HPI port for <i>TORNADO-E5402/E5409/E5416</i> DSP controllers, which has been disabled by setting on-board SW2-3 switch to the 'ON' state. In case DSP on-chip HPI port has been disabled, then HPI data bits at on-board JP7 connector can be used as general purpose I/O pins (refer to the corresponding subsection later and to original TI documentation for more details). Also, In case HPI port has been disabled for <i>TORNADO-E5402</i> on-board TMS320VC5402 DSP, then DSP of on-chip timer #1 can be routed to <i>TM/XIO-1</i> timer/I/O pin of SIOX, MXSIOX and PIOX-16 DCM sites via <i>TM/XIO-1_CNF</i> bit of <i>XIO_CNF_RG</i> IOX control register (refer to table 2-6, the corresponding subsection earlier, and to original TI documentation for more details).</p> <p><i>HPI_ENABLE=1</i> corresponds to enabled HPI port for <i>TORNADO-E5402/E5409/E5416</i> DSP controllers, which has been enabled by setting on-board SW2-3 switch to the 'OFF' state. In case DSP on-chip HPI port has been enabled, then it can be used as 8-bit enhanced HPI port only (HPI8 port). <i>TORNADO-E5402/E5409/E5416</i> DSP controllers always read <i>HPI_ENABLE</i> bit as '1'.</p>

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

On-board connector for TMS320C54x DSP on-chip HPI port

TORNADO-E54x DSP controllers provide on-board JP7 HPI port connector (figures 2-2, A-1, and 2-4), which comprises of signals for TMS320C54x DSP on-chip 8-bit HPI port.

Pinout for on-board JP7 HPI connector is shown at figure 2-4 and signal description is presented in table 2-14. All signal names for signals from the HPI connector correspond to that for TI TMS320C54x DSP datasheets.

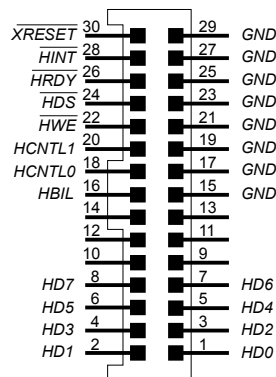


Fig.2-4. Pinout for on-board HPI port connector.

CAUTION

TMS320C54x DSP on-chip HPI port on *TORNADO-E54x* DSP controller is configured with active *HCS* host chip select input (*HCS*=0) and *HAS* host address strobe input set to the '1' state. This enables *HRDY* host ready output and requires *HDS* host data strobe only, while *HHWIL/HCNTRL0/HCNTRL1* HPI port inputs can be connected to host controller address lines.

Table 2-14. TMS320C54x DSP HPI port connector signals.

Signal name	Signal type	Description
<i>HD0..HD7</i>	I/O/Z	HPI data bus.
<i>HBIL</i> <i>HCNTL0</i> <i>HCNTL1</i>	I	HPI register selector address inputs. <i>HBIL</i> , <i>HCNTL0</i> and <i>HCNTL1</i> HPI port inputs shall be connected to host controller A0, A1 and A2 address lines correspondingly.
\overline{HDS}	I	Active low HPI data strobe. This input has on-board pull-up resistor.
\overline{HWE}	I	HPI data write enable input. This input has on-board pull-up resistor.
\overline{HRDY}	O	Active low HPI data ready output.
\overline{HINT}	O	Active low HPI-to-host interrupt request output.
\overline{XRESET}	O	Active low external reset input for on-board DSP and peripherals.
<i>GND</i>	-	Ground.

Note:

1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v TTL signals.

All HPI port signals are 3v/5v TTL compatible and allow output current load as much as $I_{out}=1.5\text{mA}$. Note, that *HDS* and *HRW* inputs have on-board pull up resistors and allow to leave the HPI connector unconnected in case TMS320C54x DSP HPI port is not used.

TORNADO-E54x on-board HPI port connector is 30-pin 2mm guarded male header from Samtec Inc. (www.samtec.com). The mating plug is Samtec TCSD-15-01-N female plug for 2mm 30-wire flat cable, which is included as standard option with **TORNADO-E54x** controller. Extra HPI connector plugs are available either from Samtec or from MicroLAB Systems upon request.

TMS320C54x DSP on-chip HPI port options

There are several options when using TMS320C54x DSP on-chip HPI port for different **TORNADO-E54x** DSP controllers:

- All **TORNADO-E54x** DSP controllers can use TMS320C54x DSP on-chip 8-bit HPI port for connection to host controller (refer to the corresponding subsection below). There are no other options available for **TORNADO-E548/E549/E5410** DSP controllers. This option is applicable to **TORNADO-E5402/E5409/E5416** DSP controllers in case DSP on-chip HPI port has been enabled via on-board SW2-3 switch (table 2-15).
- **TORNADO-E5402/E5409/E5416** DSP controllers can also disable TMS320C54x DSP on-chip HPI port via on-board SW2-3 switch, and use eight HPI data lines (*HD0..HD7*) as general purpose I/O pins. This increases total number of **TORNADO-E5402/E5409/E5416** on-board general purpose I/O lines

to 16 including USART on-chip *DIO-0..7* I/O data pins (refer to the corresponding section later in this chapter for more details).

- Finally, **TORNADO-E5402** DSP controllers with TMS320VC5402 DSP can reconfigure HINT output pin of HPI port to appear as DSP on-chip timer #1, and to configure timer #1 output to appear at the TM/XIO-1 timer/IO pin of on-board SIOX rev.B/C, MXSIOX and PIOX-16 DCM sites, in case TMS320VC5402 DSP on-chip HPI port has been disabled via on-board SW2-3 switch. This increases total number of TMS320VC5402 DSP on-chip timers to two against one timer for each other TMS320C54x DSP. For more details refer to the corresponding subsection earlier and to original TI documentation.

disable control for TMS320C54x DSP on-chip HPI port for TORNADO-E5402/E5409/E5416

TORNADO-E5402/E5409/E5416 DSP controllers provide on-board SW2-3 switch (refer to figures 2-2 and A-1) in order to disable TMS320C54x DSP on-chip HPI port.

Table 2-15. HPI port disable control for **TORNADO-E5402/E5409/E5416** DSP controllers.

SW2-3 switch	Description
OFF	<p>TMS320C54x DSP on-chip 8-bit HPI port for TORNADO-E5402/E5409/E5416 DSP controllers is enabled.</p> <p>On-board JP7 connector can be used for communication with host controller. All TMS320C54x DSP HPI features are supported, including mutual interrupt generation between host controller and TMS320C54x DSP.</p>
ON	<p>TMS320C54x DSP on-chip 8-bit HPI port for TORNADO-E5402/E5409/E5416 DSP controllers is disabled.</p> <p>HD0..HD7 data pins of JP7 connector (figure 2-4) can be used as general purpose I/O pins configured via DSP on-chip GPCR and GPSR registers (refer to original TI documentation for more details).</p> <p>TORNADO-E5402 DSP controllers can also reconfigure HINT output pin of HPI port to appear as DSP on-chip timer #1 (via bit TOUT1 of DSP on-chip GPCR register), and to configure timer #1 output to appear at the TM/XIO-1 timer/IO pin of on-board SIOX rev.B/C, MXSIOX and PIOX-16 DCM sites (via bit <i>TM/XIO-1_CNF</i> of <i>XIO_CNF_RG IOX</i> register). For more details refer to the corresponding subsection earlier and to original TI documentation.</p>

Note:

1. Highlighted configuration corresponds to default factory setting.

CAUTION

Refer to original TI documentation for details about how to use HPI port as general purpose I/O pins and how to enable TMS320VC5402 DSP on-chip timer #1.

CAUTION

TMS320C54x DSP on-chip HPI port for *TORNADO-E548/E549/E5410* DSP controllers is always enabled and cannot be disabled.

Using TMS320C54x DSP on-chip HPI port for connection to host controller

All *TORNADO-E54x* DSP controllers offer direct access from host controller to TMS320C54x on-chip 8-bit HPI port via on-board JP7 connector (figure 2-3 and table 2-14). For *TORNADO-E54x* DSP controllers this feature requires that DSP on-chip HPI port is enabled via on-board SW2-3 switch (table 2-15).

All TMS320C54x DSP HPI features are supported, including mutual interrupt generation between host controller and TMS320C54x DSP.

CAUTION

TMS320VC5409/TMS320VC5416 DSP on-chip HPI port at *TORNADO-E5409/E5416* DSP controllers is configured in HPI8 mode.

Refer to original TI documentation for details about how to program TMS320C54x DSP on-chip HPI port.

Generating DSP-to-Host Interrupt Request

TORNADO-E54x supports generation of HPI-to-host interrupt request from the on-board TMS320C54x DSP to host computer via HPI port (*HINT* signal at the HPI port connector JP7) in order to synchronize between program execution in host and on-board DSP environments.

Writing logical '1' by the DSP software to bit *HINT* of TMS320C54x DSP on-chip HPIC register will result in generation of low level *HINT* signal at the HPI port connector JP7. This signal level is active for generation of DSP-to-host interrupt request. Refer to TMS320C54x documentation for more details about for how to program the HPI port.

Processing Requests from Host Computer

TORNADO-E54x supports processing of host-to-HPI interrupt request (*DSPINT*) from host computer to TMS320C54x DSP via HPI in order to synchronize between the program execution in host and on-board DSP environments.

Writing logical '1' by the host software to the *DSPINT* bit (host-to-DSP interrupt via HPI) of HPIC register will result in generation *HPINT* DSP on-chip interrupt request from HPI port. User software for the TMS320C54x DSP should provide processing of *HPINT* interrupt request in accordance with software requirements. Refer to TMS320C54x documentation for more details about how to program the HPI port.

PIOX-16 DCM site

TORNADO-E54x controller provides on-board JP14 PIOX-16 (parallel I/O expansion interface) DCM site header (refer to figure 2-2 and A-1) for compatible high-speed AD/DA/DIO DCM.

PIOX-16 interface occupies 64Kx16 address space and is allocated directly into external I/O address space of TMS320C54x DSP and can be accessed via DSP I/O read/write instructions in case DSP XF flag is set to the '0' state (refer to table 2-3).

PIOX-16 site comprises of the TMS320C54x DSP 16-bit data and 16-bit address buses, data strobes, timer/IO TM/XIO-0/1 I/O pins, *IRQ-0/1* external interrupt requests, and $\pm 5\text{v}/\pm 12\text{v}$ power supply lines. For details about PIOX-16 site refer to the corresponding section later in this chapter.

SIOX rev.B DCM site

TORNADO-E54x provides on-board JP5 SIOX (serial I/O expansion interface) rev.B DCM site header (refer to figure 2-2 and A-1) for compatible *TORNADO* SIOX rev.B AD/DA/DIO DCM.

SIOX rev.B interface site comprises of signals for two TMS320C54x DSP-on-chip serial ports, timer/IO TM/XIO-0/1 I/O pins, *IRQ-0..2* external interrupt requests, and $\pm 5\text{v}/\pm 12\text{v}$ power supply lines.

For more details about SIOX rev.B interface site refer to the corresponding section later in this chapter.

SIOX rev.C enhanced DCM site

TORNADO-E54x also provides on-board JP6 SIOX rev.C DCM site header (refer to figure 2-2 and A-1) for compatible *TORNADO* SIOX rev.C AD/DA/DIO DCM.

SIOX rev.C interface site is an enhanced version of SIOX rev.B interface site and comprises of signals for two TMS320C54x DSP-on-chip serial ports, timer/IO TM/XIO-0/1 I/O pins, *IRQ-0* external interrupt requests, 8-bit DSP parallel data bus, 6-bit DSP address lines, parallel data strobes, and $+5\text{v}/\pm 12\text{v}$ power supply lines.

8-bit parallel data bus area of SIOX rev.C interface site is allocated directly into external I/O address space of TMS320C54x DSP and can be accessed via DSP I/O read/write instructions in case DSP XF flag is set to the '1' state (refer to table 2-3).

For more details about SIOX rev.C interface site refer to the corresponding section later in this chapter.

MXSIOX connector for external T/SU-X1 SIOX rev.B mini-extender kit

TORNADO-E548/E549/E5409/E5410/E5416 DSP controllers with three DSP on-chip BSP/TDM/McBSP serial ports provide on-board JP16 MXSIOX connector (refer to figure 2-2 and A-1) for connection to external **T/SU-X1** SIOX rev.B mini-extender kit, which can carry one compatible **TORNADO** SIOX rev.B AD/DA/DIO DCM.

MXSIOX connector comprises of signals for two TMS320C54x DSP-on-chip serial ports, timer/IO TM/XIO-0/1 I/O pins, *IRQ-1..2* external interrupt requests, and +5v/±12v power supply lines.

For more details about MXSIOX connector refer to the corresponding section later in this chapter and to Appendix B.

external reset input connector

TORNADO-E54x on-board JP2 external reset input connector (refer to figures 2-2 and A-1) must be used in order to apply active low **XRESET** external reset signal. **XRESET** external reset signal must be 3v/5v TTL compatible external digital output signal.

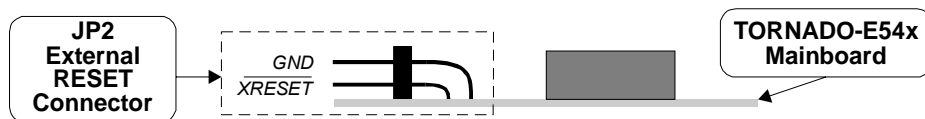


Fig. 2-5. Pinout of external reset input connector for **TORNADO-E54x**.

TORNADO-E54x on-board JP2 external reset input connector is the industry standard 2-pin 0.1" pitch dual-row right-angle male header. Compatible 2-pin female plug is available from a variety of vendors including AMP, Molex, etc..

external power input connector

TORNADO-E54x on-board JP1 external power connector (refer to fig.2-2 and fig.A-1) comprises of the ±5v and ±12v power lines. Note, that only +5v power source is required for operation of on-board **TORNADO-E54x** hardware. Other power lines (-5v and ±12v) are wired to on-board PIOX-16 and SIOX sites.

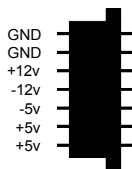


Fig. 2-6. Pinout of power input connector for **TORNADO-E54x**.

TORNADO-E54x on-board JP1 external power connector is the industry standard 7-pin 0.1" pitch single-row right-angle male power header, which is available from a variety of vendors including AMP, Molex, etc. One piece of mating power plug is included with *TORNADO-E54x* shipment package. Extra power plugs are available either from MicroLAB Systems upon request, or from AMP, Molex and other manufacturers.

2.3 Parallel I/O Expansion Interface Site (PIOX-16)

TORNADO-E54x architecture provides expansion of on-board I/O resources using 16-bit parallel I/O expansion interface (PIOX-16) site for compatible DCM, which must be installed above the *TORNADO-E54x* mainboard (refer to fig.1-1 and fig.2-7).

A variety of 'of-the-shelf' *TORNADO* PIOX-16 DCM comprises of AD/DA/DIO, application-specific and DSP coprocessor DCM for real time multi-channel high-speed telecom, instrumentation, industrial, digital radio, etc signal processing applications.

Description

TORNADO-E54x on-board JP14 PIOX-16 DCM site appears as 64Kx16 I/O address space and is allocated directly into external I/O address space of TMS320C54x DSP (refer to table 2-3). PIOX-16 interface site comprises of the TMS320C54x DSP 16-bit data and 16-bit address buses, data strobes, timer/IO TM/XIO-0/1 I/O pins, *PX_IRQ-0/1* external interrupt requests, and $\pm 5\text{V}/\pm 12\text{V}$ power supply lines. PIOX-16 supports 16-bit data transfer cycles.

Installation of PIOX-16 DCM onto *TORNADO-E54x*

Figure 2-7 shows installation of PIOX-16 DCM onto *TORNADO-E54x* DSP controller.

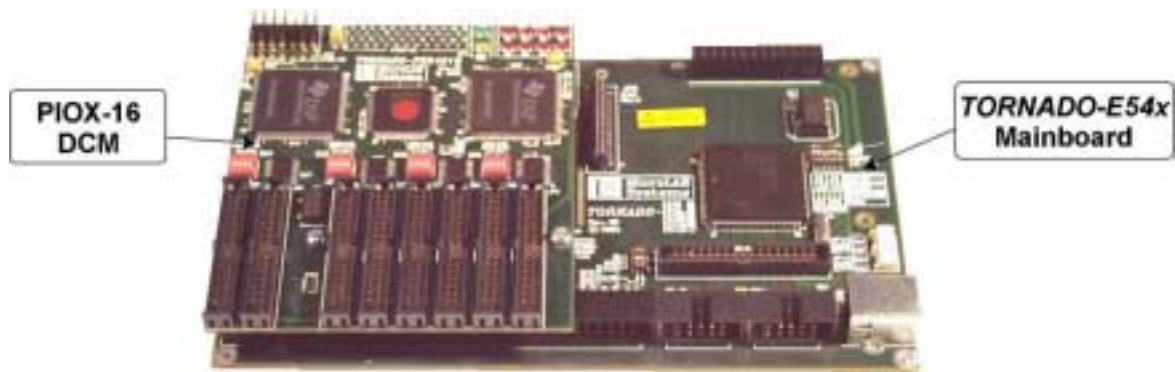


Fig.2-7. Installation of PIOX-16 DCM onto *TORNADO-E54x*.

Accessing PIOX-16 from TMS320C54x DSP environment

TORNADO-E54x on-board PIOX-16 DCM site can be accessed via DSP I/O read/write instructions in case DSP XF flag is set to the '0' state (refer to table 2-3).

PIOX-16 connector pinout

TORNADO-E54x on-board PIOX-16 connector p/n is DHB-RB50-S13NN, which is a high-density 50-pin DHB-series dual-row female connector with 0.05” pin pitch from Fujikura-DDK Ltd (www.ddkconnectors.com). Compatible PIOX-16 plug is DHB-PK50-S13NN, which are available upon request from MicroLAB Systems for design custom PIOX-16 DCM.

PIOX-16 DCM site connector pinout is shown at fig 2-8, whereas signal specifications are presented in table 2-16.

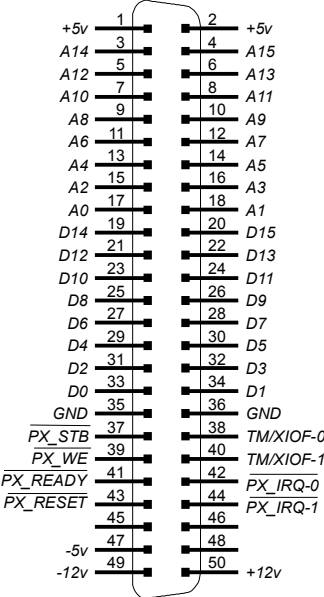


Fig.2-8. PIOX-16 DCM site connector pinout (top view).

Table 2-16. PIOX-16 DCM site signal description.

Signal name	signal type	description
Parallel Data Buss		
<i>A0..A15</i>	O	DSP address bus.
<i>D0..D15</i>	I/O	DSP data bus.
$\overline{PX_STB}$	O	Active low data transfer strobe.
$\overline{PX_WE}$	O	Active low write enable signal.
$\overline{PX_READY}$	I	Active low data ready signal, which must be generated by PIOX-16 DCM in order to complete PIOX-16 data transfer cycle. This input has on-board pull-up resistor. Refer to figure 2-9 for more details.
Timer/IO, Reset and Interrupt Requests		
<i>TM/XIO-0</i>	I/O/Z	Configured by on-board DSP software via <i>XIO_CNF_RG</i> IOX control register as either DSP on-chip timer output, or general purpose I/O pin (refer to section 2.2 and tables 2-6, 2-7 and 2-8).
<i>TM/XIO-1</i>	I/O/Z	Configured by on-board DSP software via <i>XIO_CNF_RG</i> IOX control register as either DSP on-chip timer #1 output (<i>TORNADO-E5402</i> only), or general purpose I/O pin (refer to section 2.2 and tables 2-6, 2-7 and 2-8).
$\overline{PX_RESET}$	O	Active low reset signal for on-board PIOX-16 DCM site, which is controlled via <i>PX_RESET</i> bit of <i>PXSX_RESET_RG</i> IOX control register (refer to table 2-9 and section 2.2).
$\overline{PX_IRQ-0}$, $\overline{PX_IRQ-1}$	I	Active low interrupt requests from PIOX-16 DCM site to on-board TMS320C54x DSP, which can be configured by <i>MIRQ0_SEL_RG</i> , <i>MIRQ1_SEL_RG</i> , <i>MIRQ2_SEL_RG</i> , <i>MIRQ3_SEL_RG</i> and <i>MNMI_SEL_RG</i> IOX control registers to be routed to any of DSP external interrupt inputs (INT0..3 and NMI). Refer to section 2-2 and table 2-10 for more details. Actual DSP interrupt request is generated on the falling edge of these interrupt request inputs. These interrupt request inputs have on-board pull-up resistors.

Power Supplies		
<i>GND</i>		Ground.
+5v		+5v power (from on-board JP1 power input connector).
+12v		+12v power (from on-board JP1 power input connector).
-5v		-5v power (from on-board JP1 power input connector).
-12v		-12v power (from on-board JP1 power input connector).

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v CMOS/TTL signals.

PIOX-16 data transfer cycles

PIOX-16 interface site supports 16-bit data transfer cycles only, and, therefore PIOX-16 connector does not contain the cycle definition signals.

Data transfer timing for PIOX-16

The PIOX-16 data transfer timing is presented at figure 2-9. This data transfer timing is known as MOTO mode and assumes usage of data strobe signal and write enable signal. Different *TORNADO-E54x* DSP controllers provide different timing for parallel data transfer via PIOX-16 DCM site.

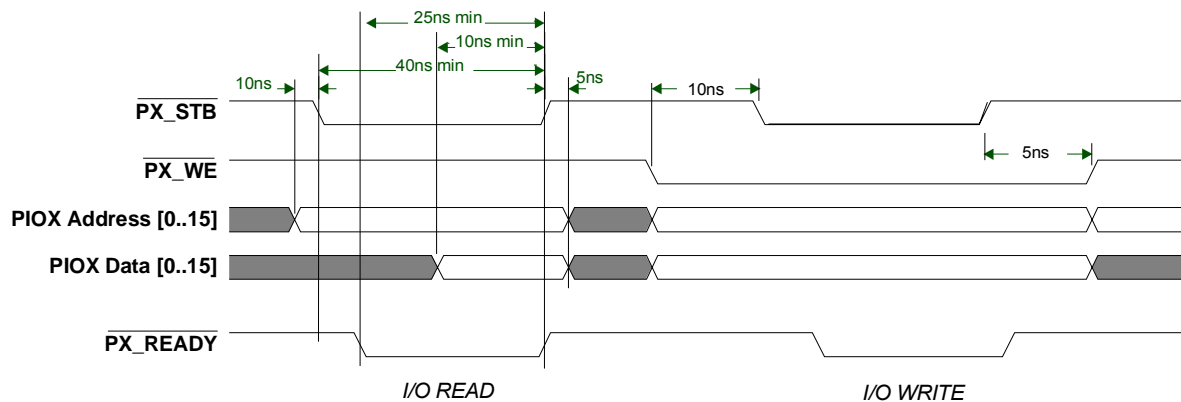


Fig.2-9a. Timing diagram for PIOX-16 parallel data transfer for *TORNADO-E549/E5402/E5410*.

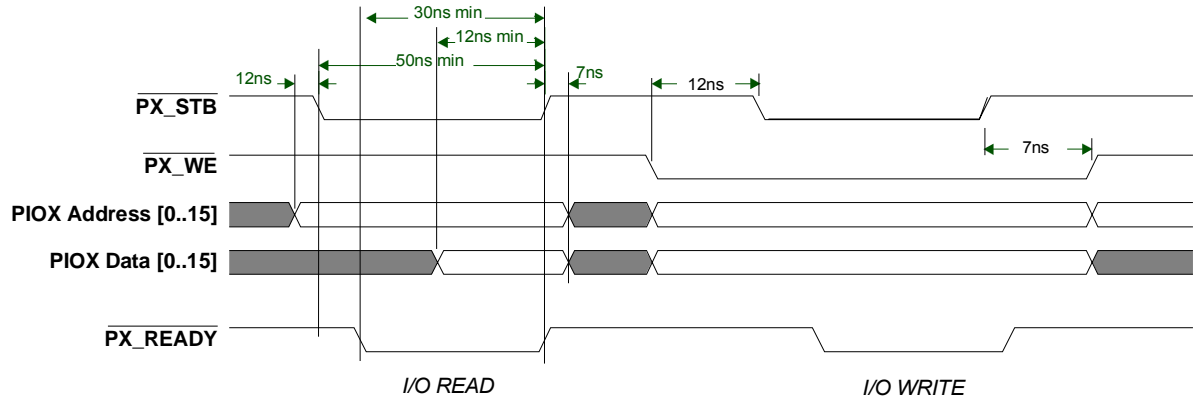


Fig.2-9b. Timing diagram for PIOX-16 parallel data transfer for *TORNADO-E548/E5409/E5416*.

CAUTION

The DSP on-chip wait state control and PLL control registers of TMS320C54x DSP shall be programmed in accordance with table 2-2 in order to meet timing requirements for *TORNADO-E54x* on-board PIOX-16 interface site.

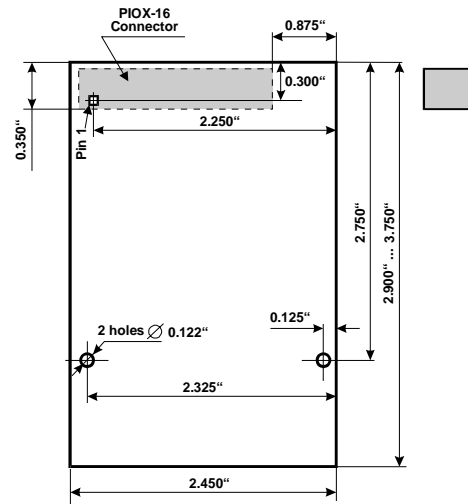
PIOX-16 data transfer cycle is terminated by *PX_READY* signal, which must be generated by installed PIOX-16 DCM.

Generating Reset Signal for PIOX/PIOX-16 Site

TORNADO-E54x provides individual reset signal for PIOX-16 DCM site, which is controlled by *PX_RESET* bit of *PXSX_RESET_RG* IOX control register (refer to table 2-9 and section 2.2 for more details). This allows correct initialization of installed PIOX-16 DCM hardware and correct synchronization with host *TORNADO-E54x* DSP software.

Physical dimensions for PIOX-16 DCM

Physical dimensions for PIOX-16 DCM are presented at fig.2-10. This information is intended for those *TORNADO* customers, who need to design custom PIOX-16 DCM.



PIOX-16 connector: DDK DHB-Px50

Fig.2-10. Physical dimensions for PIOX-16 DCM.

2.4 Serial I/O Expansion Interface Sites (SIOX)

TORNADO-E54x DSP controllers provide several on-board SIOX (serial I/O expansion) DCM sites (refer to figures 2-2 and A-1), which are designed to carry *TORNADO* SIOX compatible DCM:

A variety of 'of-the-shelf' *TORNADO* SIOX DCM comprise from AD/DA/DIO and application specific I/O coprocessors DCM for telecommunication, speech/fax/modem and audio signal processing, industrial and instrumentation applications, and many more.

Description

TORNADO-E54x DSP controllers provide three different types of on-board SIOX DCM sites (fig.2-11):

- SIOX-A rev.B site (JP5), which comprises of signals for SIO-0 and SIO-1 serial ports, TM/XIO-0/1 timer/IO pins, external SX_IRQ-0/1/2 interrupts request inputs, SIOX rev.B/C reset signal, and power supply lines
- enhanced SIOX rev.C site (JP6), which comprises of signals for SIO-0 and SIO-1 serial ports, TM/XIO-0/1 timer/IO pins, external SX_IRQ-0 interrupts request, SIOX rev.B/C reset signal, 8-bit DSP data bus, 6-bit DSP address bus, parallel data bus strobes, and power supply lines
- MXSIOX connector (*TORNADO-E548/E549/E5409/E5410/E5416* only) for connection to external *T/SU-X1* SIOX rev.B mini-extender kit (refer to Appendix B), which can carry one SIOX rev.B DCM. MXSIOX connector site comprises of signals for SIO-0 and SIO-1 serial ports, *TM/XIO-0/1* timer/IO pins, external *SX_IRQ-1/2* interrupts request inputs, MXSIOX reset signal, and power supply lines.

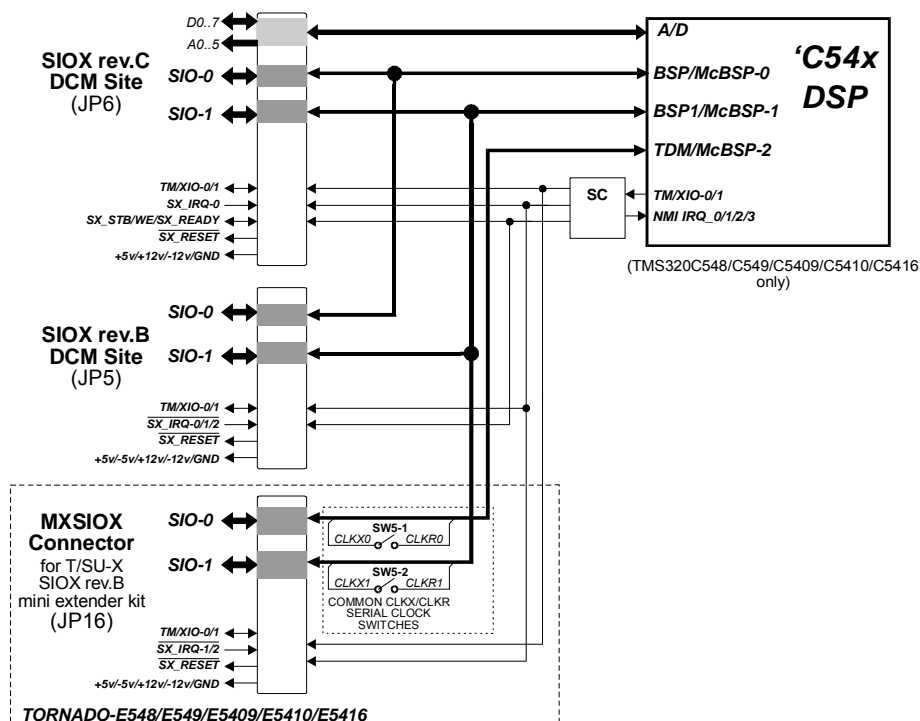


Fig.2-11. SIOX DCM sites connection diagram for TORNADO-E54x.

SIO-0 and SIO-1 ports of TORNADO-E54x on-board SIOX rev.B and rev.C sites are connected to the TMS320C54x DSP on-chip BSP/McBSP-0 and BSP1/McBSP-1 serial ports correspondingly. However, SIO-0 and SIO-1 ports of TORNADO-E548/E549/E5409/E5410/E5416 on-board MXSIOX connectors are connected to the TMS320C54x DSP on-chip TDM/McBSP-2 and BSP1/McBSP-1 serial ports correspondingly.

TORNADO-E54x on-board MXSIOX connector is also supplied with on-board SW5-1 and SW5-2 switches, which are used to set common serial clock for transmitter/receiver of MXSIOX SIO-0 and SIO-1 ports correspondingly.

Maximum throughput of SIO-0/1 serial ports of SIOX sites is 80 Mbit/s for TORNADO-E5416 DSP controllers, 50 Mbit/s for TORNADO-E549/E5402/E5410 DSP controllers, and 40 Mbit/s for TORNADO-E548/E5409 DSP controllers. Refer to original TI documentation for more details about programming TMS320C54x DSP on-chip BSP/TDM/McBSP ports.

TM/XIO-0/1 timer I/O pins of TORNADO-E54x on-board SIOX DCM sites and MXSIOX connector can be configured as either timer or general purpose I/O pins by DSP software via XIO_CNF_RG, XIO_DIR_RG and XIO_DATA_RG IOX control registers (refer to tables 2-6, 2-7, 2-8 and section 2.2).

Maximum output clock frequency for TM/XIO-0/1 pins in case they are configured as TMS320C54x DSP on-chip timer outputs (TOUT and TOUT1) is 80 MHz for TORNADO-E5416 DSP controllers, 50 MHz for TORNADO-E549/E5402/E5410 DSP controllers, and 40 MHz for TORNADO-E548/E5409 DSP controllers. Refer to original TI documentation for more details about programming TMS320C54x DSP on-chip timers.

Installation of SIOX DCM onto TORNADO-E54x

SIOX rev.B and SIOX rev.C DCM can plug directly into *TORNADO-E54x* on-board SIOX rev.B and SIOX rev.C DCM sites. External analog and digital I/O signals for installed SIOX DCM shall be connected by means of the SIOX on-module I/O connector via rear panel of host PC.

CAUTION

TORNADO-E54x on-board area for SIOX rev.B DCM is shared with the on-board area for SIOX rev.C DCM. Either SIOX rev.B DCM or SIOX rev.C can be installed onto *TORNADO-E54x* mainboard.

TORNADO-E54x on-board MXSIOX connector is used for connection to external *T/SU-X1* SIOX rev.B mini-extender kit via *T/SU-X1/XC* flat cable. *T/SU-X1* SIOX rev.B mini-extender can be used for installation of one SIOX rev.B DCM.

Figure 2-12 shows installation examples of different SIOX DCM into the corresponding DCM sites on *TORNADO-E54x* mainboard.



Fig.2-12a. TORNADO-E54x mainboard with installed SIOX rev.B DCM.

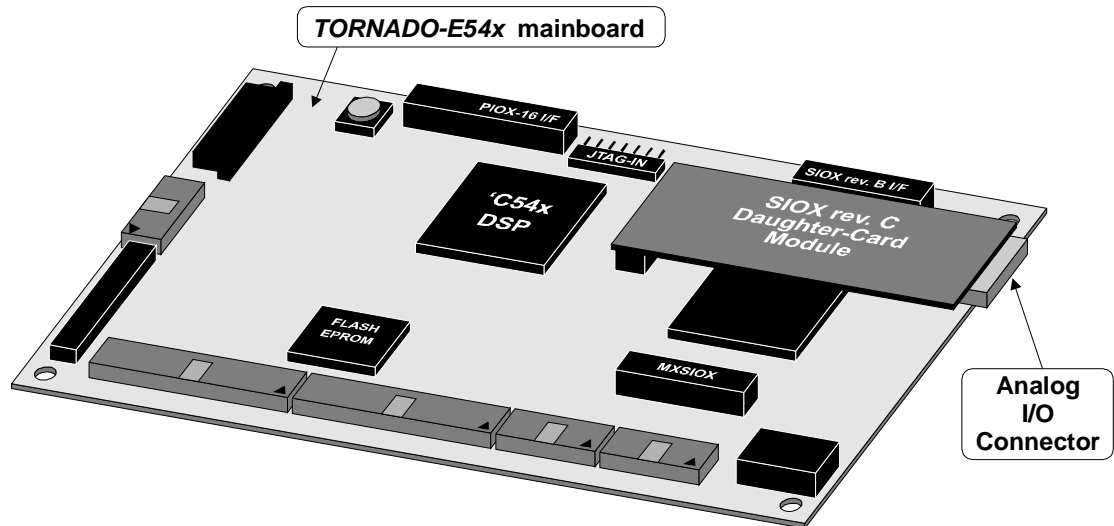


Fig.2-12b. TORNADO-E54x mainboard with installed SIOX rev.C DCM.

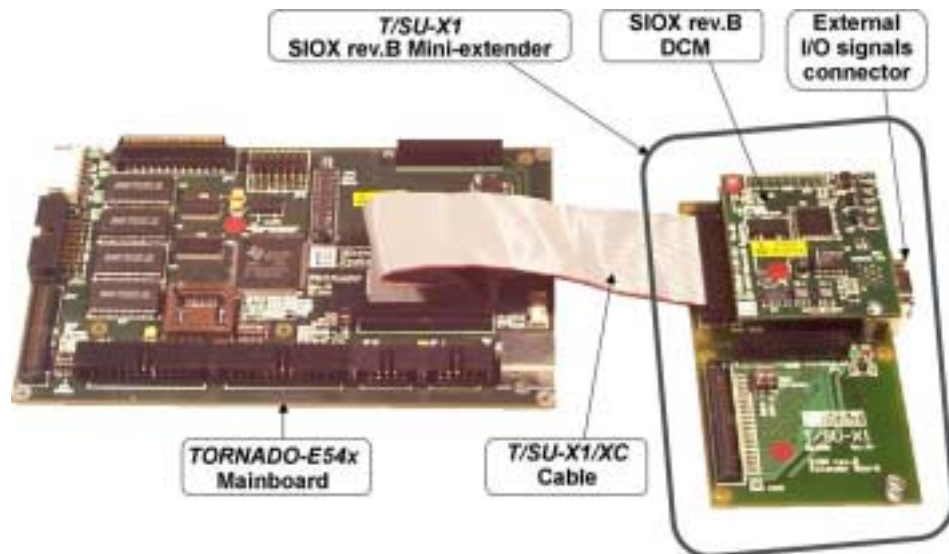


Fig.2-12c. TORNADO-E54x mainboard with external T/SU-X1 mini-extender with installed SIOX rev.C DCM.

SIOX rev.B DCM site connector and signal description

TORNADO-E54x on-board SIOX rev.B DCM site connector (JP5) is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. Mating plug is the industry standard 26-pin dual-row male header with 0.1"x0.1" pin pattern, which is available from virtually all connector manufacturers.

SIOX rev.B DCM site connector pinout is shown at figure 2-13 and signal specifications are presented in table 2-17.

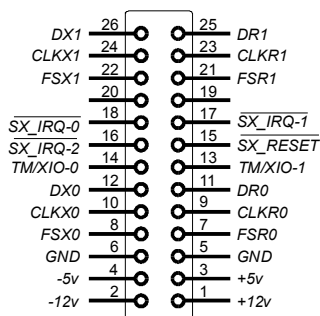


Fig.2-13. SIOX rev.B DCM site connector pinout (top view).

Table 2-17. SIOX rev.B DCM site signal specification.

SIOX signal name	signal type	description
SIO-0 port control		
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port. For SIOX rev.B site of TORNADO-E54x DSP controllers these signals correspond to the TMS320C54x DSP on-chip BSP/McBSP-0 serial port transmitter.
DR0 FSR0 CLKR0	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port. For SIOX rev.B site of TORNADO-E54x DSP controllers these signals correspond to the TMS320C54x DSP on-chip BSP/McBSP-0 serial port receiver.
SIO-1 port control		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port. For SIOX rev.B site of TORNADO-E54x DSP controllers these signals correspond to the TMS320C54x DSP on-chip BSP1/McBSP-1 serial port transmitter.
DR1 FSR1 CLKR1	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port. For SIOX rev.B site of TORNADO-E54x DSP controllers these signals correspond to the TMS320C54x DSP on-chip BSP1/McBSP-1 serial port receiver.

Timer/IO, Reset and Interrupt Requests		
<i>TM/XIO-0</i>	I/O/Z	Configured by on-board DSP software via <i>XIO_CNF_RG</i> IOX control register as either DSP on-chip timer output, or general purpose I/O pin (refer to section 2.2 and tables 2-6, 2-7 and 2-8).
<i>TM/XIO-1</i>	I/O/Z	Configured by on-board DSP software via <i>XIO_CNF_RG</i> IOX control register as either DSP on-chip timer #1 output (<i>TORNADO-E5402</i> only), or general purpose I/O pin (refer to section 2.2 and tables 2-6, 2-7 and 2-8).
<i>SX_RESET</i>	O	Active low reset signal for on-board SIOX rev.B/C DCM sites, which is controlled via <i>SX-A_RESET</i> bit of <i>PXSX_RESET_RG</i> IOX control register (refer to table 2-9 and section 2.2).
<i>SX_IRQ - 0</i> , <i>SX_IRQ - 1</i> , <i>SX_IRQ - 2</i>	I	Active low interrupt requests from SIOX rev.B/C DCM sites and MXSIOX connector to on-board TMS320C54x DSP, which can be configured by <i>MIRQ0_SEL_RG</i> , <i>MIRQ1_SEL_RG</i> , <i>MIRQ2_SEL_RG</i> , <i>MIRQ3_SEL_RG</i> and <i>MNMI_SEL_RG</i> IOX control registers to be routed to any of DSP external interrupt inputs (INT0..3 and NMI). Refer to section 2-2 and table 2-10 for more details. Actual DSP interrupt request is generated on the falling edge of these interrupt request inputs. These interrupt request inputs have on-board pull-up resistors.
Power Supplies		
<i>GND</i>		Ground.
<i>+5v</i>		+5v power (from on-board JP1 power input connector).
<i>+12v</i>		+12v power (from on-board JP1 power input connector).
<i>-5v</i>		-5v power (from on-board JP1 power input connector).
<i>-12v</i>		-12v power (from on-board JP1 power input connector).

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
1. All logical signal levels and load currents correspond to that for 3v/5v CMOS/TTL signals.

SIOX rev.C DCM site connector and signal description

TORNADO-E54x on-board SIOX rev.C DCM site connector (JP6) is a high-density dual-row 40-pin female header with 0.05"x0.05" pin pattern from Samtec Inc (www.samtec.com). Compatible SIOX rev.C plugs (Samtec p/n TFM-120-22-S-D-LC) for design of custom SIOX rev.B DCM are available from MicroLAB Systems upon request.

SIOX rev.C DCM site connector pinout is shown at figure 2-14 and signal specifications are presented in table 2-18.

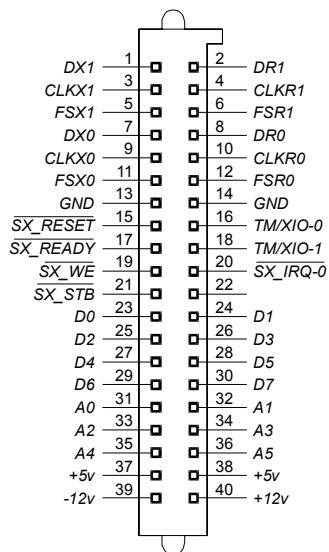


Fig.2-14. SIOX rev.C DCM site connector pinout (top view).

Table 2-18. SIOX rev.C DCM site connector signal specification.

SIOX rev.B connector pin	signal type	Description
<i>SIO-0 port control</i>		
DX0 FSX0 CLKX0	O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port. For SIOX rev.C site of <i>TORNADO-E54x</i> DSP controllers these signals correspond to the TMS320C54x DSP on-chip BSP/McBSP-0 serial port transmitter.
DR0 FSR0 CLKR0	I I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port. For SIOX rev.C site of <i>TORNADO-E54x</i> DSP controllers these signals correspond to the TMS320C54x DSP on-chip BSP/McBSP-0 serial port receiver.
<i>SIO-1 port control</i>		
DX1 FSX1 CLKX1	O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port. For SIOX rev.C site of <i>TORNADO-E54x</i> DSP controllers these signals correspond to the TMS320C54x DSP on-chip BSP1/McBSP-1 serial port transmitter.
DR1 FSR1 CLKR1	I I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port. For SIOX rev.C site of <i>TORNADO-E54x</i> DSP controllers these signals correspond to the TMS320C54x DSP on-chip BSP1/McBSP-1 serial port receiver.

Timer/IO, Reset and Interrupt Requests		
<i>TM/XIO-0</i>	I/O/Z	Configured by on-board DSP software via <i>XIO_CNF_RG</i> IOX control register as either DSP on-chip timer output, or general purpose I/O pin (refer to section 2.2 and tables 2-6, 2-7 and 2-8).
<i>TM/XIO-1</i>	I/O/Z	Configured by on-board DSP software via <i>XIO_CNF_RG</i> IOX control register as either DSP on-chip timer #1 output (<i>TORNADO-E5402</i> only), or general purpose I/O pin (refer to section 2.2 and tables 2-6, 2-7 and 2-8).
<i>SX_RESET</i>	O	Active low reset signal for on-board SIOX rev.B/C DCM sites, which is controlled via <i>SX-A_RESET</i> bit of <i>PXSX_RESET_RG</i> IOX control register (refer to table 2-9 and section 2.2).
<i>SX_IRQ - 0</i>	I	Active low interrupt request from SIOX rev.B/C DCM sites to on-board TMS320C54x DSP, which can be configured by <i>MIRQ0_SEL_RG</i> , <i>MIRQ1_SEL_RG</i> , <i>MIRQ2_SEL_RG</i> , <i>MIRQ3_SEL_RG</i> and <i>MNMI_SEL_RG</i> IOX control registers to be routed to any of DSP external interrupt inputs (INT0..3 and NMI). Refer to section 2-2 and table 2-10 for more details. Actual DSP interrupt request is generated on the falling edge of these interrupt request input. This interrupt request input has on-board pull-up resistor.
Parallel Data Bus		
<i>D0..D7</i>	I/O	DSP D0..D7 data bus.
<i>A0..A5</i>	O	DSP A0..A5 address bus.
<i>SX_STB</i>	O	Active low data transfer strobe, which is generated when <i>TORNADO-E54x</i> on-board DSP performs access to SIOX rev.C IOX address area in accordance with table 2-2.
<i>SX_WE</i>	O	Active low write enable signal.
<i>SX_READY</i>	I	Active low SIOX parallel data ready signal, which must be generated by installed SIOX rev.C DCM in order to complete current SIOX rev.C data access cycle. This input has on-board pull-up resistor.
Power Supplies		
<i>GND</i>		Ground.
<i>+5v</i>		+5v power (from on-board JP1 power input connector).
<i>+12v</i>		+12v power (from on-board JP1 power input connector).
<i>-12v</i>		-12v power (from on-board JP1 power input connector).

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v CMOS/TTL logic.

MXSIOX connector pinout and signal description for TORNADO-E548/E549/E5409/E5410/E5416

MXSIOX connector (JP16) can be used for connection to external *T/SU-X1* SIOX rev.B DCM mini-extender kit (refer to Appendix B) and is available for *TORNADO-E548/E549/E5409/E5410/E5416* DSP controllers only with TMS320C54x DSP, which provides three DSP on-chip BSP/TDM/McBSP ports. *T/SU-X1* SIOX rev.B DCM mini-extender kit can be used for installation of one SIOX rev.B DCM, therefore signal specifications for MXSIOX connector are the same as that for SIOX rev.B DCM site.

TORNADO-E54x on-board MXSIOX connector 34-pin dual-row 2mm guarded male headers from Samtec Inc (www.samtec.com). Compatible MXSIOX plug (Samtec p/n TCSD-17-01-N) comes standard with *T/SU-X1/XC* SIOX rev.B mini-extender connection cables (refer to Appendix B for more details), whereas optional MXSIOX plugs for 2mm flat cables are available either from Samtec Inc or from MicroLAB Systems upon request.

Connector pinout for *TORNADO-E54x* on-board MXSIOX connector is shown at figure 2-15 and signal specifications are presented in table 2-19.

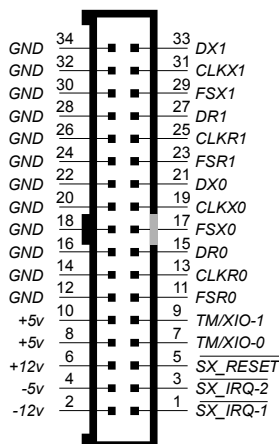


Fig.2-15. Pinout for *TORNADO-E54x* on-board MXSIOX connector (top view).

Table 2-19. Signal description for *TORNADO-E54x* on-board MXSIOX connector.

SIOX rev.B interface signal	signal type	Description
<i>SIO-0 port control</i>		
<i>DX0</i> <i>FSX0</i> <i>CLKX0</i>	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port. For MXSIOX connector of <i>TORNADO-E54x</i> DSP controllers these signals correspond to the TMS320C54x DSP on-chip TDM/McBSP-2 serial port transmitter.
<i>DR0</i> <i>FSR0</i> <i>CLKR0</i>	I I I	Data, frame synchronization and serial clock signals for receiver of SIO-0 port. For MXSIOX connector of <i>TORNADO-E54x</i> DSP controllers these signals correspond to the TMS320C54x DSP on-chip TDM/McBSP-2 serial port receiver.

SIO-1 port control		
<i>DX1</i> <i>FSX1</i> <i>CLKX1</i>	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port. For MXSIOX connector of <i>TORNADO-E54x</i> DSP controllers these signals correspond to the TMS320C54x DSP on-chip BSP1/McBSP-1 serial port transmitter.
<i>DR1</i> <i>FSR1</i> <i>CLKR1</i>	I I/O I	Data, frame synchronization and serial clock signals for receiver of SIO-1 port. For MXSIOX connector of <i>TORNADO-E54x</i> DSP controllers these signals correspond to the TMS320C54x DSP on-chip BSP1/McBSP-1 serial port receiver.
Timer/I/O, Reset and Interrupt Requests		
<i>TM/XIO-0</i>	I/O	Configured by on-board DSP software via <i>XIO_CNF_RG</i> IOX control register as either DSP on-chip timer output, or general purpose I/O pin (refer to section 2.2 and tables 2-6, 2-7 and 2-8).
<i>TM/XIO-1</i>	I/O	Configured by on-board DSP software via <i>XIO_CNF_RG</i> IOX control register as general purpose I/O pin (refer to section 2.2 and tables 2-6, 2-7 and 2-8). This pin cannot be configured as timer #1 output, since this option is available for <i>TORNADO-E5402</i> DSP controllers only, whereas <i>TORNADO-E5402</i> DSP controller does not have on-board MXSIOX connector.
<i>SX_RESET</i>	O	Active low reset signal for on-board MXSIOX connector, which is controlled via <i>SX-B_RESET</i> bit of <i>PXSX_RESET_RG</i> IOX control register (refer to table 2-9 and section 2.2).
<i>SX_IRQ - 1</i> <i>SX_IRQ - 2</i>	I	Active low interrupt requests from SIOX rev.B DCM site and MXSIOX connector to on-board TMS320C54x DSP, which can be configured by <i>MIRQ0_SEL_RG</i> , <i>MIRQ1_SEL_RG</i> , <i>MIRQ2_SEL_RG</i> , <i>MIRQ3_SEL_RG</i> and <i>MNMI_SEL_RG</i> IOX control registers to be routed to any of DSP external interrupt inputs (INT0..3 and NMI). Refer to section 2-2 and table 2-10 for more details. Actual DSP interrupt request is generated on the falling edge of these interrupt request inputs. These interrupt request inputs have on-board pull-up resistors.
Power Supplies		
<i>GND</i>		Ground.
<i>+5v</i>		+5v power (from on-board JP1 power input connector).
<i>+12v</i>		+12v power (from on-board JP1 power input connector).
<i>-5v</i>		-5v power (from on-board JP1 power input connector).
<i>-12v</i>		-12v power (from on-board JP1 power input connector).

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v CMOS signals.

Maximum serial clock frequency for MXSIOX connector and T/SU-X1 SIOX rev.B mini-extender kit

Although maximum output serial clock frequency for BSP/TDM/McBSP serial ports of *TORNADO-E54x* DSP controllers is 80 MHz for *TORNADO-E5416* DSP controllers, 50 MHz for *TORNADO-E549/E5402/E5410* DSP controllers, and 40 MHz *TORNADO-E548/E5409* for DSP controllers, actual maximum serial clock frequency for SIO-0/1 serial ports of MXSIOX connector is limited by the length of connection cables, which are used for connection to external *T/SU-X1* SIOX rev.B mini-extender, and particular by serial clock distribution configuration for installed SIOX rev.B DCM.

CAUTION

In case standard 10” long (0.25m) cable is used for connection of external *T/SU-X1* SIOX rev.B mini-extender to *TORNADO-E54x* on-board MXSIOX connector, and the corresponding *TORNADO-E54x* on-board SW5-1 and SW5-2 common serial clock enable switches are set to the ‘OFF’ state (refer to the corresponding subsection below for more details) , then the recommended maximum serial clock frequency for CLKX/CLKR signals for SIO-0/1 serial ports of MXSIOX connector is 33 MHz.

CAUTION

In case standard 10” long (0.25m) cable is used for connection of external *T/SU-X1* SIOX rev.B mini-extender to *TORNADO-E54x* on-board MXSIOX connector, and the corresponding *TORNADO-E54x* on-board SW5-1 and SW5-2 common serial clock enable switches are set to the ‘ON’ state (refer to the corresponding subsection below for more details) , then the recommended maximum serial clock frequency for CLKX/CLKR signals for SIO-0/1 serial ports of MXSIOX connector is 20 MHz.

Common CLKX/CLKR serial clock enable control for MXSIOX connector

TORNADO-E548/E549/E5409/E5410/E5416 DSP controllers with on-board MXSIOX connector provide on-board SW5-1 and SW5-2 common CLKX/CLKR serial clock enable switches (refer to figures 2-2 and 2-9 and A-1) for each of SIO-0 and SIO-1 MXSIOX serial ports correspondingly.

Table 2-20 presents available settings for on-board SW5-1 and SW5-2 common CLKX/CLKR serial clock enable switches for MXSIOX SIO-0 and SIO-1 serial ports.

Table 2-20a. Common serial clock enable switches settings for SIO-0 port of MXSIOX connector at *TORNADO-E548/E549/E5409/E5410/E5416* DSP controllers.

SW5-1 switch	description
OFF	Transmitter serial clock (CLKX) and receiver serial clock (CLKR) are disconnected for SIO-0 port of <i>TORNADO-E548/E549/E5409/E5410/E5416</i> on-board MXSIOX connector.
ON	Transmitter serial clock (CLKX) and receiver serial clock (CLKR) are connected for SIO-0 port of <i>TORNADO-E548/E549/E5409/E5410/E5416</i> on-board MXSIOX connector. This setting corresponds to reduced serial clock frequency and data transfer speed.

Note: 1. Highlighted configuration corresponds to default factory setting.

Table 2-20b. Common serial clock enable switches settings for SIO-1 port of MXSIOX connector at *TORNADO-E548/E549/E5409/E5410/E5416* DSP controllers.

SW5-2 switch	Description
OFF	Transmitter serial clock (CLKX) and receiver serial clock (CLKR) are disconnected for SIO-1 port of <i>TORNADO-E548/E549/E5409/E5410/E5416</i> on-board MXSIOX connector.
ON	Transmitter serial clock (CLKX) and receiver serial clock (CLKR) are connected for SIO-1 port of <i>TORNADO-E548/E549/E5409/E5410/E5416</i> on-board MXSIOX connector. This setting corresponds to reduced serial clock frequency and data transfer speed.

Note: 1. Highlighted configuration corresponds to default factory setting.

CAUTION

TORNADO-E54x on-board SW5-1 and SW5-2 common serial clock enable switches for MXSIOX connector shall be used in conjunction with *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switches (SW1 and SW2) in accordance with general guidelines provided in Appendix B of this manual and below in this subsection.

Background for corresponding settings of *TORNADO-E54x* on-board SW5-1 and SW5-2 common serial clock enable switches for MXSIOX connector and *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) enable switches is the ‘long-line’ compensation issue for serial clock signals distribution over connection flat cable between *TORNADO-E54x* on-board MXSIOX connector and *T/SU-X1* SIOX rev.B mini-extender due to the ‘long-line wave nature’ of connection flat cable.

Although the ‘long-line’ compensation resistors are being used for all MXSIOX SIO-0/1 serial port control signals (frame synchronization pulse, serial clock and serial data) at both *TORNADO-E54x* DSP controller and

T/SU-X1 SIOX rev.B mini-extender boards in order to exclude signal reflection, a ‘long-line’ non-compensation for serial clock signals can still occur in case installed SIOX rev.B DCM is using common shorted serial clock for transmitter and receiver of SIO port (many SIOX rev.B DCM actually use this in order to simplify design). Note, that this problem does not occur with SIO port frame synchronization and serial data signals, since these signals always use dedicated lines of SIOX interface and can’t be connected together.

CAUTION

In case installed SIOX rev.B DCM, which is installed onto external *T/SU-X1* SIOX rev.B mini-extender kit connected to **TORNADO-E54x** on-board MXSIOX connector, has been designed without on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and each serial clock is using its dedicated pins, then the corresponding **TORNADO-E54x** on-board common CLKX/CLKR serial clock enable switch (SW5-1 or SW5-2) must be set to ‘OFF’ and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to ‘ON’.

In case installed SIOX rev.B DCM, which is installed onto external *T/SU-X1* SIOX rev.B mini-extender kit connected to **TORNADO-E54x** on-board MXSIOX connector, has been designed with on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and both serial clocks are using shared pins, then the corresponding **TORNADO-E54x** on-board common CLKX/CLKR serial clock enable switch (SW5-1 or SW5-2) must be set to ‘ON’ and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to ‘OFF’.

For more information about external *T/SU-X1* SIOX rev.B mini-extendors refer to Appendix B later in this manual.

Generating reset signal for on-board SIOX rev.B/C sites and MXSIOX connector

TORNADO-E54x DSP controllers provide two reset signals for on-board SIOX DCM sites and MXSIOX connector:

- One common reset signal is provided for on-board SIOX rev.B and SIOX rev.C DCM sites, since these DCM sites are alternative and both SIOX rev.B DCM and SIOX rev.C DCM cannot be installed simultaneously (refer to figures 2-10a and 2-10b). Common reset signal for SIOX rev.B/C DCM sites is controlled by on-board DSP software via **SX-A_RESET** bit of **PXSX_RESET_RG** IOX control register (refer to table 2-9 and section 2.2).
- Second reset signal is provided for on-board MXSIOX connector of **TORNADO-E548/E549/E5409/E5410/E5416** DSP controllers for external SIOX rev.B DCM, which can be installed onto *T/SU-X1* SIOX rev.B mini-extender kit (refer to figure 2-10c), since *T/SU-X1* SIOX rev.B mini-extender kit can be installed simultaneously with either SIOX rev.B or SIOX rev.C DCM. Reset signal for MXSIOX connector is controlled by on-board DSP software via **SX-B_RESET** bit of **PXSX_RESET_RG** IOX control register (refer to table 2-9 and section 2.2).

Accessing SIOX rev.C parallel data from TMS320C54x DSP environment

TORNADO-E54x on-board SIOX rev.C DCM site can be accessed via DSP I/O read/write instructions in case DSP XF flag is set to the '1' state (refer to table 2-3). SIOX rev.C interface features 8-bit data bus, which is wired to the lowest significant byte of 16-bit DSP data bus.

Parallel data transfer timing for SIOX rev.C DCM site

Timing diagram for parallel data transfer via SIOX rev.C DCM site is presented at figure 2-16. This data transfer timing is known as the industry standard MOTO mode and assumes usage of data strobe signal and write enable signal. Different *TORNADO-E54x* DSP controllers provide different timing for parallel data transfer via SIOX rev.C DCM site.

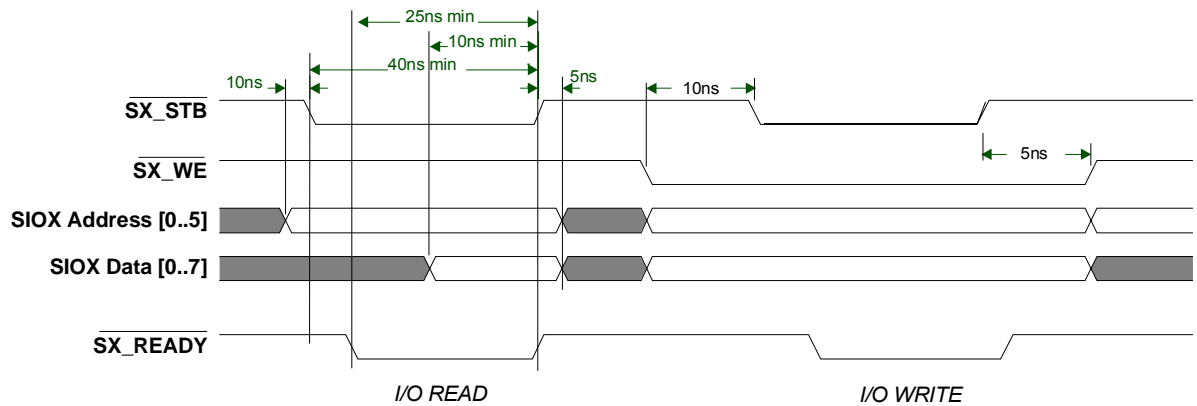


Fig.2-16a. Timing diagram for parallel data transfer via SIOX rev.C DCM site for *TORNADO-E549/E5402/E5410*.

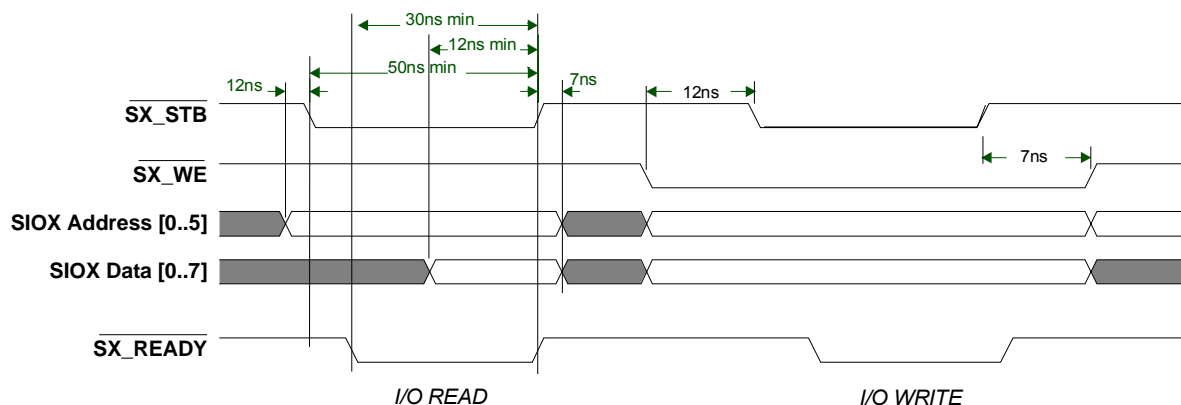


Fig.2-16b. Timing diagram for parallel data transfer via SIOX rev.C DCM site for *TORNADO-E548/E5409/E5416*.

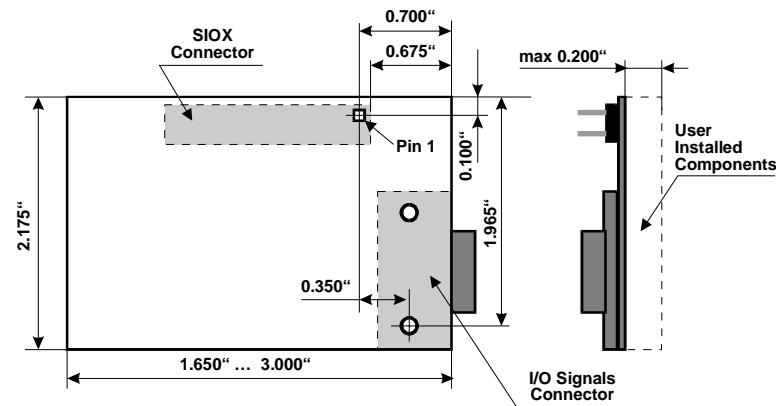
CAUTION

The DSP on-chip wait state control and PLL control registers of TMS320C54x DSP shall be programmed in accordance with table 2-2 in order to meet timing requirements for *TORNADO-E54x* on-board SIOX rev.C interface site.

Parallel data transfer cycle for SIOX rev.C DCM site is terminated by **SX_READY** signal, which must be generated by installed SIOX rev.C DCM.

Physical dimensions for SIOX DCM

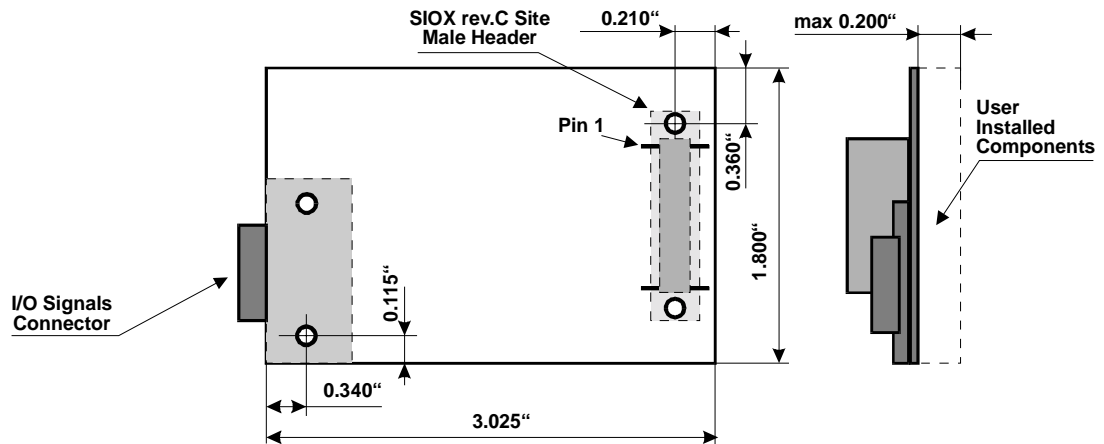
Physical dimensions for SIOX rev.B and SIOX rev.C DCM are presented at figures 2-17 and 2-17b correspondingly. This information is intended for those *TORNADO* customers, who need to design custom SIOX DCM.



SIOX connector: 20-pin or 26-pin straight dual-row mail header
(0.025" Sq., 0.1"x0.1" pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.2-17a. Physical dimensions for SIOX rev.B DCM.



SIOX rev.C Site Male Header: SAMTEC TFM-120-22-S-D-LC

Recommended connector for Analog I/O: DDK DHA-RC26-R122N

Fig.2-17b. Physical dimensions for SIOX rev.C DCM.

2.5 Dual-channel USART

TORNADO-E54x features the on-board dual-channel USART (universal synchronous/asynchronous receiver/transmitter) for communication with host computers, terminals, network adapters, or external peripherals using industry standard serial communication protocols.

USART is based around the Infineon SAB 82532 chip (www.infineon.com) and supports industry standard synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) at up to 10 Mbit/s data transfer rate and the industry-standard asynchronous protocol (ASYNC) at up to 2.5 MBaud. Protocol selection is performed independent for each channel.

Each channel of USART connects to external communication equipment via either RS232C or RS422/EIA-530 electrical interface. Selection of particular interface is performed by the on-board jumpers. RS232C interface provides communication at up to 115kBaud and the RS422/EIA-530 interface provides up to 10 Mbit/s of data transfer rate. Transmitter and received clock outputs are also available via on-board connectors for external equipment, which might need to synchronize its data I/O rate to the USART clock.

USART also provides 8-bit of general purpose parallel digital I/O (*DIO-0..7*), which is wired to the on-board JP14 connector. For details about parallel digital I/O refer to the corresponding section later in this chapter.

CAUTION

This manual does not contain detail information for architecture and programming of Infineon SAB 82532 USART.

For details about Infineon SAB 82532 USART refer to original manufacturer documentation, which is supplied in either electronic or paper form together with *TORNADO-E54x* board.

USART register set

SAB 82532 USART register set comprises of 128 8-bit registers totally for on-chip channels “A” and “B”. SAB 82532 chip is extremely flexible programmable device with build-in FIFO for each of communication channel, PLL and system configuration registers.

Accessing USART from TMS320C54x DSP environment

TORNADO-E54x on-board USART can be accessed via DSP I/O read/write instructions in case DSP XF flag is set to the ‘1’ state (refer to table 2-3). USART features 8-bit data bus, which is wired to the lowest significant byte of 16-bit DSP data bus.

USART-to-DSP interrupt

USART can generate *USART_IRQ* interrupt request to TMS320C54x DSP via any of the DSP external interrupt request inputs (INT0..3 and NMI) by means of the corresponding programming of *MIRQ0_SEL_RG*, *MIRQ1_SEL_RG*, *MIRQ2_SEL_RG*, *MIRQ3_SEL_RG* and *MNMI_SEL_RG* IOX control registers correspondingly (refer to table 2-10).

USART_IRQ interrupt request is internal logical OR from many interrupt sources inside USART including the interrupt requests from parallel digital I/O port.

CAUTION

Interrupt request output of the SAB 82532 USART chip must be configured by the DSP software via USART on-chip IPC register as “push-pull active-low” output (refer to Infineon SAB 82532 USART documentation for more details).

USART-hardware reset

USART hardware reset is performed simultaneously with the hardware reset of *TORNADO-E54x* on-board TMS320C54x DSP and all other on-board peripherals and IOX control registers.

Configuring external interfaces for USART

Each channel of USART connects to external communication equipment via either RS232C or RS422/EIA-530 electrical interface. Selection of particular external interface is performed by the on-board switch set SW4-1..3 for channel ‘A’ of USART and switch set SW4-4..6 for channel ‘B’ of USART (refer to figures 2-2 and A-1) in accordance with table 2-21 and 2-22.

Table 2-21. Configuration of external interfaces for channel “A” of USART.

Interface	interface connector on <i>TORNADO-E54x</i> board	switch SW4-1	switch SW4-2	switch SW4-3
<i>RS422/EIA-530</i> (transmitter clock is generated by the USART on-chip clock generator and does not appear at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP8	OFF	ON	OFF
<i>RS422/EIA-530</i> (external transmitter clock is used from pins CLKX+/CLKX- RS422/EIA-530 connector)	JP8	OFF	ON	ON
<i>RS422/EIA-530</i> (transmitter clock is generated by the USART on-chip clock generator and appears at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP8	OFF	OFF	OFF
<i>RS232C</i>	JP10	ON	ON	OFF

Notes:

1. Highlighted configuration corresponds to the factory settings.

Table 2-22. Configuration of external interfaces for channel “B” of USART.

Interface	interface connector on TORNADO-E54x board	switch SW4-4	switch SW4-5	switch SW4-6
RS422/EIA-530 (transmitter clock is generated by the USART on-chip clock generator and does not appear at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP9	OFF	ON	OFF
RS422/EIA-530 (external transmitter clock is used from pins CLKX+/CLKX- RS422/EIA-530 connector)	JP9	OFF	ON	ON
RS422/EIA-530 (transmitter clock is generated by the USART on-chip clock generator and appears at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP9	OFF	OFF	OFF
RS232C	JP11	ON	ON	OFF

Notes: 1. Highlighted configuration corresponds to the factory settings.

RS232C interface connectors

RS232C interface assumes the single-ended bipolar I/O signals, provides communication at up to 115 kBaud and is designed for ASYNC asynchronous protocol of USART. RS232C interface is an industry standard interface for communication with personal computers, computer peripherals, industrial control devices, etc.

Pinout for TORNADO-E54x on-board RS232C external interface connectors is presented at figure 2-18.

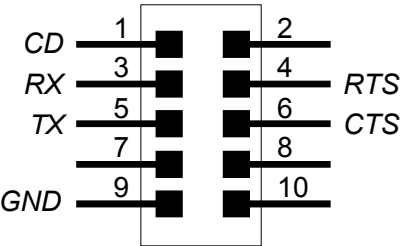


Fig. 2-18. RS232C interface connectors pinout for TORNADO-E54x.

CAUTION

TORNADO-E54x on-board RS232C connectors are the industry 10-pin 0.1"x0.1" male headers, which are widely used for connection RS232C ports to IBM PC motherboards.

You have to use standard 10-pin female to male DB-9 or DB-25 converter flat cables for PC in order to convert the *TORNADO-E54x* on-board RS232C connectors to the industry standard DB-9 or DB-25 male connectors for RS232C interface.

RS422/EIA-530 interface connectors

RS422/EIA-530 interface assumes differential unipolar I/O signals with 110 Ohm line terminators, provides communication at up to 10 Mbit/s, and is designed for all synchronous protocols. RS422/EIA-530 interface can be also used with ASYNC asynchronous protocol of USART delivering up to the 2.5 MBaud of data transfer rate, however this solution is not standard. The RS422/EIA-530 interface is an industry standard electrical interface for communication with network equipment, high-speed computer peripherals, etc.

Pinout for *TORNADO-E54x* on-board RS422/EIA-530 external interface connectors is presented at figure 2-19.

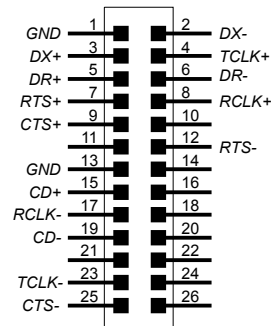


Fig. 2-19. RS422/EIA-530 interface connectors pinout for *TORNADO-E54x*.

CAUTION

TORNADO-E54x on-board RS422/EIA-530 connectors are the industry 26-pin 0.1"x0.1" male headers.

You have to use 26-pin female plug with flat cable and DB-25 end connector in order to convert the *TORNADO-E54x* on-board RS422/EIA-530 connectors to the industry standard DB-25 male connectors for RS422/EIA-530 interface.

USART transmitter/receiver output clocks

TORNADO-E54x provides optional on-board USART transmitter/receiver clocks output connectors separately for each channel (JP12 and JP13 at figures 2-2 and A-1) in order external AD/DA or I/O equipment can synchronize its clock with USART transmitter and receiver clocks. This feature is useful, for example, for satellite modems, which provide external synchronous communication from one side and AD/DA from the other side.

TORNADO-E54x on-board connectors for USART clock outputs are the industry standard 0.05" 3-pin male headers from Molex (www.molex.com). The mating plugs are included as standard with *TORNADO-E54x* shipment pack. Pinout for on-board USART transmitter/receiver clocks output connectors is presented at figure 2-20. The output USART transmitter/receiver clock signals are 5v CMOS/TTL compatible.

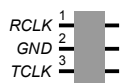


Fig. 2-20. USART transmitter/receiver clock output connectors.

2.6 Parallel Digital I/O

TORNADO-E54x also provides 8-bit of general purpose parallel digital I/O signals (*DIO-0..7*), which are wired to the on-board JP14 connector (refer to figures 2-2 and fig.A-1). Parallel digital I/O is useful for interfacing to external sensors, switches, LED, and other external peripherals and devices, which require dedicated bit I/O control.

Pinout for *TORNADO-E54x* on-board JP14 parallel digital I/O connector is presented at fig.2-21.

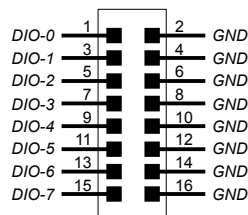


Fig.2-21. Parallel digital I/O connector pinout (*DIO-0..7* signals) for *TORNADO-E54x*.

DIO-0..7 parallel digital I/O lines are programmable I/O pins of on-board SAB82532 USART (refer to section 2.5 for more information about USART).

CAUTION

This manual does not contain detail information for architecture and programming of Infineon SAB 82532 USART.

For details about Infineon SAB 82532 USART refer to original manufacturer documentation, which is supplied in either electronic or paper form together with *TORNADO-E54x* board.

Each of the *DIO-0..7* parallel digital I/O lines allows individual programming of direction and masking of USART interrupt, which might be generated on the user programmable input signal edge.

2.7 USB Device Interface

TORNADO-E54x features the on-board 12 Mbit/s USB device interface for communication with host computers.

TORNADO-E54x on-board USB device interface is based around the Agere Systems (www.agere.com) USS-820/USS-825 USB device interface chip meets USB rev.1.1 specifications and supports the industry USB protocol at up to 12 Mbit/s data transfer rate. On-board USB connector (JP15) is the USB type 'B' device connector.

CAUTION

This manual does not contain detail information for architecture and programming of Agere Systems USS-820/USS-825 USB device controller.

For details about Agere Systems USS-820/USS-825 USB device controller refer to original manufacturer documentation, which is supplied in either electronic or paper form together with *TORNADO-E54x* board.

CAUTION

The on-board USS-820/USS-825 USB device controller is sourced from 12 MHz clock, which allows full-speed 12 Mbit/s communication over the USB bus.

USB interface connector

TORNADO-E54x on-board USB device connector is the industry standard USB type 'B' receptacle with pinout presented at figure 2-22. The mating plug is the USB device plug available on all host-to-device USB cables.

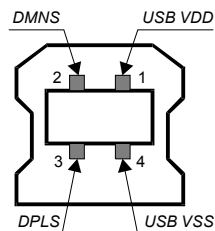


Fig. 2-22. Pinout of USB device connector for TORNADO-E54x.

USB register set

USS-820/USS-825 USB device controller register set comprises of 32 8-bit registers. USS-820/USS-825 USB controller is extremely flexible programmable device with build-in programmable FIFO for transmitter and receiver, dual-packet support, support for 16 USB endpoints, integrated USB transceivers, and many more features.

Accessing USB device controller from TMS320C54x DSP environment

TORNADO-E54x on-board USB device controller can be accessed via DSP I/O read/write instructions in case DSP XF flag is set to the '1' state (refer to table 2-3). USB device controller features 8-bit data bus, which is wired to the lowest significant byte of 16-bit DSP data bus.

CAUTION

The DPPU output pin of on-board USS-820/USS-825 USB device controller is connected to the on-board hardware, which allows simulation of the USB device disconnect.

In order to activate presence of the USS-820/USS-825 USB device controller on host USB bus, the DPPU output must be set to logical '1' value via the DPEN bit of MCSR register of USS-820/USS-825 USB device controller.

USB-to-DSP interrupt

USB device controller can generate *USB_IRQ* interrupt request to TMS320C54x DSP via any of the DSP external interrupt request inputs (INT0..3 and NMI) by means of the corresponding programming of *MIRQ0_SEL_RG*, *MIRQ1_SEL_RG*, *MIRQ2_SEL_RG*, *MIRQ3_SEL_RG* and *MNMI_SEL_RG* IOX control registers correspondingly (refer to table 2-10).

CAUTION

Interrupt request output of the SAB 82532 USART chip must be configured by the DSP software via USB controller on-chip SCR register as “active-low” output (refer to Agere Systems USS-820/USS-825 documentation for more details).

2.8 Emulation Tools for *TORNADO-E54x*

TORNADO-E54x uses scan-path emulation technique for the on-board TMS320C54x DSP in order to debug resident TMS320C54x DSP environment and software.

Compatible scan-path emulation tools include the TI XDS510 or MicroLAB' *MIRAGE-510DX* universal JTAG emulators, which connect directly to the on-board JP3 JTAG-IN connector (figures 2-2 and A-1).

2.9 Software Development Tools

TMS320C54x DSP is now an industry standard DSP and is supported by a variety of software development tools from multiple 3rd party vendors.

Compilers and Debuggers

Software development for *TORNADO-E54x* is supported by TI C5000 Code Composer Studio Compiler Tools (www.ti.com), which include C5000 DSP Optimizing C Compiler and Assembly Language Tools.

Compatible JTAG emulators include TI XDS510 and MicroLAB' *MIRAGE-510D* emulators running under TI C5000 Code Composer Studio Debug tools.

Hypersignal RIDE Visual DSP Algorithm Development and Simulation Tool

TORNADO-E54x DSP controllers are supported by DSP algorithm development tools from Hyperception Inc (www.hyperception.com), which include Hypersignal Block Diagram, RIDE and Code Generator. Hypersignal RIDE is the visual real-time integrated DSP algorithm development and simulation environment for Windows, and allows design entry using high-level function blocks (FIR, FFT, math, etc).

Real-time Multitasking Operating Systems (RTOS)

TORNADO-E54x is supported by multiple RTOS that provide multitasking capabilities:

- *DSP/BIOS* from Texas Instruments Inc (www.ti.com), which is the part of TI C5000 Code Composer Studio Compiler/Debug tools.
- *VIRTUOSO* from Eonic Systems Inc (www.eonic.com) is an industry standard high-performance RTOS and provides full feature multitasking support.
- *NUCLEUS PLUS* from Accelerated Technology Inc (www.atinucleus.com) is an industry standard single-processor high-performance RTOS and provides full feature multitasking support. It features

low cost and comes standard with source codes. Available options include *NUCLEUS FILE*, *NUCLEUS NET*, and *NUCLEUS DBUG+* , which also come in source codes.

Application Software Tools for TORNADO-E54x

Application specific tools for *TORNADO-E54x* DSP controller include a variety of function libraries for DSP, math, vector, image, etc computation, as well as function libraries for vocoder/fax/modem applications and audio multimedia.

Chapter 3. Installation and Configuration

This chapter includes instructions for installation of *TORNADO-E54x* DSP controller.

3.1 Applying the power

The power to *TORNADO-E54x* controller should apply via on-board JP1 connector (refer to fig.A-1). For proper operation the board requires +5v power only, whereas optional -5v and ± 12 v power inputs are routed to on-board SIOX rev.B/C and PIOX-16 DCM sites, and to on-board MXSIOX connector.

3.2 Installation of FLASH/EPROM chip

Installation of FLASH/EPROM chip into *TORNADO-E54x* on-board S1 socket (refer to figure 2-2 and fig.A-1) must be performed while *TORNADO-E54x* board power is off.

CAUTION

TORNADO-E54x on-board S1 socket is designed to carry the FLASH 5v-only 128K..512Kx8 chips or EPROM 128K..1Mx8 chips in the PLCC-32 IC package.

Installation of FLASH/EPROM chip other than that specified in table 2-4 may result in damage of FLASH/EPROM chip and/or of *TORNADO-E54x* hardware.

CAUTION

On-board SW3 switch must be set in accordance with table 2-4 in order to meet installed FLASH/EPROM chip type.

Installation of FLASH/EPROM chip

In order to install FLASH/EPROM chip into *TORNADO-E54x* on-board S1 socket refer to figure 3-1 and follow recommendations below:

- switch off the power
- take FLASH/EPROM chip by your fingers to have its front (labeling) surface turned at you
- adjust FLASH /EPROM chip to be parallel to surface of the *TORNADO-E54x* on-board S1 PLCC-32 socket
- orient FLASH/EPROM chip to have the key corner of its PLCC-32 package would match the corresponding corner of *TORNADO-E54x* on-board S1 socket

- safely insert FLASH/EPROM chip into *TORNADO-E54x* on-board S1 socket
- safely plug and fix FLASH/EPROM chip into the *TORNADO-E54x* on-board S1 socket
- configure *TORNADO-E54x* on-board SW3 switch set in accordance with table 2-4 in order to match installed FLASH/EPROM chip type
- switch on the power of *TORNADO-E54x* DSP controller.

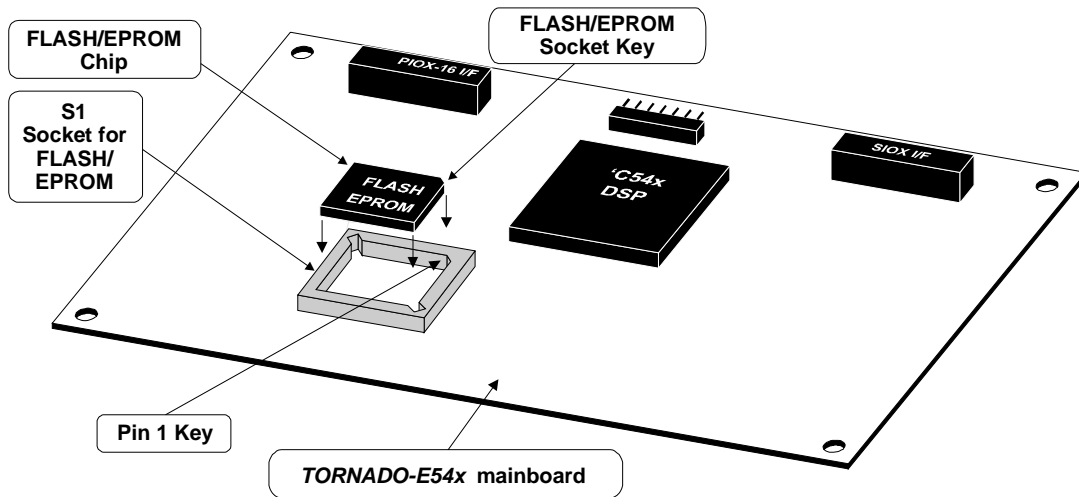


Fig.3-1. Installation of FLASH/EPROM chip into *TORNADO-E54x* on-board S1 socket.

3.3 Configuring *TORNADO-E54x* board

Generally, the following configuration procedure must be performed prior applying power to *TORNADO-E54x* DSP controller for the first time (refer to fig.A-1 for on-board jumpers and connectors list):

- configure MS320C54x DSP bootmode configuration (switches SW2-1 and SW2-2) in accordance with table 2-1
- enable or disable TMS320C54x DSP on-chip HPI port using on-board SW2-3 in accordance with table 2-15 in order to meet your application requirements
- if required, install FLASH/EPROM chip and set configuration SW3 switch in accordance with table 2-4 in order to match type of installed FLASH/EPROM chip and to enable/disable FLASH write control
- if required, select appropriate RS232 or RS422/EIA-530 interface for USART channels #A and #B and configure set configuration switches SW4-1..3 and SW4-4..6 in accordance with tables 2-21 and 2-22
- connect external power supply wires to on-board JP1 power connector
- if required, plug-in RS232C or RS422/EIA-530 cables sets into on-board JP8..JP11 connectors (figures 2-18 and 2-19) and digital I/O cable set into on-board JP14 connector (figure 2-21)
- if required, connect USB type 'B' cable plug of USB cable into on-board JP15 USB device connector (figure 2-22)

- if required, install either SIOX rev.B or SIOX rev.C DCM into on-board either JP5 SIOX rev.B DCM site or JP6 SIOX rev.C DCM site (section 2.4, figures 2-12a and 2-12b), and configure installed SIOX DCM in accordance with provided documentation
- if required, connect external *T/SU-X1* SIOX rev.B mini-extender kit to on-board MXSIOX connector (section 2.4, Appendix B, figure 2-12c), install SIOX rev.B DCM onto *T/SU-X1* mini-extender board, and configure installed SIOX DCM in accordance with provided documentation. Configure *TORNADO-E54x* on-board SW5-1 and SW5-2 common serial clock enable switches in accordance with recommendations in section 2.4 and Appendix B.
- if required, install PIOX-16 DCM into on-board JP4 PIOX-16 DCM site connector (refer to section 2.3 for more details), and configure installed PIOX-16 DCM in accordance with provided documentation
- if required, connect HPI port cable to on-board JP7 HPI port connector (section 2.2, figure 2-4)
- if required, connect external JTAG emulator to on-board JP3 JTAG-IN connector (section 2-8)
- switch on external power supply.

Appendix A. On-board Connectors, Sockets and Switches.

This Appendix includes a summarized description for the *TORNADO-E54x* on-board configuration switches, connectors, sockets and LED (light emitting diodes).

TORNADO-E54x board layout of configuration switches, connectors, sockets and LED is presented at figure.A-1.

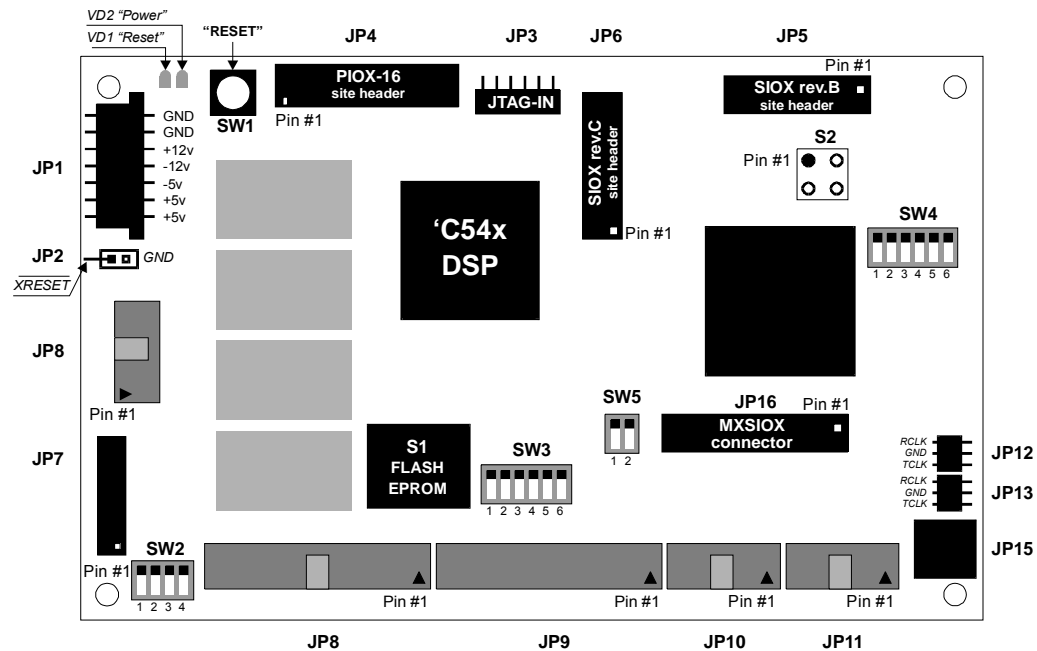


Fig.A-1. *TORNADO-E54x* board layout of configuration switches, connectors, sockets, and LED.

On-board configuration switches

List of on-board configuration switches for *TORNADO-E54x* DSP controllers is presented in table A-1.

Table A-1. On-board configuration switches for *TORNADO-E54x*.

switch	switch function description	reference information
SW1	External reset pushbutton.	Section 2.2
SW2-1 SW2-2	TMS320C54x DSP Bootmode configuration.	Section 2.2 table 2-1

SW2-3	TMS320C54x DSP on-chip HPI port disable control (<i>TORNADO-E5402/E5409/E5416</i> only).	Section 2.2 table 2-15
SW3	FLASH/EPROM chip type selector and FLASH write protection.	Sections 2.2 and 3.2 table 2-4
SW4-1 SW4-2 SW4-3	External RS232C/RS422 interface selector for USART channel "A".	Section 2.5 table 2-21
SW4-4 SW4-5 SW4-6	External RS232C/RS422 interface selector for USART channel "B".	Section 2.5 table 2-22
SW5-1 SW5-2	Common serial clock enable for SIO-0 and SIO-1 serial ports of on-board MXSIOX connector (<i>TORNADO-E548/E549/E5409/E5410/E5416</i> only)	Section 2.4, Appendix B tables 2-20a and 2-20b

On-board Connectors

List of on-board connectors for *TORNADO-E54x* DSP controllers is presented in table A-2.

Table A-2. On-board connectors for *TORNADO-E54x*.

connector ID	connector function description	reference information
JP1	External power input connector.	Sections 2.1 and 3-1.
JP2	External reset input connector.	Section 2.2 figure 2-5
JP3	JTAG-IN connector	Section 2.8
JP4	PIOX-16 DCM site connector (header).	Section 2.3 figure 2-8, table 2-16
JP5	SIOX rev.B DCM site connector (header)	Section 2.4 figure 2-13, table 2-17
JP6	SIOX rev.C DCM site connector (header)	Section 2.4 figure 2-14, table 2-18
JP7	TMS320C54x DSP HPI port connector.	Section 2.2 figure 2-4; table 2-14
JP8 JP9	RS422/EIA-530 interface connectors for USART channels "A" and "B".	Section 2.5 figure 2-19
JP10 JP11	RS232C interface connectors for USART channels "A" and "B".	Section 2.5 figure 2-18

<i>JP12</i> <i>JP13</i>	Transmitter/receiver clock output connectors for USART channels "A" and "B".	Section 2.5; figure 2-20
<i>JP14</i>	Parallel digital I/O connector.	Section 2.6 figure 2-21
<i>JP15</i>	USB type 'B' device connector.	Section 2.7; figure 2-22
<i>JP16</i>	MXSIOX connector for connection to external <i>T/SU-X1</i> SIOX rev.B mini-extender kit.	Section 2.4 figure 2-15, table 2-19

On-board Sockets

List of on-board sockets for *TORNADO-E54x* DSP controllers is presented in table A-3.

Table A-3. On-board sockets for *TORNADO-E54x*.

socket ID	socket function	reference information
<i>S1</i>	PLCC-32 FLASH/EPROM socket.	Sections 2.2 and 3-2.
<i>S2</i>	DIP-4 (0.3"x0.3") socket for 5V crystal oscillator (example: EPSON SG-531) for USART source clock.	Section 2.5

On-board LED

List of on-board LED (light emitting diodes) for *TORNADO-E54x* DSP controllers is presented in table A-4.

Table A-4. On-board LED for *TORNADO-E54x*.

switch ID	switch function
<i>VD1</i>	DSP reset LED (red).
<i>VD2</i>	Power on LED (green).

Appendix B. *T/SU-X1* SIOX rev.B Mini-Extender Kit

This appendix contains description for *T/SU-X1* external SIOX rev.B mini-extender kit, which can be used to connect external SIOX rev.B AD/DA/DIO and application specific DCM to *TORNADO* DSP controllers and coprocessors, which provide on-board compatible connector for connection to external *T/SU-X1* SIOX rev.B mini-extendors.

B.1 General Description

T/SU-X1 SIOX rev.B mini-extender kit is normally provided as dual SIOX rev.B mini-extender kit (fig.B-1), which comprises of the following components:

- two identical *T/SU-X1* SIOX rev.B mini-extender carrier boards
- PC chassis mounting bracket
- two *T/SU-X1/XC* 10" (0.25m) long connection cables.

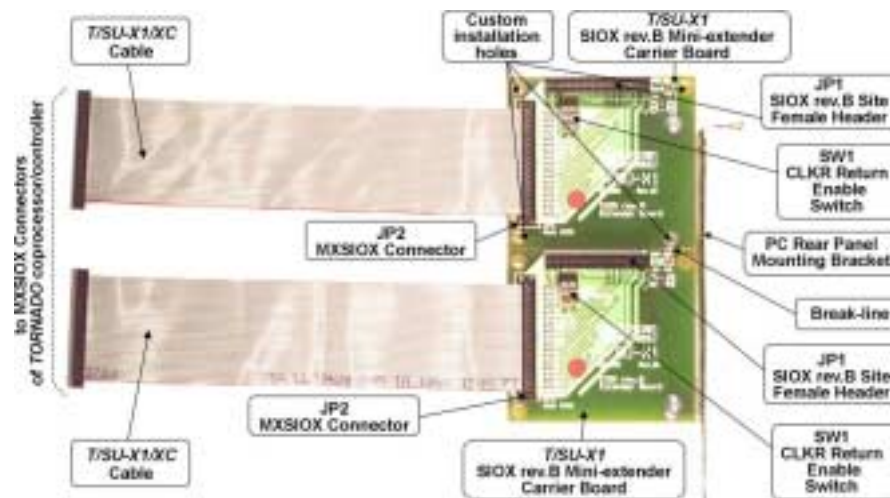


Fig.B-1. Dual *T/SU-X1* SIOX rev.B mini-extender with mounting bracket and connection cables.

Each *T/SU-X1* SIOX rev.B mini-extender carrier board provides on-board site for one full-size SIOX rev.B DCM (fig.B-2), which can be either fixed to the *T/SU-X1* carrier board via optional spacers, or screwed to the mounting bracket.

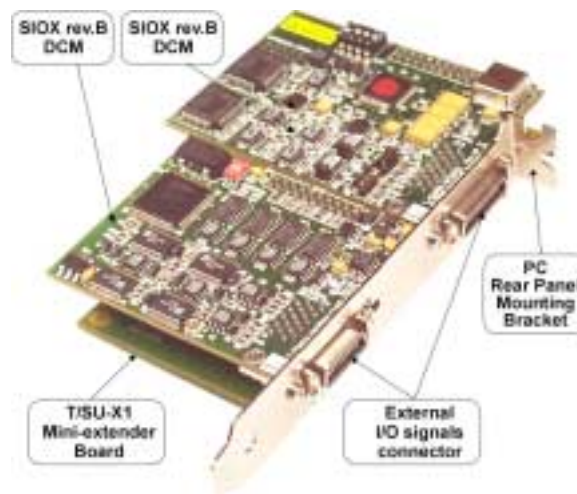


Fig.B-2. Dual *T/SU-X1* SIOX rev.B mini-extender with two installed SIOX rev.B DCM.

connection of *T/SU-X1* SIOX rev.B mini-extender to host *TORNADO* DSP controllers and coprocessors

T/SU-X1 SIOX rev.B mini-extender connects to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* 10" (0.25m) long connection cable (fig.B-3), which connects to the MXSIOX connectors on the *T/SU-X1* SIOX rev.B mini-extender on one side and to with the corresponding MXSIOX matching connector host *TORNADO* DSP controller/coprocessor.

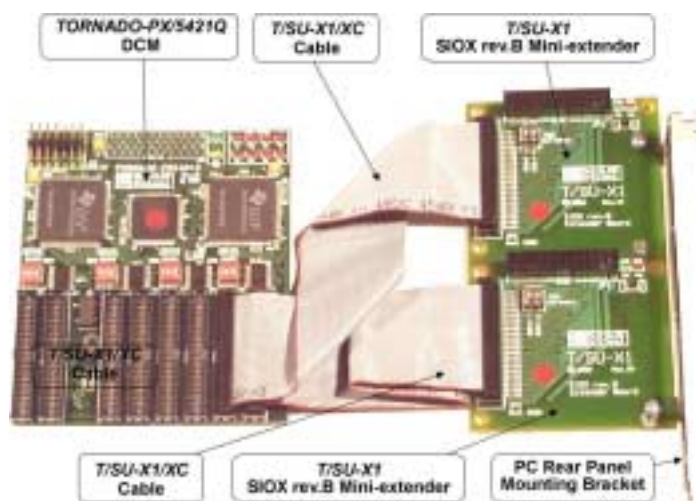


Fig.B-3. Connection of dual *T/SU-X1* SIOX rev.B mini-extender to host *TORNADO-PX5421Q* P10X-16 DSP coprocessor DCM.

installation

Dual *T/SU-X1* SIOX rev.B mini-extender can either mount at the rear panel of PC using installed mounting bracket, or can be hand-broken into two identical *T/SU-X1* SIOX rev.B mini-extendors using on-board perforated broke line (fig.B-1).

Single *T/SU-X1* SIOX rev.B mini-extender, which appears as the broken half of dual *T/SU-X1* SIOX rev.B mini-extender, can be installed into the embedded custom chassis environment.

physical dimensions

Figure B-4 provides physical dimensions for single *T/SU-X1* SIOX rev.B mini-extender and positions for all installation holes and connectors.

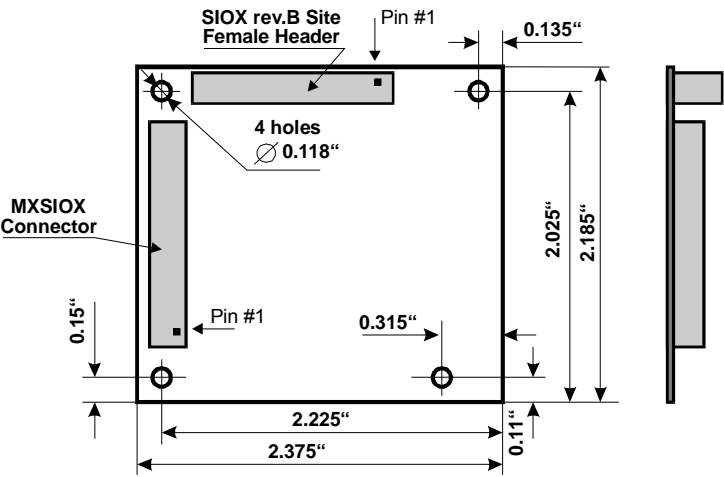


Fig.B-4. Physical dimensions of *T/SU-X1* SIOX rev.B mini-extender.

B.2 Technical Specifications

The following are technical specifications for *T/SU-X1* SIOX rev.B mini-extendors.

<u>Parameter description</u>	<u>parameter value</u>
number of SIO ports	2
number of TM/XIO I/O lines	2
number of external interrupt request inputs (<i>XIRQ</i>)	2
number of SIOX reset signals (<i>RESET</i>)	1

maximum serial clock frequency for transmitter/receiver of SIO ports	50 MHz
power supply outputs	$\pm 5\text{v}$, $\pm 12\text{v}$
optional features	LED indicators for power and SIOX reset control CLKR0/CLKR1 serial receiver clock enable switches
Dimensions	2.16"x2.36" (55x60 mm)
length of <i>T/SU-X1/XC</i> extender cable	10" (0.25m)

B.3 Technical Description

Figure B-5 presents block diagram of *T/SU-X1* SIOX rev.B mini-extender kit.

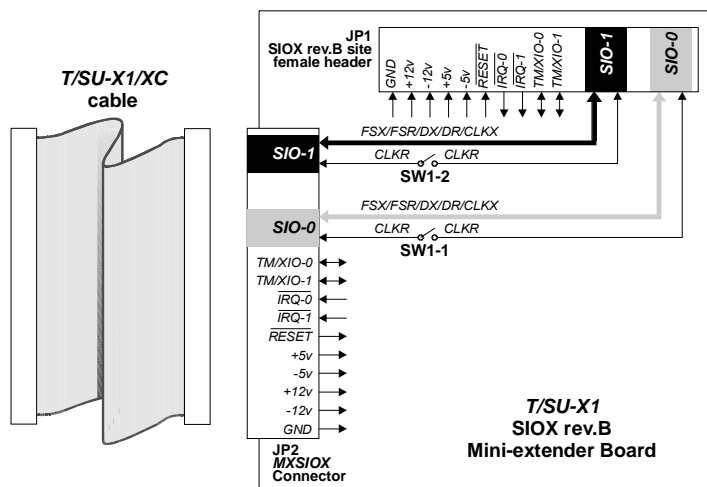


Fig.B-5. Block diagram of *T/SU-X1* SIOX rev.B mini-extender.

T/SU-X1 SIOX rev.B mini-extender carrier board

T/SU-X1 SIOX rev.B mini-extender carrier board comprises of the following components:

- SIOX rev.B site header (JP1)
- MXSIOX connector (JP2) for connection to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* connection cable
- on-board SW1 switch, which is used to enable serial receiver clock (CLKR) for each serial port.

T/SU-X1 on-board JP1 SIOX rev.B site header and JP2 MXSIOX connector for connection to host *TORNADO* DSP controller/coprocessor via *T/SU-X1/XC* connection cable comprise of the signals for two serial ports (SIO-0 and SIO-1), two timer/IO lines (*TM/XIO-0/1*), two external interrupt request inputs (*IRQ-0/1*), SIOX interface reset control output (*RESET*), and host $\pm 5V/\pm 12V$ power supply lines.

Pinout information for JP1 SIOX rev.B site header and JP2 MXSIOX connector is provided in the corresponding subsections below and figures B-6 and B-5 correspondingly. Common signal description is provided in table B-1.

T/SU-X1 on-board SW1 switch shall be used in conjunction with host *TORNADO* DSP coprocessor/controller on-board common serial clock enable switches in order to enable return of receiver' serial clock for each of two serial ports of SIOX interface to host *TORNADO* DSP coprocessor/controller depending upon the type of installed SIOX rev.B DCM. Refer to the corresponding subsection below for more details.

MXSIOX connector pinout and signal description

T/SU-X1 on-board MXSIOX connector is used for connection to host *TORNADO* DSP coprocessor/controller via *T/SU-X1/XC* connection cable.

MXSIOX connector is Samtec 34-pin dual-row 2mm guarded male header. Although MXSIOX plugs come standard with *T/SU-X1/XC* SIOX rev.B mini-extender connection cables, optional MXSIOX plugs for 2mm flat cables are available from MicroLAB Systems upon request.

MXSIOX connector pinout is presented at fig.B-6, whereas signal description is provided in table B-1.

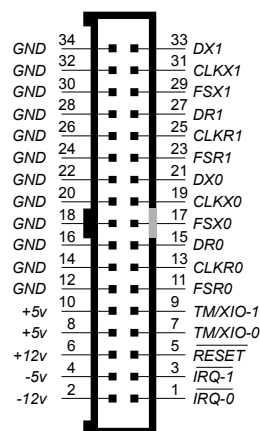


Fig.B-6. Pinout for *T/SU-X1* SIOX rev.B mini-extender on-board MXSIOX connector (top view).

Table B-1. Signal description for T/SU-X1 SIOX rev.B mini-extender on-board MXSIOX connector.

SIOX rev.B interface signal	signal type	Description
SIO-0 port control		
<i>DX0</i> <i>FSX0</i> <i>CLKX0</i>	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port, which connect to the transmitter control signals for SIO-0 serial port.
<i>DR0</i> <i>FSR0</i> <i>CLKR0</i>	I I I	Data, frame synchronization and serial clock signals for receiver of SIO-0 port, which connect to the receiver control signals for SIO-0 serial port.
SIO-1 port control		
<i>DX1</i> <i>FSX1</i> <i>CLKX1</i>	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port, which connect to the transmitter control signals for SIO-1 serial port.
<i>DR1</i> <i>FSR1</i> <i>CLKR1</i>	I I/O I	Data, frame synchronization and serial clock signals for receiver of SIO-1 port, which connect to the receiver control signals for SIO-2 serial port.
Timers/IO, DSP Reset and Interrupt Requests		
<i>TM/XIO-0</i> <i>TM/XIO-1</i>	I/O	Timer/IO pins.
<i>RESET</i>	O	Active low SIOX reset output pin.
<i>IRQ-0</i> <i>IRQ-1</i>	I	Active low external interrupt request inputs. Active DSP core' external interrupt requests are generated on the falling edge (1→0) of <i>IRQ-0</i> and <i>IRQ-1</i> .. inputs.
Power Supplies		
<i>GND</i>		Ground.
<i>+5v</i>		+5v power supply.
<i>+12v</i>		+12v power supply.
<i>-5v</i>		-5v power supply.
<i>-12v</i>		-12v power supply.

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
3. All logical signal levels and load currents correspond to that for 3v/5v CMOS signals.

SIOX rev.B site header

T/SU-X1 on-board SIOX rev.B site header with two serial ports is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM must be the industry standard either 26-pin 0.1"x0.1" male header (in case both SIO-0 and SIO-1 serial ports are used on SIOX plugged-in DCM) or 20-pin 0.1"x0.1" male header (in case only SIO-0 serial port is used on SIOX plugged-in DCM).

SIOX rev.B site connector pinout with two serial ports is shown at fig.B-7 and signal specifications are listed in table B-1.

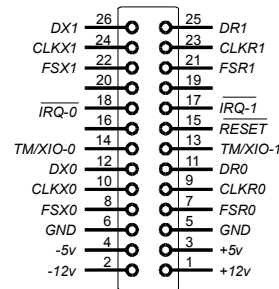


Fig.B-7. SIOX rev.B connector pinout (top view).

Signal levels for SIOX interface signals of *T/SU-X1* SIOX rev.B mini-extender is defined by host *TORNADO* DSP coprocessor/controller and correspond to that for the CMOS/TTL signals with $I_{OL}=2\text{ma}$ and $I_{OH}=-0.3\text{ma}$ load currents.

CAUTION

Some *TORNADO* boards provide SIOX interface signal levels for CMOS/TTL only, whereas other *TORNADO* boards provide SIOX interface signal levels universal for both 3V TTL and standard 5V TTL. Refer to documentation for your particular *TORNADO* board for information about SIOX interface signal levels.

T/SU-X1/XC mini-extender connection cable

T/SU-X1 SIOX rev.B mini-extender carrier board connects to host *TORNADO* DSP coprocessor/controller via *T/SU-X1/XC* 10" (0.25m) long 34-pin 2mm flat cable.

T/SU-X1/XC mini-extender connection cable plugs to MXSIOX connector of *T/SU-X1* SIOX rev.B mini-extender carrier board on one side and to MXSIOX connector of host *TORNADO* DSP coprocessor/controller on the other side (fig.B-3).

on-board receiver serial clock return enable switches

T/SU-X1 SIOX rev.B mini-extender carrier board provides on-board SW1-1 and SW1-2 switches in order to enable return of SIO-0 and SIO-1 receiver serial clock (CLKR0 and CLKR1 correspondingly) SIOX interface to host *TORNADO* DSP coprocessor/controller depending upon the type of installed SIOX rev.B DCM.

T/SU-X1 SIOX rev.B mini-extender on-board SW1-1 and SW1-2 switches shall be used in conjunction with host *TORNADO* DSP coprocessor/controller on-board common serial clock enable switches using general recommendations below.

Host *TORNADO* DSP coprocessor/controller provides on-board common CLKX/CLKR serial clock enable switches for each of serial ports of MXSIOX connectors.

CAUTION

In case on-board common serial clock enable switch of host *TORNADO* DSP coprocessor/controller is set to 'ON', then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are connected together on-board.

In case on-board common serial clock enable switch of host *TORNADO* DSP coprocessor/controller is set to 'OFF', then the corresponding transmitter serial clock (CLKX) and receiver serial clock (CLKR) are disconnected on-board.

Background for usage on-board common CLKX/CLKR serial clock enable switches of host *TORNADO* DSP coprocessor/controller and *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKR) return enable switches is the 'long-line' compensation issue for serial clock signals distribution over connection flat cable between host *TORNADO* DSP coprocessor/controller on-board MXSIOX connector and *T/SU-X1* SIOX rev.B mini-extender due to the 'long-line wave nature' of connection flat cable.

Although the 'long-line' compensation resistors are being used for control signals for serial ports at both host *TORNADO* DSP coprocessor/controller and *T/SU-X1* SIOX rev.B mini-extender boards in order to exclude signal reflection, a 'long-line' non-compensation for serial clock signals can still occur in case installed SIOX rev.B DCM is using common shorted serial clock for transmitter and receiver of SIO port (many SIOX rev.B DCM actually use this in order to simplify design). Note, that this problem does not occur with SIO port frame synchronization and serial data signals, since these signals always use dedicated lines of SIOX interface and can't be connected together.

CAUTION

In case installed SIOX rev.B DCM has been designed without on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and each serial clock is using its dedicated pins, then the corresponding host *TORNADO* DSP coprocessor/controller on-board common CLKX/CLKR serial clock enable switch must be set to 'OFF' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'ON'.

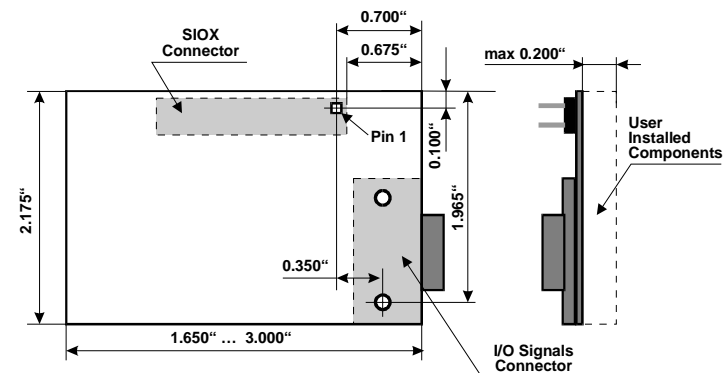
In case installed SIOX rev.B DCM has been designed with on-board common shorted CLKX/CLKR transmitter/receiver serial clock of SIO port and both serial clocks are using shared pins, then the corresponding host *TORNADO* DSP coprocessor/controller on-board common CLKX/CLKR serial clock enable switch must be set to 'ON' and the corresponding *T/SU-X1* SIOX rev.B mini-extender on-board receiver serial clock (CLKCR) return enable switch must be set to 'OFF'.

LED indicators

T/SU-X1 SIOX rev.B carrier board also provides two on-board LED indicators for host power (V1) and for SIOX reset state (V2).

B.4 Physical Dimensions for SIOX DCM

Physical dimensions for SIOX DCM are presented at fig.B-8. This information is intended for those customers, who need to design customized SIOX DCMs.



SIOX connector: 20-pin or 26-pin straight dual-row mail header
(0.025" Sq., 0.1"x0.1" pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.B-8. Physical dimensions for SIOX DCM.

Appendix C. Glossary of Terms.

This Glossary contains definition for terms and other synchronism, which are most often used along in this manual.

A

B

bootmode

TMS320C54x DSP start-up procedure, which corresponds to loading of application code to TS320C54x DSP memory from either on-board FLASH/EPROM, or HPI port, or DSP on-chip serial port, or I/O port, etc. *TORNADO-E54x* DSP controllers support *MP/NO-BMODE*, *MC/FLASH8-BMODE* and *MC/HPI-BMODE* DSP bootmodes only, which can be set via on-board SW2-1 and SW2-2 switches. Refer to section 2.2 and original TI documentation for more details.

BSP

TMS320LC548/TMS320VC549 DSP on-chip buffered serial ports. Refer to TI documentation for more details.

C

CLKX, CLKR

Serial clock for transmitter and receiver of TMS320C54x DSP on-chip BSP/TDM/McBSP serial ports. Refer to section 2.4 and Appendix B for more details.

D

DCM

Daughter-card module.

DEV_ID_RG

IOX control read-only register, which contains information about *TORNADO-E54x* device ID code and hardware revision ID code. Refer to section 2.2 for more details.

DSP

On-board TI TMS320C54x Digital Signal Processor. Refer to sections 2.1 and 2.2 for more details.

DSPINT

Host-to-DSP interrupt request via TMS320C54x DSP on-chip HPI port, which appears as the *DSPINT* bit of TMS320C54x DSP HPIC register. Refer to section 2.2 for more details.

DX, DR

Serial data for transmitter and receiver of TMS320C54x DSP on-chip BSP/TDM/McBSP serial ports. Refer to section 2.4 and Appendix B for more details.

E

EPROM

Electrically programmable read-only memory chip. 8-bit EPROM chip in PLCC-32 IC package can be installed into *TORNADO-E54* on-board S1 in order to boot application code or to provide non-volatile data. Refer to section 2.2 for more details.

F

FLASH

Electrically programmable and electrical erasable read/write memory chip. 8-bit FLASH chip in PLCC-32 IC package can be installed into *TORNADO-E54* on-board S1 in order to boot application code or to provide non-volatile data. Refer to section 2.2 for more details.

FSX, FSR

Frame synchronization for transmitter and receiver of TMS320C54x DSP on-chip BSP/TDM/McBSP serial ports. Refer to section 2.4 and Appendix B for more details.

G

H

HINT

DSP-to-host interrupt request via TMS320C54x DSP on-chip HPI port, which appears as the *HINT* bit of TMS320C54x DSP HPIC register. Refer to section 2.2 for more details.

HPI

TMS320C54x DSP on-chip 8-bit host port interface, which is used to access DSP on-chip memory and registers from host controller. Refer to section 2.2 for more details.

HPI disable control

TORNADO-E5402/E5409/E5416 on-board HPI disable switch (SW2-3), which can be used to disable DSP on-chip HPI port and to either use HPI port data lines (HD0..HD7) of on-board JP7 connector as general purpose I/O pins, or to enable TMS320VC5402 DSP on-chip timer #1 (*TORNADO-E5402* only). Refer to section 2.2 and original TI documentation for more details.

I

IOX

External I/O area for *TORNADO-E54* on-board TMS320C54x DSP. IOX area comprises of on-board peripherals (USART and USB), I/O expansion interfaces (PIOX-16 and SIOX rev.C) and IOX control registers. Refer to section 2.2 for more details.

J

JTAG

Joint Test Action Group interface, which is a part of the TMS320C2xx/VC33/C4x/C5x/C54x/C6x/C8x DSP on-chip hardware, and is used to debug *TORNADO-E54x* on-board TMS320C54x DSP software using external JTAG emulators (TI XDS510 and MicroLAB[®] *MIRAGE-510DX*, *UECMX*). Refer to section 2.8 for more details.

JTAG-IN

On-board input connector, which is used for connection to external JTAG emulator. Refer to section 2.8 and Appendix A for more details.

K

L

LED

Light emitting diode indicator. Refer to Appendix A for more details.

M

McBSP

TMS320VC5402/TMS320VC5409/TMS320VC5416 DSP on-chip serial ports. Refer to sections 2.2 and 2.4 for more details.

MC/FLASH8-BMODE

Bootmode from *TORNADO-E54x* on-board 8-bit FLASH/EPROM memory for on-board TMS320C54x DSP, which is set via on-board SW2-1 and SW2-2 switches. DSP will start-up in microcontroller mode. Refer to section 2.2 and original TI documentation for more details.

MC/HPI-BMODE

Bootmode from external host controller via HPI port of *TORNADO-E54x* on-board TMS320C54x DSP, which is set via on-board SW2-1 and SW2-2 switches. DSP will start-up in microcontroller mode. Refer to section 2.2 and original TI documentation for more details.

Microcontroller mode

TMS320C54x DSP start-up mode, which enables DSP on-chip ROM with bootloader code in order DSP can boot from external ROM, HPI port, serial port, I/O ports, etc.. Refer to section 2.2 and original TI documentation for more details.

Microprocessor mode

TMS320C54x DSP start-up mode, which disable DSP on-chip ROM with bootloader code in order DSP can start without boot process. Application code either must be already in external program memory, or can be loaded via JTAG emulator via JTAG-IN port. This DSP start-up mode is typically used for debugging application code. Refer to section 2.2 and original TI documentation for more details.

MIRQ0_SEL_RG, MIRQ1_SEL_RG, MIRQ2_SEL_RG, MIRQ3_SEL_RG, MNMI_SEL_RG

IOX control registers, which are used to configure on-board interrupt source for TMS320C54x DSP external interrupt inputs (INT0..3 and NMI). Refer to section 2.2 for more details.

MP/NO-BMODE

Bootmode for *TORNADO-E54x* on-board TMS320C54x DSP, which is set via on-board SW2-1 and SW2-2 switches and corresponds to no DSP bootmode and DSP start-up in microprocessor mode. DSP will start-up in microcontroller mode. Refer to section 2.2 and original TI documentation for more details.

MXSIOX

On-board connector for external *T/SU-X1* SIOX rev.B mini-extender. Refer to section 2.4 and Appendix B for more details.

N**O****P**

PIOX-16

16-bit Parallel I/O eXpansion interface site for compatible daughter-card modules (DCM) at *TORNADO* PC plug-in DSP systems and DSP controllers. *TORNADO-E54x* provides one on-board PIOX-16 DCM site. Refer to section 2.3 for more details.

Pod

Electronic device, which connects external JTAG emulator with *TORNADO-E54x* on-board JTAG-IN connector for uploading and debugging of TMS320C54x DSP software.

PX_IRQ-0, PX_IRQ-1

Interrupt requests from PIOX-16 DCM site. Refer to sections 2.2 and 2.3 for more details.

PX_RESET

Reset control bit of *PXSX_RESET_RG* IOX control register for PIOX-16 DCM site. Refer to sections 2.2 and 2.3 for more details.

PXSX_RESET_RG

IOX control register, which is used to control reset signals for on-board SIOX rev.B/C DCM sites, PIOX-16 DCM site, and for MXSIOX connector. Refer to section 2.2 for more details.

Q**R*****RS232C external interface***

External electrical interfaces for each channel of on-board USART chip, which provides up to 115 kBaud data transfer rate and is typically used in case the corresponding USART channel is configured for ASYNCH protocol in order to connect to external host computer or peripherals. RS232C external interface is selected via on-board SW4 switch. Refer to section 2.5 and original Infineon documentation for more details.

RS422/EIA-530 external interface

External electrical interfaces for each channel of on-board USART chip, which provides up to 10 Mbit/s data transfer rate and is typically used in case the corresponding USART channel is configured for either of HDLC/X.25, SDLC, MONOSYNC, BISYNC synchronous protocols in order to connect to external network, or high-speed peripherals or host computers. RS232C external interface is selected via on-board SW4 switch. Refer to section 2.5 and original Infineon documentation for more details.

S

SIOX rev.B

Serial I/O eXpansion interface site revision B for compatible daughter-card modules (DCM) at *TORNADO* DSP systems, controllers, and SIOX extenders. Refer to sections 2.2 and 2.4, and Appendix B for more details.

SIOX rev.C

Enhanced serial I/O eXpansion interface site revision C for compatible daughter-card modules (DCM) at *TORNADO* DSP systems, controllers. Refer to section 2.4 for more details.

SYS_STAT_RG

IOX control read-only register, which contains information about DSP start-up configuration. Refer to section 2.2 for more details.

SX-A_RESET, SX-B_RESET

Reset control bits of *PXSX_RESET_RG* IOX control register for on-board SIOX rev.B/C DCM site and MXSIOX connector. Refer to sections 2.2 and 2.3 for more details.

SX_IRQ-0, SX_IRQ-1, SX_IRQ-2

External interrupt request inputs from *TORNADO-E54x* on-board SIOX rev.B DCM site, SIOX rev.C DCM site and MXSIOX connector. Refer to section 2.4 for more details.

T**TDM**

TMS320LC548/TMS320VC549 DSP on-chip time division multiplexed serial ports. Refer to TI documentation for more details.

T/SU-X1

External SIOX rev.B mini-extender, which can carry one SIOX rev.B DCM and connect to *TORNADO-E54x* on-board MXSIOX connector. Refer to section 2.4 and Appendix B for more details.

T/SU-X1/XC

Extender connector cable, which is used to connect external SIOX rev.B mini-extender and *TORNADO-E54x* on-board MXSIOX connector. Refer to section 2.4 and Appendix B for more details.

TM/XIO-0/1

Software configurable timer/IO pins of on-board SIOX rev.B/C DCM sites, PIOX-16 DCM site and MXSIOX connector. Refer to section 2.2 for more details.

U**USART**

Universal synchronous asynchronous receiver transmitter interface chip, which is the Infineon SAB82532 ECC2 chip on *TORNADO-E* DSP controllers. Refer to section 2.5 and original Infineon documentation for more details.

USART_IRQ

Interrupt request from on-board USART chip. Refer to sections 2.2 and 2.5, and original Infineon documentation for more details.

USB device controller

Universal serial bus (USB) device controller chip, which is the Agere Systems either USS-820 or USS-825 chip on *TORNADO-E* DSP controllers. Refer to section 2.7 and original Agere Systems documentation for more details.

USB_IRQ

Interrupt request from on-board USB device controller. Refer to sections 2.2 and 2.7, and original Agere Systems documentation for more details.

V

W

WDT

Watchdog timer. Refer to section 2.2 for more details.

WDT_EN_RG

IOX control register, which is used to enable reset of *TORNADO-E54x* on-board DSP and peripherals on WDT expiration condition. Refer to section 2.2 for more details.

WDT_RESET_RG

IOX control write-only register, which is used to reset WDT. Refer to section 2.2 for more details.

X

XDM_SEL

Bit of *XDMP_RG* IOX control register, which is used to select external data memory type (on-board data SRAM or FLASH/EPROM), which will be used as external data memory for on-board TMS320C54x DSP. Refer to section 2.2 for more details.

XDMP_SEL_RG

IOX control register, which is used to select DSP external data memory type and particular memory page of selected DSP external data memory, which will be mapped into DSP external data memory space.. Refer to section 2.2 for more details.

XF

General purpose output pin of TMS320C54x DSP, which is controlled via DSP on-chip ST1 register. DSP XF output is used in *TORNADO-E54x* DSP controllers in order to select either on-board PIOX-16 DCM site, or other on-board peripherals (USART, USB and IOX control registers) and SIOX rev.C DCM site, which will be mapped into external I/O address space of on-board TMS320C54x DSP. Refer to section 2.2 and original TI documentation for more details.

XIO_CNF_RG, XIO_DIR_RG, XIO_DATA_RG

IOX control registers, which are used to control *TM/XIO-0/1* timer/IO pins of on-board SIOX rev.B/C DCM site, PIOX-16 DCM site and MXSIOX connector. Refer to sections 2.2, 2.3 and 2.4 for more details.

Y

Z