



*Ultimate DSP Development Solutions*

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**DIGITAL SIGNAL PROCESSING**

# ***TORNADO-E31***

Stand-alone DSP Controllers with 32-bit Floating-Point TMS320C31 DSP

## *User's Guide*

covers:  
*TORNADO-E31 rev.1C/1D*

### **MicroLAB Systems Ltd**

59a Beskudnikovsky bulvard, 127486, Moscow, RUSSIA  
phone/fax: +7-(095)-485-6332 Email: [info@mlabsys.com](mailto:info@mlabsys.com) WWW: [www.mlabsys.com](http://www.mlabsys.com)

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## About this Document

This user's guide contains description for *TORNADO-E31* stand-alone digital signal processing (DSP) controller with 32-bit floating-point TMS320C31 DSP from Texas Instruments Inc (TI).

This document does not include detail description neither for TI TMS320C31 DSP nor for the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C3x User's Guide.*** Texas Instruments Inc, SPRU031D, USA, 1994.
2. ***TMS320C3x C Source Debugger User's Guide.*** Texas Instruments Inc, SPRU053A, USA, 1991.
3. ***Data Communication ICs. Enhanced Serial Communication Controller ESCC2 SAB 82532. User's Manual.*** Siemens, 1994.
4. ***TMS320 Floating-Point DSP Optimizing C Compiler User's Guide.*** Texas Instruments Inc, SPRU034B, USA, 1995.
5. ***TMS320 Floating-Point DSP Assembly Language Tools User's Guide.*** Texas Instruments Inc, SPRU035B, USA, 1995.
6. ***Nucleus RTX Reference.*** Accelerated Technology Inc, USA, 1992.
7. ***Nucleus Plus Reference Manual.*** Accelerated Technology Inc, USA, 1993.
8. ***SPOX. The DSP Operating System. A Technical Overview.*** Spectron Microsystems Inc, USA, 1991.
9. ***VIRTUOSO. User Manual.*** Intelligent Systems International, Belgium, 1993.

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# Chapter 1. Introduction

This chapter contains general description for *TORNADO-E31* stand-alone DSP controller.

## 1.1 General Information

*TORNADO-E31* is high performance floating-point DSP controller with TI TMW320C31 DSP for stand-alone DSP applications. *TORNADO-E31* DSP controller feature compact size and flexible modular system construction in order to meet requirements for multiple applications while keeping a cost to a minimum.

System architecture and construction of *TORNADO-E31* DSP controller are compatible with that of *TORNADO-E* product line of DSP controllers, and the only difference implies to the type of DSP installed and memory capacity.

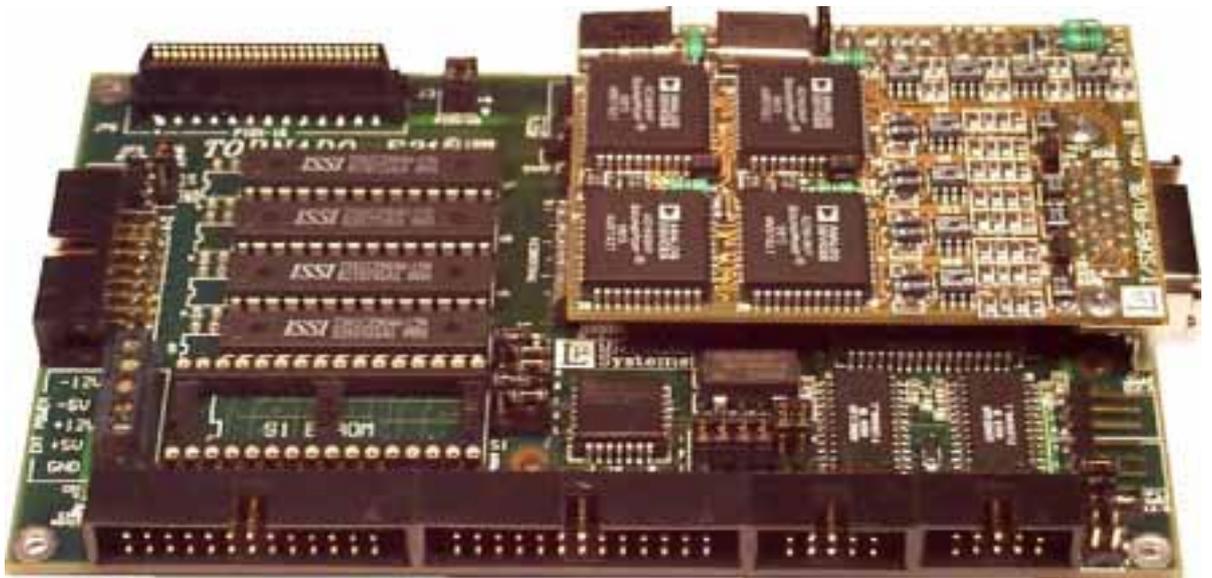


Fig.1-1. *TORNADO-E31* DSP controller board with SIOX daughter card module.

*TORNADO-E31* DSP controller features:

- 32-bit floating-point TMS320C31 DSP running at 60MHz
- up to 128Kx32 on-board static 0ws RAM and up to 1Mx8 on-board EPROM
- dual-channel 10Mbit/s USART (universal synchronous/asynchronous receiver/transmitter) with external RS232C and RS422/EIA-530 interfaces for communication with host computer and peripherals
- software boot from either the on-board EPROM, or DSP on-chip serial port, or no boot

- site for *TORNADO* serial I/O expansion (SIOX) daughter-card module for real-time telecom, speech/fax/modem, audio, instrumentation, industrial, digital radio, etc signal processing applications
- site for *TORNADO* parallel I/O expansion (PIOX-16) daughter-card module for multichannel high-speed telecom, instrumentation, industrial, digital radio, etc signal processing applications
- general purpose 10-bit parallel digital I/O for local system control
- compact size

The following are only few of many applications for *TORNADO-E31* DSP controllers:

- *real-time DSP and signal acquisition*
- *fax/modem*
- *vocoders and speech signal processing*
- *networking*
- *audio and acoustics signal processing*
- *multimedia*
- *radars*
- *digital radio*
- *instrumentation and industrial*
- *evaluation and education*
- many more ...

## 1.2 Technical Specification

The following are the technical specifications for *TORNADO-E31* DSP controllers.

<u>Parameter description</u>	<u>parameter value</u>
power supply voltage	+5V for <i>TORNADO-E31</i> board, optional -5V and $\pm 12V$ for SIOX/PIOX-16 daughter-card modules
power consumption	+5V@1.3A (t=+20°C)
DSP performance	60 MFLOPS @ 60 MHz clock
dimensions	145x90 mm
operating temperature	+5..+60°C
I/O expansion interfaces	one SIOX site one PIOX-16 site
<i>on-board SRAM and EPROM:</i>	
SRAM capacity	8K..128Kx32 0ws, 15ns access time (installed as four DIP-28/DIP-32 300MIL SRAM chips)

EPROM capacity	8K..1Mx8 ( $T_a \leq 240\text{ns}$ ) (installed as DIP-28/DIP-32 600MIL EPROM chip)
<i>watchdog timer (WDT) and reset controller:</i>	
WDT latency period	1.6 sec typical
duration of the WDT reset signal (generated by the DSP software)	>100 ns
duration of external reset input signal	>500 ns
duration of the output DSP reset signal	>0.2 sec
<i>on-board parallel digital I/O</i>	10 bits
<i>on-board USART (universal synchronous/asynchronous receiver/transmitter):</i>	
number of channels	2
supported protocols for each channel	<i>synchronous:</i> HDLC/X.25, SDLC, MONOSYNC, BISYNC  <i>asynchronous:</i> ASYNC
external electrical interfaces for each channel	RS232C or RS422/EIA-530 pinout
maximum data transfer speed for synchronous protocols (HDLC, SDLC, MONOSYNC, BISYNC) and external RS422/EIA-530 interface	10 Mbit/s
maximum data transfer speed for asynchronous protocol (ASYNC) and external RS232C interface	115 kBaud
maximum data transfer speed for asynchronous protocol (ASYNC) and external RS422/EIA-530 interface	2.5 Mbaud



## Chapter 2. System Architecture and Construction

This chapter contains description for *TORNADO-E31* system architecture, construction, and SIOX/PIOX-16 I/O expansion sites.

### 2.1 *TORNADO-E31* System Architecture

System architecture for *TORNADO-E31* DSP controller is presented at fig.2-1.

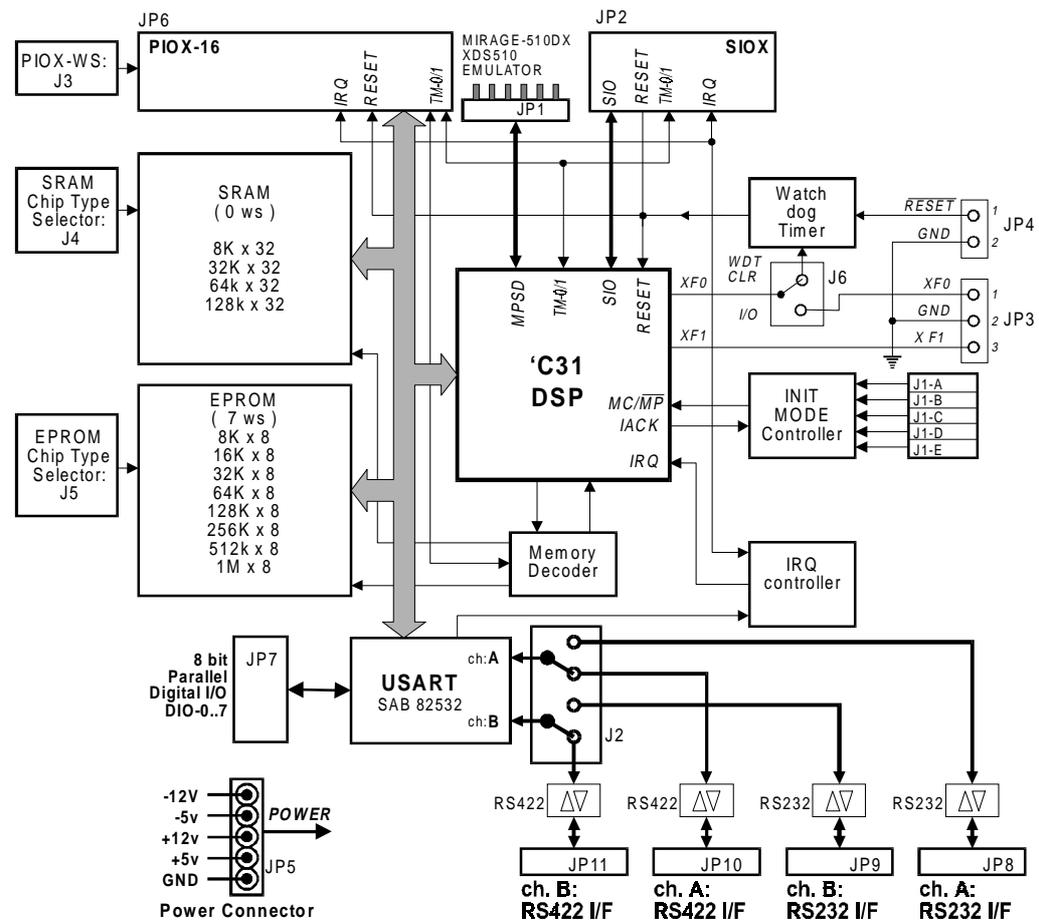


Fig.2-1. System architecture of *TORNADO-E31* DSP controller.

The main components of *TORNADO-E31* DSP controller are:

- 60MFLOPS 32-bit floating-point TMS320C31 DSP

- up to 128Kx32 0ws static RAM (SRAM) for program and data
- up to 1Mx8 EPROM memory for software boot code
- dual-channel multiprotocol 10Mbit/s USART (universal synchronous/asynchronous receiver/transmitter), which supports HDLC/X.25, SDLC, MONOSYNC, BISYNC, ASYNC protocols
- electrical interface multiplexer (UIF-MUX) for each of USART channel, which connects either to 115 kBaud RS232C or 10 Mbit/s RS422/EIA-530 interfaces
- 8-bit parallel digital I/O controller (as the part of USART) with individual masking for DSP interrupt generation and optional 2-bit XF0/XF1 DSP digital I/O
- serial I/O expansion (SIOX) interface site for SOX daughter-card module
- parallel I/O expansion (PIOX-16) interface site for PIOX-16 daughter-card module
- watch-dog timer (WDT)
- DSP reset controller (RC) and external RESET connector
- MPSD-IN connector for connection to external MPSD/JTAG emulator
- external power connector

Construction for *TORNADO-E31* DSP controller is presented at fig.2-2.

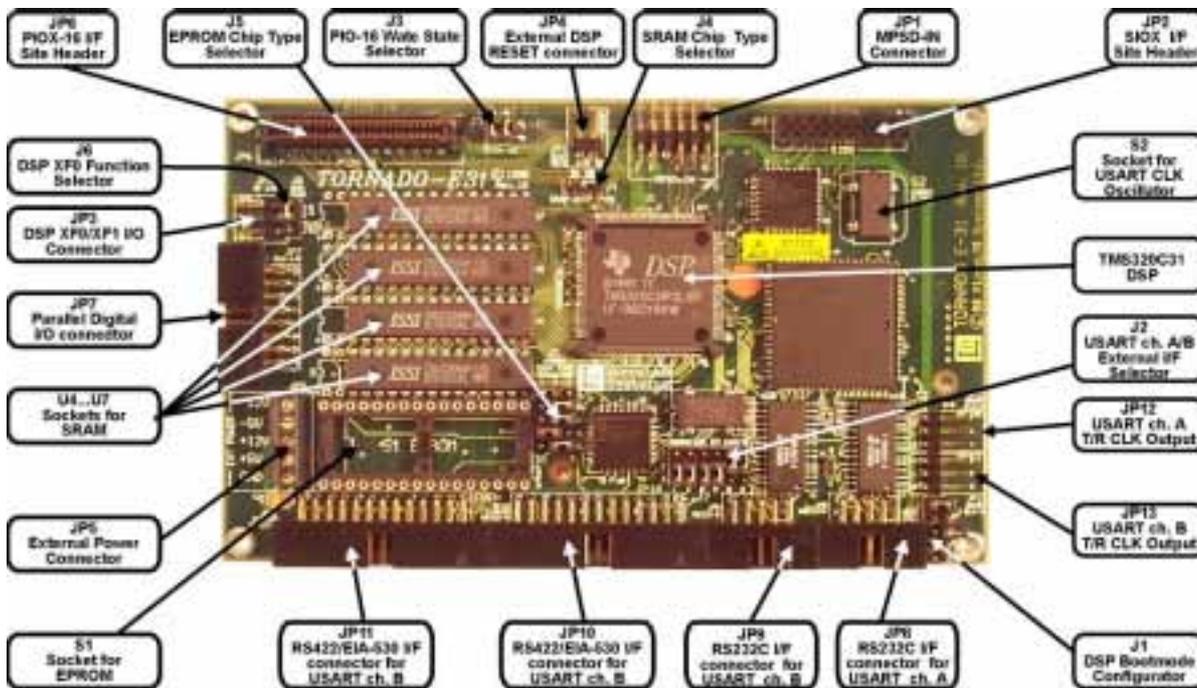


Fig.2-2. Construction of *TORNADO-E31* DSP controller.

### **TMS320C31 DSP**

The on-board TMS320C31 DSP is 32-bit floating-point 60MFLOPS@60MHz TMS320C31 DSP.

### **Static RAM (SRAM)**

*TORNADO-E31* provides up to 128Kx32 0ws user installed on-board static RAM (SRAM) for TMS320C31 DSP program and data memory areas. SRAM bank is designed to accommodate four byte-wide SRAM chips in the industry-standard DIP-28/DIP-32 300MIL packages.

### **EPROM Memory**

*TORNADO-E31* provides up to 1Mx8 of user-installed on-board EPROM memory for software boot. EPROM memory bank is designed to accommodate EPROM memory chips in DIP-28/DIP-32 600MIL package.

### **Dual-channel USART**

*TORNADO-E31* features the on-board dual-channel USART (universal synchronous/asynchronous receiver/transmitter) for communication with host computers, terminals, network adapters, or external peripherals.

USART is based around the SIEMENS SAB 82532 chip and supports popular synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) at up to 10 Mbit/s data transfer rate and industry-standard asynchronous protocol at up to 2.5 Mbaud independent for each channel.

Each channel of USART connects to external equipment via jumper selectable either RS232C or RS422/EIA-530 electrical interface.

### **Parallel digital I/O**

*TORNADO-E31* provides general purpose 8-bit parallel digital I/O, which might be used as external control I/O signals. These digital I/O signals are the part of internal USART facility, and allow generation of DSP interrupt on individually programmable high-to-low or low-to-high transitions when programmed as input pins. Also, XF0/XF1 DSP I/O pins are also available for user I/O via the edge-board connector.

### **Serial I/O Expansion Interface (SIOX) site**

*TORNADO-E31* on-board SIOX interface site is used for installation of AD/DA/DIO daughter-card module and comprises of signals for TMS320C31 DSP on-chip serial port, timers and interrupt control.

SIOX compatible daughter-card modules include a variety of AD/DA/DIO modules for telecom, speech/fax/modem, audio, and many more applications.

### **Parallel I/O Expansion Interface (PIOX-16) site**

*TORNADO-E31* feature PIOX-16 interface site for installation of high-speed AD/DA/DIO daughter-card module. PIOX-16 interface is allocated into TMS320C31 external bus.

PIOX-16 interface comprises of the signals for DSP 16-bit address and 16-bit data buses, data strobes and TMS320C31 DSP on-chip timers and interrupts control.

PIOX-16 compatible daughter-card modules include a variety of high-speed multichannel AD/DA/DIO modules for high-speed telecom, instrumentation, digital radio and many more applications.

### **Watch-dog timer (WDT)**

*TORNADO-E31* provides optional on-board watch-dog timer (WDT) in order to increase the reliability of stand-alone operation. While the DSP is operating properly, it should perform reset of WDT every 1.6 sec, otherwise the WDT will generate the DSP reset signal and will restart *TORNADO-E31*.

### **DSP Reset Controller (RC)**

The DSP reset signal for *TORNADO-E31* is generated by the DSP reset controller (RC) on the input conditions from the power supervisory circuit (PSC), watchdog timer (WDT) and external reset signal. The minimum duration of generated DSP reset signal is about 0.2 sec, whereas the minimum duration of external reset signal is 500ns. The WDT might be disconnected from the RC input using the on-board jumper in order to exclude the continuous reset generation while the software is being debugged.

### **Debugging TMS320C31 DSP Software**

Resident TMS320C31 DSP software for *TORNADO-E31* can be debugged using TI XDS510 and MicroLAB' *MIRAGE-510D* scan-path emulators using the industry standard TI C3x HLL Debugger or GoDSP TMS320C3x/C4x Code Composer IDE.

## **2.2 TMS320C31 DSP Environment**

The *TORNADO-E31* DSP controller utilizes TMS320C31 high-performance 32-bit floating point DSP from TI.

### **TMS320C31 DSP Bootmode Configurations**

The TMS320C31 DSP bootmode configuration is defined by the on-board jumper set J1-A..J1-E (refer to fig.2-2 or fig.A-1). Supported bootmode configurations are presented in table 2-1.

Table 2-1. TMS320C31 DSP Bootmode Configurations.

Bootmode ID	Description	jumper J1-A	jumper J1-B	jumper J1-C	jumper J1-D	jumper J1-E
IMODE#0	<p>Corresponds to the DSP Microprocessor start-up mode without boot process.</p> <p>After reset will be released, the DSP will fetch the reset vector from the on-board SRAM, which must contain valid DSP execution code.</p>	ON	OFF	OFF	OFF	OFF
IMODE#10	<p>Corresponds to the DSP Microcontroller start-up mode with boot from the on-board EPROM.</p> <p>The lowest 4Kx32 words of SRAM within the 000000H..000FFFH address range will be not available, since they are remapped to the DSP on-chip ROM, however full SRAM area is available at the 100000H base address. DSP must execute the IACK instruction after bootload process will complete in order to enable external DSP interrupts.</p>	OFF	ON	OFF	OFF	ON
IMODE#11	<p>Corresponds to the DSP Microcontroller start-up mode with boot from the DSP on-chip serial port.</p> <p>The lowest 4Kx32 words of SRAM within the 000000H..000FFFH address range will be not available, since they are remapped to the DSP on-chip ROM, however full SRAM area is available at the 100000H base address. DSP must execute the IACK instruction after bootload process will complete in order to enable external DSP interrupts.</p>	OFF	ON	OFF	ON	ON

<p><i>IMODE#20</i></p>	<p><i>Corresponds to the DSP Microcontroller start-up mode with boot from the on-board EPROM with further transition to the Microprocessor mode.</i></p> <p><i>The lowest 4Kx32 words of SRAM within the 000000H..000FFFH address range will be not available, since they are remapped to the DSP on-chip ROM, however full SRAM area is available at the 100000H base address. DSP must execute the IACK instruction after bootload process will complete in order to enable external DSP interrupts.</i></p> <p><i>After execution the IACK instruction the DSP on-chip ROM will be disabled, and the DSP Microprocessor mode will be set. Full SRAM will be available starting from the 000000H base address.</i></p>	<p>OFF</p>	<p>OFF</p>	<p>ON</p>	<p>OFF</p>	<p>ON</p>
<p><i>IMODE#21</i></p>	<p><i>Corresponds to the DSP Microcontroller start-up mode with boot from the DSP on-chip serial port with further transition to the Microprocessor mode.</i></p> <p><i>The lowest 4Kx32 words of SRAM within the 000000H..000FFFH address range will be not available, since they are remapped to the DSP on-chip ROM, however full SRAM area is available at the 100000H base address. DSP must execute the IACK instruction after bootload process will complete in order to enable external DSP interrupts.</i></p> <p><i>After execution the IACK instruction the DSP on-chip ROM will be disabled, and the DSP Microprocessor mode will be set. Full SRAM will be available starting from the 000000H base address.</i></p>	<p>OFF</p>	<p>OFF</p>	<p>ON</p>	<p>ON</p>	<p>ON</p>

- Note:
1. 'ON' corresponds to the installed jumper; 'OFF' corresponds to the removed jumper.
  2. Other bootmode configurations are reserved.
  3. Highlighted configuration corresponds to the factory setting.

The *IMODE#0* DSP bootmode configuration of *TORNADO-E31* corresponds to the DSP microprocessor start-up mode with the DSP vector mapped to the on-board SRAM. This mode is useful for the DSP software development and debugging.

**CAUTION**

When designing the DSP software for *TORNADO-E31* it is recommended to allocate all external DSP areas (sections) starting from the 001000H DSP address in order to provide compatibility with the DSP operation in the *IMODE#20/#21* DSP bootmodes.

The *IMODE#10/#11* DSP bootmode configurations of *TORNADO-E31* correspond to the DSP microcontroller start-up mode with boot from either the on-board EPROM or DSP on-chip serial port. The DSP reset vector is mapped to the DSP on-chip ROM. The EPROM contents and the DSP serial port input streams shall meet the format of DSP on-chip ROM bootloader requirements. After DSP executes first *IACK* instruction, the DSP external interrupts will be enabled. This mode is useful for embedded operation of *TORNADO-E31* with the DSP interrupt vectors allocated to the DSP on-chip SRAM.

The *IMODE#20/#21* DSP bootmode configurations of *TORNADO-E31* correspond to the DSP microcontroller start-up mode with boot from either the on-board EPROM or DSP on-chip serial port with further transition to the DSP microprocessor mode. The DSP reset vector is initially mapped to the DSP on-chip ROM. The EPROM contents and the DSP serial port input streams shall meet the format of DSP on-chip ROM bootloader requirements. After DSP executes first *IACK* instruction, the DSP external interrupts will be enabled and the DSP microprocessor mode will be restored and full SRAM area will be available at the 000000H base address. This mode can be used for embedded operation of *TORNADO-E31* and when full DSP on-chip memory must be used for program/data in order to get maximum DSP performance, and in order to obtain full compatibility with the *IMODE#0* software debug mode..

**CAUTION**

For *IMODE#20/#21* DSP bootmodes, the first executed *IACK* DSP instruction must be allocated beyond of the first 4K words of SRAM (000000H..000FFFH).

For *IMODE#20/#21* DSP bootmodes, the DSP Microprocessor mode will be restored after four DSP cycles after DSP will execute the *IACK* instruction.

***TMS320C31 DSP Address Space***

*TORNADO-E31* on-board TMS320C31 DSP address area comprises of the SRAM, EPROM and I/O areas in accordance with table 2-2.

Table 2-2. Address areas for TMS320C31 DSP in TORNADO-E31 DSP controllers.

Address area	DSP address range	word length	access mode	wait states	applicable DSP bootmodes
SRAM	000000H..01FFFFH  mirror at: 100000H..11FFFFH	32	r/w	0ws	<i>IMODE#0</i>
EPROM (Ta<100ns)	400000H..5FFFFFFH	8	r	0ws <sup>2)</sup>	
SRAM	001000H..01FFFFH  mirror at: 100000H..11FFFFH	32	r/w	0ws	<i>IMODE#10</i> <i>IMODE#11</i>
EPROM (Ta<100ns)	400000H..5FFFFFFH	8	r	0ws <sup>2)</sup>	
SRAM	before executing the IACK instruction: 001000H..01FFFFH  after executing the IACK instruction: 000000H..01FFFFH  mirror at: 100000H..11FFFFH	32	r/w	0ws	<i>IMODE#20</i> <i>IMODE#21</i>
EPROM (Ta<240ns)	400000H..5FFFFFFH	8	r	0ws <sup>2)</sup>	
DSP on-chip peripherals and memory	800000H..809FFFFH	32	r/w	0ws	all
USART	channel A: A00000H..A0003FH  channel B: A00040H..A0007FH	8	r/w	3ws	all
PIOX-16	FF0000H..FFFFFFFH	16	r/w	0..3ws + <i>PIOX_RDY</i>	all

Notes: 1. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

2. DSP access to the on-board EPROM is performed without on-board generated hardware wait states. In order to meet the access times of most EPROM chips ( $T_a \leq 240\text{ns}$ ), the DSP boot procedure for *IMODE#10/#11/#20/#21* must be performed with seven DSP software wait states and logical AND between the DSP software wait states and external ready signal by means of programming the DSP *Primary Bus Control Register* (@808064H) to the 000006F8H value for the DSP boot procedure. The DSP *Primary Bus Control Register* (@808064H) for the DSP boot procedure can be set via the configuration file for the *HEX30.EXE* software utility, which is the part of the TI TMS320 Floating-Point DSP Assembler Tools and TI TMS320 Floating-Point DSP Optimizing C Compiler.
3. 'Ta' denotes the access time.

**CAUTION**

In order to provide correct operation of the on-board hardware, the DSP *Primary Bus Control Register* (@808064H) must be set to the 00000400H value during user software execution.

**CAUTION**

In order to provide correct operation of the on-board hardware, the DSP *Primary Bus Control Register* (@808064H) must be set to the 000006F8H value during DSP bootmode procedure for *IMODE#10/#11/#20/#21* DSP boot modes.

**SRAM Area**

*TORNADO-E31* on-board SRAM operates at the DSP clock without any hardware wait states. On-board SRAM can be used for storing both program and data.

*TORNADO-E31* on-board SRAM bank comprises of four byte-wide SRAM chips and is designed to accommodate different types of SRAM chips from multiple SRAM manufacturers in the industry standard DIP-28/DIP-32 300MIL packages and operating at the 5v power supply. The particular SRAM chip type installed must match the setting of the on-board jumper J4 in accordance with table 2-3.

Table 2-3. Setting the SRAM chip type.

SRAM chips capacity and access time	SRAM IC package	jumper J4
8Kx8 @15ns	DIP-28 300MIL	2-3
32Kx8 @15ns	DIP-28 300MIL	1-2
64Kx8, 128Kx8 @15ns	DIP-32 300MIL	1-2

Note: 1. Highlighted configuration corresponds to default factory setting.

### **EPROM Area**

On-board EPROM of *TORNADO-E31* should be used to store the DSP application software boot code, which will be reloaded to the on-board SRAM during DSP boot procedure. EPROM bank assumes installation of 128K..1Mx8 EPROM chip with access time below 240ns and in the DIP-28/DIP-32 600MIL package into the dedicated on-board DIP-32 socket (refer to fig.2-2).

The EPROM chip must be programmed in the external programmer only, and can be used for read-only software boot purposes in *TORNADO-E31*.

The on-board J5 jumper set (jumpers J5-A..J5-E) must be used to select the particular EPROM chip type in accordance with table 2-4.

Table 2-4. EPROM chip type selector.

EPROM type	configuration jumpers J5					EPROM IC package
	J5-A	J5-B	J5-C	J5-D	J5-E	
2764	2-3	2-3	2-3	2-3	2-3	DIP-28 600MIL
27128	2-3	2-3	2-3	2-3	2-3	DIP-28 600MIL
27256	1-2	2-3	2-3	2-3	2-3	DIP-28 600MIL
27512	1-2	2-3	2-3	1-2	2-3	DIP-28 600MIL
27010	1-2	2-3	2-3	1-2	2-3	DIP-32 600MIL
27020	1-2	1-2	2-3	1-2	2-3	DIP-32 600MIL
27040	1-2	1-2	1-2	1-2	2-3	DIP-32 600MIL
27080	1-2	1-2	1-2	1-2	1-2	DIP-32 600MIL

Note: 1. Highlighted configuration corresponds to default factory setting.

### CAUTION

TMS320C31 DSP allocates 8-bit EPROM data words  
on the 32-bit data word boundaries.

### **Dual-channel USART**

*TORNADO-E31* features the on-board dual-channel USART (universal synchronous/asynchronous receiver/transmitter) for communication with host computers, terminals, network adapters, or external peripherals using industry standard serial communication protocols.

USART is based around the SIEMENS SAB 82532 chip and supports popular synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) at up to 10 Mbit/s data transfer rate and the industry-standard asynchronous protocol (ASYNC) at up to 2.5 Mbaud independently for each channel.

Each channel of USART connects to external communication equipment via either RS232C or RS422/EIA-530 electrical interface. Selection of particular interface is performed by the on-board jumper set J2.

For detail information about USART and how to configure external RS232C/RS422 interfaces for USART please refer to the *USART* section later in this chapter.

### **PIOX-16 Parallel I/O Expansion Interface Site**

*TORNADO-E31* controller provides on-board 16-bit parallel I/O expansion interface (PIOX-16) site for compatible high-speed AD/DA/DIO daughter card modules. PIOX-16 area is mapped directly to the address space of TMS320C31 DSP.

PIOX-16 occupies 64Kx16 address area within the address space of TMS320C31 DSP. PIOX-16 site comprises of the TMS320C31 DSP 16-bit data and 16-bit address buses, data strobes, DSP-on-chip timers TM-0/TM-1 input/output, *INT0..INT2* external interrupt requests and  $\pm 5v/\pm 12v$  power supply lines. For details about PIOX-16 site refer to the corresponding section later in this chapter.

### **External Hardware Interrupts for TMS320C31 DSP**

*TORNADO-E31* on-board TMS320C31 DSP supports four external hardware interrupt requests *INT0..INT3* with the *INT0* request having the highest priority. These requests correspond to the following events:

- *INT0..INT2* interrupt requests can be generated by SIOX/PIOX/PIOX-16 daughter-card modules
- *INT3* is wired to the interrupt request from the on-board USART.

*TORNADO-E31* hardware provides direct wiring of external *INT0..INT3* interrupt request signals to the corresponding *INT0..INT3* interrupt request pins of TMS320C31 DSP chip via the on-board interrupt controller. Both static and pulse interrupt requests are supported with active falling edge and active pulse duration 66ns and longer.

#### **CAUTION**

*TORNADO-E31* hardware is designed for external DSP interrupts *INT0..INT3* with inverse polarity inputs.

### **TMS320C31 DSP Reset Controller (RC)**

*TORNADO-E31* feature TMS320C31 DSP reset controller (RC), which generates TMS320C31 DSP reset pulse in case any of the following conditions:

- during the power-on and in case of power failure (the power is controlled by the PSC power supervisory circuit)
- external reset signal is applied from connector JP4
- WDT feature is enabled by jumper J6 and the WDT latency period (1.6 sec typical) is expired.

If any of the above conditions comes true, then the generated DSP reset signal has duration min 0.2 sec and is indefinitely prolonged while this condition(s) is still true.

### **XF0/XF1 DSP I/O pins**

*TORNADO-E31* provides optional two-bit external I/O via on-board JP3 connector and DSP XF0/1 I/O pins, which are controlled by the TMS320C31 DSP on-chip IOF register.

The XF1 I/O pin of TMS320C31 DSP is directly wired to the on-board JP3 connector, and can be used for external I/O purposes only.

However, the XF0 I/O pin of TMS320C31 DSP can be used for external I/O purpose via the on-board JP3 connector, or for the on-board watch-dog timer (WDT) reset. The particular function of the DSP XF0 pin is defined by the on-board J6 jumper in accordance with table 2-5.

*Table 2-5. Setting the function of the DSP XF0 pin.*

<b>DSP XF0 pin function</b>	<b>jumper J3</b>
<i>DSP XF0 pin is used as the I/O pin via the on-board JP3 jumper. WDT feature is disabled.</i>	1-2
<i>DSP XF0 pin is used as the output pin for the WDT reset. External I/O feature via JP3 connector is disabled.</i>	2-3

*Note:* 1. Highlighted configuration corresponds to default factory setting.

### **Watchdog Timer (WDT)**

*TORNADO-E31* provides the on-board watchdog timer (WDT), which can generate the DSP reset (restart) pulse in case the WDT feature is enabled, and in case WDT is not reset by the on-board DSP software during the WDT latency period. The WDT feature might be used to increasing the software and system operation reliability.

Duration of the WDT latency period is typical 0.8 sec. Once WDT feature is enabled and activated, then WDT must be periodically reset (with the period less than the WDT latency period) by the DSP software by means of retrogressing the DSP XF0 output pin.

**CAUTION**

The WDT feature is enabled by setting the J6 jumper to the 1-2 position in accordance with table 2-5.

Once enabled, the WDT feature might be activated by programming the DSP XF0 pin as the output pin via the DSP on-chip IOF register. The particular output value of the XF0 pin is insignificant, and the WDT will be reset by changing the output state of the XF0 pin.

**SIOX Serial I/O Expansion Interface Site**

*TORNADO-E31* provides on-board site for serial I/O expansion interface (SIOX) for compatible AD/DA/DIO daughter-card modules.

SIOX site comprises of the TMS320C31 DSP-on-chip serial port control lines, DSP-on-chip timers TM-0/TM-1 input/output, *INT0..2* external interrupt requests and  $\pm 5\text{v}/\pm 12\text{v}$  ISA-bus power supply lines. For details about SIOX site refer to the corresponding section later in this chapter.

**External Power Connector**

External power connector (JP8) for *TORNADO-E31* (see fig.2-2 and fig.A-1) comprises of the  $\pm 5\text{v}$  and  $\pm 12\text{v}$  power lines. Note, that only +5v power input is actually required for operation of on-board *TORNADO-E31* hardware. Other power lines (-5v and  $\pm 12\text{v}$ ) are wired to PIOX-16 and SIOX daughter-card sites.

## 2.3 Parallel I/O Expansion Interface Site (PIOX-16)

*TORNADO-E31* architecture provides expansion of the on-board I/O resources using 16-bit parallel I/O expansion interface (PIOX-16) site.

PIOX-16 daughter-card sites are designed for compatible PIOX-16 daughter modules. PIOX-16 daughter-card modules are installed above the *TORNADO-E31* mainboard (see fig.1-1 and fig.2-6) and are compatible with all *TORNADO* DSP systems and controllers.

**Description**

*TORNADO-E31* PIOX-16 interfaces appear as 64Kx16 I/O address area of the TMS320C31 DSP address space. PIOX-16 includes DSP data/address buses, data strobes, TMS320C31 DSP on-chip timers I/O pins and external interrupt inputs, DSP reset signal, and power supply lines. PIOX-16 supports 16-bit data transfer cycles only.

**Installation of PIOX-16 daughter-card modules onto TORNADO-E31**

Figure 2-3 shows installation of PIOX-16 daughter-card module onto *TORNADO-E31* DSP controller.

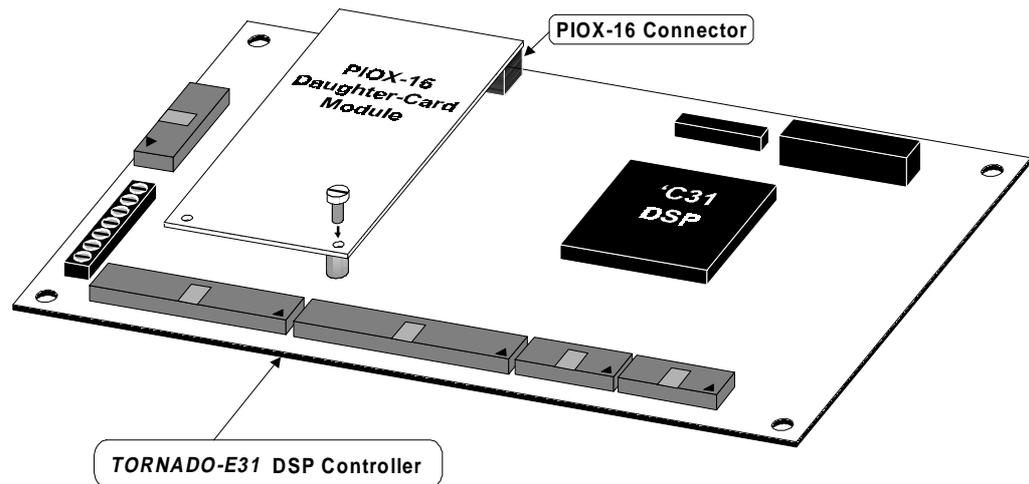


Fig.2-3. Installation of PIOX-16 daughter-card module onto *TORNADO-E31*.

### ***PIOX-16 connector pinout***

*TORNADO-E31* on-board PIOX-16 connector is a high-density DDK 50-pin DHB-series dual-row female connector with 0.05" pin pitch. Compatible PIOX-16 plugs for customer designed daughter-card modules are available on request from MicroLAB Systems upon request.

PIOX-16 connector pinout specification is presented at fig 2-4 whereas signal specifications are listed in table 2-6.

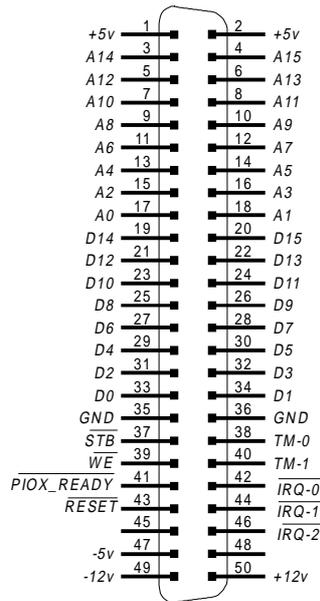


Fig.2-4. PIOX-16 connector pinout (top view).

Table 2-6. PIOX-16 signal description.

Signal name	signal type	description
A0..A15	O	Address bus.
D0..D15	I/O	Data bus.
$\overline{STB}$	O	Active low data transfer strobe ( $\overline{STB}=0$ ).
$\overline{WE}$	O	Active low write enable signal ( $\overline{WE}=0$ ).
$\overline{PIOX\_READY}$	I	Active low data ready ( $\overline{PIOX\_READY}=0$ ) signal. Generated by PIOX-16 daughter-card module in order to match the PIOX-16 cycle timing with timing requirements of memory and I/O devices used in PIOX-16 module.
TM-0	I/O	Input/output signal from TMS320C31 DSP on-chip Timer-0.
TM-1	I/O	Input/output signal from TMS320C31 DSP on-chip Timer-1.
$\overline{RESET}$	O	Reset signal ( $\overline{RESET}=0$ ) for the on-board TMS320C31 DSP chip.

$\overline{IRQ-0}, \overline{IRQ-1}, \overline{IRQ-2}$	I	Active low external interrupt request lines for the on-board TMS320C31 DSP chip. These lines are pulled up with the on-board resistors. DSP interrupt request is generated on the falling edge of input signals. The minimum duration of interrupt request signals must be 66ns.
GND		Ground.
+5v		+5v power.
+12v		+12v power.
-5v		-5v power.
-12v		-12v power.

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
2. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

### PIOX-16 data transfer cycles

PIOX-16 interface site supports 16-bit data transfer cycles only, and, therefore PIOX-16 connector does not contain the cycle definition signals.

### Data transfer timing for PIOX-16

The PIOX-16 data transfer timing is presented at fig.2-5. This data transfer timing is known as MOTO mode and assumes usage of data strobe signal and write enable signal.

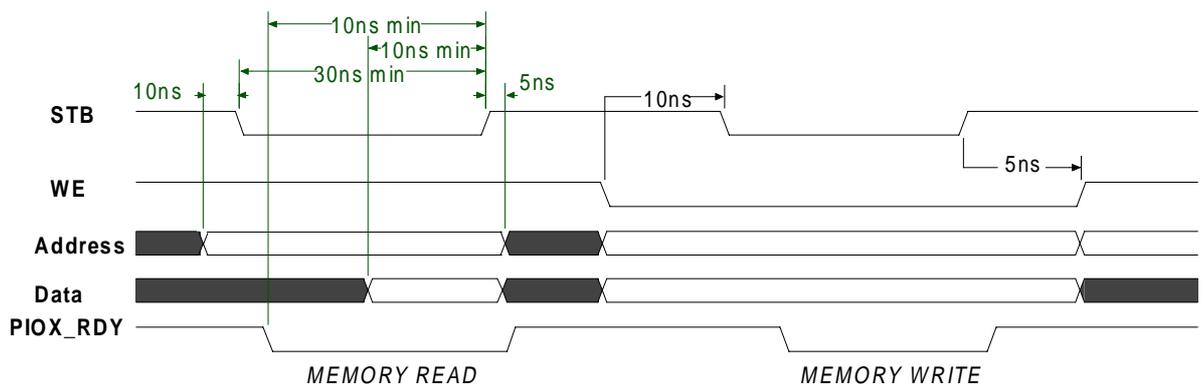


Fig.2-5. Timing diagram for PIOX-16 data transfer strobe.

### PIOX-16 wait states control

TORNADO-E31 on-board PIOX-16 interface supports generation of up to three hardware programmable wait states using on-board J3 jumper set in accordance with table 2-7. This feature is important in case PIOX-16

daughter-card module contains dual-port RAM and other memory devices with delayed ready signal generation.

**CAUTION**

Final data transfer acknowledgement over PIOX-16 interface is performed by means of asynchronous *PIOX\_READY* signal.

*Table 2-7. Setting data strobe width for PIOX-16.*

Data strobe width	jumper J3-A	jumper J3-B	Description
<i>PIOX_READY</i>	OFF	OFF	Data strobe width is defined by <i>PIOX_READY</i> signal only.
<i>1ws &amp; PIOX_READY</i>	ON	OFF	Data strobe width is at least 1ws (132ns) and afterthat is defined by <i>PIOX_READY</i> signal only.
<i>2ws &amp; PIOX_READY</i>	OFF	ON	Data strobe width is at least 2ws (198ns) and afterthat is defined by <i>PIOX_READY</i> signal only.
<i>3ws &amp; PIOX_READY</i>	ON	ON	Data strobe width is at least 1ws (264ns) and afterthat is defined by <i>PIOX_READY</i> signal only.

- Notes:
1. Jumper positions: *OFF* - jumper is not installed; *ON* - jumper installed.
  2. Highlighted configuration corresponds to the factory default setting.

**Physical dimensions for PIOX-16 daughter-card modules**

Physical dimensions for PIOX-16 daughter-card modules are presented at fig.2-6. This information is intended for those *TORNADO* customers, who need to design customized PIOX-16 daughter-card modules.

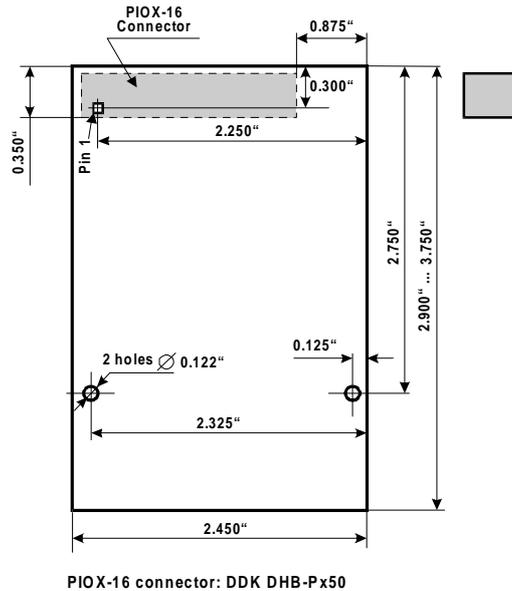


Fig.2-6. Physical dimensions for PIOX-16 daughter-card modules.

## 2.4 Serial I/O Expansion Interface Site (SIOX)

*TORNADO-E31* architecture provides expansion of the on-board TMS320C31 I/O resources via on-board serial I/O expansion interface site (SIOX) (refer to fig.1-1 and fig.2-2), which are designed to carry compatible daughter-card modules.

On-board SIOX site of *TORNADO-E31* are compatible with that for all *TORNADO* DSP systems and controllers.

Available SIOX daughter cards for *TORNADO* include a variety of AD/DA/DIO daughter cards for telecommunication, speech and audio signal processing, industrial and instrumentation applications, and many more.

### Description

SIOX site comprises of signals for TMS320C31 DSP on-chip serial port, timers and interrupts control, as well as DSP reset signal and power supply lines.

The SIO-0 port of SIOX site of *TORNADO-E31* is connected directly to the corresponding pins of TMS320C31 DSP on-chip serial port.

Maximum throughput of SIO-0 serial port of SIOX site on *TORNADO-E31* DSP controllers is 12.6Mbit/s for external serial clock and 15Mbit/s for DSP generated serial clock.

External analog and digital I/O signals for installed SIOX daughter-card modules should be attached by means of the SIOX on-module I/O connector via rear panel of host PC.

**Installation of SIOX daughter-card modules onto TORNADO-E31**

Figure 2-7 shows installation of SIOX daughter-card modules onto TORNADO-E31 DSP controller.

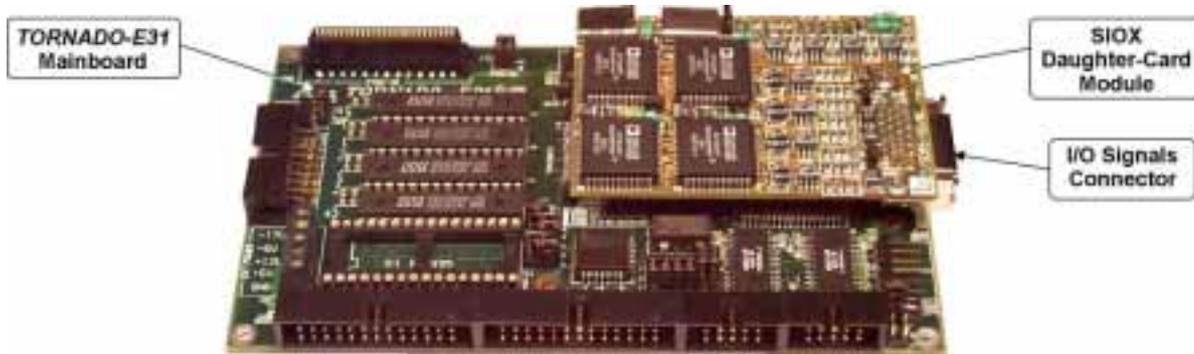


Fig.2-7. TORNADO-E31 with SIOX daughter-card module installed.

**SIOX site connector**

SIOX site connector is an industry standard dual-row 20-pin female header with 0.1"x0.1" pin pattern. SIOX connector pinout is presented at fig.2-8 and signal specifications are listed in table 2-8.

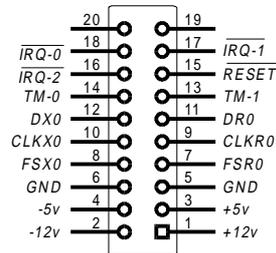


Fig.2-8. SIOX connector pinout (top view).

Table 2-8. SIOX signal specification.

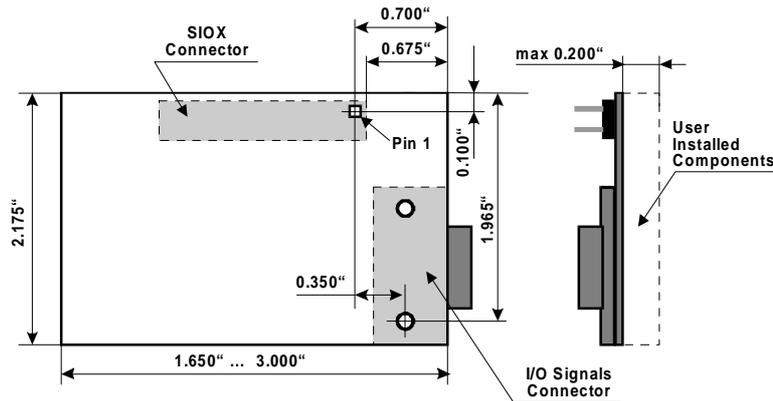
SIOX signal name	signal type	description
<b>SIO-0 port control</b>		
<i>DX0</i> <i>FSX0</i> <i>CLKX0</i>	O/Z I/O I/O	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX site. For SIOX site of <i>TORNADO-E31</i> DSP controllers these signals correspond to the TMS320C31 DSP on-chip serial port transmitter and are wired directly to its pins.
<i>DR0</i> <i>FSR0</i> <i>CLKR0</i>	I I/O I/O	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX site. For SIOX site of <i>TORNADO-E31</i> DSP controllers these signals correspond to the TMS320C31 DSP on-chip serial port receiver and are wired directly to its pins.
<b>Timers, Reset and Interrupt Requests</b>		
<i>TM-0</i>	I/O	Input/output signal from TMS320C31 DSP on-chip Timer-0.
<i>TM-1</i>	I/O	Input/output signal from TMS320C31 DSP on-chip Timer-1.
$\overline{RESET}$	O	Reset signal ( $\overline{RESET} = 0$ ) for TMS320C31 DSP.
$\overline{IRQ-0}$ , $\overline{IRQ-1}$ , $\overline{IRQ-2}$	I	Active low external interrupt request lines for the on-board TMS320C31 DSP chip. These line are pulled up with the on-board resistors. DSP interrupt request is generated on the falling edge of input signals. The minimum duration of interrupt request signals must is 66ns.
<b>Power Supplies</b>		
<i>GND</i>		Ground.
<i>+5v</i>		+5v power.
<i>+12v</i>		+12v power.
<i>-5v</i>		-5v power.
<i>-12v</i>		-12v power.

Note:

- Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
- All logical signal levels and load currents correspond to that for CMOS/TTL signals.

### Physical dimensions for SIOX daughter-card modules

Physical dimensions for SIOX daughter-card module are presented at fig.2-9. This information is intended for those *TORNADO* customers, who need to design customized SIOX daughter-card modules.



SIOX connector: 20-pin or 26-pin straight dual-row mail header  
(0.025" Sq., 0.1"x0.1" pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N  
DDK DHA-RC20-R122N  
DDK DHA-RC26-R122N

Fig.2-9. Physical dimensions for SIOX daughter-card modules.

## 2.5 Dual-channel USART

*TORNADO-E31* features the on-board dual-channel USART (universal synchronous/asynchronous receiver/transmitter) for communication with host computers, terminals, network adapters, or external peripherals using industry standard serial communication protocols.

USART is based around the SIEMENS SAB 82532 chip and supports popular synchronous protocols (HDLC/X.25, SDLC, MONOSYNC, BISYNC) at up to 10 Mbit/s data transfer rate and the industry-standard asynchronous protocol at up to 2.5 Mbaud. Protocol selection is performed independent for each channel.

Each channel of USART connects to external communication equipment via either RS232C or RS422/EIA-530 electrical interface. Selection of particular interface is performed by the on-board jumpers. The RS232C interface provides communication at up to 115kbaud and the RS422/EIA-530 interface provides up to 10 Mbit/s of data transfer rate.

USART also provides 8-bit of general purpose parallel digital I/O (*DIO-0..7*), which is wired to the on-board JP7 connector. For details about parallel digital I/O refer to the corresponding section later in this chapter.

### *USART register set*

The USART register set comprises of 128 8-bit registers totally for on-chip channels "A" and "B". SAB 82532 chip is extremely flexible software programmable device with build-in FIFO for each of communication channel, PLL and system configuration registers. For details about how to program SIEMENS SAB 82532 USART refer to original manufacturer documentation, which is supplied in electronic or paper form together with *TORNADO-E31* board.

USART is allocated in the 32-bit I/O memory area of the on-board TMS320C31 DSP (see table 2-2). USART has 8-bit data bus, which is wired to the lowest significant byte of 32-bit DSP data bus. Therefore, the 8-bit USART registers are allocated at the 32-bit word boundaries of DSP data bus.

### **USART-to-DSP interrupt**

USART can generate the interrupt request to TMS320C31 DSP via the DSP *INT3* external interrupt request line. The USART interrupt is internal logical OR from many interrupt sources inside USART including the interrupt requests from parallel digital I/O port.

#### **CAUTION**

The interrupt request of the SAB 82532 USART chip must be configured by the DSP software as “pushed-pulled” “active-low” output (refer to SIEMENS SAB 82532 USART documentation for how to configure the interrupt request output).

### **USART-hardware reset**

USART hardware reset is performed simultaneously with the hardware reset of *TORNADO-E31* board, and is actually the hardware reset signal for on-board TMS320C31 DSP.

### **Configuring external RS232C/RS422 interfaces for USART**

Each channel of USART connects to external communication equipment via either RS232C or RS422/EIA-530 electrical interface. Selection of particular interface is performed by the on-board jumpers set J2 (see fig.A-1) in accordance with table 2-9 for channel “A” and in accordance with table 2-10 for channel “B” of USART.

Table 2-9. Configuration of external interfaces for channel "A" of USART.

Interface	interface connector on TORNADO-E31 board	jumper J2-A	jumper J2-C	jumper J2-D
<i>RS422/EIA-530</i> (transmitter data transfer clock is generated by the USART on-chip clock generator and does not appear at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP10 (DB-25 male)	2-3	1-2	2-3
<i>RS422/EIA-530</i> (external data transfer clocking is used from pins CLKX+/CLKX- RS422/EIA-530 connector)	JP10 (DB-25 male)	2-3	1-2	1-2
<i>RS422/EIA-530</i> (transmitter data transfer clock is generated by the USART on-chip clock generator and appears at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP10 (DB-25 male)	2-3	2-3	2-3
<i>RS232C</i>	JP8 (DB-9 male)	1-2	1-2	2-3

Notes: 1. The highlighted configuration corresponds to the factory settings.

Table 2-10. Configuration of external interfaces for channel “B” of USART.

Interface	interface connector on TORNADO-E31 board	jumper J2-B	jumper J2-E	jumper J2-F
<i>RS422/EIA-530</i> (transmitter data transfer clock is generated by the USART on-chip clock generator and does not appear at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP11 (DB-25 male)	2-3	1-2	2-3
<i>RS422/EIA-530</i> (external data transfer clocking is used from pins CLKX+/CLKX- RS422/EIA-530 connector)	JP11 (DB-25 male)	2-3	1-2	1-2
<i>RS422/EIA-530</i> (transmitter data transfer clock is generated by the USART on-chip clock generator and appears at the CLKX+/CLKX- pins of RS422/EIA-530 connector)	JP11 (DB-25 male)	2-3	2-3	2-3
<i>RS232C</i>	JP9 (DB-9 male)	1-2	1-2	2-3

Notes: 1. The highlighted configuration corresponds to the factory settings.

### RS232C interface connectors

RS232C interface assumes the single-ended bipolar I/O signals, provides communication at up to 115 kBaud and is generally designed for usage in tandem with ASYNC asynchronous protocol of USART. The RS232C interface is an industry standard interface for communication with personal computers, computer peripherals, industrial control devices, etc.

The *TORNADO-E31* on-board RS232C interface connectors pinout is presented at figure 2-10.

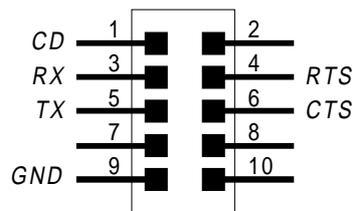


Fig. 2-10. RS232C interface connectors pinout for *TORNADO-E31*.

**CAUTION**

*TORNADO-E31* on-board RS232C connectors are the industry 10-pin 0.1"x0.1" male headers, which are widely used for connection RS232C ports to IBM PC motherboards.

You have to use standard 10-pin female to male DB-9 or DB-26 converter flat cables for PC to convert the *TORNADO-E31* on-board RS232C connectors to the industry standard DB-9 or DB-26 male connectors for RS232C interface.

**RS422/EIA-530 interface connectors**

RS422/EIA-530 interface assumes differential unipolar I/O signals with 110 Ohm line terminators, provides communication at up to 10 Mbit/s and is generally designed for usage in tandem with all synchronous protocols. RS422/EIA-530 interface may be also used with ASYNC asynchronous protocol of USART delivering up to the 2.5 Mbaud of data transfer rate, however this solution is not standard. The RS422/EIA-530 interface is an industry standard electrical interface for communication with network equipment, high-speed computer peripherals, etc.

The *TORNADO-E31* on-board RS422/EIA-530 interface connectors pinout is presented at figure 2-11.

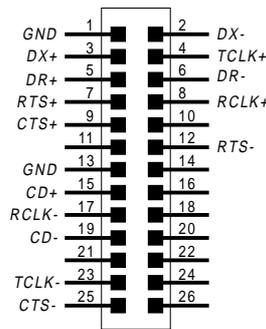


Fig. 2-11. RS422/EIA-530 interface connectors pinout for *TORNADO-E31*.

**2.6 Parallel Digital I/O**

*TORNADO-E31* also provides 8-bit of general purpose parallel digital I/O signals (*DIO-0..7*), which are wired to the on-board JP7 connector (see fig.2-2 and fig.A-1) and 2-bit general purpose I/O (*XF0/XF1*), which are wired to the on-board JP3 connector.

Digital I/O lines are useful for interfacing to external sensors, switches, etc and for generation of local control signals in a variety of applications.

### **DIO-0..DIO-7 parallel I/O**

*DIO-0..7* parallel digital I/O lines are programmable I/O pins of the on-board SAB 82532 USART (for more information about USART refer to the corresponding section earlier in this chapter).

Each of the *DIO-0..7* parallel digital I/O lines allows individual programming of direction and masking of USART interrupt, which might be generated on the user programmable input signal edge.

For more details about how to program the parallel digital I/O signals of USART refer to the original manufacturing documentation for SIEMENS SAB 82532 USART.

The JP7 parallel digital I/O connector pinout is presented at fig.2-12.

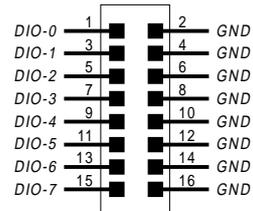


Fig.2-12. Parallel digital I/O connector pinout (*DIO-0..7* signals) for *TORNADO-E31*.

### **XF0/XF1 parallel I/O**

*XF0/XF1* parallel digital I/O lines are programmable I/O pins of the on-board TMS320C31 DSP, which are available via the JP3 on-board connector (fig.2-13).

For more details about how to use *XF0/XF1* DSP I/O line refer to the ‘TMS320C31 DSP Environment’ section earlier in this chapter and to table 2-5.

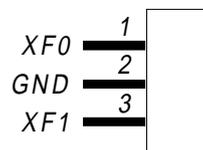


Fig.2-13. XF0/XF1 I/O signal connector of *TORNADO-E31*.

## **2.7 Emulation Tools for *TORNADO-E31***

*TORNADO-E31* uses scan-path emulation technique for the on-board TMS320C31 DSP in order to debug resident TMS320C31 DSP environment and software. Compatible scan-path emulation tools include the TI XDS510 or MicroLAB’ *MIRAGE-510D* universal JTAG/MPSD emulators with MPSD (C3x) external pod.

## 2.8 Software Development Tools

TMS320C31 DSP is now an industry standard DSP and is supported by a variety of software development tools from multiple 3<sup>rd</sup> party vendors.

### *Compilers and Debuggers*

Software development for *TORNADO-E31* is supported by TI TMS320C31 DSP Optimizing C Compiler and Assembly Language Tools.

Compatible emulators include TI XDS510 and MicroLAB' *MIRAGE-510D* emulators running under TI C3x HLL Debugger or TMS320C3x/C4x Code Composer IDE from GoDSP Corp ([www.go-dsp.com](http://www.go-dsp.com)).

### *Hypersignal RIDE Visual DSP Algorithm Development and Simulation Tool*

*TORNADO-E31* DSP controllers are supported by DSP algorithm development tools from Hyperception Inc ([www.hyperception.com](http://www.hyperception.com)), which include Hypersignal Block Diagram, RIDE and Code Generator. Hypersignal RIDE is the visual real-time integrated DSP algorithm development and simulation environment for Windows 95/NT, and allows design entry using high-level function blocks (FIR, FFT, math, etc). The designed DSP algorithm is compiled and might be loaded into *TORNADO-E31* in order to evaluate the algorithm parameters for real-time execution and to benefit from the ultra-high performance of *TORNADO-E31* DSP controllers.

### *Real-time Multitasking Operating Systems (RTOS)*

*TORNADO-E31* is supported by multiple RTOS that provide multitasking capabilities:

- *VIRTUOSO* from Eonic Systems Inc ([www.eonic.com](http://www.eonic.com)) is an industry standard high-performance RTOS and provides full feature multitasking support. It comes standard with capabilities for host file, keyboard and screen text/graphics I/O from DSP environment via *TORNADO-E31* host ISA-bus interface, and is available with a wide selection of function libraries for DSP, math, matrix, 2D, etc. computations.
- *NUCLEUS PLUS* from Accelerated Technology Inc ([www.atinucleus.com](http://www.atinucleus.com)) is an industry standard single-processor high-performance RTOS and provides full feature multitasking support. It features low cost and comes standard with source codes. Available options include *NUCLEUS FILE*, *NUCLEUS NET*, and *NUCLEUS DBUG+* that also come in source codes.
- *SPOX* from Spectron Microsystems Inc ([www.spectron.com](http://www.spectron.com)) is an industry standard RTOS for DSP that provides multitasking support. It is available with a selection of function libraries for DSP, math, matrix, etc. computations.

### *Application Software Tools for TORNADO-E31*

Application specific tools for *TORNADO-E31* DSP controller include a variety of function libraries for DSP, math, vector, image, etc computation, as well as function libraries for vocoder/fax/modem applications and audio multimedia.

## Chapter 3. Installation and Configuration

This chapter includes instructions for installation of *TORNADO-E31* DSP controller.

### 3.1 Applying the power

The power to *TORNADO-E31* controller should apply via on-board JP8 connector (see fig.A-1). For proper operation the board requires +5v power only, whereas optional -5v and  $\pm 12v$  power inputs are routed to the on-board SIOX and PIOX-16 daughter-card sites.

### 3.2 Installation of EPROM chip

Installation of EPROM chip (refer to fig.2-2 and fig.A-1) into the S1 socket on *TORNADO-E31* board should be performed while the board power is off (fig.3-1).

#### CAUTION

*TORNADO-E31* mainboards are designed to carry the EPROM 8K..1Mx8 5v chips in either DIP-28 or DIP-32 600 MIL IC packages.

#### CAUTION

You have to set the on-board J5 jumper in accordance with table 2-4 in order to meet the installed EPROM chip type.

#### *Installation of EPROM chip*

In order to install EPROM chip into the dedicated socket on *TORNADO-E31* mainboard follow the recommendations below (see fig. 3-1):

- switch off the power
- take EPROM chip by your fingers in such way that its front (labeling) surface is turned at you
- adjust EPROM chip to be parallel to surface of the corresponding S1 socket on *TORNADO-E31* board
- orient EPROM chip in such way, that pin #1 of its DIP-32 (DIP-28) package will match the corresponding position of pin #1 (pin#3) of on-board S1 socket
- safely insert EPROM chip into the on-board S1 socket
- set J5 jumper in accordance with table 2-4 to meet the installed EPROM chip type
- switch on the power

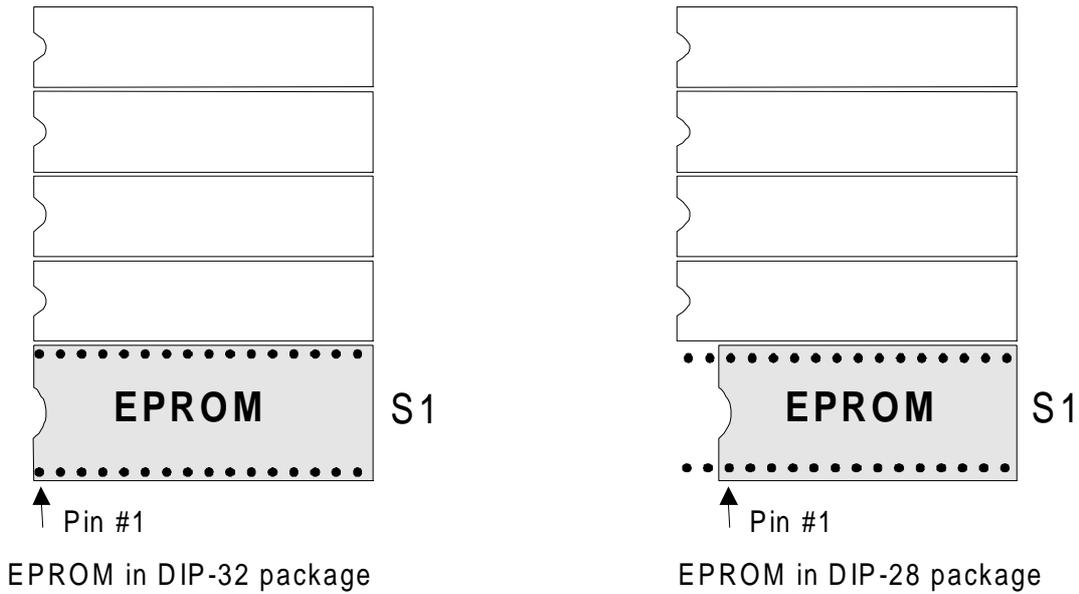


Fig.3-1. Installation of EPROM chip onto *TORNADO-E31* board.

### 3.3 Installation of SRAM chips

Installation of SRAM chips (refer to fig.2-2 and fig.A-1) into the U4..U7 sockets of SRAM bank on *TORNADO-E31* board should be performed while the board power is off (fig.3-2).

#### CAUTION

*TORNADO-E31* mainboards are designed to carry four identical 8K..128Kx8 15ns 5v SRAM chips 5v chips in either DIP-28 or DIP-32 300 MIL IC packages.

You have to install all four SRAM chips simultaneously into the corresponding sockets on *TORNADO-E31* board in order to provide correct operation of the on-board hardware.

**CAUTION**

You have to set the on-board J4 jumper in accordance with table 2-3 in order to meet the installed SRAM chip type.

**Installation of SRAM chips**

In order to install SRAM chips into the dedicated socket on *TORNADO-E31* mainboard follow the recommendations below (see fig. 3-2) :

- switch off the power
- take SRAM chip by your fingers in such way that its front (labeling) surface is turned at you
- adjust SRAM chip to be parallel to surface of the corresponding U4..U7 socket on *TORNADO-E31* board
- orient SRAM chip in such way, that pin #1 of its DIP-32 (DIP-28) package will match the corresponding position of pin #1 (pin#3) of on-board U4..U7 socket
- safely insert SRAM chip into the on-board U4..U7 socket
- set J4 jumper in accordance with table 2-3 to meet the installed SRAM chip type
- switch on the power

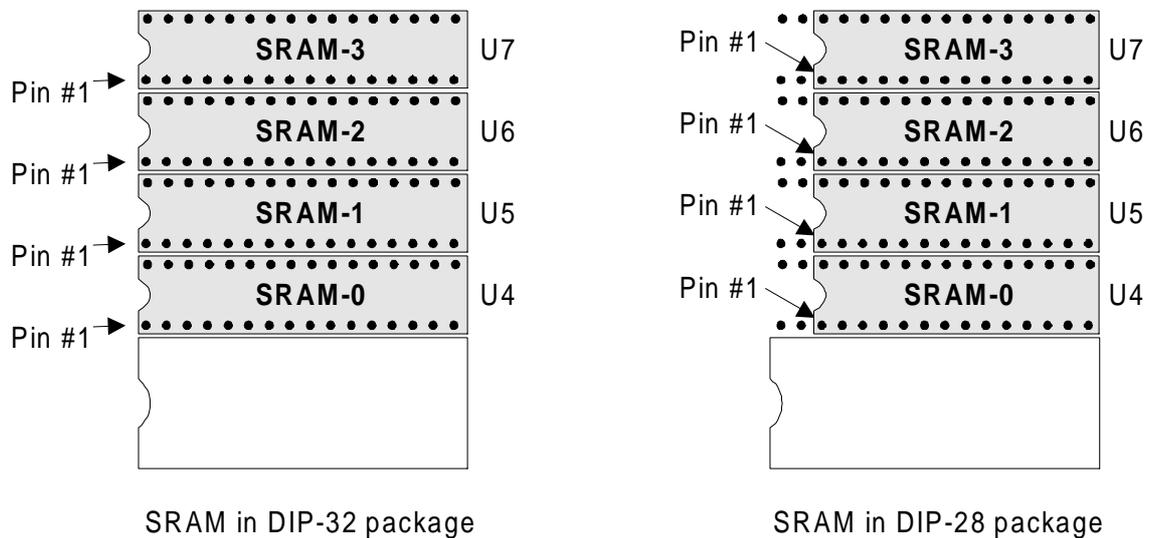


Fig.3-2. Installation of SRAM chips onto *TORNADO-E31* board.

### 3.3 Configuring *TORNADO-E31* board

Generally, the following first-time configuration efforts should be done prior usage and applying power to *TORNADO-E31* DSP controller (refer to fig.A-1 for on-board jumpers and connectors list):

- set up the TMS320C31 DSP bootmode configuration (jumper J1) in accordance with table 2-1
- install SRAM chips and set jumper J4 in accordance with the SRAM chip type
- install EPROM chip (if required) and set jumper J5 in accordance with the EPROM chip type
- configure jumper J6 in accordance with the function of XF0 I/O pin (refer to table 2-5)
- select appropriate RS232 or RS422/EIA-530 interface for each channel of USART and set configuration jumper J2 in accordance with tables 2-9 and 2-10
- connect power supply wires to power connector JP7
- connect RS232C or RS422/EIA-530 cables to connectors JP8..JP11 and digital I/O cable to connector JP10
- install SIOX and/or PIOX-16 daughter-card module(s)
- connect MPSD of external emulator to the MPSD-IN connector (JP1)
- switch on the power supply

# Appendix A. On-board Jumpers and Connectors.

This Appendix includes a summarized description for the *TORNADO-E31* on-board configuration jumpers, connectors and sockets.

Board layout for *TORNADO-E31* configuration jumpers and connectors is presented at fig.A-1.

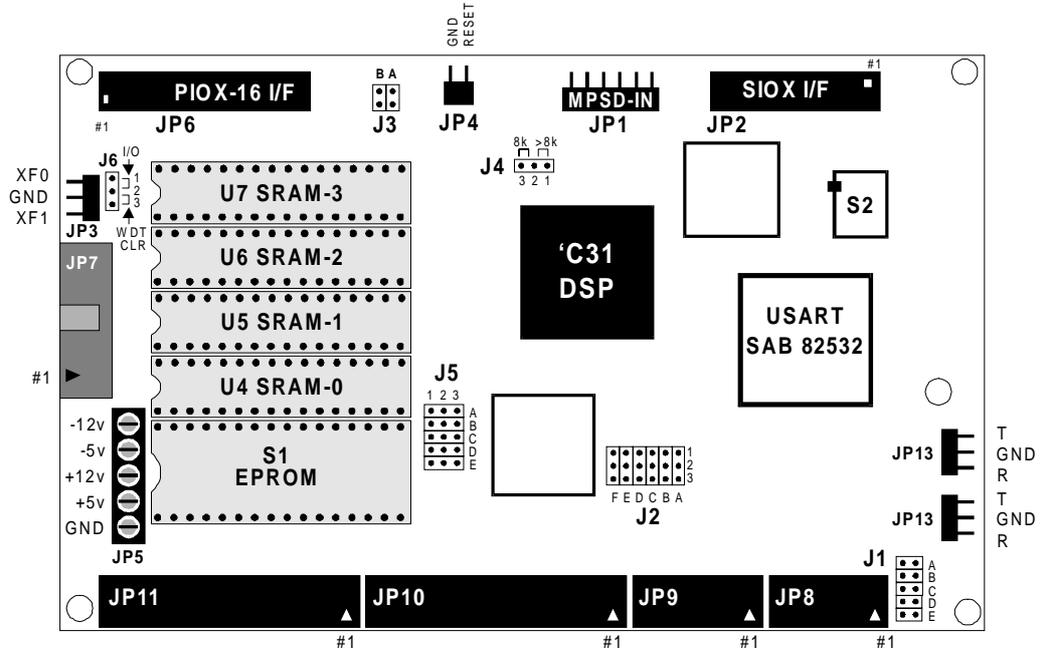


Fig.A-1. On-board layout for *TORNADO-E31*.

### On-board Configuration Jumpers

All on-board configuration jumpers for *TORNADO-E31* DSP controller are summarized in table A-1.

Table A-1. On-board configuration jumpers for *TORNADO-E31*.

jumper ID	jumper function description	reference information
J1 (J1-A..J1-E)	TMS320C31 DSP Bootmode configuration.	Section 2.2; table 2-1.

<i>J2</i> ( <i>J2-A..J2-F</i> )	External RS232C and RS422/EI-530 interface selector for USART channels "A" and "B".	Section 2.5; tables 2-9 and 2-10;. figures 2-10 and 2-11
<i>J3</i> ( <i>J3-A..J3-B</i> )	PIOX-16 wait state selector.	Section 2.3; table 2-7
<i>J4</i>	SRAM chip type selector.	Sections 2.2 and 3.3; table 2-3
<i>J5</i> ( <i>J2-A..J2-B</i> )	EPROM chip type selector.	Sections 2.2 and 3.2 table 2-4 figure 3-1
<i>J6</i>	DSP XF0 function configurator.	Section 2.2. table 2-5

### On-board Connectors

All on-board connectors for *TORNADO-E31* DSP controller are summarized in table A-2.

Table A-2. On-board connectors for *TORNADO-E31*.

Connector ID	connector function description	reference information
<i>JP1</i>	MPSD-IN connector for external emulator	Section 2.7
<i>JP2</i>	SIOX expansion interface site header.	Section 2.4 figure 2-8
<i>JP3</i>	DSP XF0/XF1 I/O connector	Sections 2.2 and 2.6 figure 2-13
<i>JP4</i>	External DSP Reset connector.	Section 2.2.
<i>JP5</i>	External power connector.	Section 3-1.
<i>JP6</i>	PIOX-16 expansion interface site header.	Section 2.3 figure 2-4
<i>JP7</i>	8-bit parallel digital I/O connector.	Section 2.6 figure 2-12
<i>JP8</i> <i>JP9</i>	RS232C interface connectors for channels "A" and "B" of USART.	Section 2.5 figure 2-11
<i>JP10</i> <i>JP11</i>	RS422/EIA-530 interface connectors for channels "A" and "B" of USART.	Section 2.5 figure 2-10.

JP12 JP13	Transmitter/receiver clock outputs for USART channels "A" and "B".	Section 2.5
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### **On-board Sockets**

All on-board sockets for *TORNADO-E31* DSP controller are summarized in table A-3.

*Table A-3. On-board sockets for TORNADO-E31.*

socket ID	socket function description	reference information
S1	EPROM chip socket	Sections 2.2 and 3-2
U4..U7	SRAM chips sockets	Sections 2.2 and 3-3



