

TORNADO-E2/6xxx

2nd Generation Stand-alone DSP Controllers with
Ultra-High Performance TI TMS320C6xxx DSP

User's Guide

covers:
TORNADO-E2/6713 rev.1A

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This user's guide contains description for *TORNADO-E2/6xxx* 2nd generation stand-alone controllers with ultra-high performance 32-bit TMS320C6xxx digital signal processors (DSP) from Texas Instruments Inc (TI).

This document does not include detail description neither for TI TMS320C6xxx DSP nor for the other on-board peripherals and the corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

- ***TMS320C6xxx Peripheral Reference Guide.*** Texas Instruments Inc, SPRU190D, 2001.
- ***TMS320C6000 CPU and Instruction Set.*** Texas Instruments Inc, SPRU189F, 2000.
- ***TMS320C6713 DSP Data Sheet.*** Texas Instruments Inc, SPRS294B, 2006.
- ***DS1501/DS1511 Watchdog Real-Time Clocks.*** Dallas Semiconductor, 2004.
- ***ST16C2550 Dual UART with 16-byte of Transmit and Receive FIFO's.*** Exar Corporation, 2000.
- ***USS-820/USS-825 USB Device Controller.*** Lucent Technologies, 1999.
- ***NET2272 USB 2.0 Peripheral Controller.*** NetChip Technology Inc, 2003.
- ***ISP1761 Hi-Speed USB On-The-Go Controller.*** Philips Electronics N.V., 2005.

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Contents

Chapter 1. Introduction	1
1.1 General Information	1
Overview	2
External communication interfaces	2
I/O expansion	3
Applications	3
1.2 Technical Specification	4
Chapter 2. System Architecture	7
2.1 TORNADO-E2/6xxx System Architecture	7
TMS320C6xxx DSP	10
Memory	10
External communication interfaces	10
Peripheral I/O interfaces	10
Serial I/O Expansion (SIOX) DCM sites	11
2 nd generation Parallel I/O Expansion (PIOX2) DCM site	11
Host Control Expansion (HCX) DCM site	11
Watch-dog timer (WDT)	11
Real-time clock (RTC) controller and external power supply control	11
DSP external interrupts and NMI	12
System controller	12
Debugging of TMS320C6x DSP Software	12
2.2 TMS320C6xxx DSP Environment	12
DSP endian mode	12
DSP operation modes and DSP bootmodes	12
DSP reset control	16
DSP on-chip PLL (TORNADO-E2/6713 only)	17
EMIF Spread Spectrum Clock option	18
DSP memory map	18
DSP EMIF registers settings	22
DSP speed grade ID	23
Synchronous burst static RAM (SBSRAM) memory area	23
Synchronous dynamic RAM (SDRAM) memory area	24
FLASH memory area	25
DSP external control registers area	29
Asynchronous and synchronous sections of Parallel I/O Expansion (PIOX2) DCM site interface	29
Synchronous section of HCX DCM site interface	29
Dual-channel UART	29
USB interface	30
Real-time clock (RTC) controller	30
On-board watch-dog timer (WDT)	31

<i>DSP on-chip timers</i>	31
<i>DSP on-chip serial peripherals (McBSP, McASP, I²C ports)</i>	32
<i>External General Purpose I/O (GPIO)</i>	37
<i>DSP external interrupt requests</i>	38
<i>DSP-to-HCX interrupt request</i>	39
<i>HCX-to-DSP interrupt request</i>	39
2.3 DSP external control registers area	40
<i>DSP_DSP_CNF_RG DSP external control register for identification of the DSP start-up configuration</i>	40
<i>DSP_DCM_CNF_RG DSP external control register for identification of installed DCM</i>	41
<i>DSP_SYS_CNF1_RG DSP external control register for identification of TORNADO-E2/6xxx DSP controller</i>	42
<i>DSP_SYS_CNF2_RG DSP external control register for identification of board revision, DSP clock frequency and EMIF spread spectrum clock presence</i>	43
<i>DSP_SYS_CNF3_RG DSP external control register for identification of on-board external DSP memories</i>	44
<i>DSP_SYS_CNF4_RG DSP external control register for identification of on-board external parallel peripherals</i>	45
<i>DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG, DSP_EXT_INT7_SEL_RG and DSP_NMI_SEL_RG DSP external control registers for selection of interrupt request source for DSP EXT_INT4..7 and NMI external interrupt requests</i>	46
<i>DSP_PORTS_CNTR_RG DSP external control register for on-board serial ports buffers configuration (TORNADO-E2/6713 only)</i>	47
<i>DSP_FLASH_PAGE_RG DSP external FLASH memory page control register</i>	49
<i>DSP_FLASH_CNTR_RG DSP external FLASH memory control register</i>	50
<i>DSP_WDT_RTC_CNTR_RG DSP external control register for WDT and RTC control</i>	52
<i>DSP_WDT_RESET_RG DSP external control register for WDT reset</i>	53
<i>DSP_GPIO_DIR_RG and DSP_GPIO_DATA_RG DSP external control registers for GPIO pins control</i>	53
<i>DSP_DCM_RESET_RG DSP external control register for reset control of PIOX2/SIOX/ASIOX DCM sites</i>	54
<i>DSP_SIOX_XIO_CNF_RG and DSP_SIOX_XIO_DATA_RG DSP external control registers for configuring DSP Timers/XIO pins</i>	55
<i>DSP_HCX_SYNC_PAGE_RG DSP external control register for address extension of synchronous HCX DCM site interface</i>	56
2.4 HCX DCM Site Interface	57
<i>General description of HCX DCM site interface</i>	57
<i>Enable and reset control for HCX DCM site interface</i>	58
<i>HCX control registers and address map for HCX-ASYNC interface</i>	59
<i>HCX_AX_SYS_CNF1_RG, HCX_AX_SYS_CNF2_RG, and HCX_AX_SYS_CNF3_RG read-only HCX control registers for board configuration information</i>	61
<i>HCX_AX_CNTR1_RG HCX control register for DSP reset control</i>	63
<i>HCX_AX_CNTR2_RG HCX control register for DSP start-up configuration control</i>	64
<i>DSP-to-Host interrupt requests via HCX-ASYNC interface</i>	66
<i>HCX_AX_INT_STAT_RG read-only HCX control register for status information of DSP-to-Host interrupt request sources via HCX-ASYNC interface</i>	67
<i>HCX_AX_HIRQ0_SEL_RG and HCX_AX_HIRQ1_SEL_RG registers for configuration of 32-bit asynchronous HCX DCM site interface interrupt request outputs</i>	67
<i>DSP on-chip HPI port area of HCX-ASYNC interface</i>	68
<i>Timeout control for access to DSP on-chip HPI port of HCX-ASYNC interface</i>	69
<i>HCX_AX_CLR_HPI_TMOUT_ERR_RG write-only HCX control register for clearing of HPI access timeout error flag</i>	71

Processing of DSP-to-host interrupt request via HCX-ASYNC interface	71
Generation of Host-to-DSP interrupt request via HCX-ASYNC interface	72
HCX-SYNC synchronous section of HCX DCM site interface	73
2.5 DSP Software Development Tools	73
Connection of external JTAG emulator to TORNADO-E2/6xxx on-board DSP	73
On-board JTAG path for connection to external JTAG emulator	74
Maximum JTAG clock frequency	74
Configuring TI Code Composer Studio TMS320C6xxx emulator drivers to debug TORNADO-E2/6xxx on-board DSP	75
Chapter 3. Installation and Configuration	77
3.1 Installation of TORNADO-E2/6xxx Controller in DSP Stand-alone Operation Mode	77
3.2 Installation of TORNADO-E2/6xxx Controller in DSP Host Operation Mode	77
Appendix A. On-board Switches and Connectors.	79
A.1 On-board Switches	80
A.2 On-board Connectors	80
JP1 external power connector	81
JP2 external DSP reset connector	82
JP3 JTAG emulator connector	82
JP8 and JP9 RS232C interface connectors	82
JP13 GPIO general purpose digital I/O connector	83
JP14, JP15 I ² C interface connectors	83
JP16 external power supply control connector	84
A.3 On-board Sockets	84
A.4 On-board LED Indicators	84
A.5 Physical Dimensions for TORNADO-E2/6xxx board	85
Appendix B. External Cable Sets for TORNADO-E2/6xxx DSP controllers	87
B.1 T/X-JTAG/C1 JTAG Converter Cable	87
B.2 T/X-UART/C1 RS232C Interface Converter Cable	87
Appendix C. Serial I/O Expansion DCM Sites (SIOX and ASIOX)	89
C.1 General Description	89
Installation of SIOX rev.B and ASIOX rev.D DCMs onto TORNADO-E2/6xxx board	89
C.2 Technical Description	90
SIOX rev.B DCM site connector	90
ASIOX rev.D DCM site connector	92
Maximum serial data transfer speed for SIO-0/1 serial ports of SIOX DCM sites	97
DSP Timer/I/O pins	97
Generating Reset Signal for SIOX DCM Sites	97
ASIO-0/1 audio serial ports of TORNADO-E2/6713 ASIOX rev.D DCM site interface	97
Asynchronous parallel interface of ASIOX rev.D site	98
Data Transfer Timing for asynchronous parallel interface of ASIOX rev.D DCM Site	98
C.3 Physical Dimensions for SIOX and ASIOX DCMs	99
Appendix D. P/OX2 DCM Site Interface	101

D.1	General Description	101
	<i>Installation of PIOX-16 and PIOX-32 rev.1 DCMs into PIOX2 rev.2 DCM site</i>	101
D.2	PIOX2 DCM Site Interface Connector and Signals	102
	<i>Asynchronous section of PIOX2 DCM site interface</i>	102
	<i>Synchronous section of PIOX2 DCM site interface</i>	103
	<i>PIOX2 DCM site interface connectors and signals description</i>	103
	<i>Timing diagram for data transfers cycle via asynchronous section of PIOX2 DCM site interface</i>	107
	<i>Timing diagram for data transfers cycle via synchronous PIOX2 DCM site interface</i>	107
D.3	Physical Dimensions for PIOX2 DCM	109
Appendix E.	HCX DCM Site Interface	111
E.1	General Description	111
	<i>HCX DCM site interface</i>	111
	<i>HCX DCM installation</i>	112
Appendix F.	Software Utilities for TORNADO-E2/6xxx DSP controllers	113
F.1	Software Utilities for TORNADO-E2/6xxx on-board TMS320C6xxx DSP	113
F.2	TORNADO-E2/6xxx GEL-files for TI CCS TMS320C6xxx Debugger	114
Appendix G.	FLASH Memory Programming	115
G.1	Accessing FLASH Memory at TORNADO-E2/6xxx DSP controllers	115
	<i>FLASH memory capacity</i>	115
	<i>FLASH memory addressing</i>	115
	<i>FLASH memory write protection</i>	115
G.2	FLASH Chip Description	116
	<i>Command Definitions</i>	116
	<i>Reading Array Data</i>	119
	<i>Reset Command</i>	119
	<i>Autoselect Command Sequence</i>	119
	<i>Byte Program Command Sequence</i>	120
	<i>Unlock Bypass Command Sequence</i>	121
	<i>Chip Erase Command Sequence</i>	122
	<i>Sector Erase Command Sequence</i>	122
	<i>Erase Suspend/Erase Resume Commands</i>	123
	<i>WRITE Operation Status</i>	123
	<i>DQ7: Data# Polling</i>	124
	<i>DQ6: Toggle Bit I</i>	125
	<i>DQ2: Toggle Bit II</i>	126
	<i>Reading Toggle Bits DQ6/DQ2</i>	126
	<i>DQ5: Exceeded Timing Limits</i>	127
	<i>DQ3: Sector Erase Timer</i>	127
Appendix H.	Dual-channel UART (DUART)	129
H.1	General Description	129
	<i>Connection diagram</i>	129
	<i>DUART control registers set</i>	130

	<i>DUART source clock and the bit rate frequency</i>	131
	<i>DUART-to-DSP interrupt requests</i>	131
	<i>DUART-hardware reset</i>	131
	<i>RS232C interface connectors</i>	131
Appendix I. USB interface		133
I.1	General Description	133
I.2	Philips ISP1761 USB rev.2.0 Three-channel Host/Device Controller	133
	<i>ISP1761 internal architecture</i>	133
	<i>Connection diagram</i>	134
	<i>ISP1761 USB 2.0 controller registers set</i>	134
	<i>USB-to-DSP interrupt and DMA requests</i>	136
	<i>TORNADO-E2/6xxx on-board USB receptacle connectors</i>	137
	<i>Hardware reset for USB controller</i>	137
I.3	PLX/NetChip NET2272 USB 2.0 One-channel Device Controller	137
	<i>Connection diagram</i>	137
	<i>NET2272 USB 2.0 device controller registers set</i>	137
	<i>USB-to-DSP interrupt request</i>	139
	<i>TORNADO-E2/6xxx on-board USB receptacle connector</i>	139
	<i>Hardware reset for NET2272 USB controller</i>	139
I.4	Lucent Technologies USS-820 USB 1.1 One-channel Device Controller	139
	<i>Connection diagram</i>	140
	<i>USS-820 USB 1.1 device controller registers set</i>	140
	<i>USB-to-DSP interrupt request</i>	141
	<i>TORNADO-E2/6xxx on-board USB receptacle connector</i>	141
	<i>Hardware reset for USS-820 USB controller</i>	141
Appendix J. Real-time Clock (RTC) Controller		143
J.1	General Description	143
	<i>RTC backup battery</i>	143
	<i>RTC control register set</i>	143
	<i>RTC clock oscillator control</i>	144
	<i>RTC-to-DSP interrupts</i>	145
	<i>DSP reset control by RTC</i>	145
	<i>External power supply control</i>	145
Glossary of Terms		147
Index		155

Figures

Figure 1-1.	TORNADO-E2/6713 DSP controller.	1
Figure 1-2.	TORNADO-E2/6713 DSP controller with installed HCX DCM.	2
Figure 1-3.	TORNADO-E2/6713 DSP controller with SIOX rev.B and PIOX DCM installed.	3
Figure 2-1.	Block diagram of TORNADO-E2/6713.	8
Figure 2-2.	TORNADO-E2/6713 board.	9
Figure 2-3.	Interrupt request selectors for DSP EXT_INT4..7/NMI external interrupt request inputs of TORNADO-E2/6713 DSP controller.	39
Figure 2-4.	Timing diagram for normal termination of host-to-HPI access cycle.	70
Figure 2-5.	Timing diagram for termination of host-to-HPI access cycle on the timeout condition.	71
Figure 2-6.	Connection of external JTAG emulator to TORNADO-E2/6xxx on-board DSP.	74
Figure 2-7.	TORNADO-E2/6xxx DSP controllers on-board JTAG path for connection to external JTAG emulator.	74
Figure 3-1.	Installation of asynchronous-only HCX DCM into HCX DCM site of TORNADO-E2/6xxx.	78
Figure 3-2.	Installation of asynchronous/synchronous HCX DCM into HCX DCM site of TORNADO-E2/6xxx.	78
Figure A-1.	TORNADO-E2/6713 board layout.	79
Figure A-2.	Pinout of JP1 external power connector for TORNADO-E2/6713 board.	82
Figure A-3.	Pinout of JP2 external DSP reset input connector for TORNADO-E2/6713 board.	82
Figure A-4.	Pinout of JP3 JTAG emulator connector for TORNADO-E2/6713 board.	82
Figure A-5.	Pinout of JP8 and JP9 RS232C interface connectors for TORNADO-E2/6713 board.	83
Figure A-6.	Pinout of JP13 GPIO connector for TORNADO-E2/6713 board.	83
Figure A-7.	Pinout of JP14 and JP15 I ² C interface connectors for TORNADO-E2/6713 board.	84
Figure A-8.	Pinout of JP16 external power supply control connector for TORNADO-E2/6713 board.	84
Figure A-9.	Physical dimensions for TORNADO-E2/6xxx DSP controller board.	85
Figure B-1.	T/X-JTAG/C1 JTAG converter cable.	87
Figure B-2.	T/X-UART/C1 RS232C interface converter cable.	87
Figure B-3.	Connection diagram for T/X-UART/C1 RS232C interface converter cable.	88
Figure C-1.	TORNADO-E2/6713 board with SIOX rev.B DCM installed.	89
Figure C-2.	TORNADO-E2/6713 board with ASIOX rev.D DCM installed.	90

Figure C-3. Connection diagram for SIOX and ASIOX DCM site interfaces of TORNADO-E2/6713.	90
Figure C-4. Pinout for SIOX rev.B DCM site connector.	91
Figure C-5. ASIOX rev.D DCM site connector pinout (top view).	93
Figure C-6. Timing diagram for parallel data transfer via ASIOX rev.D DCM site.	99
Figure C-7. Physical dimensions of SIOX rev.B DCM.	99
Figure C-8. Physical dimensions of ASIOX rev.D DCM.	100
Figure D-1. PIOX2 DCM site at TORNADO-E2/6713 DSP controller board.	101
Figure D-2. TORNADO-E2/6713 board with PIOX-32 rev.1 DCM installed.	102
Figure D-3. Pinout of PIOX2 DCM site interface connector.	104
Figure D-4. Timing diagram of data transfer cycles via asynchronous section of PIOX2 DCM site interface of TORNADO-E2/6713.	107
Figure D-5. Timing diagram of data transfer cycles via synchronous section of PIOX2 DCM site interface of TORNADO-E2/6713.	108
Figure D-6. Physical dimensions for PIOX2 DCM with asynchronous-only interface (A) and PIOX2 DCM with full asynchronous-synchronous interfaces (B).	109
Figure E-1. HCX DCM site of TORNADO-E2/6713 board.	111
Figure G-1. Program Operation.	121
Figure G-2. Erase Operation.	122
Figure G-3. Data# Polling Algorithm.	125
Figure G-4. Toggle Polling Algorithm.	126
Figure H-1. Connection diagram for TORNADO-E2/6713 on-board DUART.	129
Figure I-1. Connection diagram for TORNADO-E2/6713 on-board ISP1761 USB controller.	134
Figure I-2. Connection diagram for TORNADO-E2/6713 on-board NET2272 USB controller.	137
Figure I-3. Connection diagram for TORNADO-E2/6713 on-board USS820 USB controller.	140
Figure J-1. Connection diagram for TORNADO-E2/6713 DSP controller on-board RTC.	143

Tables

<i>Table 1-1. Technical specifications for TORNADO-E2/6xxx DSP controllers.</i>	<i>4</i>
<i>Table 2-1. DSP Operation Modes and Bootmode Configurations for TORNADO-E2/6713.</i>	<i>14</i>
<i>Table 2-2. DSP memory map for TORNADO-E2/6713.</i>	<i>19</i>
<i>Table 2-3. Recommended settings for TMS320C6713 DSP on-chip EMIF control registers for TORNADO-E2/6713.</i>	<i>23</i>
<i>Table 2-4. FLASH memory page selection.</i>	<i>26</i>
<i>Table 2-5. FLASH write protection control.</i>	<i>27</i>
<i>Table 2-6. 64Mx8 FLASH 1st sector write protection control.</i>	<i>28</i>
<i>Table 2-7. TORNADO-E2/6713 on-board serial peripherals configurations.</i>	<i>33</i>
<i>Table 2-8. DSP_DSP_CNF_RG register bits.</i>	<i>41</i>
<i>Table 2-9. DSP_DCM_CNF_RG register bits.</i>	<i>42</i>
<i>Table 2-10. DSP_SYS_CNF1_RG register bits.</i>	<i>43</i>
<i>Table 2-11. DSP_SYS_CNF2_RG register bits.</i>	<i>43</i>
<i>Table 2-12. DSP_SYS_CNF3_RG register bits.</i>	<i>44</i>
<i>Table 2-13. DSP_SYS_CNF4_RG register bits.</i>	<i>45</i>
<i>Table 2-14. Interrupt request sources for DSP interrupt selectors of TORNADO-E2/6713 DSP controller.</i>	<i>46</i>
<i>Table 2-15. DSP_PORTS_CNTR_RG register bits for TORNADO-E2/6713.</i>	<i>48</i>
<i>Table 2-16. DSP_FLASH_PAGE_RG register bits.</i>	<i>49</i>
<i>Table 2-17. DSP_FLASH_CNTR_RG register bits.</i>	<i>51</i>
<i>Table 2-18. DSP_WDT_RTC_CNTR_RG register bits.</i>	<i>52</i>
<i>Table 2-19. DSP_GPIO_DIR_RG register bits.</i>	<i>53</i>
<i>Table 2-20. DSP_GPIO_DATA_RG register bits.</i>	<i>54</i>
<i>Table 2-21. DSP_DCM_RESET_RG register bits.</i>	<i>54</i>
<i>Table 2-22. DSP_SIOX_XIO_CNF_RG register bits.</i>	<i>55</i>
<i>Table 2-23. DSP_SIOX_XIO_DATA_RG register bits.</i>	<i>56</i>
<i>Table 2-24. DSP_HCX_SYNC_PAGE_RG register bits for TORNADO-E2/6713.</i>	<i>57</i>
<i>Table 2-25. Host HCX controller address map for HCX-ASYNC interface of TORNADO-E2/6713 DSP controller.</i>	<i>60</i>
<i>Table 2-26. HCX_AX_SYS_CNF1_RG register bits.</i>	<i>62</i>
<i>Table 2-27. HCX_AX_SYS_CNF2_RG register bits.</i>	<i>62</i>
<i>Table 2-28. HCX_AX_SYS_CNF3_RG register bits.</i>	<i>63</i>
<i>Table 2-29. HCX_AX_CNTR1_RG register bits.</i>	<i>63</i>
<i>Table 2-30. HCX_AX_CNTR2_RG register bits.</i>	<i>64</i>
<i>Table 2-31. HCX_AX_INT_STAT_RG register bits.</i>	<i>67</i>

<i>Table 2-32. HCX_AX_HIRQ0_SEL_RG and HCX_AX_HIRQ1_SEL_RG register bits.</i>	68
<i>Table A-1. On-board switches for TORNADO-E2/6713.</i>	80
<i>Table A-2. TORNADO-E2/6713 on-board connectors.</i>	80
<i>Table A-3. On-board sockets for TORNADO-E2/6713.</i>	84
<i>Table A-4. On-board LED indicators for TORNADO-E2/6713.</i>	85
<i>Table C-1. Signal description for SIOX rev.B DCM site interface.</i>	91
<i>Table C-2. Signal description for ASIOX rev.D DCM site connector.</i>	94
<i>Table D-1. Signal description for PIOX2 DCM site interface.</i>	105
<i>Table G-1. FLASH Command Definitions for 512Kx8, 1Mx8 and 8Mx8 FLASH memory chips.</i>	116
<i>Table G-2. FLASH Command Definitions for 64Mx8 FLASH memory chip.</i>	118
<i>Table G-3. Uniform Sector Address Table for 512Kx8 FLASH memory.</i>	120
<i>Table G-4. Uniform Sector Address Table for 64Mx8 FLASH memory.</i>	120
<i>Table G-5. Write Operation Status.</i>	124
<i>Table H-1. DSP memory map for accessing DUART control registers.</i>	130
<i>Table I-1. DSP memory map for on-chip registers of ISP1761 USB 2.0 controller for TORNADO-E2/6713 board.</i>	135
<i>Table I-2. DSP memory map for on-chip registers of NET2272 USB 2.0 controller for TORNADO-E2/6713 board.</i>	138
<i>Table I-3. DSP memory map for on-chip registers of USS-820 USB 1.1 controller for TORNADO-E2/6713 board.</i>	141
<i>Table J-1. Control register list for DS1501 RTC controller for TORNADO-E2/6713.</i>	144

Chapter 1. Introduction

This chapter contains general description for *TORNADO-E2/6xxx* 2nd generation stand-alone DSP controllers.

IMPORTANT NOTE

TORNADO-E2/6xxx DSP controllers have been designed to accommodate 32-bit TMS320C6xxx DSP from TI.

The particular DSP installed onto *TORNADO-E2/6xxx* DSP controller defines final name of this DSP controller, i.e. *TORNADO-E2/6713* (with TMS320C6713 DSP).

IMPORTANT NOTE

'*TORNADO-E2/6xxx*' notation denotes that the supplied information is applicable to all *TORNADO-E2/6xxx* DSP controllers.

'*TORNADO-E2/67xx*' notation denotes that the supplied information is applicable to all *TORNADO-E2/6xxx* DSP controllers with TMS320C67xx floating-point DSP.

Should the provided information be a product specific, then either the name of the corresponding product (*TORNADO-E2/6713*), or the name of the corresponding product group (*TORNADO-E2/67xx*) will be highlighted.

1.1 General Information

TORNADO-E2/6xxx DSP controllers are 2nd generation of *TORNADO-E* series of DSP controllers designed for ultra-high performance embedded DSP applications.

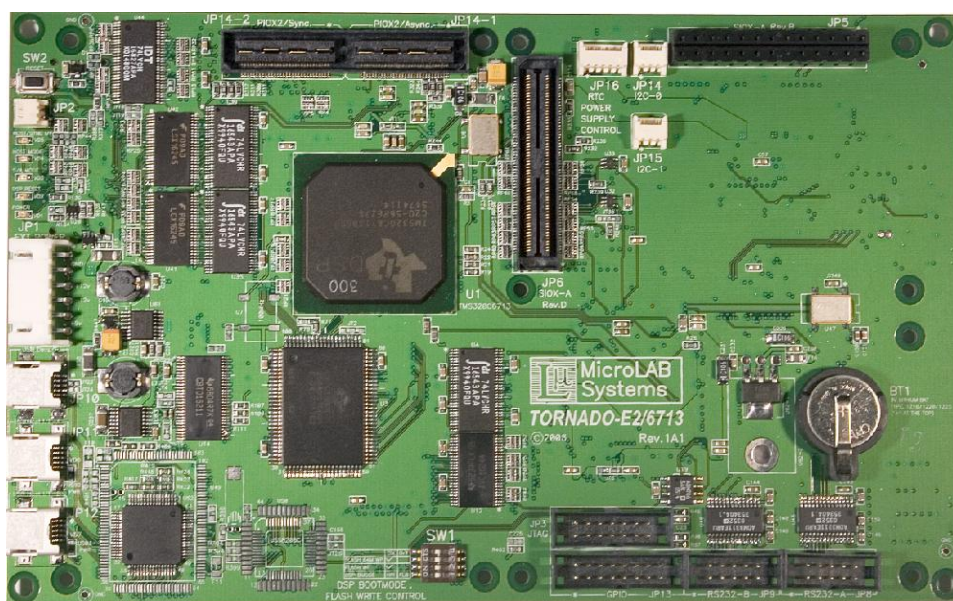


Figure 1-1. *TORNADO-E2/6713* DSP controller.

TORNADO-E2/6xxx comply industry-standard 3U form-factor and provide user expandable flexible modular system construction with daughter-card modules (DCM). All *TORNADO-E2/6xxx* DSP controllers feature compatible system architecture and compatible DSP environments in order to meet requirements for multiple applications while keeping a cost to a minimum. System architecture and construction of *TORNADO-E2/6xxx* are upward compatible upgrades for that of *TORNADO-E6xxx* product line, while adding a set of new powerful features.

TORNADO-E2/6xxx product line includes the following boards:

- *TORNADO-E2/6713* floating-point DSP controller ([Figure 1-1](#)).

TORNADO-E2/6xxx DSP controllers are designed for stand-alone applications, however they can be easily expanded with powerful host communication features and high-performance communication interfaces (Gigabit Ethernet, USB, etc) using optional host control expansion (HCX) DCM. [Figure 1-2](#) shows *TORNADO-E2/6713* DSP controller with installed HCX DCM.

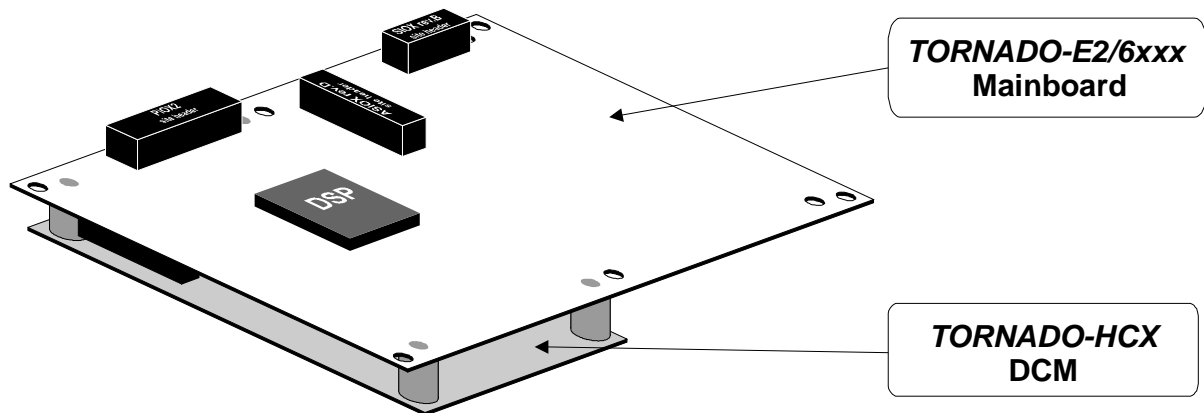


Figure 1-2. *TORNADO-E2/6713* DSP controller with installed HCX DCM.

Overview

TORNADO-E2/6xxx provide on-board ultra-high performance 32-bit TI TMS320C6xxx DSP:

- *TORNADO-E2/6713* DSP controller uses TI 32-bit floating-point TMS320C6713 DSP running at 300MHz and featuring 2400 MIPS and 1800 MFLOPS.

On-board memory includes up to 512Kx32 on-board synchronous burst static RAM (SBSRAM) for program and data, up to 16Mx32 on-board synchronous dynamic RAM (SDRAM) for program and data, and up to 64Mx8 on-board FLASH for boot code and non-volatile data.

TORNADO-E2/6xxx on-board industry-standard communication interfaces (UART, USB and I²C) are used to connect to external host PC, networks and peripherals.

Battery back-up RTC/calendar with external power supply control feature is included for timekeeping and time-scheduled power-saving stand-alone applications with activation of external power supply on programmable time events.

On-board peripherals also include general purpose 8-bit I/O and watchdog timer.

TORNADO-E2/6xxx DSP controllers have been designed with modular construction in mind and provide several on-board DCM sites for quick system reconfiguration using a variety of 'off-the-shelf' DCMs in order to meet customer application requirements for real-time I/O, digital radio, audio and many more.

External communication interfaces

TORNADO-E2/6xxx DSP controllers offer powerful set of industry-standard interfaces for communication with external host computers and peripherals:

- Dual-channel 384 kBaud UART (universal asynchronous receiver/transmitter) with external RS232C interfaces, which allows direct connections to host computers, modems, and peripherals using industry-standard asynchronous serial protocol.
- One of the following USB interface options (defined during board ordering):

- 480 Mbit/s USB rev.2.0 three-channel host/device interface, which offers connection to one host computer and two USB devices.
- 480 Mbit/s USB rev.2.0 single-channel device interface, which offers connection to one host computer.
- Legacy 12 Mbit/s USB rev.1.1 single-channel device interface, which offers connection to one host computers. This option is provided for backward compatibility with USB interface of *TORNADO-E6x* DSP controllers.
- Two I²C serial ports with 7-bit and 10-bit addressing modes and data transfer rates up to 400 kbps are used for connection to external peripherals.

I/O expansion

TORNADO-E2/6xxx DSP controllers provide several on-board DCM sites for optional I/O expansion using compatible DCMs:

- Serial I/O expansion (*SIOX*) DCM site (rev.B)
- Audio serial I/O expansion (*ASIOX*) DCM site (rev.D)
- 2nd generation Parallel I/O expansion (*PIOX2*) DCM site
- Host control expansion (*HCX*) DCM site (rev.A).

SIOX (serial I/O expansion) rev.B DCM site and *ASIOX* (audio serial I/O expansion) rev.D DCM site allow installation of one either *SIOX* rev.B or *ASIOX* rev.D DCM for real-time telecom, speech/fax/modem, professional audio, instrumentation, industrial applications. Legacy *SIOX* rev.B DCM site interface is standard for all *TORNADO-Exxx* stand-alone DSP controllers and comprises signals for DSP on-chip serial ports and timers. *ASIOX* rev.D DCM site is new for *TORNADO-E2/6xxx* and adds signals for DSP on-chip audio serial ports and 16-bit parallel asynchronous interface and allow professional audio and general purpose control applications.

TORNADO high-speed 2nd generation parallel I/O expansion (*PIOX2*) DCM site is used to install of *PIOX2* DCM. *PIOX2* DCM site interface comprises parallel asynchronous (compatible with legacy *PIOX* DCM site for *TORNADO-Exxx* DSP controllers) and synchronous interfaces for high-speed data transfers. A variety of ‘off-the-shelf’ *TORNADO PIOX* and *PIOX2* DCMs comprises AD/DA/DIO, application-specific and DSP coprocessor DCMs for real time multi-channel high-speed telecom, instrumentation, industrial, digital radio, etc signal processing applications.

TORNADO host control expansion (*HCX*) rev.A DCM site is used to install *HCX* DCM, which adds powerful host CPU and high-performance communication interfaces for post processing and connection to external computers, networks and peripherals.

[Figure 1-3](#) illustrates installation of different DCM at *TORNADO-E2/6713* DSP controller board.



Figure 1-3. *TORNADO-E2/6713* DSP controller with *SIOX* rev.B and *PIOX* DCM installed.

Applications

TORNADO-E2/6xxx stand-alone DSP controllers have been designed for high-performance embedded DSP applications with communication with external host computers/peripherals and real-time signal I/O. The following are only few of many applications for *TORNADO-E2/6xxx* DSP controllers:

- real-time general purpose DSP and analog signal acquisition
- embedded DSP with optional hosting & networking
- professional audio
- high-speed multichannel fax/modem communication
- multichannel vocoders and speech signal processing

- *cellular base stations*
- *computer telephony*
- *networking*
- *multimedia*
- *radars and sonars*
- *digital radio*
- *instrumentation and industrial*
- *biomedical signal processing and medical imaging*
- *evaluation and education*
- many more ...

1.2 Technical Specification

This section provides technical specifications for *TORNADO-E2/6xxx* DSP controllers.

Table 1-1. Technical specifications for *TORNADO-E2/6xxx* DSP controllers.

parameter description	parameter value
<i>DSP and on-board Memories</i>	
DSP type	300 MHz (2400MIPS, 1800 MFLOPS) TMS320C6713B (<i>TORNADO-E2/6713</i>)
static RAM (SBRAM) ¹⁾	128K/256K/512Kx32
synchronous dynamic RAM (SDRAM) ¹⁾	4M/16Mx32
FLASH memory capacity ¹⁾	512K/8M/64Mx8
FLASH memory write protection	via hardware and software
<i>Watchdog Timer (WDT) and DSP Reset Controller (RC)</i>	
WDT latency period	1.6 sec typ
duration of external reset input signal	>500 ns
duration of the output DSP reset signal	>0.2 sec
input signal levels for external DSP reset input	3v/5v TTL
<i>Dual-channel UART (DUART)</i>	
number of UART channels	2
external I/O electrical interface	RS232C
maximum communication speed	384 kBaud

USB Interface	
USB interface ¹⁾	<p>480 Mbit/s USB three-channel host/device interface (Host-Host-Device), meets USB rev.2.0 specifications, one USB Mini-'AB' type receptacle connector and two USB Mini-'A' type receptacle connectors</p> <p>480 Mbit/s USB one-channel device interface, meets USB rev.2.0 specifications, one USB Mini-'B' type receptacle connector</p> <p>12 Mbit/s USB one-channel device interface, meets USB rev.1.1 specifications, one USB Mini-'B' type receptacle connector</p>
Real-time clock (RTC)	
real-time clock	battery backed-up real-time clock with 2100 year calendar, programmable alarm interrupt and programmable watch-dog timer interrupt, external power supply control
I²C serial ports	
number of channels ¹⁾	2
maximum data transfer rate	400 kbps
supported addressing modes for each channel	7-bit and 10-bit
General Purpose I/O (GPIO)	
number of programmable GPIO pins	8
I/O signal level	3v/5v TTL
output load current	< 1.6 mA
I/O expansion sites for daughter-card modules (DCM)	
DCM sites	<p>one SIOX rev.B DCM site (3v/5v TTL)</p> <p>one ASIOX rev.D DCM site (3v/5v TTL)</p> <p>one PIOX2 DCM site (3v/5v TTL)</p> <p>one HCX rev.A DCM site (3v/5v TTL)</p>
JTAG Interface	
JTAG I/O signal levels	3v/5v TTL
Maximum JTAG clock frequency	30 MHz
Physical and Power	
Dimensions	3U (100x160 mm)
power supply voltages	<p>+5V for TORNADO-E2/6xxx on-board hardware,</p> <p>optional ±12V power supply inputs are routed to SIOX/PIOX2/HCX DCM sites only and are used upon installed DCM requirements</p>
power consumption	+5V@0.5A (t=+20°C)
external operating temperature	0°C .. +60°C

Notes: 1. This item is a configuration specific. Particular value/configuration/option of this item is specified during the product purchase. Call MicroLAB Systems for more information.

Chapter 2. System Architecture

This chapter contains technical description and programming reference for *TORNADO-E2/6xxx*.

IMPORTANT NOTE

This user's guide does not contain technical description and programming details for on-board TI TMS320C6xxx DSP.

For more details about TI TMS320C6xxx DSP refer to original TI datasheets and user's guides, which are available from www.ti.com.

2.1 *TORNADO-E2/6xxx* System Architecture

Block diagram and board construction of *TORNADO-E2/6xxx* DSP controllers are shown at [Figure 2-1](#) and [Figure 2-2](#) correspondingly.

TORNADO-E2/6xxx DSP controllers include the following on-board units:

- TI TMS320C6xxx DSP (TMS320C6713 DSP for *TORNADO-E2/6713*)
- synchronous burst static RAM (SBSRAM) for program and data
- synchronous DRAM (SDRAM) for program and data
- FLASH memory chip for DSP source boot code and/or non-volatile data
- dual-channel 384 kBaud UART, which supports ASYNC protocol
- one of the following USB interface options (defined during board ordering):
 - 480 Mbit/s USB rev.2.0 three-channel host/device interface with two industry-standard mini-‘A’ type and one industry-standard mini-‘AB’ type USB receptacle connectors
 - 480 Mbit/s USB rev.2.0 single-channel device interface with one industry-standard mini-‘B’ type USB receptacle connector
 - 12 Mbit/s USB rev.1.1 single-channel device interface with one industry-standard mini-‘B’ type USB receptacle connector (for backward compatibility with *TORNADO-E6x* stand-alone DSP controllers)
- battery back-up real-time clock (RTC) and calendar with external power supply controller
- two on-board I²C serial ports
- 8-bit general purpose I/O
- serial I/O expansion *SIOX* rev.B and *ASIOX* rev.D DCM sites
- 2nd generation parallel I/O expansion (*PIOX2*) DCM site
- host control expansion (*HGX*) DCM site
- watch-dog timer (WDT)
- system controller (SCU)
- DSP JTAG interface connector
- external RESET connector and on-board RESET switch
- external power supply connector.

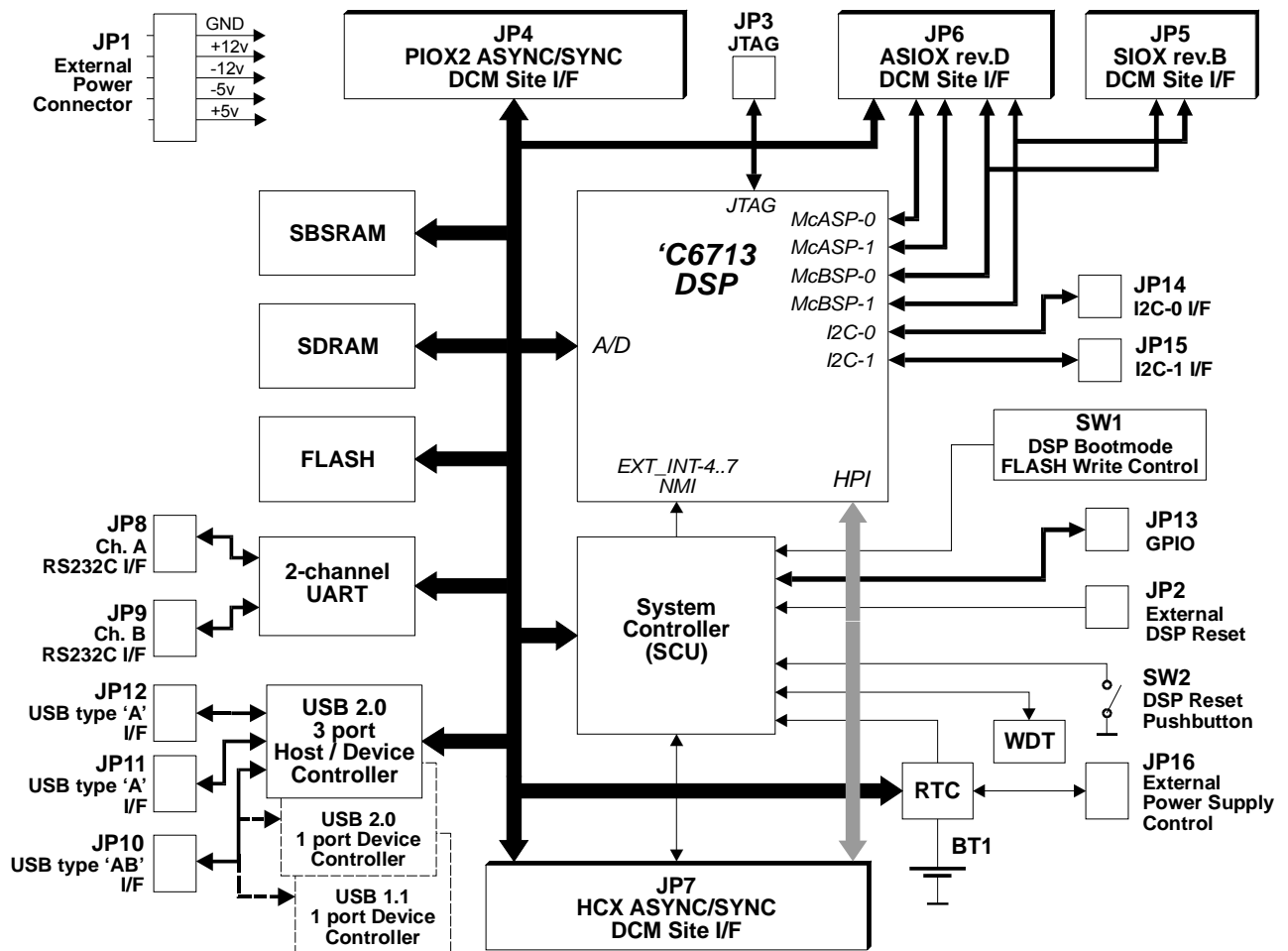
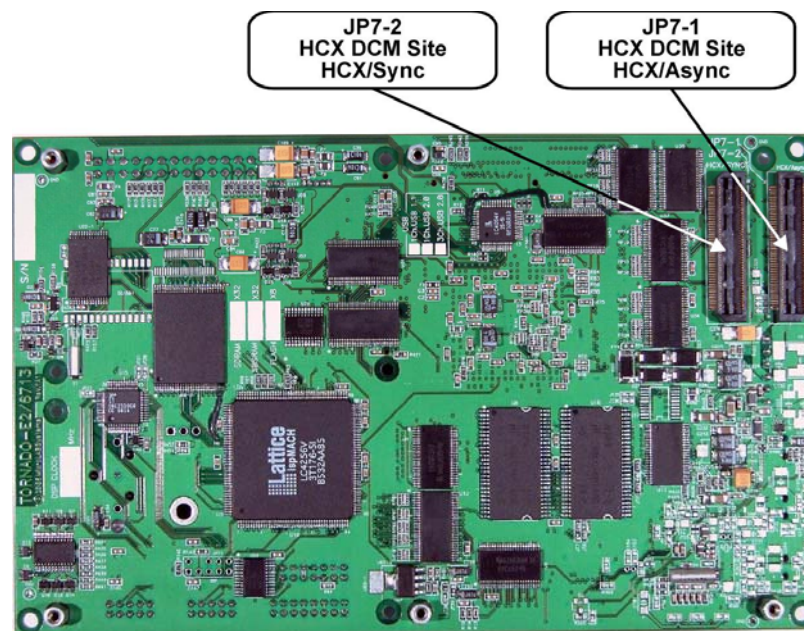
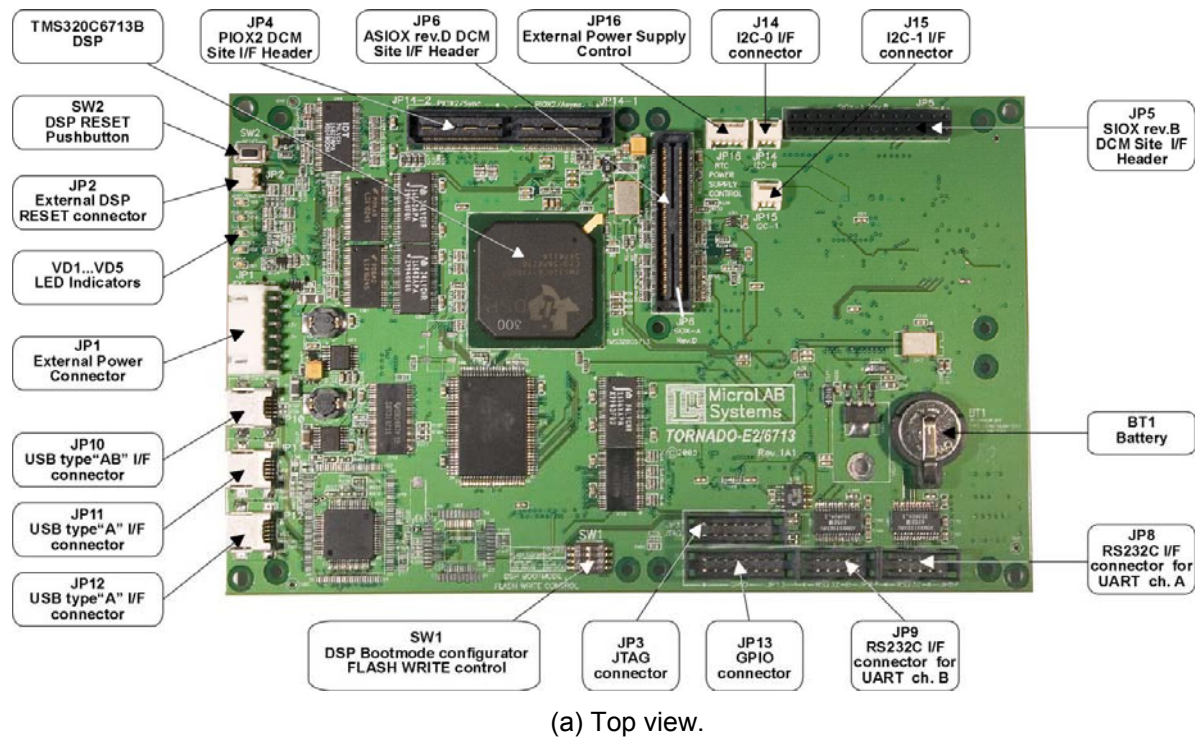


Figure 2-1. Block diagram of TORNADO-E2/6713.



(b) Bottom view.

Figure 2-2. TORNADO-E2/6713 board.

TMS320C6xxx DSP

TORNADO-E2/6xxx DSP controllers have been designed with TI fixed and floating-point TMS320C6xxx DSPs, which all feature code compatible advanced VelociTI very-long instruction word (VLIW) on-chip architecture and deliver ultra-high DSP performance :

- TORNADO-E2/6713 carries 300 MHz 32-bit floating-point TMS320C6713 DSP, which delivers 2400 MIPS and 1800 MFLOPS. TMS320C6713 DSP features on-chip 256 kbyte L2 memory shared between program and data spaces. DSP on-chip peripheral set includes two Multichannel Audio Serial Ports (McASPs), two Multichannel Buffered Serial Ports (McBSPs), two Inter-Integrated Circuit (I²C) buses and two general-purpose timers. High-speed DSP external parallel memory interface (EMIF) is used to access external SBSRAM, SDRAM and FLASH memories and external parallel peripherals (DUART, USB, RTC controllers, etc). For external host control, TMS320C6713 DSP provides on-chip host port interface (HPI).

NOTE

For more details about TI TMS320C6xxx DSP refer to original TI datasheets and user's guides, which are available from www.ti.com.

TORNADO-E2/6xxx architecture has been designed to deliver user access to all DSP on-chip peripherals via on-board DCM sites and to benefit from high DSP performance when accessing on-board memory resources.

For details about TORNADO-E2/6xxx on-board DSP environment refer to section "[TMS320C6xxx DSP Environment](#)" below.

Memory

TORNADO-E2/6xxx DSP controllers provide large on-board memory pool:

- up to 512Kx32 synchronous burst static RAM (SBSRAM) for TMS320C6xxx DSP program and data (refer to subsection "[Synchronous burst static RAM \(SBSRAM\) memory area](#)" below);
- up to 16Mx32 of synchronous dynamic RAM (SDRAM) for DSP program and data (refer to subsection "[Synchronous dynamic RAM \(SDRAM\) memory area](#)" below);
- up to 64Mx8 of FLASH memory for DSP boot code and/or for non-volatile data (refer to subsection "[FLASH memory area](#)" below).

External communication interfaces

TORNADO-E2/6xxx DSP controllers provide on-board industry-standard interfaces for communication with external peripherals:

- dual-channel UART (DUART) with RS232C interfaces is included for interfacing to external peripherals and for communication with host computer using asynchronous protocol and RS232C interface (refer to subsection "[Dual-channel UART](#)" below)
- one of the following USB interface options (defined during board ordering) (refer to subsection "[USB interface](#)" below):
 - 480 Mbit/s USB rev.2.0 three-channel host/device interface with two industry-standard mini-'A' type and one industry-standard mini-'AB' type USB receptacle connectors, which offers connection to one host PC and two USB devices;
 - 480 Mbit/s USB rev.2.0 single-channel device interface with one industry-standard mini-'B' type USB receptacle connector, which offers connection to one host PC;
 - 12 Mbit/s USB rev.1.1 one-channel device interface with one industry-standard mini-'B' type USB receptacle connector, which offers connection to one host PC.

Peripheral I/O interfaces

TORNADO-E2/6xxx DSP controllers provide two DSP on-chip I²C serial ports, which support both master and slave functionality, and general purpose 8-bit I/O (GPIO), which can be used as external control I/O signals.

For more details about *TORNADO-E2/6xxx* on-board I²C serial ports and general purpose I/O refer to subsections “[DSP on-chip serial peripherals \(McBSP, McASP, I2C ports\)](#)” and “[External General Purpose I/O \(GPIO\)](#)” below.

Serial I/O Expansion (SIOX) DCM sites

TORNADO-E2/6xxx on-board *SIOX* DCM sites pool includes one *SIOX* rev.B DCM site and one *ASIOX* rev.D DCM site, and is used for alternative installation of one compatible either *SIOX* rev.B or *ASIOX* rev.D DCM.

A variety of ‘off-the-shelf’ *SIOX* and *ASIOX* DCMs include DCMs for telecom, speech/fax/modem, professional audio, and many more applications.

Both *SIOX* and *ASIOX* DCM site interfaces use high-speed serial data transfer via DSP on-chip serial peripherals at speeds up to 100 Mbit/s. *SIOX* DCM site is used to transfer data via DSP on-chip McBSP ports only and is therefore used for telecom and instrumentation applications. *ASIOX* DCM site interface is a further enhancement for *SIOX* and adds data transfer possibility via DSP on-chip McASP ports and simple parallel asynchronous interface thus extending applications to multi-channel professional audio, telecom coprocessors and many more.

For more details about the on-board *SIOX* and *ASIOX* DCM sites refer to [Appendix C](#).

2nd generation Parallel I/O Expansion (PIOX2) DCM site

TORNADO-E2/6xxx DSP controllers feature *PIOX2* DCM site for installation of *PIOX2* high-speed AD/DA/DIO and application specific DCMs.

PIOX2 comprises parallel asynchronous and synchronous interfaces. Asynchronous interface is compatible with legacy 1st generation *TORNADO PIOX* interface. Adapters boards are available for installation of 1st generation *PIOX* DCMs with *TORNADO-E2/6xxx* DSP controllers.

PIOX2 synchronous interface runs at DSP EMIF clock and allows high-speed synchronous data transfers between on-board DSP and synchronous DCMs.

For more details about the on-board *PIOX2* DCM site interface refer to [Appendix D](#).

Host Control Expansion (HCX) DCM site

TORNADO-E2/6xxx controllers have been designed with powerful host control expansion in mind via *HCX* rev.A DCM site. In case the *HCX* DCM is installed, then it grabs host interface of *TORNADO-E2/6xxx* on-board DSP and offers a pool of high performance external communication interfaces (Ethernet, USB, etc) thus unloading the on-board DSP from time consuming external data transfer tasks.

For more details about *HCX* DCM site refer to section “[HCX DCM Site Interface](#)” later in this chapter and to [Appendix E](#) of this user guide.

Watch-dog timer (WDT)

TORNADO-E2/6xxx provides on-board watch-dog timer (WDT) for reliable application functionality. As long as DSP application runs correctly with the WDT feature enabled, then the DSP must periodically reset WDT, otherwise WDT will generate a DSP reset signal and restart *TORNADO-E2/6xxx*.

For more details about *TORNADO-E2/6xxx* on-board WDT refer to subsection “[On-board watch-dog timer \(WDT\)](#)” below.

Real-time clock (RTC) controller and external power supply control

TORNADO-E2/6xxx DSP controllers provide on-board battery back-up real-time clock (RTC) with built-in 2100 year calendar, 256 bytes of user NvRAM for non-volatile data, programmable alarm, and programmable watch-dog timer.

RTC is also used for external power supply control in order to activate external power supply on programmable wakeup event or kickstart condition.

For more details about *TORNADO-E2/6xxx* on-board RTC and external power supply control refer to “[Real-time clock \(RTC\) controller](#)” and [Appendix J](#).

DSP external interrupts and NMI

TORNADO-E2/6xxx DSP controllers feature multi-source software configurable DSP external interrupts and NMI. Interrupt sources comprise interrupt requests from *SIOX*, *ASIOX*, *PIOX2* and *HCX* DCM sites, and on-board interfaces and peripheral controllers.

For more details about TORNADO-E2/6xxx DSP software configurable external interrupts refer to subsection “[DSP external interrupt requests](#)” below.

System controller

On-board system controller unit (SCU) includes a set of configuration and control registers, which are used to control on-board DSP and DSP environment (refer to section “[DSP external control registers area](#)”).

Debugging of TMS320C6x DSP Software

TMS320C6xxx DSP software for TORNADO-E2/6713 can be debugged using MicroLAB Systems *MIRAGE* and TI JTAG emulators using industry standard TI C6000 Code Composer Studio IDE tools.

2.2 TMS320C6xxx DSP Environment

TORNADO-E2/6xxx DSP controllers utilize state of the art TMS320C6xxx ultra-high performance 32-bit DSPs from TI:

- 2400 MIPS and 1800 MFLOPS 32-bit floating-point TMS320C6713 DSP in TORNADO-E2/6713 running at 300 MHz.

IMPORTANT NOTE

This user's guide does not contain description and programming details for on-board TI TMS320C6xxx DSP.

For more information refer to original TI datasheets and user's guides for TMS320C6xxx DSP, which are provided in electronic form along with this user's guide.

DSP endian mode

TORNADO-E2/6xxx DSP controllers have been designed for little-only endian mode of on-board TMS320C6xxx DSP. Big endian mode for on-board TMS320C6xxx DSP is not supported.

DSP operation modes and DSP bootmodes

TORNADO-E2/6xxx on-board DSP can be configured to run in either *Stand-alone operation mode* or *Host operation mode*. DSP operation mode is defined by the fact of installation of compatible *HCX* DCM, i.e. in other words whether on-board DSP is either hosted by *HCX* DCM, or runs without host control.

DSP stand-alone operation mode is automatically selected in case no compatible *HCX* DCM is installed onto TORNADO-E2/6xxx board. In this mode DSP must perform communication with external host PC or other equipment via on-board UARTs and/or USB interfaces. In this mode the *HCX* interface of TORNADO-E2/6xxx is disabled thus enabling all DSP on-chip serial peripherals, and DSP can boot either from on-board FLASH memory or in debug emulator mode. This mode is useful for true embedded applications of TORNADO-E2/6xxx, which do not require intensive communication between on-board DSP and host PC and when real-time data flow is localized within the DSP environment.

In case compatible *HCX* DCM is installed onto TORNADO-E2/6xxx board, then *DSP host operation mode* is automatically selected. The *HCX* DCM adds a set of high-performance communication interfaces for real-time data transfer to host PC or network and offloads DSP from external communication tasks thus allowing a DSP application to benefit from maximum DSP performance. In this mode, the DSP can boot either from on-board FLASH memory or via DSP HPI port. For TORNADO-E2/6713 boards with TMS320C6713 DSP, the DSP on-chip HPI port can be disabled in *DSP host operation mode* via host *HCX* controller application in order to allow DSP applications, which make use of both McASP-0

and McASP-1 DSP on-chip audio serial ports. *DSP host operation mode* is useful for applications, which require intensive communication between the on-board DSP and host PC with real-time data flow spreading outside the DSP environment.

NOTE

The DSP operation mode ID is available via read-only *DSP_OPMODE* bit of [DSP_DSP_CNF_RG](#) DSP external control register ([Table 2-8](#)) for on-board DSP software.

NOTE

The DSP bootmode ID is available via read-only *DSP_BMODE* bit of [DSP_DSP_CNF_RG](#) DSP external control register ([Table 2-8](#)) for on-board DSP software.

[Table 2-1](#) lists all DSP operation modes and available DSP bootmode configurations.

For *DSP stand-alone operation mode*, the DSP bootmode is selected via on-board SW1-1 switch ([Figure 2-2](#) and [Figure A-1](#)).

NOTE

In the *DSP stand-alone operation mode*, the DSP bootmode is selected via on-board SW1-1 switch as long as DSP is held in the reset state.

As soon as DSP is released from the reset state, the on-board logic latches selected DSP bootmode and all further changes of SW1-1 switch are ignored until DSP is returned back into the reset state.

SA/BMODE-NONE DSP bootmode corresponds to the DSP no boot mode and is used to debug the DSP software via external JTAG emulator. For *TORNADO-E2/6713* board with TMS320C6713 DSP this bootmode corresponds to the *DSP EMULATION BOOT* in accordance with TI documentation for TMS320C6713 DSP. After DSP reset signal is released, the DSP kernel is held in the reset state. These guarantees that the DSP kernel will not get into unknown state in case there is no valid executable code in the DSP memory thus allowing safe and correct DSP JTAG debugger start.

CAUTION

In case the *SA/BMODE-NONE* DSP bootmode is selected for *TORNADO-E2/6713* board without JTAG emulator connected, then the DSP kernel will remain in the reset state after the DSP reset signal is released. DSP kernel will not start until JTAG emulator is connected and debugger is run.

Table 2-1. DSP Operation Modes and Bootmode Configurations for TORNADO-E2/6713.

SW1-1 switch	DSP_BMODE bit of HCX_AX_CNTR2_RG register ²⁾	DSP_HPI_EN bit of HCX_AX_CNTR2_RG register ²⁾	Read-only DSP_BMODE bit of DSP_DSP_CNF_RG registers	Read-only DSP_OPMODE bit of DSP_DSP_CNF_RG registers	DSP bootmode ID	Description
DSP STAND-ALONE OPERATION MODE (HCX DCM is not installed)						
ON	-	-	0	0	SA/BMODE-NONE	Corresponds to the <i>DSP stand-alone operation</i> with DSP no boot mode. This mode shall be used for DSP software debugging only with JTAG emulator connected.
OFF	-	-	1	0	SA/BMODE-FLASH8	Corresponds to the <i>DSP stand-alone operation mode</i> with DSP boot from on-board 8-bit FLASH memory.
DSP HOST OPERATION MODE (HCX DCM is installed)						
x	0	0	0	1	HOST/BMODE-NONE	Corresponds to the <i>DSP host operation mode</i> with HPI port disabled and DSP no boot mode. This mode shall be used for DSP software debugging only with JTAG emulator connected.
x	0	1	0	1	HOST/BMODE-HPI	Corresponds to the <i>DSP host operation mode</i> with boot via DSP on-chip HPI port. HPI port is enabled.
x	1	X	1	1	HOST/BMODE-FLASH8	Corresponds to the <i>DSP host operation mode</i> with DSP boot from on-board 8-bit FLASH memory. DSP on-chip HPI port can be either enabled or disabled via DSP_HPI_EN bit of HCX_AX_CNTR2_RG HCX control register.

Notes:

1. Highlighted configuration for *DSP stand-alone operation mode* corresponds to default factory setting. Highlighted configuration for *DSP host operation mode* sets as default on the HCX DCM reset and during power-on conditions.
2. The [DSP_BMODE](#) and [DSP_HPI_EN](#) bits of [HCX_AX_CNTR2_RG](#) register of HCX interface are available in the *DSP host operation mode* and can be written only while DSP is held in the reset state.

SA/BMODE-FLASH8 DSP bootmode is used for true stand-alone embedded applications of TORNADO-E2/6xxx with the DSP boot from on-board 8-bit FLASH memory on power on and without JTAG emulator connector. After DSP reset signal is released, the 1 kbyte long FLASH memory contents at 000000H FLASH address is transferred to the DSP on-chip memory at 00000000H address and execution starts at 00000000H address.

NOTE

In case TMS320C6xxx DSP application is written using 'C' programming language, then the size of the output binary module (code and data) may easily exceed the 1 kbyte.

In this case the first 1 kbyte area of FLASH memory must contain an executable for user designed secondary bootloader, which is used to load main DSP application into the DSP environment. TI provides code samples for such bootloader.

For *DSP host operation mode*, the DSP bootmode is selected by host *HCX* controller software via *DSP_BMODE* and *DSP_HPI_EN* bits of [HCX_AX_CNTR2_RG](#) *HCX* control register of *HCX* interface.

NOTE

In *DSP host operation mode*, the DSP bootmode is set by *HCX* controller software via the *DSP_BMODE* and *DSP_HPI_EN* bits of [HCX_AX_CNTR2_RG](#) *HCX* control register ([Table 2-30](#)) of *HCX* interface only while DSP is held in the reset state, i.e. when the *DSP_RUN* bit of [HCX_AX_CNTR1_RG](#) *HCX* control register ([Table 2-29](#)) is set to the '0' state.

As soon as *HCX* controller releases DSP from the reset state by setting the *DSP_RUN* bit of [HCX_AX_CNTR1_RG](#) *HCX* control register of *HCX* interface into the '1' state, then all further writes to the *DSP_BMODE* and *DSP_HPI_EN* bits of [HCX_AX_CNTR2_RG](#) *HCX* control register are ignored.

Read-back of the DSP bootmode ID is always available for *HCX* controller software via the *DSP_BMODE* and *DSP_HPI_EN* bits of [HCX_AX_CNTR2_RG](#) *HCX* control register, and is also available for on-board DSP application via the *DSP_BMODE* and *DSP_HPI_EN* bits of [DSP_DSP_CNF_RG](#) DSP external control register ([Table 2-8](#)).

HOST/BMODE-NONE DSP bootmode is valid for *TORNADO-E2/6713* board only and must be used with caution and only for debugging DSP executable with JTAG emulator connected. The DSP on-chip HPI port is disabled via *DSP_HPI_EN* bit of [HCX_AX_CNTR2_RG](#) *HCX* control register. This bootmode corresponds to the *DSP EMULATION BOOT* in accordance with TI documentation for TMS320C6713 DSP.

CAUTION

In case the *HOST/BMODE-NONE* DSP bootmode is set for *TORNADO-E2/6713* board without JTAG emulator connected, then the DSP kernel will remain in the reset state after the DSP reset signal is released. DSP kernel will not start until JTAG emulator is connected and debugger is run.

After DSP reset signal is released by host *HCX* application, the DSP kernel will be held in the reset state. These guarantees that the DSP kernel will not get into unknown state in case there is no valid executable code in the DSP memory thus allowing safe and correct DSP JTAG debugger start. Since DSP on-chip HPI port is disabled, then host *HCX* application cannot upload DSP executable into the DSP environment, so this can be done via DSP JTAG debugger only.

HOST/BMODE-HPI DSP bootmode is used to upload DSP executable into the DSP environment via DSP on-chip HPI port. HPI port is enabled via *DSP_HPI_EN* bit of [HCX_AX_CNTR2_RG](#) *HCX* control register. After DSP reset signal is released, the DSP kernel will be held in the reset state while the remainder of the DSP device is functional, including the DSP on-chip HPI port and EMIF external memory interface. *HCX* application can access entire on-board DSP environment including the DSP on-chip and off-chip memories and peripherals in order to upload executable code and data into the DSP environment. The DSP kernel is released from the reset state and DSP application starts execution from the DSP memory

address 00000000H as soon as host *HCX* application sets the *DSPINT* bit of DSP on-chip *HPIC* register (either *HCX_AX_HPI32_DSP_HPIC_RG*, or *HCX_AX_DSP_HPIC_LSW_RG* and *HCX_AX_DSP_HPIC_MSW* registers of *TORNADO-E2/6xxx* *HCX* interface, refer to subsection “[DSP on-chip HPI port area of HCX-ASYNC interface](#)” later in this chapter for more details). Note, that the *HOST/BMODE-HPI* DSP bootmode is the only way to upload the DSP code and data from *HCX* application into the DSP environment.

NOTE

When accessing the DSP off-chip memory areas (SBSRAM, SDRAM, FLASH) and DSP external control registers area from host *HCX* application in the *HOST/BMODE-HPI* DSP bootmode, it is required that host *HCX* software previously configures all DSP on-chip EMIF and PLL control registers via DSP HPI port in accordance with the [Table 2-3](#) and recommendations below.

HOST/BMODE-FLASH8 DSP bootmode is used to boot the DSP code and data from on-board FLASH memory on release of the DSP reset signal. DSP on-chip HPI port can be either enabled or disabled upon application requirements via *DSP_HPI_EN* bit of [HCX_AX_CNTR2_RG](#) *HCX* control register. As soon as the DSP reset signal is released, the 1 kbyte long FLASH memory area at 000000H FLASH address is transferred to the DSP on-chip memory at 00000000H address and DSP starts execution at 00000000H address.

NOTE

In case TMS320C6xxx DSP application is written using ‘C’ programming language, then the size of the output binary module (code and data) may easily exceed the 1 kbyte.

In this case the first 1 kbyte area of FLASH memory must contain an executable for user designed secondary bootloader, which is used to load main DSP application into the DSP environment. TI provides code samples for such bootloader.

Refer to the original TI TMS320C6xxx DSP documentation for more details about the DSP bootmodes.

DSP reset control

Generation of reset signal for *TORNADO-E2/6xxx* on-board DSP is different for different DSP operation modes.

For the *DSP stand-alone operation mode*, the DSP reset signal is defined as a logical OR of the following conditions:

- External +5V power on and power off conditions.
- On-board SW2 reset pushbutton is pressed on ([Figure 2-2](#) and [Figure A-1](#)).
- Active low external DSP reset input is applied via on-board JP2 connector (minimum duration of external reset signal is 500 ns).
- WDT is expired in case the WDT feature is enabled via [DSP_WDT_RTC_CNTR_RG](#) DSP external control register.
- In case on-board RTC is installed, then DSP reset is activated on power-on and power-off conditions, and on WDT expiration event, in case RTC on-chip WDT is enabled.

Any combination of the above conditions results in generation of DSP reset signal. As soon as all of the above conditions get false, the DSP reset signal is released after approximately 0.2 sec.

For the *DSP host operation mode*, the DSP reset signal is controlled exclusively by host *HCX* application software via *DSP_RUN* bit of [HCX_AX_CNTR1_RG](#) *HCX* control register (refer to [Table 2-26](#) for more details), and there is no delay on release of the DSP reset signal. In this mode, WDT is disabled and on-board SW2 and JP2 connector are not used for generation of the DSP reset signal.

The on-board VD2 LED indicator (refer to [Figure 2-2](#) and [Figure A-1](#)) is provided for visual indication of a current state of the DSP reset signal.

DSP on-chip PLL (TORNADO-E2/6713 only)

Some of *TORNADO-E2/6xxx* controllers are using the on-board TMS320C6xxx DSP, which has on-chip software programmable PLL circuit. The following is a list of applicable *TORNADO-E2/6xxx* controllers:

- *TORNADO-E2/6713* controller with TMS320C6713 DSP.

DSP on-chip software-programmable PLL delivers extra flexibility for system design and is used to generate individual clocks for different DSP on-chip units (DSP core, peripheral data bus, EMIF, McASPs, etc) from DSP input clock as it is required by particular application.

NOTE

For *TORNADO-E2/6713* the DSP input clock is 50 MHz.

As default, DSP on-chip PLL is disabled on the DSP reset condition and on-chip clocks are derived directly from the DSP input clock by means of dividing the DSP reference clock without its multiplication and thus not delivering maximum of the DSP performance. For example, *TORNADO-E2/6713* DSP controller with TMS320C6713 DSP and DSP input reference clock 50 MHz, sets the DSP core clock to 50 MHz, the DSP EMIF clock to 25 MHz, the McASP high-frequency clock source to 50 MHz, and other DSP on-chip peripherals clock source to 25 MHz on the DSP reset condition. In order to benefit from maximum DSP performance, the DSP on-chip PLL must be programmed after DSP reset.

NOTE

For *TORNADO-E2/6713* with TMS320C6713 DSP, the DSP on-chip PLL registers shall be programmed to set the DSP core clock to 300 MHz, the EMIF clock to 100 MHz, the McASP high-frequency clock to 50 MHz, and other DSP on-chip peripherals clock to 150 MHz.

The TMS320C6713 DSP on-chip PLL must be allowed about 200uS to lock.

IMPORTANT NOTE

The DSP on-chip PLL control registers shall be modified either by the DSP application or via JTAG emulator from the DSP debugger. DSP on-chip HPI port shall not be used to directly access the DSP PLL controller registers while DSP application is running.

IMPORTANT NOTE

It is recommended, that the DSP on-chip PLL controller registers for *TORNADO-E2/6713* controller are not directly configured from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user's guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

For more information about TMS320C6xxx DSP on-chip PLL refer to the corresponding original TI datasheets, which are provided in electronic form along with this user's guide.

EMIF Spread Spectrum Clock option

TORNADO-E2/6xxx controllers can use optional Spread Spectrum Clock as the DSP EMIF clock. Spread Spectrum clock features narrow band modulation of central clock frequency thus spreading an energy across the wider band (typically 1..2% of the central frequency) than that for regular clock, which has a very concentrated spectral characteristics. This allows reducing the RF radiation caused by DSP EMIF, which is the main radiation source for *TORNADO-E2/6xxx* controllers.

NOTE

DSP EMIF Spread Spectrum Clock is an option for *TORNADO-E2/6xxx* DSP controllers, which must be specified during board purchase. Call MicroLAB Systems for more information.

NOTE

Presence of DSP EMIF Spread Spectrum Clock on particular *TORNADO-E2/6xxx* controller is checked via *DSP_SSCLK* bit of [DSP_SYS_CNF2_RG](#) read-only DSP external control register.

Some of *TORNADO-E2/6xxx* controllers allow software configured selection between EMIF regular clock and EMIF spread spectrum clock (in case it is installed). The following is a list of applicable *TORNADO-E2/6xxx* controllers:

- *TORNADO-E2/6713* controller with TMS320C6713 DSP.

For *TORNADO-E2/6713*, the EMIF clock source selection is performed via the *EKSRC* bit of *DEVCFG* DSP on-chip device configuration register (@0x019C0200). In case the PLL output is used as the EMIF clock, then this is the regular clock. However, in case external EMIF source clock is selected, then this is the spread spectrum EMIF clock.

IMPORTANT NOTE

It is recommended, that the *DEVCFG* TMS320C6713 DSP on-chip device configuration register (@0x019C0200) for *TORNADO-E2/6713* controller is not directly configured from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user's guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

DSP memory map

Memory map for *TORNADO-E2/6xxx* on-board DSP comprises the DSP on-chip memory and peripherals areas as well as external EMIF memory and I/O areas. Although all *TORNADO-E2/6xxx* DSP controllers generally have similar on-board memory and I/O resources, particular DSP memory map is unique for every controllers type.

The following is a list of DSP memory and I/O areas for *TORNADO-E2/6xxx* on-board TMS320C6713 DSP:

- DSP on-chip memory and registers areas in accordance with the TMS320C6713 DSP on-chip memory map (refer to original TI documentation for TMS320C6713 DSP for more details)
- EMIF CE-0 area, which is used to access the on-board SBSRAM memory bank and synchronous interfaces of *PIOX2* and *HCXDCM* sites
- EMIF CE-1 area, which is used to access the on-board FLASH memory
- EMIF CE-2 area, which is used to access the on-board SDRAM memory bank
- EMIF CE-3 area, which is used to access the on-board DSP external control registers and on-board parallel peripherals (DUART, RTC, USB controllers, and asynchronous interfaces of *ASIOX* and *PIOX2* DCM sites).

NOTE

TMS320C6xxx DSP feature byte addressing capability.

8-bit data words (bytes) are allocated on the x1 address boundaries. 16-bit data words are allocated on the x2 address boundaries. 32-bit data words are allocated on x4 address boundaries.

Detail DSP memory maps for *TORNADO-E2/6xxx* controllers are presented in [Table 2-2](#).

Table 2-2. DSP memory map for *TORNADO-E2/6713*.

DSP memory area or register name	DSP address range	Valid data word bits @EMIF area data word format	Data access formats	Access mode	EMIF area and mode
On-board (DSP off-chip) memories					
SBSRAM	80000000H ..8007FFFFH (128Kx32) 80000000H ..801FFFFFH (512Kx32)	D0..D31 @W32	x8 x16 x32	r/w	EMIF CE-0 32-bit SBSRAM mode
FLASH	90000000H ..9007FFFFH (512Kx8) 90000000H ..907FFFFFH (8Mx8) 90000000H ..93FFFFFH (64Mx8)	D0..D7 @W8	x8	r/w	EMIF CE-1 8-bit ASYNC mode
SDRAM	A0000000H ..A0FFFFFFFH (4Mx32) A0000000H ..A3FFFFFFFH (16Mx32)	D0..D31 @W32	x8 x16 x32	r/w	EMIF CE-2 32-bit SDRAM mode
DSP external control registers ¹⁾					
DSP_SYS_CNF1_RG (DSP controller device ID)	B0000000H	D0..D7 @W32	x8	r	EMIF CE-3 32-bit ASYNC mode
DSP_SYS_CNF2_RG (DSP controller board revision ID, DSP frequency ID, spread spectrum clock presence ID)	B0000004H	D0..D7 @W32	x8	r	
DSP_SYS_CNF3_RG (DSP external memory configuration)	B0000008H	D0..D7 @W32	x8	r	

<u>DSP_SYS_CNF4_RG</u> (DSP controller peripherals configuration)	B000000CH	D0..D7 @W32	x8	r
<u>DSP_DSP_CNF_RG</u> (DSP system configuration information)	B0000018H	D0..D7 @W32	x8	r
<u>DSP_DCM_CNF_RG</u> (DCM installation status information)	B000001CH	D0..D7 @W32	x8	r
<u>DSP_FLASH_PAGE_RG</u> (FLASH memory pages selector)	B0000020H	D0..D7 @W32	x8	r/w
<u>DSP_FLASH_CNTR_RG</u> (FLASH memory WRITE control)	B0000024H	D0..D7 @W32	x8	r/w
<u>DSP_HCX_SYNC_PAGE_RG</u> (32-bit synchronous HCX DCM site interface extended address control)	B000002CH	D0..D7 @W32	x8	r/w
<u>DSP_EXT_INT4_SEL_RG</u> (DSP EXT_INT4 source selector)	B0000030H	D0..D7 @W32	x8	r/w
<u>DSP_EXT_INT5_SEL_RG</u> (DSP EXT_INT5 source selector)	B0000034H	D0..D7 @W32	x8	r/w
<u>DSP_EXT_INT6_SEL_RG</u> (DSP EXT_INT6 source selector)	B0000038H	D0..D7 @W32	x8	r/w
<u>DSP_EXT_INT7_SEL_RG</u> (DSP EXT_INT7 source selector)	B000003CH	D0..D7 @W32	x8	r/w
<u>DSP_NMI_SEL_RG</u> (DSP NMI source selector)	B0000040H	D0..D7 @W32	x8	r/w
<u>DSP_DCM_RESET_RG</u> (PIOX2/SIOX/ASIOX reset control)	B0000060H	D0..D7 @W32	x8	r/w
<u>DSP_WDT_RTC_CNTR_RG</u> (µP WDT/RTC control)	B0000064H	D0..D7 @W32	x8	r/w
<u>DSP_GPIO_DATA_RG</u> (GPIO pins data control)	B0000068H	D0..D7 @W32	x8	r/w
<u>DSP_GPIO_DIR_RG</u> (GPIO pins direction control)	B000006CH	D0..D7 @W32	x8	r/w
<u>DSP_SIOX_XIO_DATA_RG</u> (SIOX rev.B SX_TM/XIO-0/1 pins data control)	B0000070H	D0..D7 @W32	x8	r/w
<u>DSP_SIOX_XIO_CNF_RG</u> (SIOX rev.B SX_TM/XIO-0/1 pins mode/direction control)	B0000074H	D0..D7 @W32	x8	r/w
<u>DSP_PORTS_CNTR_RG</u> (DSP on-chip serial ports buffers control)	B000007CH	D0..D7 @W32	x8	r/w
<u>DSP_WDT_RESET_RG</u> (WDT reset control register)	B01C0000H	written data is ignored @W32	x8	w

On-board DSP parallel peripherals					
32-bit synchronous <i>P/IOX2</i> DCM site interface area (refer to Appendix D for more details)	80200000H .. 8023FFFFH 80240000H .. 8027FFFFH	D0..D31 @W32	x8 x16 x32	r/w	EMIF CE-0 32-bit SBRAM mode
32-bit synchronous <i>HCX</i> DCM site interface area (refer to Appendix E for more details)	80300000H .. 803FFFFFH	D0..D31 @W32	x8 x16 x32	r/w	
Dual-channel UART <i>channel-A registers</i> <i>channel-B registers</i>	B0040040H .. B004005FH B0040000H .. B004001FH	D0..D7 @W32	x8	r/w	EMIF CE-3 32-bit ASYNC mode
Real-time clock (RTC) controller registers	B0080000H .. B008001FH	D0..D7 @W32	x8	r/w	
USB interface <ul style="list-style-type: none">• <i>Lucent Technologies USS-820 USB 1.1 single-channel device controller registers</i>• <i>Netchip NET2272 USB 2.0 single-channel device controller registers</i>• <i>Philips ISP1761 USB 2.0 three-channel host/device controller:</i><ul style="list-style-type: none">❑ <i>USB controller on-chip registers</i>❑ <i>peripheral controller DMA port</i>❑ <i>host controller DMA port</i>	B00C0000H .. B00C001FH B00C0000H .. B00C001FH B00C0000H .. B00CFFFFH B0100000H B0140000H	D0..D7 @W32 D0..D7/D15 @W32 D0..D15/D31 @W32 D0..D15/D31 @W32 D0..D15/D31 @W32	x8 x8 x16 x16 x32	r/w	
32-bit asynchronous <i>P/IOX2</i> DCM site interface area (refer to Appendix D for more details)	B03C0000H ..B03FFFFFH	D0..D31 @W32	x32	r/w	
16-bit <i>AS/IOX</i> rev.D DCM site parallel interface area (refer to Appendix C for more details)	B02C0000H ..B02FFFFFH	D0..D15 @W32	x16	r/w	
DSP on-chip memory and peripheral control registers					
TMS320C6713 DSP on-chip RAM (refer to original TI documentation for more details)	00000000H ..0003FFFFH	D0..D31	x8 x16 x32	r/w	-
TMS320C6713 DSP on-chip peripheral registers (refer to original TI documentation for more details)	01800000H ..02000033H	D0..D31	x32	r/w	-

- Notes:
1. DSP external control registers area denotes on-board system controller.
 2. @W32 denotes that the address step for consecutive data words of this DSP EMIF area corresponds to 32-bit data words. Refer to the corresponding subsection below for more details.
 3. Register access modes: *r* - read only, *w* - write only, *r/w* - read/write.

NOTE

DSP memory areas, which are not listed in [Table 2-2](#), are reserved and shall be not accessed from DSP application.

IMPORTANT NOTE

TORNADO-E2/6713 on-board DSP peripherals and external control registers are allocated at least significant 8-bit and 16-bit data words of 32-bit data words (*UNSIGNED INT 'C'*-type variables) at x4 DSP address boundaries.

DSP EMIF registers settings

User DSP application shall correctly configure DSP on-chip EMIF control registers in accordance with the [Table 2-3](#) in order to provide correct operation of DSP EMIF and to benefit from maximum DSP performance of *TORNADO-E2/6xxx*.

NOTE

It is recommended, that the DSP on-chip EMIF control registers are not directly configured from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user's guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

NOTE

DSP EMIF clock for *TORNADO-E2/6713* controller is 100 MHz.

For more details about TMS320C6xxx DSP EMIF control registers refer to original documentation for TI TMS320C6xxx DSP, which is included in electronic form along with this user's guide.

Table 2-3. Recommended settings for TMS320C6713 DSP on-chip EMIF control registers for *TORNADO-E2/6713*.

TMS320C6713 on-chip EMIF control register	EMIF area mode	register value
EMIF Global Control Register (EMIF_GBLCTL)	-	0x00003068
EMIF CE-0 Space Control Register (EMIF_CE0CTL) (area controls the 32-bit SBSRAM)	32-bit SBSRAM	0x00000040
EMIF CE-1 Space Control Register (EMIF_CE1CTL) (area controls the on-board FLASH memory)	8-bit ASYNCR/w strobe: 12 clk (120ns) r/w setup: 2 clk (20ns) r/w hold: 1 clk (10ns)	0x23124c01
EMIF CE-2 Space Control Register (EMIF_CE2CTL) (area controls the 32-bit SDRAM)	32-bit SDRAM	0x00000030
EMIF CE-3 Space Control Register (EMIF_CE3CTL) (area controls the DSP external control registers and on-board parallel peripherals)	32-bit ASYNCR/w strobe: 3 clk (30ns) r/w setup: 2 clk (20ns) r/w hold: 1 clk (10ns)	0x20d24321
EMIF SDRAM Control Register (EMIF_SDCTL)	-	0x57115000 (SDRAM 4Mx32) 0x63115000 (SDRAM 16Mx32)
EMIF SDRAM Extension Register (EMIF_SDEXT)	-	0x00054529
EMIF SDRAM Timing Register (EMIF_SDTIM)	-	1562 (SDRAM 4Mx32) 781 (SDRAM 16Mx32)

DSP speed grade ID

The read-only DSP speed grade ID (*DSP clock frequency value*) for *TORNADO-E2/6xxx* on-board DSP can be either read via {*DSP_CLK_FREQ_ID-0..1*} bits of [DSP_SYS_CNF2_RG](#) DSP external control register (refer to [Table 2-11](#)) for DSP environment, or via [HCX_AX_SYS_CNF2_RG](#) HCX control register for host HCX controller environment, or can be read at the text label at the bottom of *TORNADO-E2/6xxx* board.

This feature allows automatic run-time configuration of the DSP and host HCX controller software.

Synchronous burst static RAM (SBSRAM) memory area

TORNADO-E2/6xxx DSP controllers provide on-board SBSRAM, which can be used by on-board DSP for real-time application specific data, which require fast access. SBSRAM capacity depends upon the controller type.

NOTE

SBSRAM capacity cannot be updated by the user and must be specified during board purchase. Call MicroLAB Systems for more information.

NOTE

TORNADO-E2/6713 DSP controller provides either 128Kx32 or 512Kx32 on-board SBSRAM running at 100 MHz clock and allocated to the DSP EMIF CE-0 external memory area.

NOTE

On-board SBSRAM can be accessed either of 8-/16-/32-bit data formats.

TORNADO-E2/6xxx on-board SBSRAM can be also accessed by host *HCX* controller via *HCX* interface of *TORNADO-E2/6xxx* DSP controllers (refer to section “[HCX DCM Site Interface](#)” later in this chapter for more details).

Both DSP and host *HCX* controller applications can identify on-board SBSRAM capacity via {*SBSRAM_LEN_ID-0..1*} bits of [DSP_SYS_CNF3_RG](#) DSP external control register (refer to [Table 2-12](#)) and [HCX_AX_SYS_CNF3_RG](#) *HCX* control register correspondingly in order to perform run-time configuration of the corresponding software environments.

Synchronous dynamic RAM (SDRAM) memory area

TORNADO-E2/6xxx DSP controllers provide on-board SDRAM, which is used by on-board DSP to save large real-time data arrays. SDRAM capacity depends upon the controller type.

NOTE

SDRAM capacity cannot be updated by the user and must be specified during board purchase. Call MicroLAB Systems for more information.

NOTE

TORNADO-E2/6713 DSP controller provides either 4Mx32 or 16Mx32 on-board SDRAM running at 100 MHz clock and allocated to the DSP EMIF CE-2 external memory area.

NOTE

On-board SDSRAM can be accessed either of 8-/16-/32-bit data formats.

TORNADO-E2/6xxx on-board SDRAM can be also accessed by host *HCX* controller via *HCX* interface of *TORNADO-E2/6xxx* DSP controllers (refer to section “[HCX DCM Site Interface](#)” later in this chapter for more details).

Both DSP and host *HCX* controller applications can identify on-board SDRAM capacity via {*SDRAM_LEN_ID-0..1*} bits of [DSP_SYS_CNF3_RG](#) DSP external control register (refer to [Table 2-12](#)) and [HCX_AX_SYS_CNF3_RG](#) *HCX* control register correspondingly in order to perform run-time configuration of the corresponding software environments.

FLASH memory area

TORNADO-E2/6xxx DSP controllers provide either 512Kx8, or 1Mx8, or 8Mx8, or 64Mx8 on-board FLASH memory, which is used for DSP boot code in *SA/BMODE-FLASH8* and *HOST/BMODE-FLASH8* DSP bootmodes (refer to [Table 2-1](#) for more details), and/or can be also used to save application specific non-volatile data.

NOTE

FLASH capacity cannot be updated by the user and must be specified during board purchase. Call MicroLAB Systems for more information.

TORNADO-E2/6xxx on-board DSP software and host software both can identify on-board FLASH memory capacity via {*FLASH_LEN_ID-0..3*} bits of [DSP_SYS_CNF3_RG](#) DSP external control register (refer to [Table 2-12](#)) and [HCX_AX_SYS_CNF3_RG](#) *HCX* control register correspondingly in order to perform run-time configuration of the corresponding software environments.

TORNADO-E2/6xxx on-board FLASH memory can be also accessed by *HCX* controller via *HCX* interface of *TORNADO-E2/6xxx* DSP controllers (refer to section “[HCX DCM Site Interface](#)” later in this chapter for more details).

NOTE

Although it is generally possible to program the on-board FLASH memory from host *HCX* controller application, it is recommended, that FLASH is programmed from the DSP application in order to meet FLASH timing requirements.

TORNADO-E2/6713 on-board FLASH memory is mapped to the DSP EMIF CE-1 external memory area.

NOTE

For all *TORNADO-E2/6xxx* DSP controllers, the on-board FLASH memory appears as asynchronous 8-bit memory with access time 120ns.

512Kx8 and 1Mx8 FLASH memories exactly fit into the 1Mx8 address area of the DSP EMIF CE1 external memory area, and therefore every FLASH memory location for these FLASH capacities can be directly accessed from DSP application by means of addressing the corresponding byte within the FLASH memory area.

However, in case the 8Mx8 or 64Mx8 FLASH memory is installed, then the paging method is used in order to access the FLASH memory since the 8Mx8 or 64Mx8 full FLASH memory capacity exceeds the 1Mx8 address area of DSP EMIF CE-1 external memory space. Therefore, the 8Mx8 or 64Mx8 FLASH memory capacity is split into 8 or 64 pages each having the 1Mx8 capacity and the currently selected FLASH memory page can be directly accessed via the DSP EMIF

CE-1 external memory space. In order to select a FLASH memory page, {*FPAGE-5..0*} bits of [DSP_FLASH_PAGE_RG](#) DSP external control register are used (refer to [Table 2-4](#)).

IMPORTANT NOTE

It is recommended, that the {*FPAGE-5..0*} bits, which are used to select the FLASH memory page, are not directly configured from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user's guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

Table 2-4. FLASH memory page selection.

FLASH capacity	FLASH page selector bits of <i>DSP_FLASH_PAGE_RG</i> register						Addressed FLASH area	Description
	<i>FPAGE</i> -5	<i>FPAGE</i> -4	<i>FPAGE</i> -3	<i>FPAGE</i> -2	<i>FPAGE</i> -1	<i>FPAGE</i> -0		
512Kx8	x	x	x	x	X	X	0x000000..0x07ffff	No FLASH paging method is used to access this FLASH memory.
8Mx8	x	x	x	0	0	0	0x000000..0x0fffff	FLASH page #0 is selected.
	x	x	x	0	0	1	0x100000..0x1fffff	FLASH page #1 is selected.
	x	x	x	0	1	0	0x200000..0x2fffff	FLASH page #2 is selected.
	x	x	x	0	1	1	0x300000..0x3fffff	FLASH page #3 is selected.
	x	x	x	1	0	0	0x400000..0x4fffff	FLASH page #4 is selected.
	x	x	x	1	0	1	0x500000..0x5fffff	FLASH page #5 is selected.
	x	x	x	1	1	0	0x600000..0x6fffff	FLASH page #6 is selected.
	x	x	x	1	1	1	0x700000..0x7fffff	FLASH page #7 is selected.
64Mx8	0	0	0	0	0	0	0x0000000..0x00fffff	FLASH page #0 is selected.
	0	0	0	0	0	1	0x0100000..0x01fffff	FLASH page #1 is selected.
	0	0	0	0	1	0	0x0200000..0x02fffff	FLASH page #2 is selected.
	...							
	1	1	1	1	0	1	0x3d00000..0x3dfffff	FLASH page #61 is selected.
	1	1	1	1	1	0	0x3e00000..0x3efffff	FLASH page #62 is selected.
	1	1	1	1	1	1	0x3f00000..0x3fffff	FLASH page #63 is selected.

Note:

1. Highlighted FLASH memory page is selected as default on the DSP reset condition.
2. 'X' denotes don't care condition.

TORNADO-E2/6xxx DSP controllers provide both user hardware and software control for multi-level write protection of on-board FLASH memory contents via on-board switches and via [DSP_FLASH_CNTR_RG](#) DSP external control register (Table 2-17) and [HCX_AX_CNTR2_RG](#) HCX control register (Table 2-30). This multi-level FLASH write protection mechanism guarantees safety of FLASH contents.

At first, there is hardware FLASH write protection control via on-board SW1-2 and SW1-3 switches (Figure 2-2 and Figure A-1). SW1-2 switch is used to globally enable FLASH write access, whereas SW1-3 switch is used for 64Mx8 FLASH memories only in order to enable write protection of 1st FLASH sector only. Table 2-5 and Table 2-6 provide details about the SW1-2 and SW1-3 switches settings at *TORNADO-E2/6xxx* board.

In case FLASH is globally write protected via SW1-2 switch that there is no way to write to FLASH memory. Typically, FLASH shall be globally write disabled via onboard SW1-2 switch only in case user DSP application is assumed to perform no FLASH writes and/or there are serious reasons to keep FLASH contents unaltered.

Table 2-5. FLASH write protection control.

SW1-2 switch	FLASH_WR_EN bit of HCX_AX_CNTR2_RG register ⁴⁾	FLASH_WR_EN bit of DSP_FLASH_CNTR_RG register	Description
DSP STAND-ALONE OPERATION MODE			
OFF	N/A	x	FLASH write is permanently disabled.
ON	N/A	0	FLASH write is disabled by DSP application. DSP application must set <i>FLASH_WR_EN</i> bit of DSP_FLASH_CNTR_RG register to the '1' state in order to enable FLASH writes.
ON	N/A	1	FLASH write is enabled.
DSP HOST OPERATION MODE			
OFF	x	x	FLASH write is permanently disabled.
ON	0	x	FLASH write is disabled by host HCX controller. Host application must set <i>FLASH_WR_EN</i> bit of HCX_AX_CNTR2_RG register to the '1' state in order to allow DSP application to enable FLASH writes via <i>FLASH_WR_EN</i> bit of DSP_FLASH_CNTR_RG register.
ON	1	0	FLASH write is enabled by host HCX controller. DSP application must set <i>FLASH_WR_EN</i> bit of DSP_FLASH_CNTR_RG register to the '1' state in order to enable FLASH writes.
ON	1	1	FLASH write is enabled.

- Notes:
1. Highlighted configuration corresponds to FLASH writes enabled.
 2. 'X' denotes don't care condition.
 3. 'N/A' denotes that this bit is not available for this configuration.
 4. *FLASH_WR_EN* bit of [HCX_AX_CNTR2_RG](#) HCX control register (Table 2-30) can be set only in case the on-board DSP is in the reset state.

However, in case FLASH is global write enabled via on-board SW1-2 switch, then there is a second level of FLASH write protection used via [DSP_FLASH_CNTR_RG](#) DSP external control register (Table 2-17), and via [HCX_AX_CNTR2_RG](#) HCX control register (Table 2-30) for *DSP host operation mode* only. The second level of FLASH write protection assumes that DSP application must explicitly enable FLASH write access by setting *FLASH_WR_EN* bit of [DSP_FLASH_CNTR_RG](#) DSP external control register (Table 2-17) into the '1' state before updating FLASH contents. For *DSP host operation mode*, there is also an extra FLASH write protection possibility for host HCX controller application via *FLASH_WR_EN* bit of [HCX_AX_CNTR2_RG](#) HCX control register (Table 2-30), which must be set to the '1' state in order to allow DSP application to set the *FLASH_WR_EN* bit of [DSP_FLASH_CNTR_RG](#) DSP external control register. Such a multi-level FLASH write protection control excludes accidental writes to the FLASH memory and unintended corruption of its contents thus significantly increasing safety of FLASH contents.

Table 2-6. 64Mx8 FLASH 1st sector write protection control.

SW1-2 switch	FLASH_WR_EN bit of HCX_AX_CNTR2_RG register	FLASH_WR_EN bit of DSP_FLASH_CNTR_RG register	SW1-3 switch	FLASH64M_BOOT_SECTOR_WR_EN bit of HCX_AX_CNTR2_RG register	FLASH64M_BOOT_SECTOR_WR_EN bit of DSP_FLASH_CNTR_RG register	Description
DSP STAND-ALONE OPERATION MODE						
OFF	N/A	x	x	N/A	x	FLASH write (including write to 1 st sector) is permanently disabled.
x	N/A	x	ON	N/A	x	Write to FLASH 1 st sector is permanently disabled.
ON	N/A	0	OFF	N/A	x	FLASH write (including write to 1 st sector) is disabled by DSP application. DSP application must set FLASH_WR_EN bit of DSP_FLASH_CNTR_RG register to the '1' state in order to enable FLASH writes.
ON	N/A	1	OFF	N/A	0	FLASH write is enabled by DSP application, however write to 1 st sector is disabled. DSP application must set FLASH64M_BOOT_SECTOR_WR_EN bit of DSP_FLASH_CNTR_RG register to the '1' state in order to enable writes to FLASH 1 st sector.
ON	N/A	1	OFF	N/A	1	Write to FLASH 1 st sector is enabled.
DSP HOST OPERATION MODE						
OFF	x	x	x	x	x	FLASH write (including write to 1 st sector) is permanently disabled.
x	x	x	ON	x	x	Write to FLASH 1 st sector is permanently disabled.
ON	0	x	OFF	x	x	FLASH write (including write to 1 st sector) is disabled by host HCX controller. Host application must set FLASH_WR_EN bit of HCX_AX_CNTR2_RG register to the '1' state in order to allow DSP application to enable FLASH writes via FLASH_WR_EN bit of DSP_FLASH_CNTR_RG register.
ON	1	0	OFF	x	x	FLASH write is enabled by host HCX controller. FLASH write (including write to 1 st sector) is disabled by DSP application. DSP application must set FLASH_WR_EN bit of DSP_FLASH_CNTR_RG register to the '1' state in order to enable FLASH writes.
ON	1	1	OFF	0	x	FLASH write is enabled by DSP application, however write to 1 st sector is disabled by host HCX controller. Host application must set FLASH64M_BOOT_SECTOR_WR_EN bit of HCX_AX_CNTR2_RG register to the '1' state in order to allow DSP application to enable writes to 1 st sector via FLASH64M_BOOT_SECTOR_WR_EN bit of DSP_FLASH_CNTR_RG register.
ON	1	1	OFF	1	0	Write to FLASH 1 st sector is enabled by host HCX controller. DSP application must set FLASH64M_BOOT_SECTOR_WR_EN bit of DSP_FLASH_CNTR_RG register to the '1' state in order to enable writes to FLASH 1 st sector.
ON	1	1	OFF	1	1	Write to FLASH 1 st sector is enabled.

- Notes:
1. Highlighted configuration corresponds to FLASH 1st sector writes enabled.
 2. 'X' denotes don't care condition.
 3. 'N/A' denotes that this bit is not available for this configuration.

For more details about programming of *TORNADO-E2/6xxx* on-board FLASH memory refer to [Appendix G](#) of this user's guide.

DSP external control registers area

TORNADO-E2/6xxx on-board *DSP external control registers area* comprises a set of control registers and is used for run-time configuration and control of on-board system controller, parallel peripherals (DUART, USB, RTC controllers, DCM sites interfaces) and DSP external environment (external interrupt selectors, WDT control, etc).

DSP external control registers area is mapped into the sub-space of DSP EMIF CE-3 asynchronous external memory area (refer to [Table 2-2](#)).

NOTE

All *DSP external control registers* have 8-bit data format and are allocated to the least significant bytes of DSP 32-bit data words.

For more details about *DSP external control registers area* refer to section “[DSP external control registers area](#)” later in this chapter.

Asynchronous and synchronous sections of Parallel I/O Expansion (PIOX2) DCM site interface

TORNADO-E2/6xxx on-board *PIOX2* DCM site interface comprises parallel 32-bit asynchronous and 32-bit synchronous interface sections, which are both mapped into the DSP memory map (refer to [Table 2-2](#)).

For more details about the on-board *PIOX2* DCM site interface refer to [Appendix D](#).

Synchronous section of HCX DCM site interface

TORNADO-E2/6xxx on-board synchronous section of *HCX* rev.A DCM site interface (*HCX-SYNC*) mapped into the DSP memory map (refer to [Table 2-2](#)).

HCX-SYNC interface is 32-bit parallel interface with 24-bit addressing capabilities. Due to a limited addressing capabilities, *TORNADO-E2/6713* on-board DSP provides direct addressing to 256Kx32 page of *HCX-SYNC* interface only, whereas the addressed page is selected via [DSP_HCX_SYNC_PAGE_RG](#) DSP external control register.

For more details about *HCX* DCM site refer to section “[HCX DCM Site Interface](#)” later in this chapter and to [Appendix E](#) of this user guide.

Dual-channel UART

TORNADO-E2/6xxx on-board Exar ST16C2550 dual-channel UART (DUART with channel-A and channel-B) controller is a hardware compatible superset for the industry standard PC COM port and provides communication with external peripherals at the speeds up to 384 kBaud via RS232C interface.

Each DUART channel has eight 8-bit control registers, which are mapped to the DSP EMIF CE-3 external memory area of on-board DSP (refer to [Table 2-2](#)). DUART generates two interrupts to on-board DSP via any of the DSP EXT_INT4..7 external interrupt requests (*UART_IRQ-A* and *UART_IRQ-B* interrupt sources at [Figure 2-3](#)).

NOTE

All DUART 8-bit control registers are allocated to the least significant bytes of DSP 32-bit data words.

TORNADO-E2/6xxx have been designed to generate the shortest possible DUART access cycles, which is the sum of read/write setup wait states, read/write strobe length, and read/write hold wait states.

For more details about DUART refer to [Appendix H](#) of this user's guide.

USB interface

TORNADO-E2/6xxx DSP controllers may be shipped with one of the following on-board USB interfaces:

- 480 Mbit/s Philips ISP1761 USB 2.0 three-channel host/device controller comprises a large set of on-chip 32-bit registers, a large buffer of internal memory and two DMA ports for host and peripheral controllers, which are mapped to the corresponding sub-space of EMIF CE-3 external memory space of on-board DSP (refer to [Table 2-2](#)). This architecture of USB 2.0 controller delivers a higher performance for data transfers from DSP to USB controller and vice versa. The USB controller can generate two dedicated interrupts and two DMA requests to the on-board DSP via the DSP EXT_INT4..7 external interrupt requests (*USB_DC_IRQ*, *USB_HC_IRQ*, *USB_DC_DREQ* and *USB_HC_DREQ* interrupt sources at [Figure 2-3](#)).
- 480 Mbit/s PLX/Netchip NET2272 USB 2.0 one-channel device controller comprises a large set of on-chip 8-bit and 16-bit registers, which can be accessed directly and indirectly. Directly accessed USB 2.0 controller registers are mapped to the corresponding sub-space of EMIF CE-3 external memory space of on-board DSP (refer to [Table 2-2](#)). USB 2.0 device controller can generate dedicated interrupt to the on-board DSP via any of the DSP EXT_INT4..7 external interrupt requests (*USB_IRQ* interrupt sources at [Figure 2-3](#)).
- 12 Mbit/s Lucent Technologies USS-820 USB 1.1 one-channel device controller comprises a set of on-chip 8-bit registers, which are mapped to the corresponding sub-space of EMIF CE-3 external memory space of on-board DSP (refer to [Table 2-2](#)). USB 1.1 device controller can generate dedicated interrupt to the on-board DSP via any of the DSP EXT_INT4..7 external interrupt requests (*USB_IRQ* interrupt sources at [Figure 2-3](#)).

NOTE

On-board USB controller cannot be replaced by the user and must be specified during board purchase.
Call MicroLAB Systems for more information.

USB controller on-chip control registers are mapped to the DSP EMIF CE-3 external memory area of on-board DSP (refer to [Table 2-2](#)).

NOTE

USB controller on-chip 8-bit and 16-bit control registers are allocated to the least significant bytes of DSP 32-bit data words.

TORNADO-E2/6xxx have been designed to generate the shortest possible USB controller access cycles, which is the sum of read/write setup wait states, read/write strobe length, and read/write hold wait states.

For more details about USB interface refer to [Appendix I](#) of this user's guide.

Real-time clock (RTC) controller

For applications, which require accurate timing and calendar management, TORNADO-E2/6xxx controllers provide on-board real-time clock controller (RTC), which is based on Dallas Semiconductor DS1501 RTC controller. RTC interface includes sixteen 8-bit control registers and 256 bytes of non-volatile RAM. RTC registers are mapped to the DSP EMIF CE-3 external memory area (refer to [Table 2-2](#)).

NOTE

RTC on-chip 8-bit control registers are allocated to the least significant bytes of DSP data words.

RTC controller generates interrupt to the on-board DSP via any of the DSP EXT_INT4..7 external interrupt requests (*RTC_IRQ* interrupt source at [Figure 2-3](#)).

TORNADO-E2/6xxx have been designed to generate the shortest possible RTC access cycles, which is the sum of read/write setup wait states, read/write strobe length, and read/write hold wait states.

For more details about RTC controller refer to [Appendix J](#) of this user's guide.

On-board watch-dog timer (WDT)

TORNADO-E2/6xxx DSP controllers provide on-board watchdog timer (WDT), which is used to increase system reliability for embedded applications and to minimize system 'dead' times caused by DSP software hanging or DSP environment crashing.

In case on-board DSP is configured to run in the *DSP stand-alone operation mode* (refer to subsection "[DSP operation modes and DSP bootmodes](#)" for more details) with the WDT feature enabled (i.e. automatic DSP reset on WDT expiration event), then the DSP application must periodically reset WDT (with the period about 1 sec), otherwise WDT will generate DSP reset signal and will restart DSP application. WDT feature is typically used to increase system reliability for embedded applications and to minimize system 'dead' times caused by DSP software hanging or DSP environment crashing.

WDT is enabled via the *WDT_EN* bit of [DSP_WDT_RTC_CNTR_RG](#) DSP external control register for *DSP stand-alone operation mode* only. In order to reset the on-board WDT, DSP application must perform the write operation to the [DSP_WDT_RESET_RG](#) write-only DSP external control register.

Along with automatic generation of the DSP reset signal on the WDT expiration event, WDT can be also used to generate DSP interrupt requests via DSP EXT_INT4..7/NMI external interrupt requests (refer to [Table 2-14](#)) in both *DSP stand-alone operation mode* and *DSP host operation mode*. The most typical solution is to configure [DSP_NMI_SEL_RG](#) DSP external control register to generate DSP NMI interrupt request on the WDT expiration event and to have the DSP NMI interrupt service routine to either restart DSP application or to perform application specific reset of the DSP software environment.

DSP on-chip timers

TORNADO-E2/6xxx on-board DSP provides either two or three DSP on-chip timers (depending upon the controller/DSP type), which can be used as either timers or as general purpose I/O.

TORNADO-E2/6713 controller with TMS320C6713 DSP provides two DSP on-chip timers.

NOTE

DSP timers inputs are not supported in *TORNADO-E2/6713* DSP controller.

TORNADO-E2/6xxx DSP on-chip timers are configured via the corresponding TMS320C6xxx DSP on-chip timers control registers and are routed directly to on-board *SIOX* rev.B DCM site header (*SIOX_TM/XIO-0* and *SIOX_TM/XIO-1* pins). *SIOX_TM/XIO-0* and *SIOX_TM/XIO-1* pins of *TORNADO-E2/6xxx* on-board *SIOX* rev.B DCM site can be either connected to the corresponding TMS320C6xxx DSP on-chip timer output pins (TOUT0 and TOUT1), or used as general purpose I/O pins (XIO-0 and XIO-1). Configuration of these pins is controlled via [DSP_SIOX_XIO_CNF_RG](#) and [DSP_SIOX_XIO_DATA_RG](#) DSP external control registers (refer to [Table 2-22](#) and [Table 2-23](#) for more details).

For *TORNADO-E2/6713*, in case the DSP timers output pins are used, then they shall be also enabled via *DEVCFG* TMS320C6713 DSP on-chip device configuration register (@0x019C0200) (refer to [Table 2-7](#)).

NOTE

For more information about configuration of TMS320C6xxx DSP on-chip timers control registers refer to original TI TMS320C6xxx user's guide, which is provided in electronic form along with this user's guide

IMPORTANT NOTE

It is recommended, that the *DEVCFG* TMS320C6713 DSP on-chip device configuration register (@0x019C0200) bits are not directly configured from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user's guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

For more details about the on-board *SIOX* DCM sites refer to [Appendix C](#).

DSP on-chip serial peripherals (McBSP, McASP, I²C ports)

TI TMS320C6xxx DSP provides a powerful set of on-chip serial peripherals, which varies upon the DSP type. *TORNADO-E2/6xxx* controllers are designed to benefit from all DSP on-chip peripherals, which deliver extraordinary user application flexibility.

TORNADO-E2/6713 controller with TMS320C6713 DSP makes use of the following DSP on-chip peripherals:

- two Multichannel Buffered Serial Ports (McBSP-0/1),
- two Multichannel Audio Serial Ports (McASP-0/1),
- two I²C serial ports (I²C-0/1).

NOTE

This subsection provides only application specific information about TMS320C6xxx DSP on-chip serial peripherals as far as it is required to describe architecture of *TORNADO-E2/6xxx* DSP controllers.

For more information about TMS320C6xxx DSP on-chip serial peripherals refer to original TI TMS320C6xxx user's guides, which are supplied in electronic form along with this user's guide.

McBSP ports are standard serial ports coming standard thru all TMS320C6xxx DSP and are available via *TORNADO-E2/6xxx* on-board *SIOX* rev.B and *ASIOX* rev.D DCM sites (refer to [Figure A-1](#) and [Appendix C](#)).

McASP ports are application specific serial ports optimized for the needs of multi-channel audio applications. McASP ports are available at *TORNADO-E2/6713* controller with TI TMS320C6713 DSP via on-board *ASIOX* rev.D DCM site (refer to [Figure A-1](#)). Each McASP port consists of a transmitter and receiver section, which may either run independently with different audio data formats, different master clocks, bit clocks, and frame synchronization, or alternatively, they may be synchronized. Each McASP port includes a pool of 16 data shift registers each corresponding particular data I/O pin, which may be individually configured to map to either transmitter, or receiver, or configured as general-purpose I/O (GPIO).

I²C serial ports allow simple two-wire interface to compatible industry-standard peripherals. I²C ports are available at *TORNADO-E2/6713* controller with TI TMS320C6713 DSP via on-board JP14 and JP15 connectors (refer to [Figure A-1](#) and subsection "[JP14, JP15 I2C interface connectors](#)" for more details).

For *TORNADO-E2/6713* controller with TMS320C6713 DSP, the DSP IC package pins for serial ports are shared between McBSP ports, McASP ports, I²C ports and HPI port in order to minimize number of package pins. This implies restrictions for available DSP serial ports configurations, and these restrictions are different for *DSP stand-alone and host operation modes*. In order to enable particular DSP on-chip serial peripherals, TMS320C6713 DSP has the DSP on-chip *DEVCFG* device configuration register (@0x019C0200) (refer to [Table 2-7](#)). In addition to that, *TORNADO-E2/6713* controller provides [DSP_PORTS_CNTR_RG](#) DSP external control register, which must be set in accordance with the setting of the DSP on-chip *DEVCFG* device configuration register in order to allow correct routing and buffering of DSP serial ports to *TORNADO-E2/6713* on-board *SIOX* and *ASIOX* DCM sites. [Table 2-7](#) below lists all available configurations of DSP on-chip serial peripherals for *TORNADO-E2/6713* controller.

IMPORTANT NOTE

It is recommended, that the *DEVCFG* TMS320C6713 DSP on-chip device configuration register (@0x019C0200) and [DSP_PORTS_CNTR_RG](#) DSP external control register bits are not directly configured from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user's guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

Table 2-7. *TORNADO-E2/6713* on-board serial peripherals configurations.

Configuration ID for E2/6713 DSP software utilities	DSP on-chip peripherals							DSP_HPL_EN bit of <u>HCX_AX_CNTR2_RG</u> register	DEVCFG DSP on-chip register (@0x019C0200) bits				<u>DSP_PORTS_CNTR_RG</u> DSP external control register bits					DCM site interface	
	McBSP-0	McBSP-1	McASP-0	McASP-1	I ² C-1	Timer-0	Timer-1		TOUTSEL	TOUTOSEL	MCBSP0DIS	MCBSP1DIS	DSP_I2C1_BUF_EN	DSP_MCBSP1_BUF_EN	DSP_MCBSP0_BUF_EN	DSP_MCASP1_BUF_EN	{DSP_MCASP0_BUF_EN4..1}	SIOX rev.B	ASIOX rev.D
DSP stand-alone operation mode: McBSP-0 port is enabled																			
1	√							N/A	1	1	0	1	0	0	1	0	[0,0,0,0]	√	√
2	√	√						N/A	1	1	0	0	0	1	1	0	[0,0,0,0]	√	√
3	√				√			N/A	1	1	0	1	1	0	1	0	[0,0,0,0]	√	√
6	√					√		N/A	1	0	0	1	0	0	1	0	[0,0,0,0]	√	
7	√						√	N/A	0	1	0	1	0	0	1	0	[0,0,0,0]	√	
8	√	√				√		N/A	1	0	0	0	0	1	1	0	[0,0,0,0]	√	
9	√	√					√	N/A	0	1	0	0	0	1	1	0	[0,0,0,0]	√	
10	√				√	√		N/A	1	0	0	1	1	0	1	0	[0,0,0,0]	√	
11	√					√	√	N/A	0	0	0	1	0	0	1	0	[0,0,0,0]	√	
12	√				√		√	N/A	0	1	0	1	1	0	1	0	[0,0,0,0]	√	
13	√	√				√	√	N/A	0	0	0	0	0	1	1	0	[0,0,0,0]	√	
14	√				√	√	√	N/A	0	0	0	1	1	0	1	0	[0,0,0,0]	√	
24	√			√				N/A	1	1	0	1	0	0	1	1	[0,0,0,0]		√
25	√	√		√				N/A	1	1	0	0	0	1	1	1	[0,0,0,0]		√
26	√			√	√			N/A	1	1	0	1	1	0	1	1	[0,0,0,0]		√
DSP host operation mode: McBSP-0 port is enabled																			
1	√							X	1	1	0	1	0	0	1	0	[0,0,0,0]	√	√
2	√	√						X	1	1	0	0	0	1	1	0	[0,0,0,0]	√	√
3	√				√			X	1	1	0	1	1	0	1	0	[0,0,0,0]	√	√
6	√					√		X	1	0	0	1	0	0	1	0	[0,0,0,0]	√	
7	√						√	X	0	1	0	1	0	0	1	0	[0,0,0,0]	√	

8	√	√				√		X	1	0	0	0	0	1	1	0	[0,0,0,0]	√	
9	√	√					√	X	0	1	0	0	0	1	1	0	[0,0,0,0]	√	
10	√				√	√		X	1	0	0	1	1	0	1	0	[0,0,0,0]	√	
11	√					√	√	X	0	0	0	1	0	0	1	0	[0,0,0,0]	√	
12	√				√		√	X	0	1	0	1	1	0	1	0	[0,0,0,0]	√	
13	√	√				√	√	X	0	0	0	0	0	1	1	0	[0,0,0,0]	√	
14	√				√	√	√	X	0	0	0	1	1	0	1	0	[0,0,0,0]	√	
24	√			√				0	1	1	0	1	0	0	1	1	[0,0,0,0]		√
25	√	√		√				0	1	1	0	0	0	1	1	1	[0,0,0,0]		√
26	√			√	√			0	1	1	0	1	1	0	1	1	[0,0,0,0]		√
DSP stand-alone operation mode: McBSP-1 port is enabled																			
2	√	√						N/A	1	1	0	0	0	1	1	0	[0,0,0,0]	√	√
4		√						N/A	1	1	1	0	0	1	0	0	[0,0,0,0]	√	√
8	√	√				√		N/A	1	0	0	0	0	1	1	0	[0,0,0,0]	√	
9	√	√					√	N/A	0	1	0	0	0	1	1	0	[0,0,0,0]	√	
13	√	√				√	√	N/A	0	0	0	0	0	1	1	0	[0,0,0,0]	√	
15		√				√		N/A	1	0	1	0	0	1	0	0	[0,0,0,0]	√	
16		√					√	N/A	0	1	1	0	0	1	0	0	[0,0,0,0]	√	
17		√				√	√	N/A	0	0	1	0	0	1	0	0	[0,0,0,0]	√	
25	√	√		√				N/A	1	1	0	0	0	1	1	1	[0,0,0,0]		√
27		√	√ ⁶⁾					N/A	1	1	1	0	0	1	0	0	[1,1,0,1]		√
28		√		√				N/A	1	1	1	0	0	1	0	1	[0,0,0,0]		√
29		√	√ ⁶⁾	√				N/A	1	1	1	0	0	1	0	1	[1,1,0,1]		√
DSP host operation mode: McBSP-1 port is enabled																			
2	√	√						X	1	1	0	0	0	1	1	0	[0,0,0,0]	√	√
4		√						X	1	1	1	0	0	1	0	0	[0,0,0,0]	√	√
8	√	√				√		X	1	0	0	0	0	1	1	0	[0,0,0,0]	√	
9	√	√					√	X	0	1	0	0	0	1	1	0	[0,0,0,0]	√	
13	√	√				√	√	X	0	0	0	0	0	1	1	0	[0,0,0,0]	√	
15		√				√		X	1	0	1	0	0	1	0	0	[0,0,0,0]	√	
16		√					√	X	0	1	1	0	0	1	0	0	[0,0,0,0]	√	
17		√				√	√	X	0	0	1	0	0	1	0	0	[0,0,0,0]	√	
25	√	√		√				0	1	1	0	0	0	1	1	1	[0,0,0,0]		√
27		√	√ ⁶⁾					0	1	1	1	0	0	1	0	0	[1,1,0,1]		√
28		√		√				0	1	1	1	0	0	1	0	1	[0,0,0,0]		√
29		√	√ ⁶⁾	√				0	1	1	1	0	0	1	0	1	[1,1,0,1]		√
35		√	√ ⁶⁾					1	1	1	1	0	0	1	0	0	[1,1,0,1]		√
DSP stand-alone operation mode: McASP-0 port is enabled																			
27		√	√ ⁶⁾					N/A	1	1	1	0	0	1	0	0	[1,1,0,1]		√
29		√	√ ⁶⁾	√				N/A	1	1	1	0	0	1	0	1	[1,1,0,1]		√

30			√					N/A	1	1	1	1	0	0	0	0	[1,1,1,1]		√
31			√	√				N/A	1	1	1	1	0	0	0	1	[1,1,1,1]		√
32			√		√			N/A	1	1	1	1	1	0	0	0	[1,1,1,1]		√
34			√	√	√			N/A	1	1	1	1	1	0	0	1	[1,1,1,1]		√
DSP host operation mode: McASP-0 port is enabled																			
27			√	√ ⁶⁾				0	1	1	1	0	0	1	0	0	[1,1,0,1]		√
29			√	√ ⁶⁾	√			0	1	1	1	0	0	1	0	1	[1,1,0,1]		√
30			√					0	1	1	1	1	0	0	0	0	[1,1,1,1]		√
31			√	√				0	1	1	1	1	0	0	0	1	[1,1,1,1]		√
32			√		√			0	1	1	1	1	1	0	0	0	[1,1,1,1]		√
34			√	√	√			0	1	1	1	1	1	0	0	1	[1,1,1,1]		√
35			√	√ ⁶⁾				1	1	1	1	0	0	1	0	0	[1,1,0,1]		√
36			√					1	1	1	1	1	0	0	0	0	[1,1,1,1]		√
37			√		√			1	1	1	1	1	1	0	0	0	[1,1,1,1]		√
DSP stand-alone operation mode: McASP-1 port is enabled																			
24	√				√			N/A	1	1	0	1	0	0	1	1	[0,0,0,0]		√
25	√	√			√			N/A	1	1	0	0	0	1	1	1	[0,0,0,0]		√
26	√				√	√		N/A	1	1	0	1	1	0	1	1	[0,0,0,0]		√
28		√			√			N/A	1	1	1	0	0	1	0	1	[0,0,0,0]		√
29		√	√ ⁶⁾		√			N/A	1	1	1	0	0	1	0	1	[1,1,0,1]		√
31			√	√				N/A	1	1	1	1	0	0	0	1	[1,1,1,1]		√
33					√	√		N/A	1	1	1	1	1	0	0	1	[0,0,0,0]		√
34			√	√	√			N/A	1	1	1	1	1	0	0	1	[1,1,1,1]		√
DSP host operation mode: McASP-1 port is enabled																			
24	√				√			0	1	1	0	1	0	0	1	1	[0,0,0,0]		√
25	√	√			√			0	1	1	0	0	0	1	1	1	[0,0,0,0]		√
26	√				√	√		0	1	1	0	1	1	0	1	1	[0,0,0,0]		√
28		√			√			0	1	1	1	0	0	1	0	1	[0,0,0,0]		√
29		√	√ ⁶⁾		√			0	1	1	1	0	0	1	0	1	[1,1,0,1]		√
31			√	√				0	1	1	1	1	0	0	0	1	[1,1,1,1]		√
33					√	√		0	1	1	1	1	1	0	0	1	[0,0,0,0]		√
34			√	√	√			0	1	1	1	1	1	0	0	1	[1,1,1,1]		√
DSP stand-alone operation mode: I²C-1 port is enabled																			
3	√					√		N/A	1	1	0	1	1	0	1	0	[0,0,0,0]	√	√
5						√		N/A	1	1	1	1	1	0	0	0	[0,0,0,0]	√	√
10	√					√	√	N/A	1	0	0	1	1	0	1	0	[0,0,0,0]	√	
12	√					√		N/A	0	1	0	1	1	0	1	0	[0,0,0,0]	√	
14	√					√	√	N/A	0	0	0	1	1	0	1	0	[0,0,0,0]	√	
21						√	√	N/A	1	0	1	1	1	0	0	0	[0,0,0,0]	√	
22						√		N/A	0	1	1	1	1	0	0	0	[0,0,0,0]	√	

23					√	√	√	N/A	0	0	1	1	1	0	0	0	[0,0,0,0]	√	
26	√			√	√			N/A	1	1	0	1	1	0	1	1	[0,0,0,0]		√
32			√		√			N/A	1	1	1	1	1	0	0	0	[1,1,1,1]		√
33				√	√			N/A	1	1	1	1	1	0	0	1	[0,0,0,0]		√
34			√	√	√			N/A	1	1	1	1	1	0	0	1	[1,1,1,1]		√
DSP host operation mode: I²C-1 port is enabled																			
3	√				√			X	1	1	0	1	1	0	1	0	[0,0,0,0]	√	√
5					√			X	1	1	1	1	1	0	0	0	[0,0,0,0]	√	√
10	√				√	√		X	1	0	0	1	1	0	1	0	[0,0,0,0]	√	
12	√				√		√	X	0	1	0	1	1	0	1	0	[0,0,0,0]	√	
14	√				√	√	√	X	0	0	0	1	1	0	1	0	[0,0,0,0]	√	
21					√	√		X	1	0	1	1	1	0	0	0	[0,0,0,0]	√	
22					√		√	X	0	1	1	1	1	0	0	0	[0,0,0,0]	√	
23					√	√	√	X	0	0	1	1	1	0	0	0	[0,0,0,0]	√	
26	√			√	√			0	1	1	0	1	1	0	1	1	[0,0,0,0]		√
32			√		√			0	1	1	1	1	1	0	0	0	[1,1,1,1]		√
33				√	√			0	1	1	1	1	1	0	0	1	[0,0,0,0]		√
34			√	√	√			0	1	1	1	1	1	0	0	1	[1,1,1,1]		√
37			√		√			1	1	1	1	1	1	0	0	0	[1,1,1,1]		√
DSP stand-alone operation mode: Timer-0 output is enabled																			
6	√					√		N/A	1	0	0	1	0	0	1	0	[0,0,0,0]	√	
8	√	√				√		N/A	1	0	0	0	0	1	1	0	[0,0,0,0]	√	
10	√				√	√		N/A	1	0	0	1	1	0	1	0	[0,0,0,0]	√	
11	√					√	√	N/A	0	0	0	1	0	0	1	0	[0,0,0,0]	√	
13	√	√				√	√	N/A	0	0	0	0	0	1	1	0	[0,0,0,0]	√	
14	√				√	√	√	N/A	0	0	0	1	1	0	1	0	[0,0,0,0]	√	
15		√				√		N/A	1	0	1	0	0	1	0	0	[0,0,0,0]	√	
17		√				√	√	N/A	0	0	1	0	0	1	0	0	[0,0,0,0]	√	
18						√		N/A	1	0	1	1	0	0	0	0	[0,0,0,0]	√	
20						√	√	N/A	0	0	1	1	0	0	0	0	[0,0,0,0]	√	
21					√	√		N/A	1	0	1	1	1	0	0	0	[0,0,0,0]	√	
23					√	√	√	N/A	0	0	1	1	1	0	0	0	[0,0,0,0]	√	
DSP host operation mode: Timer-0 output is enabled																			
6	√					√		X	1	0	0	1	0	0	1	0	[0,0,0,0]	√	
8	√	√				√		X	1	0	0	0	0	1	1	0	[0,0,0,0]	√	
10	√				√	√		X	1	0	0	1	1	0	1	0	[0,0,0,0]	√	
11	√					√	√	X	0	0	0	1	0	0	1	0	[0,0,0,0]	√	
13	√	√				√	√	X	0	0	0	0	0	1	1	0	[0,0,0,0]	√	
14	√				√	√	√	X	0	0	0	1	1	0	1	0	[0,0,0,0]	√	
15		√				√		X	1	0	1	0	0	1	0	0	[0,0,0,0]	√	

17		√				√	√	X	0	0	1	0	0	1	0	0	[0,0,0,0]	√	
18						√		X	1	0	1	1	0	0	0	0	[0,0,0,0]	√	
20						√	√	X	0	0	1	1	0	0	0	0	[0,0,0,0]	√	
21					√	√		X	1	0	1	1	1	0	0	0	[0,0,0,0]	√	
23					√	√	√	X	0	0	1	1	1	0	0	0	[0,0,0,0]	√	
DSP stand-alone operation mode: Timer-1 output is enabled																			
7	√						√	N/A	0	1	0	1	0	0	1	0	[0,0,0,0]	√	
9	√	√					√	N/A	0	1	0	0	0	1	1	0	[0,0,0,0]	√	
11	√						√	√	N/A	0	0	0	1	0	0	1	[0,0,0,0]	√	
12	√				√		√	N/A	0	1	0	1	1	0	1	0	[0,0,0,0]	√	
13	√	√				√	√	N/A	0	0	0	0	0	1	1	0	[0,0,0,0]	√	
14	√				√	√	√	N/A	0	0	0	1	1	0	1	0	[0,0,0,0]	√	
16		√					√	N/A	0	1	1	0	0	1	0	0	[0,0,0,0]	√	
17		√				√	√	N/A	0	0	1	0	0	1	0	0	[0,0,0,0]	√	
19							√	N/A	0	1	1	1	0	0	0	0	[0,0,0,0]	√	
20					√		√	N/A	0	0	1	1	0	0	0	0	[0,0,0,0]	√	
22					√		√	N/A	0	1	1	1	1	0	0	0	[0,0,0,0]	√	
23					√	√	√	N/A	0	0	1	1	1	0	0	0	[0,0,0,0]	√	
DSP host operation mode: Timer-1 output is enabled																			
7	√						√	X	0	1	0	1	0	0	1	0	[0,0,0,0]	√	
9	√	√					√	X	0	1	0	0	0	1	1	0	[0,0,0,0]	√	
11	√						√	√	X	0	0	0	1	0	0	1	[0,0,0,0]	√	
12	√				√		√	X	0	1	0	1	1	0	1	0	[0,0,0,0]	√	
13	√	√				√	√	X	0	0	0	0	0	1	1	0	[0,0,0,0]	√	
14	√				√	√	√	X	0	0	0	1	1	0	1	0	[0,0,0,0]	√	
16		√					√	X	0	1	1	0	0	1	0	0	[0,0,0,0]	√	
17		√				√	√	X	0	0	1	0	0	1	0	0	[0,0,0,0]	√	
19							√	X	0	1	1	1	0	0	0	0	[0,0,0,0]	√	
20					√		√	X	0	0	1	1	0	0	0	0	[0,0,0,0]	√	
22					√		√	X	0	1	1	1	1	0	0	0	[0,0,0,0]	√	
23					√	√	√	X	0	0	1	1	1	0	0	0	[0,0,0,0]	√	

Notes:

1. All peripherals are disabled as default on the DSP reset condition.
2. '√' denotes enabled peripheral.
3. 'X' denotes don't care condition.
4. 'N/A' denotes that this bit is not available for this operation mode.
5. Configuration ID is used in TORNADO-E2/6xxx DSP control software utilities (refer to [Appendix F](#)).
6. McASP-0 audio serial port is enabled without AXR0[5], AXR0[6], AXR0[7] and AMUTE0 peripheral pins in these configurations.

External General Purpose I/O (GPIO)

TORNADO-E2/6xxx DSP controllers provide general purpose 8-bit I/O (GPIO), which can be used as external control I/O signals.

TORNADO-E2/6xxx on-board GPIO-0..7 general purpose I/O pins are available at JP13 connector (refer to [Figure A-1](#) and subsection "[JP13 GPIO general purpose digital I/O connector](#)" for more details).

GPIO-0..7 external general purpose I/O pins can be individually configured as either input or output pins via [DSP_GPIO_DIR_RG](#) and [DSP_GPIO_DATA_RG](#) DSP external control registers.

For *TORNADO-E2/6xxx* board, the *GPIO-0* pin can be also used to generate DSP interrupt request via any of the DSP EXT_INT4..EXT_INT7 and NMI external interrupt (refer to [Table 2-14](#) for more details).

DSP external interrupt requests

TORNADO-E2/6xxx DSP controllers provide software configured interrupt request selectors for each of TMS320C6xxx DSP EXT_INT4..EXT_INT7 and NMI external interrupt request inputs ([Figure 2-3](#)). This allows outstanding flexibility for run-time control of DSP external interrupt sources and allows to meet requirements of virtually any DSP application.

Selection of particular interrupt request sources for each of DSP EXT_INT4..EXT_INT7 and NMI external interrupt request inputs is performed via the [DSP_EXT_INT4_SEL_RG](#), [DSP_EXT_INT5_SEL_RG](#), [DSP_EXT_INT6_SEL_RG](#), [DSP_EXT_INT7_SEL_RG](#) and [DSP_NMI_SEL_RG](#) DSP external control registers correspondingly.

Each of interrupt request selectors for DSP EXT_INT4..EXT_INT7 external interrupt request inputs allows selection from 15 different interrupt request sources, whereas interrupt request selector for the DSP NMI external interrupt request input provides limited functionality and allows selection from only 3 interrupt request sources. All DSP external interrupt selector registers default to the 00H state on the DSP reset condition, which corresponds to disabled interrupt requests.

NOTE

TMS320C6xxx DSP on-chip *EXTERNAL INTERRUPT POLARITY* register (@0x019C0008) must be set to the 0x00000000 value in order to enable detection of external interrupt requests on low-to-high transitions at the corresponding external interrupt request inputs.

As default, TMS320C6xxx DSP on-chip high/low interrupt multiplexer registers (@0x019C0000 and @0x019C0004) map DSP external EXT_INT4..7 interrupt request inputs to the DSP internal #4..#7 interrupt requests/priorities correspondingly on the DSP power-on and reset conditions. However, if this default DSP on-chip interrupt selection priority is not satisfactory for user application, then TMS320C6xxx DSP on-chip high/low interrupt multiplexer registers have to be re-configured to meet application requirements.

NOTE

For more information about how to configure the TMS320C6xxx DSP on-chip high/low interrupt multiplexer registers refer to original TI TMS320C6xxx documentation, which is provided in electronic form along with this user's guide

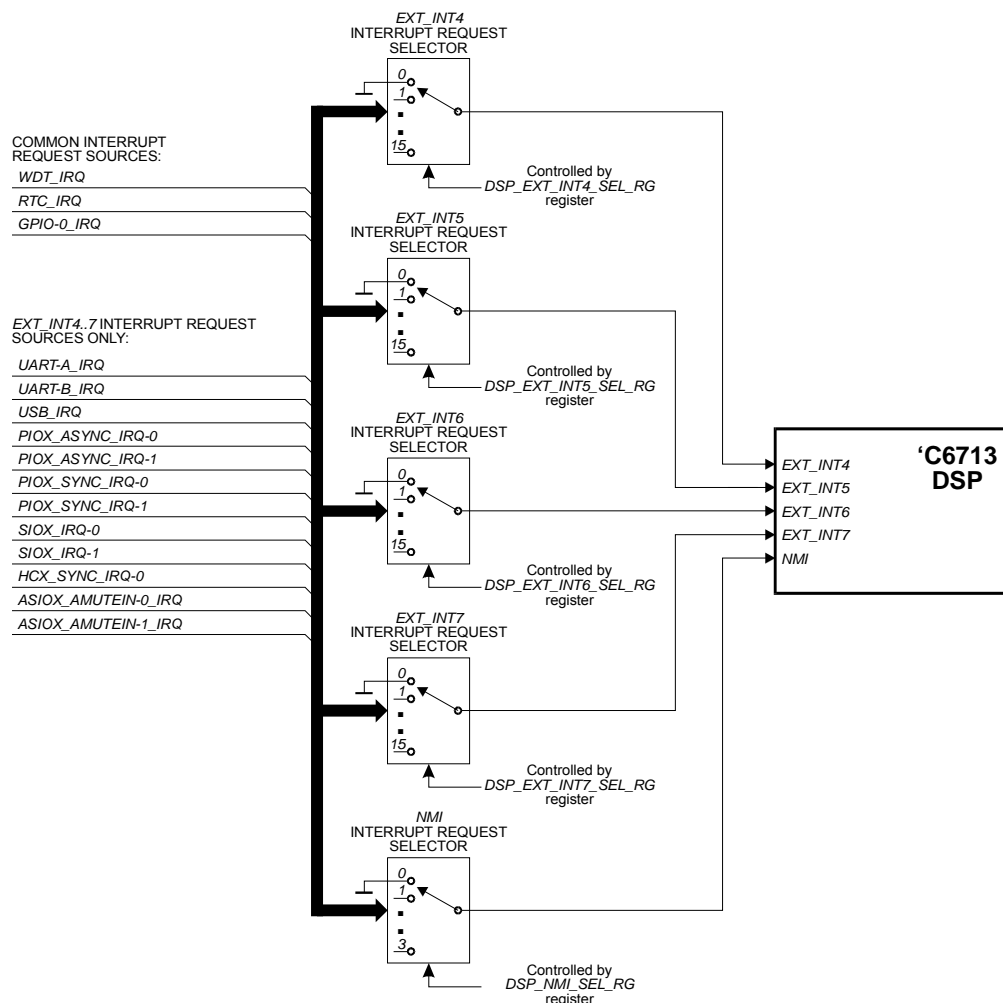


Figure 2-3. Interrupt request selectors for DSP EXT_INT4..7/NMI external interrupt request inputs of TORNADO-E2/6713 DSP controller.

DSP-to-HCX interrupt request

TORNADO-E2/6xxx DSP controllers support generation of interrupt request from on-board DSP to host *HCX* controller via any of *HCX* interrupt request lines (`HCX_X1_AIRQ-0..3`) using `DSP_HPI_HINT` DSP-to-host interrupt request output from DSP on-chip HPI port. `DSP_HPI_HINT` is actually the *HINT* bit of DSP on-chip HPI port control register (HPIC).

Refer to subsection “[Processing of DSP-to-host interrupt request via HCX-ASYNC interface](#)” later in this chapter for more details about generation of DSP-to-host interrupt request from on-board DSP.

HCX-to-DSP interrupt request

TORNADO-E2/6xxx DSP controllers support generation of interrupt request from host *HCX* controller to on-board DSP via DSP on-chip HPI port. This interrupt is actually the *DSPINT* bit of DSP on-chip HPI port control register (HPIC).

Refer to subsection “[Generation of Host-to-DSP interrupt request via HCX-ASYNC interface](#)” later in this chapter for more details about generation of host-to-DSP interrupt request to TMS320C6xxx DSP via DSP on-chip HPI port.

2.3 DSP external control registers area

DSP external control registers are used for run-time configuration and control of on-board system controller, parallel peripherals (DUART, USB, RTC controllers, DCM expansion site interfaces), DSP external environment (external interrupt selectors, WDT control, etc) and for achieving system information about *TORNADO-E2/6xxx* DSP controllers.

DSP external control registers area includes the following control registers:

- read-only system information registers:
 - read-only [DSP_DSP_CNF_RG](#) register (DSP operation mode, DSP bootmode)
 - read-only [DSP_DCM_CNF_RG](#) register (DCM installation status)
 - read-only [DSP_SYS_CNF1_RG](#) register (device ID)
 - read-only [DSP_SYS_CNF2_RG](#) register (board revision ID, DSP clock frequency ID, spread spectrum clock presence ID)
 - read-only [DSP_SYS_CNF3_RG](#) register (memory length IDs for external DSP memories)
 - read-only [DSP_SYS_CNF4_RG](#) register (external parallel peripherals ID: RTC, USB)
- DSP environment control registers:
 - [DSP_NMI_SEL_RG](#) register (DSP NMI non-maskable interrupt source selector) and [DSP_EXT_INT4_SEL_RG..DSP_EXT_INT7_SEL_RG](#) registers (DSP EXT_INT4..7 external interrupt source selectors)
 - [DSP_FLASH_PAGE_RG](#) register (FLASH memory page)
 - [DSP_FLASH_CNTR_RG](#) register (FLASH write enable control)
 - [DSP_WDT_RTC_CNTR_RG](#) and write-only [DSP_WDT_RESET_RG](#) registers (μP Supervisory WDT and RTC control and WDT reset)
 - [DSP_GPIO_DATA_RG](#) and [DSP_GPIO_DIR_RG](#) registers (GPIO data and direction control)
- DCM site interfaces control registers:
 - [DSP_DCM_RESET_RG](#) register (software reset control for SIOX/PIOX2 DCM sites)
 - [DSP_PORTS_CNTR_RG](#) register (DSP on-chip serial ports buffers control: McBSP-0/1, McASP-0/1, I²C-1)
 - [DSP_SIOX_XIO_CNF_RG](#) and [DSP_SIOX_XIO_DATA_RG](#) registers (TM_XIO-0/1 mode/direction and data control)
 - [DSP_HCX_SYNC_PAGE_RG](#) register (32-bit synchronous HCX DCM interface address page).

The following subsections provide detailed description of DSP external control registers bit settings.

DSP_DSP_CNF_RG DSP external control register for identification of the DSP start-up configuration

Read-only *DSP_DSP_CNF_RG* DSP external control register is used by DSP application to identify the DSP bootmode configuration, DSP operation mode and HPI enable status of *TORNADO-E2/6xxx* DSP controller.

DSP_DSP_CNF_RG register (r)

<i>DSP_OPMODE</i> (r)	<i>DSP_HPI_ENABLE</i> (r) (TORNADO-E2/6713 only)	0	0	0	0	0	<i>DSP_BMODE</i> (r)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-8](#) provides details about *DSP_DSP_CNF_RG* register bits.

Table 2-8. *DSP_DSP_CNF_RG* register bits.

register bits	access mode	value on DSP reset	Description
<i>DSP_BMODE</i>	r	-	<p>This bit returns DSP bootmode configuration in accordance with Table 2-1. Note, that DSP bootmode configuration must be processed in combination with the <i>DSP_OPMODE</i> bit of this register, which defines DSP operation mode configuration.</p> <p><i>DSP_BMODE</i> = 0 denotes that <i>DSP</i> has booted either in the <i>SA/BMODE-NONE</i> bootmode (in case <i>DSP_OPMODE</i> bit is in the '0' state), or in the <i>HOST/BMODE-HPI</i>, or in the <i>HOST/BMODE-NONE</i> bootmode (in case <i>DSP_OPMODE</i> bit is in the '1' state).</p> <p><i>DSP_BMODE</i> = 1 denotes that <i>DSP</i> has started either in the '<i>SA/BMODE-FLASH8</i>' bootmode (in case <i>DSP_OPMODE</i> bit is in the '0' state), or in the '<i>HOST/BMODE-FLASH8</i>' bootmode (in case <i>DSP_OPMODE</i> bit is in the '1' state).</p>
<i>DSP_HPI_ENABLE</i> (<i>TORNADO-E2/6713</i> only)	r	-	<p>This bit is valid in <i>DSP host operation mode</i> only and indicates whether DSP on-chip HPI port is enabled. It always reads as '0' in <i>DSP stand-alone operation mode</i>. HPI port enable is set by host <i>HCX</i> application via <i>DSP_HPI_EN</i> bit of HCX_AX_CNTR2_RG <i>HCX</i> control register. HPI port is always disabled when <i>TORNADO-E2/6713</i> on-board DSP is in the <i>DSP stand-alone operation mode</i> thus enabling all DSP on-chip serial peripherals.</p> <p><i>DSP_HPI_ENABLE</i> = 0 denotes that DSP on-chip HPI port is disabled.</p> <p><i>DSP_HPI_ENABLE</i> = 1 denotes that DSP on-chip HPI port is enabled.</p>
<i>DSP_OPMODE</i>	r	-	<p>This bit returns current DSP operation mode in accordance with Table 2-1.</p> <p><i>DSP_OPMODE</i> = 0 denotes that DSP is in the <i>DSP stand-alone operation mode</i>.</p> <p><i>DSP_OPMODE</i> = 1 denotes that DSP is in the <i>DSP host operation mode</i>.</p>

Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

***DSP_DCM_CNF_RG* DSP external control register for identification of installed DCM**

Read-only *DSP_DCM_CNF_RG* DSP external control register is used to identify installed DCMs.

***DSP_DCM_CNF_RG* register (r)**

<i>DSP_HCX_DCM_TYPE1</i> (r)	<i>DSP_HCX_DCM_TYPE1</i> (r)	0	0	<i>DSP_ASIOX_DCM_TYPE1</i> (r)	<i>DSP_ASIOX_DCM_TYPE0</i> (r)	<i>DSP_PIOX_DCM_TYPE1</i> (r)	<i>DSP_PIOX_DCM_TYPE0</i> (r)
Bit-7	bit-6	bit-5	bit-4	Bit-3	Bit-2	bit-1	Bit-0

[Table 2-9](#) provides details about the *DSP_DCM_CNF_RG* register bits.

Table 2-9. *DSP_DCM_CNF_RG* register bits.

register bits	access mode	value on DSP reset	Description
<i>{DSP_PIOX_DCM_TYPE1..0}</i>	r	-	These bits identify presence and type of installed <i>PIOX</i> DCM. <i>{DSP_PIOX_DCM_TYPE1..0} = [0,0]</i> denotes that <i>PIOX</i> DCM is not installed. <i>{DSP_PIOX_DCM_TYPE1..0} = [0,1]</i> denotes that <i>PIOX</i> DCM has asynchronous-only interface. <i>{DSP_PIOX_DCM_TYPE1..0} = [1,1]</i> denotes that <i>PIOX</i> DCM has both asynchronous and synchronous interfaces. <i>{DSP_PIOX_DCM_TYPE1..0} = [1,0]</i> setting is reserved.
<i>{DSP_ASIOX_DCM_TYPE1..0}</i>	r	-	These bits identify presence and type of installed <i>ASIOX</i> rev.D DCM. <i>{DSP_ASIOX_DCM_TYPE1..0} = [0,0]</i> denotes that <i>ASIOX</i> rev.D DCM is not installed. <i>{DSP_ASIOX_DCM_TYPE1..0} = [0,1]</i> denotes that <i>ASIOX</i> rev.D DCM has serial ports (either McBSP or McASP) only. <i>{DSP_ASIOX_DCM_TYPE1..0} = [1,1]</i> denotes that <i>ASIOX</i> rev.D DCM has serial ports and parallel interface. <i>{DSP_ASIOX_DCM_TYPE1..0} = [1,0]</i> setting is reserved.
<i>{DSP_HCX_DCM_TYPE1..0}</i>	r	-	These bits identify presence and type of installed <i>HCX</i> rev.A DCM. <i>{DSP_HCX_DCM_TYPE1..0} = [0,0]</i> denotes that <i>HCX</i> rev.A DCM is not installed. <i>{DSP_HCX_DCM_TYPE1..0} = [0,1]</i> denotes that <i>HCX</i> rev.A DCM has asynchronous-only interface. <i>{DSP_HCX_DCM_TYPE1..0} = [1,1]</i> denotes that <i>HCX</i> rev.A DCM has both asynchronous and slave synchronous interfaces. <i>{DSP_HCX_DCM_TYPE1..0} = [1,0]</i> setting is reserved.

Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

***DSP_SYS_CNF1_RG* DSP external control register for identification of TORNADO-E2/6xxx DSP controller**

Read-only *DSP_SYS_CNF1_RG* DSP external control register is used by DSP application to identify the type of *TORNADO-E2/6xxx* DSP controller.

***DSP_SYS_CNF1_RG* register (r)**

<i>DEV_ID-7</i> (r)	<i>DEV_ID-6</i> (r)	<i>DEV_ID-5</i> (r)	<i>DEV_ID-4</i> (r)	<i>DEV_ID-3</i> (r)	<i>DEV_ID-2</i> (r)	<i>DEV_ID-1</i> (r)	<i>DEV_ID-0</i> (r)
Bit-7	bit-6	bit-5	bit-4	Bit-3	Bit-2	bit-1	Bit-0

[Table 2-10](#) provides details about the *DSP_SYS_CNF1_RG* register bits.

Table 2-10. DSP_SYS_CNF1_RG register bits.

register bits	access mode	value on DSP reset	Description
{DEV_ID-7..0}	r	-	These bits return <i>TORNADO-E2/6xxx</i> device ID. {DEV_ID-7..0} = [0,0,0,0,0,0,0,1] corresponds to <i>TORNADO-E2/6713</i> DSP controller. All other {DEV_ID-7..0} field settings are reserved.

Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

NOTE

Read-only ID data, which is returned via [DSP_SYS_CNF1_RG](#) DSP external control register, is also available via the corresponding bits of [HCX_AX_SYS_CNF1_RG](#) HCX control register (refer to section “[HCXDCM Site Interface](#)” for more details).

DSP_SYS_CNF2_RG DSP external control register for identification of board revision, DSP clock frequency and EMIF spread spectrum clock presence

Read-only *DSP_SYS_CNF2_RG* DSP external control register is used by DSP application to identify *TORNADO-E2/6xxx* DSP controller board revision, DSP core clock frequency and presence of spread spectrum clock for DSP EMIF in order to minimize RF radiation.

DSP_SYS_CNF2_RG register (r)

0	DSP_SSCLK_ID (r)	DSP_CLK_FREQ_ID-1 (r)	DSP_CLK_FREQ_ID-0 (r)	REV_ID-3 (r)	REV_ID-2 (r)	REV_ID-1 (r)	REV_ID-0 (r)
Bit-7	bit-6	bit-5	bit-4	Bit-3	Bit-2	bit-1	Bit-0

[Table 2-11](#) provides details about the *DSP_SYS_CNF2_RG* register bits.

Table 2-11. DSP_SYS_CNF2_RG register bits.

register bits	access mode	value on DSP reset	Description
{REV_ID-3..0}	r	-	Return board firmware revision ID for <i>TORNADO-E2/6xxx</i> DSP controllers. {REV_ID-3..0} = [0,0,0,0] is reserved. {REV_ID-3..0} = [0,0,0,1] corresponds to firmware revision 1A of <i>TORNADO-E2/6713</i> .
{DSP_CLK_FREQ_ID-1..0}	r	-	Return DSP core clock frequency ID for on-board TMS320C6xxx DSP. {DSP_CLK_FREQ_ID-1..0} = [0,0] setting is reserved. {DSP_CLK_FREQ_ID-1..0} = [0,1] corresponds to the 300 MHz TMS320C6713 DSP. This setting is available for <i>TORNADO-E2/6713</i> DSP controller firmware rev.1A only.

<i>DSP_SSCLK_ID</i>	r	-	Identifies presence of spread spectrum clock for DSP EMIF, which is used to minimize board's RF radiation. <i>DSP_SSCLK_ID</i> = 0 denotes that DSP EMIF does not have spectrum clock. <i>DSP_SSCLK_ID</i> = 1 denotes that DSP EMIF has spread spectrum clock.
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Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

NOTE

Read-only ID data, which is returned via [DSP_SYS_CNF2_RG](#) DSP external control register, is also available via the corresponding bits of [HCX_AX_SYS_CNF2_RG](#) HCX control register (refer to section “[HCXDCM Site Interface](#)” for more details).

DSP_SYS_CNF3_RG DSP external control register for identification of on-board external DSP memories

Read-only *DSP_SYS_CNF3_RG* DSP external control register is used by DSP application to identify capacity of TORNADO-E2/6xxx on-board SBSRAM, SDRAM and FLASH memories.

DSP application must know the capacity for on-board SBSRAM, SDRAM and FLASH memories in order to adjust length of data arrays allocated in these memories. Also, knowledge of on-board SDRAM memory capacity is required in order to correctly configure TMS320C6xxx DSP EMIF SDRAM control registers (refer to [Table 2-3](#) for more details).

DSP_SYS_CNF3_RG register (r)

<i>FLASH_LEN_ID-3</i> (r)	<i>FLASH_LEN_ID-2</i> (r)	<i>FLASH_LEN_ID-1</i> (r)	<i>FLASH_LEN_ID-0</i> (r)	<i>SDRAM_LEN_ID-1</i> (r)	<i>SDRAM_LEN_ID-0</i> (r)	<i>SBSRAM_LEN_ID-1</i> (r)	<i>SBSRAM_LEN_ID-0</i> (r)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-12](#) provides details about the *DSP_SYS_CNF3_RG* register bits.

Table 2-12. *DSP_SYS_CNF3_RG* register bits.

register bits	access mode	value on DSP reset	Description
{ <i>SBSRAM_LEN_ID-1..0</i> }	r	-	Return capacity ID for on-board SBSRAM memory. Refer to Table 2-2 for more details. { <i>SBSRAM_LEN_ID-1..0</i> } = [0,0] denotes that SBSRAM is not installed. { <i>SBSRAM_LEN_ID-1..0</i> } = [0,1] corresponds to 128Kx32 SBSRAM. { <i>SBSRAM_LEN_ID-1..0</i> } = [1,0] corresponds to 512Kx32 SBSRAM.
{ <i>SDRAM_LEN_ID-1..0</i> }	r	-	Return capacity ID for on-board SDRAM memory. Refer to Table 2-2 for more details. { <i>SDRAM_LEN_ID-1..0</i> } = [0,0] denotes that SDRAM is not installed. { <i>SDRAM_LEN_ID-1..0</i> } = [0,1] corresponds to 4Mx32 SDRAM. { <i>SDRAM_LEN_ID-1..0</i> } = [1,0] corresponds to 16Mx32 SDRAM.

{FLASH_LEN_ID-3..0}	r	-	<p>Return the capacity ID for on-board FLASH memory. Refer to Table 2-2 and subsection “FLASH memory area” for more details.</p> <p>{FLASH_LEN_ID-3..0} = [0,0,0,0] denotes that FLASH is not installed.</p> <p>{FLASH_LEN_ID-3..0} = [0,0,0,1] corresponds to 512Kx8 FLASH.</p> <p>{FLASH_LEN_ID-3..0} = [0,0,1,0] corresponds to 1Mx8 FLASH.</p> <p>{FLASH_LEN_ID-3..0} = [0,0,1,1] corresponds to 8Mx8 FLASH.</p> <p>{FLASH_LEN_ID-3..0} = [0,1,0,0] corresponds to 64Mx8 FLASH.</p>
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- Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
 2. Highlighted configurations correspond to default settings on DSP reset condition.

NOTE

Read-only ID data, which is returned via [DSP_SYS_CNF3_RG](#) DSP external control register, is also available via the corresponding bits of [HCX_AX_SYS_CNF3_RG](#) HCX control register (refer to section “[HCXDCM Site Interface](#)” for more details).

DSP_SYS_CNF4_RG DSP external control register for identification of on-board external parallel peripherals

Read-only [DSP_SYS_CNF4_RG](#) DSP external control register is used by DSP application to identify *TORNADO-E2/6xxx* DSP controller external parallel peripherals (USB, RTC controllers).

DSP_SYS_CNF4_RG register (r)

0	0	0	0	RTC_ID-1 (r)	RTC_ID-0 (r)	USB_ID-1 (r)	USB_ID-0 (r)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-13](#) provides details about the [DSP_SYS_CNF4_RG](#) register bits.

Table 2-13. DSP_SYS_CNF4_RG register bits.

register bits	access mode	value on DSP reset	Description
{USB_ID-1..0}	r	-	<p>Return ID for on-board USB controller.</p> <p>{USB_ID-1..0} = [0,0] denotes that USB controller is not installed.</p> <p>{USB_ID-1..0} = [0,1] corresponds to Lucent Technologies USS-820 USB 1.1 one-channel device USB controller.</p> <p>{USB_ID-1..0} = [1,0] corresponds to PLX/Netchip NET2272 USB 2.0 one-channel device USB controller.</p> <p>{USB_ID-1..0} = [1,1] corresponds to Philips ISP1761USB 2.0 three-channel host/device USB controller.</p>
{RTC_ID-1..0}	r	-	<p>Return ID for on-board RTC controller.</p> <p>{RTC_ID-1..0} = [0,0] denotes that RTC controller is not installed.</p> <p>{RTC_ID-1..0} = [0,1] corresponds to Dallas Semiconductor DS1501 RTC controller installed.</p>

- Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
 2. Highlighted configurations correspond to default settings on DSP reset condition.

DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG, DSP_EXT_INT7_SEL_RG and DSP_NMI_SEL_RG DSP external control registers for selection of interrupt request source for DSP EXT_INT4..7 and NMI external interrupt requests

Selection of particular interrupt request sources for each of DSP_EXT_INT4..EXT_INT7 and NMI external interrupt request inputs is performed via the DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG, DSP_EXT_INT7_SEL_RG and DSP_NMI_SEL_RG DSP external control registers correspondingly.

DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG and DSP_EXT_INT7_SEL_RG registers (r/w)

0	0	0	0	INT_SEL-3 (r/w, 0+)	INT_SEL-2 (r/w, 0+)	INT_SEL-1 (r/w, 0+)	INT_SEL-0 (r/w, 0+)
bit-7	bit-6	bit-5	Bit-4	Bit-3	bit-2	bit-1	bit-0

DSP_NMI_SEL_RG register (r/w)

0	0	0	0	0	0	INT_SEL-1 (r/w, 0+)	INT_SEL-0 (r/w, 0+)
bit-7	bit-6	bit-5	Bit-4	Bit-3	bit-2	bit-1	bit-0

Table 2-14 provides details about selection of interrupt request sources for DSP external interrupt request inputs via DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG, DSP_EXT_INT7_SEL_RG and DSP_NMI_SEL_RG DSP external control registers of TORNADO-E2/6xxx DSP controllers.

Table 2-14. Interrupt request sources for DSP interrupt selectors of TORNADO-E2/6713 DSP controller.

DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG, DSP_EXT_INT7_SEL_RG, DSP_NMI_SEL_RG register bits				interrupt request source
INT_SEL-3 ¹⁾	INT_SEL-2 ¹⁾	INT_SEL-1	INT_SEL-0	
common interrupt request sources for DSP_EXT_INT4..7 and NMI external interrupt request inputs				
0	0	0	0	Interrupt is disabled.
0	0	0	1	Interrupt request on WDT expiration event (WDT_IRQ). Refer to subsection “ On-board watch-dog timer (WDT) ” for more details.
0	0	1	0	Interrupt request from RTC controller (RTC_IRQ). Refer to subsection “ Real-time clock (RTC) controller ” and to Appendix J for more details.
0	0	1	1	Interrupt request on the falling edge of GPIO-0 pin (GPIO-0_IRQ) at connector JP13. Refer to subsection “ External General Purpose I/O (GPIO) ” for more details.
optional interrupt request sources for DSP_EXT_INT4..7 external interrupt request inputs only (not available for NMI external interrupt request input)				
0	1	0	0	Interrupt request from channel-A of DUART (UART-A_IRQ). Refer to subsection “ Dual-channel UART ” and to Appendix H for more details.

0	1	0	1	Interrupt request from channel-B of DUART (UART-B_IRQ). Refer to subsection "Dual-channel UART" and to Appendix H for more details.
0	1	1	0	<p>Interrupt request from USB controller. Interrupt source from USB controller is configuration specific.</p> <p>For USB 1.1 and USB 2.0 one-channel device USB controllers there is only one interrupt request from the USB controller (USB_IRQ).</p> <p>For USB 2.0 three-channel host/device USB controller, there are four independent interrupt requests, which are configured as following:</p> <ul style="list-style-type: none"> interrupt request from USB 2.0 Peripheral controller (USB_DC_IRQ) is routed to DSP EXT_INT4 external interrupt request input interrupt request from USB 2.0 Host controller (USB_HC_IRQ) is routed to DSP EXT_INT5 external interrupt request input DMA request from USB 2.0 Peripheral controller (USB_DC_DREQ) is routed to DSP EXT_INT6 external interrupt request input DMA request from USB 2.0 Host controller (USB_HC_DREQ) is routed to DSP EXT_INT7 external interrupt request input. <p>Refer to subsection "USB interface" and to Appendix I for more details.</p>
0	1	1	1	PIOX_ASYNC_IRQ-0 interrupt request from asynchronous interface of PIOX2 DCM site. Refer to Appendix D for more details.
1	0	0	0	PIOX_ASYNC_IRQ-1 interrupt request from asynchronous interface of PIOX2 DCM site. Refer to Appendix D for more details.
1	0	0	1	PIOX_SYNC_IRQ-0 interrupt request from synchronous interface of PIOX2 DCM site. Refer to Appendix D for more details.
1	0	1	0	PIOX_SYNC_IRQ-1 interrupt request from synchronous interface of PIOX2 DCM site. Refer to Appendix D for more details.
1	0	1	1	SIOX_IRQ-0 interrupt request from SIOX rev.B DCM site interface. Refer to Appendix C for more details.
1	1	0	0	SIOX_IRQ-1 interrupt request from SIOX rev.B DCM site interface. Refer to Appendix C for more details.
1	1	0	1	HGX_SYNC_IRQ-0 interrupt request from synchronous interface of HGX rev.A DCM site. Refer to section " HGX DCM Site Interface " for more details.
1	1	1	0	ASIOX_AMUTEIN-0_IRQ interrupt request from McASP-0 AMUTEIN0 input pin of ASIOX rev.D DCM site interface. Refer to Appendix C for more details.
1	1	1	1	ASIOX_AMUTEIN-1_IRQ interrupt request from McASP-1 AMUTEIN1 input pin of ASIOX rev.D DCM site interface. Refer to Appendix C for more details.

Note:

1. This bit is not available for DSP_NMI_SEL_RG register.
2. Highlighted configurations correspond to default settings on DSP reset condition.

DSP_PORTS_CNTR_RG DSP external control register for on-board serial ports buffers configuration (TORNADO-E2/6713 only)

DSP_PORTS_CNTR_RG DSP external control register is used to configure TORNADO-E2/6713 on-board buffers and signal routing for DSP McBSP-0/1, McASP-0/1, I²C-1 serial ports buffers.

NOTE

DSP_PORTS_CNTR_RG DSP external control register setting must strongly match setting of TMS320C6713 DSP on-chip *DEVCFG* register as it is shown in [Table 2-7](#). Incorrect register setting may result in damage of on-board hardware.

***DSP_PORTS_CNTR_RG* register (r/w)**

<i>DSP_I2C1_BUF_EN</i> (r/w, 0+)	<i>DSP_MCBSP1_BUF_EN</i> (r/w, 0+)	<i>DSP_MCBSP0_BUF_EN</i> (r/w, 0+)	<i>DSP_MCASP1_BUF_EN</i> (r/w, 0+)	<i>DSP_MCASP0_BUF_EN4</i> (r/w, 0+)	<i>DSP_MCASP0_BUF_EN3</i> (r/w, 0+)	<i>DSP_MCASP0_BUF_EN2</i> (r/w, 0+)	<i>DSP_MCASP0_BUF_EN1</i> (r/w, 0+)
Bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-15](#) provides details about the *DSP_PORTS_CNTR_RG* register bits.

Table 2-15. *DSP_PORTS_CNTR_RG* register bits for TORNADO-E2/6713.

register bits	Access mode	value on DSP reset	Description
{ <i>DSP_MCASP0_BUF_EN4..1</i> }	r/w	[0,0,0,0]	Enable McASP-0 DSP audio serial port buffers. { <i>DSP_MCASP0_BUF_EN4..1</i> } = [0,0,0,0] disables McASP-0 DSP audio serial port buffers. For other available settings refer to Table 2-7 .
<i>DSP_MCASP1_BUF_EN</i>	r/w	0	Enables McASP-0 DSP audio serial port buffers. <i>DSP_MCASP1_BUF_EN</i> = 0 disables McASP-1 DSP audio serial port buffer. <i>DSP_MCASP1_BUF_EN</i> = 1 enables McASP-1 DSP audio serial port buffer. This setting allows McASP-1 DSP audio serial port signals to route to ASIOX rev.D DCM site. For TORNADO-E2/6713, McASP-1 DSP audio serial port peripheral pins can be enabled only when TMS320C6713 HPI port is disabled (refer to Table 2-7).
<i>DSP_MCBSP0_BUF_EN</i>	r/w	0	Enables McBSP-0 DSP serial port buffer. <i>DSP_MCBSP0_BUF_EN</i> = 0 disables McBSP-0 DSP serial port external buffer. <i>DSP_MCBSP0_BUF_EN</i> = 1 enables McBSP-0 DSP serial port buffer. This setting allows McBSP-0 DSP serial port signals to route to SIOX rev.B and ASIOX rev.D DCM sites. For TORNADO-E2/6713, McBSP-0 DSP serial port peripheral pins shall be also enabled via <i>DEVCFG</i> TMS320C6713 DSP on-chip device configuration register (@0x019C0200) (refer to Table 2-7).
<i>DSP_MCBSP1_BUF_EN</i>	r/w	0	Enables McBSP-1 DSP serial port buffer. <i>DSP_MCBSP1_BUF_EN</i> = 0 disables McBSP-1 DSP serial port buffer. <i>DSP_MCBSP1_BUF_EN</i> = 1 setting enables McBSP-1 DSP serial port buffer. This setting allows McBSP-1 DSP serial port signals to route to SIOX rev.B and ASIOX rev.D DCM sites. For TORNADO-E2/6713 McBSP-1 DSP serial port peripheral pins shall be also enabled via <i>DEVCFG</i> TMS320C6713 DSP on-chip device configuration register (@0x019C0200) (refer to Table 2-7).

<i>DSP_I2C1_BUF_EN</i>	r/w	0	<p>Enables I²C-1 DSP serial port buffer.</p> <p><i>DSP_I2C1_BUF_EN</i> = 0 setting disables I²C-1 DSP serial port buffer.</p> <p><i>DSP_I2C1_BUF_EN</i> = 1 setting enables I²C-1 DSP serial port buffer. This setting allows I²C-1 DSP serial port signals to route to JP15 I²C-1 interface connector (refer to subsection “JP14, JP15 I2C interface connectors”).</p> <p>For <i>TORNADO-E2/6713</i>, I²C-1 DSP serial port peripheral pins shall be also enabled via <i>DEVCFG</i> TMS320C6713 DSP on-chip device configuration register (@0x019C0200) (refer to Table 2-7).</p>
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Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

IMPORTANT NOTE

It is recommended, that for safety reasons the TMS320C6713 DSP on-chip *DEVCFG* device configuration register (@0x019C0200) and [DSP_PORTS_CNTR_RG](#) DSP external control register bits are not directly set from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user’s guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

Refer to subsection “[DSP on-chip serial peripherals \(McBSP, McASP, I2C ports\)](#)” in this chapter for more details about DSP on-chip serial ports configuration.

DSP_FLASH_PAGE_RG DSP external FLASH memory page control register

DSP_FLASH_PAGE_RG DSP external control register is used to select currently addressed 1Mx8 FLASH memory page in case on-board FLASH has capacity either 8Mx8 or 64Mx8.

***DSP_FLASH_PAGE_RG* register (r/w)**

0	0	<i>FPAGE-5</i> (r/w, 0+) (64Mx8 FLASH)	<i>FPAGE-4</i> (r/w, 0+) (64Mx8 FLASH)	<i>FPAGE-3</i> (r/w, 0+) (64Mx8 FLASH)	<i>FPAGE-2</i> (r/w, 0+) (8M/64Mx8 FLASH)	<i>FPAGE-1</i> (r/w, 0+) (8M/64Mx8 FLASH)	<i>FPAGE-0</i> (r/w, 0+) (8M/64Mx8 FLASH)
		0 (r) (512K/1M/8Mx8 FLASH)	0 (r) (512K/1M/8Mx8 FLASH)	0 (r) (512K/1M/8Mx8 FLASH)	0 (r) (512K/1Mx8 FLASH)	0 (r) (512K/1Mx8 FLASH)	0 (r) (512K/1Mx8 FLASH)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

[Table 2-16](#) provides details about the *DSP_FLASH_PAGE_RG* register bits.

Table 2-16. *DSP_FLASH_PAGE_RG* register bits.

register bits	access mode	value on DSP reset	Description
{ <i>FPAGE-5..0</i> }	r/w	[0,0,0,0,0,0]	Select the 1Mx8 FLASH memory page, which is currently accessed via the EMIF CE1 external DSP memory space. Refer to Table 2-4 for more details.

Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

NOTE

For 512Kx8 and 1Mx8 FLASH memories, all {*FPAGE-5..0*} bits of *DSP_FLASH_PAGE_RG* DSP external control register are not available.

NOTE

For 8Mx8 FLASH memory, only {*FPAGE-2..0*} bits of *DSP_FLASH_PAGE_RG* DSP external control register are available.

IMPORTANT NOTE

It is recommended, that the {*FPAGE-5..0*} bits, which are used to select the FLASH memory page, are not directly configured from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user's guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

For more details about programming of *TORNADO-E2/6xxx* on-board FLASH memory refer to subsection “[FLASH memory area](#)” earlier in this chapter and to [Appendix G](#) of this user's guide.

***DSP_FLASH_CNTR_RG* DSP external FLASH memory control register**

DSP_FLASH_CNTR_RG DSP external control register is used to to control FLASH write protection feature.

***DSP_FLASH_CNTR_RG* register (r/w)**

<i>FLASH_WR_EN</i> (r/w, 0+)	<i>FLASH64M_BOOT_SECTOR_WR_EN</i> (r/w, 0+) (64Mx8 FLASH)	<i>FLASH_XWRPROT_STAT</i> (r)	<i>FLASH64M_BOOT_SECTOR_XWRPROT_STAT</i> (r) (64Mx8 FLASH)	0	0	0	0
	0 (r) (512K/1M/8Mx8 FLASH)		0 (r) (512K/1M/8Mx8 FLASH)				
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-17](#) provides details about the *DSP_FLASH_CNTR_RG* register bits.

Table 2-17. *DSP_FLASH_CNTR_RG* register bits.

register bits	access mode	value on DSP reset	Description
<i>FLASH64M_BOOT_SECTOR_XWRPROT_STAT</i>	r	-	<p>This bit returns the status of external write protection for the 1st sector of 64Mx8 FLASH for DSP application: the state of write protection switch SW1-3 in the <i>DSP stand-alone operation mode</i> or logical OR of the state of write protection switch SW1-3 and the state of <i>FLASH64M_BOOT_SECTOR_WR_EN</i> bit of HCX_AX_CNTR2_RG HCX control register in the <i>DSP host operation mode</i>. This bit is not available for 512Kx8, 1Mx8 and 8Mx8 FLASH.</p> <p><i>FLASH64M_BOOT_SECTOR_XWRPROT_STAT</i> = 1 denotes that write access to the 1st sector of 64Mx8 FLASH is externally disabled for DSP application by the write protection switch SW1-3 in the <i>DSP stand-alone operation mode</i>, or by the write protection switch SW1-3 or the state of <i>FLASH64M_BOOT_SECTOR_WR_EN</i> bit of HCX_AX_CNTR2_RG HCX control register in the <i>DSP host operation mode</i>.</p> <p><i>FLASH64M_BOOT_SECTOR_XWRPROT_STAT</i> = 0 denotes that write access to the 1st sector of 64Mx8 FLASH is externally enabled for DSP application. However write access to the 1st sector of 64Mx8 FLASH can be performed only in case of conditions listed in Table 2-6 and as described in subsection “FLASH memory area” earlier in this chapter.</p>
<i>FLASH_XWRPROT_STAT</i>	r	-	<p>This bit returns the status of external FLASH write protection for DSP application: the state of write protection switch SW1-2 in the <i>DSP stand-alone operation mode</i> or logical OR of the state of write protection switch SW1-2 and the state of <i>FLASH_WR_EN</i> bit of HCX_AX_CNTR2_RG HCX control register in the <i>DSP host operation mode</i>.</p> <p><i>FLASH_XWRPROT_STAT</i> = 1 denotes that write access to on-board FLASH memory is externally disabled for DSP application by the write protection switch SW1-2 in the <i>DSP stand-alone operation mode</i>, or by the write protection switch SW1-2 or the state of <i>FLASH_WR_EN</i> bit of HCX_AX_CNTR2_RG HCX control register in the <i>DSP host operation mode</i>.</p> <p><i>FLASH_XWRPROT_STAT</i> = 0 denotes that write access to on-board FLASH is externally enabled for DSP application. However write access to on-board FLASH can be performed only in case of conditions listed in Table 2-5 and as described in subsection “FLASH memory area” earlier in this chapter.</p>
<i>FLASH64M_BOOT_SECTOR_WR_EN</i>	r/w	0	<p>Write protection control for 1st sector of 64Mx8 FLASH memory. This bit is not available for 512Kx8, 1Mx8 and 8Mx8 FLASH.</p> <p><i>FLASH64M_BOOT_SECTOR_WR_EN</i> = 0 disables write access to the 1st sector of 64Mx8 FLASH.</p> <p><i>FLASH64M_BOOT_SECTOR_WR_EN</i> = 1 enables write access to the 1st sector of 64Mx8 FLASH. This bit can be set to the ‘1’ state only in case of conditions listed in Table 2-6 and as described in subsection “FLASH memory area” earlier in this chapter.</p>
<i>FLASH_WR_EN</i>	r/w	0	<p>Write protection control for on-board FLASH memory.</p> <p><i>FLASH_WR_EN</i> = 0 disables write access to on-board FLASH memory.</p> <p><i>FLASH_WR_EN</i> = 1 enables write access to on-board FLASH. This bit can be set to the ‘1’ state only in case of conditions listed in Table 2-5 and as described in subsection “FLASH memory area” earlier in this chapter.</p>

- Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
 2. Highlighted configurations correspond to default settings on DSP reset condition.

NOTE

For 512Kx8, 1Mx8 and 8Mx8 FLASH memories, only *FLASH_WR_EN* and *FLASH_XWRPROT_STAT* bits of *DSP_FLASH_CNTR_RG* DSP external control register are available.

For more details about programming of *TORNADO-E2/6xxx* on-board FLASH memory refer to subsection “[FLASH memory area](#)” earlier in this chapter and to [Appendix G](#) of this user’s guide.

***DSP_WDT_RTC_CNTR_RG* DSP external control register for WDT and RTC control**

DSP_WDT_RTC_CNTR_RG DSP external control register is used to enable WDT feature (i.e. automatic DSP reset on WDT expiration event for *DSP stand-alone operation mode*) and to enable access to *TORNADO-E2/6xxx* on-board RTC controller.

***DSP_WDT_RTC_CNTR_RG* register (r/w)**

0	0	0	0	<i>RTC_XPS_EN</i> (r, 1+)	<i>RTC_EN</i> (r/w, 0+)	1	<i>WDT_EN</i> (r/w, 0+)
bit-7	bit-6	bit-5	Bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-18](#) provides details about the *DSP_WDT_RTC_CNTR_RG* register bits.

Table 2-18. *DSP_WDT_RTC_CNTR_RG* register bits.

register bits	access mode	value on DSP reset	Description
<i>WDT_EN</i>	r/w	0	<p>Enables control for the WDT feature for <i>DSP stand-alone operation mode</i>. The setting of this bit is ignored in <i>DSP host operation mode</i>.</p> <p><i>WDT_EN</i>=0 corresponds to the WDT feature disabled.</p> <p><i>WDT_EN</i>=1 corresponds to the WDT feature enabled. DSP application must periodically reset WDT with the period about 1 sec by writing to the DSP_WDT_RESET_RG DSP external control register in order to exclude automatic DSP restart.</p>
<i>RTC_EN</i>	r/w	0	<p>Enables access to on-board RTC controller. Software enabled control for RTC controller access provides RTC data integrity and excludes accidental RTC access when DSP executes thru invalid code.</p> <p><i>RTC_EN</i>=0 corresponds to disabled RTC accesses, i.e. all accesses to RTC controller on-chip registers will be ignored and no RTC data will be read or written. This is default setting on power on and DSP reset conditions.</p> <p><i>RTC_EN</i>=1 corresponds to enabled RTC accesses, i.e. accesses to RTC controller area (refer to Table 2-2) will result in access to the RTC controller on-chip registers.</p>
<i>RTC_XPS_EN</i>	r	1	<p>This bit returns status of external power supply control output signal of RTC controller. This bit is used by DSP application to check current power enable status in case <i>TORNADO-E2/6xxx</i> DSP controller is powered by external power supply, which is controlled by on-board RTC power supply control circuitry. This signal is active only when kickstart or wake-up features of RTC controller are used (refer to Appendix J for more details).</p> <p><i>RTC_XPS_EN</i> = 1 denotes that external power supply is enabled.</p> <p><i>RTC_XPS_EN</i> = 0 denotes that external power supply is disabled.</p>

- Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
 2. Highlighted configurations correspond to default settings on DSP reset condition.

DSP_WDT_RESET_RG DSP external control register for WDT reset

WDT is enabled via the *WDT_EN* bit of [DSP_WDT_RTC_CNTR_RG](#) DSP external control register for *DSP stand-alone operation mode* only. In order to reset the on-board WDT, DSP application must perform write operation to the *DSP_WDT_RESET_RG* write-only DSP external control register (refer to [Table 2-2](#)).

DSP_WDT_RESET_RG register (w)

x	x	x	x	X	x	x	x
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

NOTE

Data written to the write-only *DSP_WDT_RESET_RG* register has no meaning and is ignored during writes. Only register write event is used to reset the WDT.

DSP_GPIO_DIR_RG and DSP_GPIO_DATA_RG DSP external control registers for GPIO pins control

DSP_GPIO_DIR_RG and *DSP_GPIO_DATA_RG* DSP external control registers are used for direction control and data I/O of general purpose I/O pins (GPIO) which are available via on-board JP13 connector ([Figure A-1](#)).

DSP_GPIO_DIR_RG register (r/w)

GPIO-7_DIR (r/w, 0+)	GPIO-6_DIR (r/w, 0+)	GPIO-5_DIR (r/w, 0+)	GPIO-4_DIR (r/w, 0+)	GPIO-3_DIR (r/w, 0+)	GPIO-2_DIR (r/w, 0+)	GPIO-1_DIR (r/w, 0+)	GPIO-0_DIR (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-19](#) provides details about the *DSP_GPIO_DIR_RG* register bits.

Table 2-19. DSP_GPIO_DIR_RG register bits.

register bits	access mode	value on DSP reset	Description
{GPIO-7..0_DIR}	r/w	[0,0,0,0,0,0,0,0]	Individual direction control for <i>GPIO</i> pins. GPIO- <i>n</i> _DIR = 0 configures the corresponding <i>GPIO-n</i> pin (<i>n</i> =0..7) as an INPUT. GPIO- <i>n</i> _DIR = 1 configures the corresponding <i>GPIO-n</i> pin (<i>n</i> =0..7) as an OUTPUT.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

DSP_GPIO_DATA_RG DSP external control register is used for data I/O via GPIO pins.

DSP_GPIO_DATA_RG register (r/w)

GPIO-7_DATA (r/w, 1+)	GPIO-6_DATA (r/w, 1+)	GPIO-5_DATA (r/w, 1+)	GPIO-4_DATA (r/w, 1+)	GPIO-3_DATA (r/w, 1+)	GPIO-2_DATA (r/w, 1+)	GPIO-1_DATA (r/w, 1+)	GPIO-0_DATA (r/w, 1+)
bit-7	bit-6	bit-5	bit-4	Bit-3	Bit-2	bit-1	bit-0

[Table 2-20](#) provides details about the *DSP_GPIO_DATA_RG* register bits.

Table 2-20. DSP_GPIO_DATA_RG register bits.

register bits	access mode	value on DSP reset	Description
{GPIO-7..0_DATA}	r/w	r: <application specific> w: [0,0,0,0,0,0,0]	During read, return current state of GPIO pins. Power-on value for read is application specific. Write to this register has effect to those bits only, which correspond to the GPIO pins configured as OUTPUTs and define output state of those GPIO pins. Write has no immediate effect to those bits, which correspond to the GPIO pins configured as INPUTs, however last written data is stored for these bits and will come effective immediately as soon as the corresponding GPIO pins will be configured as OUTPUTs. GPIO-n_DATA = 0 corresponds to the '0' state of GPIO-n pin (n=0..7). GPIO-n_DATA = 1 corresponds to the '0' state of GPIO-n pin (n=0..7).

Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

DSP_DCM_RESET_RG DSP external control register for reset control of PIOX2/SIOX/ASIOX DCM sites

DSP_DCM_RESET_RG DSP external control register is used to generate individual reset signals for on-board SIOX, ASIOX and PIOX2 DCM sites. This allows correct initialization of installed DCM hardware and its synchronization with DSP application.

DSP_DCM_RESET_RG register (r/w)

0	0	0	0	0	0	$\overline{\text{SIOX_RESET}}$ (r/w, 0+)	$\overline{\text{PIOX_ASYNC_RESET}}$ (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-21](#) provides details about the DSP_DCM_RESET_RG register bits.

Table 2-21. DSP_DCM_RESET_RG register bits.

Register bits	access mode	value on DSP reset	Description
$\overline{\text{PIOX_ASYNC_RESET}}$	r/w	0	Controls reset signal for on-board PIOX2 DCM site. For more details about on-board PIOX2 DCM site refer to Appendix D in this user's guide. $\overline{\text{PIOX_ASYNC_RESET}} = 0$ corresponds to active reset signal for PIOX2 DCM site. This is default setting on power on and DSP reset conditions. $\overline{\text{PIOX_ASYNC_RESET}} = 1$ corresponds to released reset signal for PIOX2 DCM site and enables operation of installed PIOX2 DCM hardware.
$\overline{\text{SIOX_RESET}}$	r/w	0	Controls reset signal for on-board SIOX rev.B and ASIOX rev.D DCM sites. Both SIOX rev.B and ASIOX rev.D on-board DCM sites share common reset signal. For more details about on-board SIOX DCM sites refer to Appendix C in this user's guide. $\overline{\text{SIOX_RESET}} = 0$ applies reset signal for SIOX rev.B and ASIOX rev.D DCM sites. This is default setting on power on and DSP reset conditions. $\overline{\text{SIOX_RESET}} = 1$ releases reset signal for SIOX rev.B and ASIOX rev.D DCM sites and enables operation of installed SIOX DCM hardware.

Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

DSP_SIOX_XIO_CNF_RG and DSP_SIOX_XIO_DATA_RG DSP external control registers for configuring DSP Timers/XIO pins

DSP_SIOX_XIO_CNF_RG and DSP_SIOX_XIO_DATA_RG DSP external control registers are used for direction and data control of legacy SIOX rev.B I/O pins (SIOX_TM/XIO-0/1) which are available at SIOX rev.B DCM site interface (refer to [Appendix C](#)). These pins can be configured as either DSP on-chip timers outputs (DSP timers inputs are not supported for TORNADO-E2/6713 DSP controller), or as general purpose I/O pins. Configuration of SIOX_TM/XIO-0/1 pins is set via DSP_SIOX_XIO_CNF_RG DSP external control register.

NOTE

DSP timers inputs are not supported for TORNADO-E2/6713 DSP controller.

DSP_SIOX_XIO_CNF_RG register (r/w)

0	0	SIOX_XIO-1_CNF1 (r/w, 0+)	SIOX_XIO-1_CNF0 (r/w, 0+)	0	0	SIOX_XIO-0_CNF1 (r/w, 0+)	SIOX_XIO-0_CNF0 (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-22](#) provides details about the DSP_SIOX_XIO_CNF_RG register bits.

Table 2-22. DSP_SIOX_XIO_CNF_RG register bits.

Register bits	access mode	value on DSP reset	Description
{SIOX_XIO-0_CNF1..0}	r/w	[0,0]	<p>Function selection for SIOX rev.B SX_TM/XIO-0 pin.</p> <p>{SIOX_XIO-0_CNF1..0} = [0,0] configures SIOX_TM/XIO-0 pin as general purpose INPUT pin.</p> <p>{SIOX_XIO-0_CNF1..0} = [0,1] configures SIOX_TM/XIO-0 pin as general purpose OUTPUT pin. Data control for this pin is performed via SIOX_XIO-0_DATA bit of DSP_SIOX_XIO_DATA_RG DSP external control register.</p> <p>{SIOX_XIO-0_CNF1..0} = [1,0] configures SIOX_TM/XIO-0 pin as DSP timer #0 output. For TORNADO-E2/6713 controller with TMS320C6713 DSP, the DSP timer #0 output pin (TOUT0) must be enabled via DEVCFG TMS320C6713 DSP on-chip device configuration register (@0x019C0200) (refer to Table 2-7).</p> <p>{SIOX_XIO-0_CNF1..0} = [1,1] setting is reserved.</p>
{SIOX_XIO-1_CNF1..0}	r/w	[0,0]	<p>Function selection for SIOX rev.B SIOX_TM/XIO-1 pin.</p> <p>{SIOX_XIO-1_CNF1..0} = [0,0] configures SIOX_TM/XIO-1 pin as general purpose INPUT pin.</p> <p>{SIOX_XIO-1_CNF1..0} = [0,1] configures SIOX_TM/XIO-1 pin as general purpose OUTPUT pin. Data control for this pin is performed via SIOX_XIO-1_DATA bit of DSP_SIOX_XIO_DATA_RG DSP external control register.</p> <p>{SIOX_XIO-1_CNF1..0} = [1,0] configures SIOX_TM/XIO-1 pin as DSP timer #1 output. For TORNADO-E2/6713 controller with TMS320C6713 DSP, the DSP timer #1 output pin (TOUT1) must be enabled via DEVCFG TMS320C6713 DSP on-chip device configuration register (@0x019C0200) (refer to Table 2-7).</p> <p>{SIOX_XIO-1_CNF1..0} = [1,1] setting is reserved.</p>

- Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
 2. Highlighted configurations correspond to default settings on DSP reset condition.

IMPORTANT NOTE

It is recommended, that TMS320C6713 DSP on-chip *DEVCFG* device configuration register (@0x019C0200) bits are not directly configured from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user's guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

Data control is set via *DSP_SIOX_XIO_DATA_RG* DSP external control register.

***DSP_SIOX_XIO_DATA_RG* register (r/w)**

0	0	0	0	0	0	SX_XIO-1_DATA (r/w, 1+)	SX_XIO-0_DATA (r/w, 1+)
bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

[Table 2-23](#) provides details about the *DSP_SIOX_XIO_DATA_RG* register bits.

Table 2-23. *DSP_SIOX_XIO_DATA_RG* register bits.

Register bits	access mode	value on DSP reset	Description
{SIOX_XIO-1..0_DATA}	r/w	r: <application specific> w: [0,0]	During read, return current state of SIOX rev.B SX_TM/XIO-0/1 pins in case those are configured as general purpose I/O pins via the corresponding SIOX_XIO-n_CNF (n=0,1) bits of <i>DSP_SIOX_XIO_CNF_RG</i> DSP external control register (refer to Table 2-22). Power-on value for read is application specific. Write to this register has effect to those bits only, which correspond to the SIOX_TM/XIO-n pins configured as OUTPUTs and define output state of those SIOX_TM/XIO-n pins. Write has no immediate effect to those bits, which correspond to the SIOX_TM/XIO-n pins configured as INPUTs, however last written data is stored for these bits and will come effective immediately as soon as the corresponding SIOX_TM/XIO-n pins will be configured as OUTPUTs. SIOX_XIO-n_DATA = 0 (n=0,1) corresponds to the '0' state of SIOX_TM/XIO-n I/O pin. SIOX_XIO-n_DATA = 1 (n=0,1) corresponds to the '1' state of SIOX_TM/XIO-n I/O pin.

Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

***DSP_HCX_SYNC_PAGE_RG* DSP external control register for address extension of synchronous HCX DCM site interface**

DSP_HCX_SYNC_PAGE_RG DSP external control register is used to extend addressing capabilities of the *TORNADO-E2/6xxx* when accessing synchronous section of *HCX* DCM site interface.

For *TORNADO-E2/6713* DSP controller, the on-board DSP can directly address only 256Kx32 area of synchronous section of *HCX* DCM site interface, that can be insufficient for accessing full on-board shared memory resources of *HCX* controller. In accordance with *HCX* DCM specification, full addressing capabilities of synchronous section of *HCX* DCM site interface is 16Mx32.

In order to extend DSP addressing capabilities for access to synchronous section of *HCX* DCM site interface of *TORNADO-E2/6xxx* controllers, memory paging technique is used with extra memory page bits available via *DSP_HCX_SYNC_PAGE_RG* register.

DSP_HCX_SYNC_PAGE_RG register (r/w)
(TORNADO-E2/6713)

0	0	HCX_SYNC_A23 (r/w, 0+)	HCX_SYNC_A22 (r/w, 0+)	HCX_SYNC_A21 (r/w, 0+)	HCX_SYNC_A20 (r/w, 0+)	HCX_SYNC_A19 (r/w, 0+)	HCX_SYNC_A18 (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-24](#) provides details about the *DSP_HCX_SYNC_PAGE_RG* registers bits.

Table 2-24. DSP_HCX_SYNC_PAGE_RG register bits for TORNADO-E2/6713.

Register bits	access mode	value on DSP reset	Description
{HCX_SYNC_A23..18}	r/w	[0,0,0,0,0,0]	Memory page selector for access to synchronous section of <i>HCX</i> DCM interface.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on DSP reset condition.

Refer to subsection “[HCX-SYNC synchronous section of HCX DCM site interface](#)” later in this chapter for more details about 32-bit synchronous *HCX* DCM site interface.

2.4 HCX DCM Site Interface

Host *HCX* DCM site rev.A interface (hereafter as *HCX* DCM site interface) of *TORNADO-E2/6xxx* DSP controllers has been designed for host control and high-speed real-time data transfer between *TORNADO-E2/6xxx* and optional host *HCX* DCM.

Host *HCX* controller DCM provides industry-standard high-speed communication interfaces for communication with external computers and networks and allows to off-load DSP application from time-consuming host communication task using industry-standard complicated communication protocols and to benefit from maximum DSP performance.

This section contains general description and programming details for *HCX* DCM site interface of *TORNADO-E2/6xxx* DSP controllers. For hardware details about host *HCX* DCM site interface, refer to [Appendix E](#).

General description of HCX DCM site interface

Host *HCX* rev.A DCM site interface of *TORNADO-E2/6xxx* DSP controllers comprises two sections:

- Mandatory 32-bit asynchronous section, which is hereafter denoted as *HCX-ASYNC* interface.
- Optional 32-bit synchronous section, which is hereafter denoted as *HCX-SYNC* interface.

Host *HCX* rev.A DCM site interface of *TORNADO-E2/6xxx* DSP controllers is automatically enabled in case compatible *HCX* DCM is installed. On-board logic automatically detects type of installed *HCX* DCM and returns configuration IDs via [DSP_DCM_CNF_RG](#) DSP external control register (refer to [Table 2-9](#)) for DSP environment.

HCX-ASYNC interface includes a set of *HCX* control registers for host control of on-board DSP and allows access from host *HCX* controller into entire DSP environment via DSP on-chip HPI port.

NOTE

HCX-ASYNC interface of *TORNADO-E2/6xxx* DSP controllers is controlled exclusively by host *HCX* controller, and on-board DSP does not have access to *HCX* DCM site interface control registers.

HCX-ASYNC interface of *TORNADO-E2/6xxx* DSP controllers is mapped into the address space of host *HCX* controller.

Depending upon particular type of *TORNADO-E2/6xxx* board, *HCX-ASYNC* interface provides either 16-bit or 32-bit wide data bus and either two or four DSP-to-Host interrupt requests.

For *HCX-ASYNC* interface, real-time data transfer between DSP and host *HCX* controller is performed via DSP on-chip HPI port, which typically provides 100..300 Kword/s throughput performance. In most cases this path is used to upload DSP executable and for general DSP application control.

Instead, optional 32-bit wide *HCX-SYNC* interface provides highest possible data transfer performance for particular DSP type and runs at the speed of DSP EMIF, i.e. at 100 Mwords/s for *TORNADO-E2/6713* controller. *HCX-SYNC* interface has been designed for high-speed real-data transfer between DSP and host *HCX* controller applications using either shared memory or FIFO resources available at *HCX* DCM. *HCX-SYNC* interface also provides one to four Host-to-DSP interrupt requests, which are used for data transfer synchronization and for general purpose DSP interrupt request.

NOTE

HCX-SYNC interface of *TORNADO-E2/6xxx* DSP controllers is controlled exclusively by on-board DSP and is mapped into DSP external memory area (refer to [Table 2-2](#) for more details).

Enable and reset control for *HCX* DCM site interface

Once compatible host *HCX* DCM is installed onto *TORNADO-E2/6xxx* board, then this puts *TORNADO-E2/6xxx* on-board DSP into *DSP host operation mode* as it is listed in [Table 2-1](#). Correspondingly, in case *HCX* DCM is not installed, then this mode corresponds to the *DSP stand-alone operation mode* with host *HCX* DCM site interface disabled.

NOTE

For *DSP stand-alone operation mode* (i.e. in case no *HCX* DCM is installed), host *HCX* DCM site interface of *TORNADO-E2/6xxx* DSP controllers is automatically disabled with all *HCX* control registers default to their reset states (as it is described in the corresponding subsections below).

HCX-ASYNC interface includes hardware reset signal ($\overline{HCX_RESET}$ signal at *HCX-ASYNC* interface connector, refer to [Appendix E](#) for more details), which is controlled by host *HCX* controller. This signal is used by host *HCX* application to reset *HCX* DCM site interface of *TORNADO-E2/6xxx* to its default state and/or to synchronize DSP application with host *HCX* controller application.

NOTE

In case host *HCX* controller asserts active reset signal for *HCX-ASYNC* interface, then all *HCX* control registers default to their reset states and on-board DSP is held in the reset state. All writes to *HCX* control registers are ignored while *HCX* reset signal is asserted, however all reads of *HCX* control register proceed normally.

In order to write to *HCX* control registers and to get access to the DSP on-chip HPI port, host *HCX* controller application shall release reset signal for *HCX* DCM site interface of *TORNADO-E2/6xxx*. Refer to technical documentation for *HCX* controller for more details.

For *DSP host operation mode*, the DSP reset signal is controlled exclusively by host *HCX* controller application via the *DSP_RUN* bit of [HCX_AX_CNTR1_RG](#) *HCX* control register ([Table 2-26](#)).

HCX control registers and address map for HCX-ASYNC interface

HCX-ASYNC interface provides access from host *HCX* controller to a set of *HCX* control registers and to DSP HPI port registers area.

NOTE

HCX-ASYNC interface of *TORNADO-E2/6xxx* is mapped into address space of host *HCX* controller.

HCX-ASYNC interface of *TORNADO-E2/6xxx* has 32-bit data word format, however particular number of valid data bits depends upon the addressed register and type of *TORNADO-E2/6xxx* controller.

8-bit *HCX* control registers are used by host *HCX* controller application to control *TORNADO-E2/6xxx* on-board DSP and to configure *HCX-ASYNC* interface:

- [HCX_AX_SYS_CNF1_RG](#), [HCX_AX_SYS_CNF2_RG](#) and [HCX_AX_SYS_CNF3_RG](#) *HCX* control registers for read-only board configuration information (device ID, board revision, memory capacity, etc).
- [HCX_AX_CNTR1_RG](#) and [HCX_AX_CNTR2_RG](#) *HCX* control registers for DSP reset control and DSP start-up configuration control, etc.
- [HCX_AX_INT_STAT_RG](#) *HCX* control register for DSP-to-Host status information.
- [HCX_AX_CLR_HPI_TMOUT_ERR_RG](#) write-only *HCX* control register for clearing DSP on-chip HPI port timeout error.
- [HCX_AX_HIRQ0_SEL_RG](#) and [HCX_AX_HIRQ1_SEL_RG](#) *HCX* control registers for DSP-to-Host interrupt request configuration.

DSP HPI port registers area is used by host *HCX* controller application to access entire DSP environment (DSP on-chip RAM and registers, on-board SBSRAM, SDRAM, FLASH, etc) via DSP on-chip HPI port. *TORNADO-E2/6713* DSP controller features 16-bit DSP on-chip HPI port registers. Refer to subsection “[DSP on-chip HPI port area of HCX-ASYNC interface](#)” for more details.

[Table 2-25](#) provides details about host *HCX* controller address map for *HCX-ASYNC* interface of *TORNADO-E2/6713* DSP controller.

Table 2-25. Host HCX controller address map for HCX-ASYNC interface of TORNADO-E2/6713 DSP controller.

register of HCX-ASYNC interface	access mode	valid data bits	host HCX controller address range ⁴⁾
8-bit HCX Control Registers area			
<u>HCX_AX_SYS_CNF1_RG</u> register (device ID)	r	D0..D7	BA + 0000H*WAS (bits D0..D7 only)
<u>HCX_AX_SYS_CNF2_RG</u> register (board revision ID, DSP clock frequency ID and spread spectrum clock feature ID)	r	D0..D7	BA + 0002H*WAS (bits D0..D7 only)
<u>HCX_AX_SYS_CNF3_RG</u> register (DSP external memory capacity IDs)	r	D0..D7	BA + 0003H*WAS (bits D0..D7 only)
<u>HCX_AX_CNTR1_RG</u> register (DSP reset control)	r/w	D0..D7	BA + 0004H*WAS (bits D0..D7 only)
<u>HCX_AX_CNTR2_RG</u> register (DSP bootmode control, DSP HPI port enable and HPI timeout error enable control)	r/w	D0..D7	BA + 0005H*WAS (bits D0..D7 only)
<u>HCX_AX_HIRQ0_SEL_RG</u> register (HIRQ-0 interrupt selector)	r/w	D0..D7	BA + 0008H*WAS (bits D0..D7 only)
<u>HCX_AX_HIRQ1_SEL_RG</u> register (HIRQ-1 interrupt selector)	r/w	D0..D7	BA + 0009H*WAS (bits D0..D7 only)
<u>HCX_AX_INT_STAT_RG</u> register (interrupt status for DSP-to-host interrupt request via HPI and HPI timeout)	r	D0..D7	BA + 000CH*WAS (bits D0..D7 only)
<u>HCX_AX_CLR_HPI_TMOUT_ERR_RG</u> register (clear HPI timeout error)	w	D0..D7	BA + 000FH*WAS (write data is ignored)
16-bit DSP on-chip HPI port registers area			
<u>HCX_AX_DSP_HPIC_LSW16_RG</u> register (16-bit LSW of HPI control register)	r/w	D0..D15	BA + 0018H*WAS
<u>HCX_AX_DSP_HPIC_MSW16_RG</u> register (16-bit MSW of HPI control register)	r/w	D0..D15	BA + 0019H*WAS
<u>HCX_AX_DSP_HPIA_LSW16_RG</u> register (16-bit LSW of HPI address register)	r/w	D0..D15	BA + 001AH*WAS
<u>HCX_AX_DSP_HPIA_MSW16_RG</u> register (16-bit MSW of HPI address register)	r/w	D0..D15	BA + 001BH*WAS
<u>HCX_AX_DSP_HPID_AINC_LSW16_RG</u> register (16-bit LSW of HPI data register with address postincrement)	r/w	D0..D15	BA + 001CH*WAS
<u>HCX_AX_DSP_HPID_AINC_MSW16_RG</u> register (16-bit MSW of HPI data register with address postincrement)	r/w	D0..D15	BA + 001DH*WAS
<u>HCX_AX_DSP_HPID_LSW16_RG</u> register (16-bit LSW of HPI data register)	r/w	D0..D15	BA + 001EH*WAS
<u>HCX_AX_DSP_HPID_MSW16_RG</u> register (16-bit MSW of HPI data register)	r/w	D0..D15	BA + 001FH*WAS

- Notes:
1. Access modes: *r* - read only, *w* - write only, *r/w* - read/write.
 2. 'BA' states for base address of *HCX-ASYNC* interface of *TORNADO-E2/6xxx* inside memory map of host *HCX* controller. Refer to the user's guide for your host *HCX* controller for more details.
 3. 'WAS' denotes host *HCX* controller data word address step in it's memory map when addressing *HCX-ASYNC* interface of *TORNADO-E2/6xxx*. *WAS* normally equals to '4' for currently released *HCX* controllers, however it can generally differ for future *HCX* controllers. Refer to the user's guide for your host *HCX* controller for more details.

NOTE

When accessing *HCX control registers* of *HCX-ASYNC* interface from host *HCX* application, only D0..D7 least significant data bits of 32-bit data words of *HCX-ASYNC* interface are valid. Unused D8..D31 bits of 32-bit datawords are ignored during writes and return undefined data during reads.

NOTE

When accessing *DSP on-chip HPI port registers area* of *HCX-ASYNC* interface of *TORNADO-E2/6713* from host *HCX* controller application, , only D0..D15 data bits of 32-bit data words of *HCX-ASYNC* interface are valid. Unused D16..D31 bits of 32-bit data words are ignored during writes and return undefined data during reads.

The 'BA' and 'WAS' parameters in [Table 2-25](#) define *base address* of *HCX-ASYNC* interface in host *HCX* controller memory map and *word address step* within this memory map.

It must be noted that the *BA* parameter is not only *HCX* controller specific (i.e. may differ for different *HCX* controllers), but it is also host application specific, i.e. it may vary across different *HCX* controller applications and real-time OS used for the same *HCX* controller due to software configured host *HCX* controller memory map. Therefore, refer to documentation for your *HCX* controller DCM for more details.

The *WAS* host data word address step parameter normally equals to the '4' value for all 32-bit *HCX* controllers, however it is generally *HCX* controller specific and host *HCX* controller application/OS specific. Therefore, refer to documentation for your *HCX* controller DCM for more details.

HCX_AX_SYS_CNF1_RG, HCX_AX_SYS_CNF2_RG, and HCX_AX_SYS_CNF3_RG read-only HCX control registers for board configuration information

HCX_AX_SYS_CNF1_RG, *HCX_AX_SYS_CNF2_RG* and *HCX_AX_SYS_CNF3_RG* read-only *HCX* control registers are used to obtain device ID, board revision ID, DSP core clock frequency ID, on-board memory capacity IDs and other board specific configuration information for *TORNADO-E2/6xxx* DSP controllers from host *HCX* controller application. These registers contain similar information, which is available via [DSP_SYS_CNF1_RG](#), [DSP_SYS_CNF2_RG](#) and [DSP_SYS_CNF3_RG](#) read-only DSP external control registers inside the DSP environment.

Note, that when accessing *HCX_AX_SYS_CNF1_RG*, *HCX_AX_SYS_CNF2_RG* and *HCX_AX_SYS_CNF3_RG* read-only *HCX* control registers, only D0..D7 bits of 32-bit data words of *HCX-ASYNC* interface are valid.

HCX_AX_SYS_CNF1_RG register (r)

DEV_ID-7 (r)	DEV_ID-6 (r)	DEV_ID-5 (r)	DEV_ID-4 (r)	DEV_ID-3 (r)	DEV_ID-2 (r)	DEV_ID-1 (r)	DEV_ID-0 (r)
Bit-7	bit-6	bit-5	bit-4	Bit-3	Bit-2	bit-1	Bit-0

HCX_AX_SYS_CNF2_RG register (r)

0	DSP_SSCLK_ID (r)	DSP_CLK_FREQ_ID-1 (r)	DSP_CLK_FREQ_ID-0 (r)	REV_ID-3 (r)	REV_ID-2 (r)	REV_ID-1 (r)	REV_ID-0 (r)
Bit-7	bit-6	bit-5	bit-4	Bit-3	Bit-2	bit-1	Bit-0

HCX_AX_SYS_CNF3_RG register (r)

FLASH_LEN_ID-3 (r)	FLASH_LEN_ID-2 (r)	FLASH_LEN_ID-1 (r)	FLASH_LEN_ID-0 (r)	SDRAM_LEN_ID-1 (r)	SDRAM_LEN_ID-0 (r)	SBSRAM_LEN_ID-1 (r)	SBSRAM_LEN_ID-0 (r)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-26](#), [Table 2-27](#) and [Table 2-28](#) provide details about the register bits of *HCX_AX_SYS_CNF1_RG*, *HCX_AX_SYS_CNF2_RG* and *HCX_AX_SYS_CNF3_RG* read-only *HCX* control registers correspondingly.

Table 2-26. HCX_AX_SYS_CNF1_RG register bits.

register bits	access mode	value on HCX reset	Description
{DEV_ID-7..0}	r	-	These bits return <i>TORNADO-E2/6xxx</i> device ID. { DEV_ID-7..0} = [0,0,0,0,0,0,0,1] corresponds to the <i>TORNADO-E2/6713</i> DSP controller. All other {DEV_ID-7..0} field settings are reserved.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

Table 2-27. HCX_AX_SYS_CNF2_RG register bits.

register bits	access mode	value on HCX reset	Description
{REV_ID-3..0}	r	-	Return board firmware revision ID for <i>TORNADO-E2/6xxx</i> DSP controllers. {REV_ID-3..0} = [0,0,0,0] is reserved. {REV_ID-3..0} = [0,0,0,1] corresponds to firmware revision 1A of <i>TORNADO-E2/6713</i> .
{DSP_CLK_FREQ_ID-1..0}	r	-	Return DSP core clock frequency ID for on-board TMS320C6xxx DSP. {DSP_CLK_FREQ_ID-1..0} = [0,0] setting is reserved. {DSP_CLK_FREQ_ID-1..0} = [0,1] corresponds to the 300 MHz TMS320C6713 DSP. This setting is available for <i>TORNADO-E2/6713</i> DSP controller firmware rev.1A only.
DSP_SSCLK_ID	r	-	Identifies presence of spread spectrum clock for DSP EMIF, which is used to minimize board's RF radiation. DSP_SSCLK_ID = 0 denotes that DSP EMIF does not have spectrum clock. DSP_SSCLK_ID = 1 denotes that DSP EMIF has spread spectrum clock.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

Table 2-28. *HCX_AX_SYS_CNF3_RG* register bits.

register bits	access mode	value on <i>HCX</i> reset	Description
{ <i>SBSRAM_LEN_ID-1..0</i> }	r	-	Return capacity ID for on-board SBSRAM memory. Refer to Table 2-2 for more details. { <i>SBSRAM_LEN_ID-1..0</i> } = [0,0] denotes that SBSRAM is not installed. { <i>SBSRAM_LEN_ID-1..0</i> } = [0,1] corresponds to 128Kx32 SBSRAM. { <i>SBSRAM_LEN_ID-1..0</i> } = [1,0] corresponds to 512Kx32 SBSRAM.
{ <i>SDRAM_LEN_ID-1..0</i> }	r	-	Return capacity ID for on-board SDRAM memory. Refer to Table 2-2 for more details. { <i>SDRAM_LEN_ID-1..0</i> } = [0,0] denotes that SDRAM is not installed. { <i>SDRAM_LEN_ID-1..0</i> } = [0,1] corresponds to 4Mx32 SDRAM. { <i>SDRAM_LEN_ID-1..0</i> } = [1,0] corresponds to 16Mx32 SDRAM.
{ <i>FLASH_LEN_ID-3..0</i> }	r	-	Return the capacity ID for on-board FLASH memory. Refer to Table 2-2 and subsection " FLASH memory area " for more details. { <i>FLASH_LEN_ID-3..0</i> } = [0,0,0,0] denotes that FLASH is not installed. { <i>FLASH_LEN_ID-3..0</i> } = [0,0,0,1] corresponds to 512Kx8 FLASH. { <i>FLASH_LEN_ID-3..0</i> } = [0,0,1,0] corresponds to 1Mx8 FLASH. { <i>FLASH_LEN_ID-3..0</i> } = [0,0,1,1] corresponds to 8Mx8 FLASH. { <i>FLASH_LEN_ID-3..0</i> } = [0,1,0,0] corresponds to 64Mx8 FLASH.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

***HCX_AX_CNTR1_RG* *HCX* control register for DSP reset control**

HCX_AX_CNTR1_RG *HCX* control register is used to control reset signal for on-board DSP from host *HCX* controller application.

***HCX_AX_CNTR1_RG* register (r/w)**

0	0	0	0	0	0	0	<i>DSP_RUN</i> (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-29](#) provides details about bits of *HCX_AX_CNTR1_RG* *HCX* control register.

Table 2-29. *HCX_AX_CNTR1_RG* register bits.

register bits	access mode	value on <i>HCX</i> reset	Description
<i>DSP_RUN</i>	r/w	0	Reset control for <i>TORNADO-E2/6xxx</i> on-board DSP. <i>DSP_RUN</i> = 0 setting asserts active DSP RESET signal and holds DSP in the reset state. While DSP is held in the reset state, then the DSP bootmode, HPI port enable and FLASH write protection can be set. <i>DSP_RUN</i> = 1 setting releases DSP RESET signal and DSP starts upon the selected DSP bootmode.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on *HCX* interface reset condition.

While the on-board DSP is held in the reset state via *DSP_RUN* bit of *HCX_AX_CNTR1_RG* *HCX* control register, then host *HCX* application can configure DSP bootmode and environment using the following options:

- The DSP bootmode can be set via *DSP_BMODE* bit of *HCX_AX_CNTR2_RG* *HCX* control register ([Table 2-30](#)).
- The DSP on-chip HPI port can be enabled for *TORNADO-E/6713* controller with TMS320C6713 DSP via *DSP_HPI_EN* bit of *HCX_AX_CNTR2_RG* *HCX* control register ([Table 2-30](#)).
- The DSP FLASH memory write can be enabled via *FLASH_WR_EN* and *FLASH64M_BOOT_SECTOR_WR_EN* bits of *HCX_AX_CNTR2_RG* *HCX* control register ([Table 2-30](#)).

NOTE

As soon as the DSP reset signal is released by host *HCX* controller application by setting the *DSP_RUN* bit of *HCX_AX_CNTR1_RG* *HCX* control register into the '1' state, then the last settings for DSP bootmode, HPI port enable and FLASH memory write enable control via *HCX_AX_CNTR2_RG* *HCX* control register are latched and can't be updated until the DSP reset signal is asserted again.

For user convenience, the on-board VD2 LED indicator (refer to [Figure 2-2](#) and [Figure A-1](#)) is provided for visual indication of a current state for the DSP reset signal.

HCX_AX_CNTR2_RG *HCX* control register for DSP start-up configuration control

HCX_AX_CNTR2_RG register of *HCX* interface is used to read-back DSP operation mode and to set DSP bootmode, enable DSP FLASH memory write and DSP HPI port, and to enable HPI port timeout control.

HCX_AX_CNTR2_RG register (r/w)

0	0	<i>FLASH_WR_EN</i> (r/w, 0+)	<i>FLASH64M_BOOT_SECTOR_WR_EN</i> (r/w, 0+) (64Mx8 FLASH) 0 (r) (512K/1M/8Mx8 FLASH)	<i>DSP_HPI_TMOUT_EN</i> (r/w, 0+)	<i>DSP_HPI_EN</i> (r/w, 1+) (TORNADO-E2/6713 only)	0	<i>DSP_BMODE</i> (r/w, 0+)
bit-7	bit-6	Bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-30](#) provides details about bits of *HCX_AX_CNTR2_RG* *HCX* control register.

Table 2-30. *HCX_AX_CNTR2_RG* register bits.

Register bits	access mode	value on <i>HCX</i> reset	Description
<i>DSP_BMODE</i>	r/w	0	<p>Defines DSP bootmode in accordance with Table 2-1. Refer to subsection “DSP operation modes and DSP bootmodes” for more details. This bit can be written only while DSP is held in the reset state. This bit always returns current DSP bootmode configuration during reads.</p> <p><i>DSP_BMODE</i> = 0 corresponds to <i>HOST/BMODE-HPI</i> bootmode configuration in accordance with Table 2-1.</p> <p><i>DSP_BMODE</i> = 1 state corresponds to <i>HOST/BMODE-FLASH8</i> bootmode configuration in accordance with Table 2-1.</p>

<i>DSP_HPI_EN</i> (<i>TORNADO-E2/6713</i> only)	r/w	1	<p>Used to enable DSP on-chip HPI port for <i>TORNADO-E2/6713</i> controller only. This bit can be written only while DSP is held in the reset state. This bit always returns current HPI port enable status during reads. Note, that in case DSP on-chip HPI port is enabled, then host <i>HCX</i> application can upload DSP executable into the DSP environment and get access to entire DSP environment, however this results in impossibility to utilize DSP on-chip McASP-1 port in accordance with Table 2-7. In order to enable DSP on-chip serial peripherals, HPI port must be disabled.</p> <p><i>DSP_HPI_EN</i> = 0 setting disables on-board DSP HPI port of <i>TORNADO-E2/6xxx</i> DSP controller.</p> <p><i>DSP_HPI_EN</i> = 1 setting enables on-board DSP HPI port of <i>TORNADO-E2/6xxx</i> DSP controller. This is default setting on <i>HCX</i> interface reset condition.</p>
<i>DSP_HPI_TMOUT_EN</i>	r/w	0	<p>Enables timeout control for host-to-HPI access cycles. For <i>TORNADO-E2/6713</i> controller, this bit is valid only while DSP on-chip HPI port is enabled. Refer to subsection “Timeout control for access to DSP on-chip HPI port of HCX-ASYNC interface” later in this section for more details.</p> <p><i>DSP_HPI_TMOUT_EN</i> = 0 disables timeout control for host-to-HPI access cycles. This setting allows the host-to-HPI access cycle to proceed infinitely unless HPI request will be completed within the DSP. Care must be taken to ensure that host <i>HCX</i> controller application will not get stalled due to possible infinite pending of the host-to-HPI accesses inside DSP chip.</p> <p><i>DSP_HPI_TMOUT_EN</i> = 1 enables timeout control for host-to-HPI access cycles. This imposes maximum 10 μS duration for all host-to-HPI access cycles. In case HPI request will not complete within 10 μS, then it will be automatically cancelled by <i>HCX-ASYNC</i> interface controller with the <i>DSP_HPI_TMOUT_ERR</i> error bit set to the ‘1’ state within the HCX_AX_INT_STAT_RG <i>HCX</i> control register (Table 2-31). <i>DSP_HPI_TMOUT_ERR</i> error bit can be configured to generate interrupt request to host <i>HCX</i> controller via any of <i>HCX-ASYNC_HIRQ0</i> or <i>HCX-ASYNC_HIRQ1</i> interrupt request outputs in case this is configured via HCX_AX_HIRQ0_SEL_RG and HCX_AX_HIRQ1_SEL_RG <i>HCX</i> control registers (Table 2-32). This is a recommended setting for <i>DSP_HPI_TMOUT_EN</i> bit.</p>
<i>FLASH64M_BOOT_SECTOR_WR_EN</i>	r/w	0	<p>Host write protection control for 1st sector of 64Mx8 FLASH memory. This bit is not available for 512Kx8, 1Mx8 and 8Mx8 FLASH. This bit has a priority over <i>FLASH64M_BOOT_SECTOR_WR_EN</i> bit of DSP_FLASH_CNTR_RG DSP external control register as it is described in Table 2-6 and subsection “FLASH memory area” earlier in this chapter. This bit can be written only while DSP is held in the reset state.</p> <p><i>FLASH64M_BOOT_SECTOR_WR_EN</i> = 0 disables write access to the 1st sector of on-board 64Mx8 FLASH on the host <i>HCX</i> controller side. DSP will be not able to set <i>FLASH64M_BOOT_SECTOR_WR_EN</i> bit of DSP_FLASH_CNTR_RG DSP external control register.</p> <p><i>FLASH64M_BOOT_SECTOR_WR_EN</i> = 1 enables write access to the 1st sector of on-board 64Mx8 FLASH on the host <i>HCX</i> controller side. DSP will be able to set <i>FLASH64M_BOOT_SECTOR_WR_EN</i> bit of DSP_FLASH_CNTR_RG DSP external control register. This bit can be set to the ‘1’ state only in case on-board SW1-2 is set to the ON state and SW1-3 is set to the OFF state.</p>
<i>FLASH_WR_EN</i>	r/w	0	<p>Host write protection control for on-board FLASH memory. This bit has a priority over <i>FLASH_WR_EN</i> bit of DSP_FLASH_CNTR_RG DSP external control register as it is described in Table 2-5 and subsection “FLASH memory area” earlier in this chapter. This bit can be written only while DSP is held in the reset state.</p> <p><i>FLASH_WR_EN</i> = 0 disables write access to on-board FLASH on the host <i>HCX</i> controller side. DSP will be not able to set <i>FLASH_WR_EN</i> bit of DSP_FLASH_CNTR_RG DSP external control register.</p> <p><i>FLASH_WR_EN</i> = 1 enables write access to on-board FLASH on the host <i>HCX</i> controller side. DSP will be able to set <i>FLASH_WR_EN</i> bit of DSP_FLASH_CNTR_RG DSP external control register. This bit can be set to the ‘1’ state only in case on-board SW1-2 is set to the ON state.</p>

- Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
 2. Highlighted configurations correspond to default settings on *HCX* interface reset condition.

NOTE

DSP_BMODE, *DSP_HPI_EN*, *FLASH_WR_EN* and *FLASH64M_BOOT_SECTOR_WR_EN* bits of [HCX_AX_CNTR2_RG](#) HCX control register can be written only while the DSP is held in the reset state by setting the *DSP_RUN* bit of [HCX_AX_CNTR1_RG](#) HCX control register ([Table 2-29](#)) into the '0' state.

As soon as the DSP reset signal is released by host HCX controller application by setting the *DSP_RUN* bit of [HCX_AX_CNTR1_RG](#) HCX control register into the '1' state, then the last settings for *DSP_BMODE*, *DSP_HPI_EN*, *FLASH_WR_EN* and *FLASH64M_BOOT_SECTOR_WR_EN* bits of [HCX_AX_CNTR2_RG](#) HCX control register are latched and can't be updated until the DSP reset signal is asserted again.

DSP-to-Host interrupt requests via HCX-ASYNC interface

HCX-ASYNC interface can generate one to four DSP-to-Host interrupt requests (*HCX_AX_HIRQ-0..3*) to host HCX controller, which are used for general Host-to-DSP communication. The particular number of DSP-to-Host interrupt requests depends upon the controller type.

NOTE

TORNADO-E2/6713 DSP controller provides two Host-to-DSP interrupt request outputs (*HCX_AX_HIRQ-0* and *HCX_AX_HIRQ-0*) via HCX-ASYNC interface.

Each of the DSP-to-Host interrupt request outputs of TORNADO-E2/6xxx DSP controllers is individually configured to generate interrupt request from available on-board host interrupt request sources:

- *DSP_HPI_HINT* DSP-to-host interrupt request via DSP on-chip HPI port, which also appears as the *HINT* bit of the DSP on-chip HPI port control register (HPIC). *DSP_HPI_HINT* interrupt request is asserted as soon as the *HINT* bit of DSP on-chip HPIC register will be set to the '1' state by DSP application. On host HCX controller side, *DSP_HPI_HINT* interrupt request is available for a software polling via the *DSP_HPI_HINT* bit of [HCX_AX_INT_STAT_RG](#) HCX control register ([Table 2-31](#)) and via the *HINT* bit of the DSP on-chip HPIC register. *DSP_HPI_HINT* DSP-to-host interrupt request via DSP on-chip HPI port is cleared when host software writes the '1' value into the *HINT* bit of HPIC register (refer to subsection "[DSP on-chip HPI port area of HCX-ASYNC interface](#)" later in this section for more details).
- *DSP_HPI_TMOUT_ERR* timeout error flag, which is set in case HCX-ASYNC interface of TORNADO-E2/6xxx DSP controllers detects the timeout condition during host HCX controller to any of the DSP on-chip HPI port registers (refer to subsection "[Timeout control for access to DSP on-chip HPI port of HCX-ASYNC interface](#)" later in this section for more details). *DSP_HPI_TMOUT_ERR* error flag is available for software polling via the [HCX_AX_INT_STAT_RG](#) HCX control register ([Table 2-31](#)). *DSP_HPI_TMOUT_ERR* error flag is cleared when host HCX controller application writes to the [HCX_AX_CLR_HPI_TMOUT_ERR_RG](#) HCX control register (written data is ignored).

The following HCX control registers are used to configure DSP-to-Host interrupt request and to read status of host interrupt request sources:

- [HCX_AX_HIRQ0_SEL_RG](#) and [HCX_AX_HIRQ1_SEL_RG](#) HCX control registers are used to configure *HCX_AX_HIRQ-0* and *HCX_AX_HIRQ-0* DSP-to-Host interrupt request outputs correspondingly of HCX-ASYNC interface of TORNADO-E2/6713 controller.
- [HCX_AX_INT_STAT_RG](#) read-only HCX control register is used to read status of interrupt request sources.

NOTE

All DSP-to-Host interrupt request outputs of *TORNADO-E2/6xxx* DSP controllers default to the OFF on *HCX* interface reset condition.

HCX_AX_INT_STAT_RG read-only HCX control register for status information of DSP-to-Host interrupt request sources via HCX-ASYNC interface

HCX_AX_INT_STAT_RG read-only *HCX* control register is used to read status information DSP-to-Host interrupt request sources via *HCX-ASYNC* interface of *TORNADO-E2/6xxx* DSP controllers.

HCX_AX_INT_STAT_RG register (r)

0	0	0	0	0	0	DSP_HPI_TMOUT_ERR (r, 0+)	DSP_HPI_HINT (r, 0+)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-31](#) provides details about bits of *HCX_AX_INT_STAT_RG* *HCX* control register.

Table 2-31. *HCX_AX_INT_STAT_RG* register bits.

Register bits	Access mode	Value on <i>HCX</i> reset	Description
<i>DSP_HPI_HINT</i>	R	0	<p>Current status of DSP-to-host interrupt request via DSP on-chip HPI port. This bit is actually the <i>HINT</i> bit of DSP on-chip HPI control register (HPIC).</p> <p><i>DSP_HPI_HINT</i> = 0 denotes that there is no DSP-to-host interrupt request via HPI port.</p> <p><i>DSP_HPI_HINT</i> = 1 denotes that there is active DSP-to-host interrupt request via HPI port. <i>DSP_HPI_HINT</i> DSP-to-host interrupt request is set when DSP software writes the '1' value to the <i>HINT</i> bit of DSP on-chip HPIC register. Refer to subsection "Processing of DSP-to-host interrupt request via HCX-ASYNC interface" for more details.</p>
<i>DSP_HPI_TMOUT_ERR</i>	R	0	<p>Current status of HPI access timeout error flag. This flag is set in case of timeout condition during host-to-HPI access cycles with HPI timeout error control enabled via the <i>DSP_HPI_TMOUT_EN</i> bit of <i>HCX_AX_CNTR2_RG</i> <i>HCX</i> control register (Table 2-30). Refer to subsection "Timeout control for access to DSP on-chip HPI port of HCX-ASYNC interface" for more details.</p> <p><i>DSP_HPI_TMOUT_ERR</i> = 0 denotes that no HPI access timeout error condition has been detected.</p> <p><i>DSP_HPI_TMOUT_ERR</i> = 1 denotes that timeout error condition has been detected during host-to-HPI access. Once set, this flag remains in the '1' state until it is cleared by host <i>HCX</i> controller application by means of writing to the <i>HCX_AX_CLR_HPI_TMOUT_ERR_RG</i> <i>HCX</i> control register (written data is ignored). Refer to subsection "Timeout control for access to DSP on-chip HPI port of HCX-ASYNC interface" for more details.</p>

Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on *HCX* interface reset condition.

HCX_AX_HIRQ0_SEL_RG and HCX_AX_HIRQ1_SEL_RG registers for configuration of 32-bit asynchronous HCX DCM site interface interrupt request outputs

HCX_AX_HIRQn_SEL_RG *HCX* control registers (n=0,1) are used to select interrupt request source for *HCX_AX_HIRQ-0..1* interrupt request outputs of *HCX-ASYNC* interface.

HCX_AX_HIRQ0_SEL_RG and HCX_AX_HIRQ1_SEL_RG registers (r/w)

0	0	0	0	0	0	HIRQ_SEL-1 (r/w, 0+)	HIRQ_SEL-0 (r/w, 0+)
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

[Table 2-32](#) provides details about bits for *HCX_AX_HIRQ0_SEL_RG* and *HCX_AX_HIRQ1_SEL_RG* *HCX* control registers.

Table 2-32. HCX_AX_HIRQ0_SEL_RG and HCX_AX_HIRQ1_SEL_RG register bits.

register bits	access mode	value on <i>HCX</i> reset	Description
{ <i>HIRQ_SEL-1..0</i> }	r/w	[0,0]	<p>Select interrupt request source for the corresponding <i>HCX</i> interrupt request output of <i>HCX-ASYNC</i> interface.</p> <p>{<i>HIRQ_SEL-1..0</i>} = [0,0] corresponds to no interrupt request source selected. The corresponding <i>HCX</i> interrupt request output will remain in inactive state.</p> <p>{<i>HIRQ_SEL-1..0</i>} = [0,1] corresponds to <i>DSP_HPI_TMOUT_ERR</i> HPI access timeout error flag source selected as an interrupt request source. Refer to subsection "Timeout control for access to DSP on-chip HPI port of <i>HCX-ASYNC</i> interface" for more details.</p> <p>{<i>HIRQ_SEL-1..0</i>} = [1,0] setting corresponds to the <i>DSP_HPI_HINT</i> DSP-to-host interrupt request via DSP on-chip HPI port selected as an interrupt request source. <i>DSP_HPI_HINT</i> is actually the <i>HINT</i> bit of the DSP on-chip HPIC register. Refer to subsection "Processing of DSP-to-host interrupt request via <i>HCX-ASYNC</i> interface" for more details.</p> <p>{<i>HIRQ_SEL-1..0</i>} = [1,1] setting is reserved.</p>

Note:

1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on *HCX* interface reset condition.

DSP on-chip HPI port area of *HCX-ASYNC* interface

HCX-ASYNC interface of *TORNADO-E2/6xxx* DSP controllers allows host *HCX* controller access to the DSP on-chip HPI port registers in order to communicate with the DSP application and to upload/download real-time data and executable.

NOTE

This subsection provides limited information about TMS320C6xxx DSP on-chip HPI port registers as far as it is required to describe *HCX-ASYNC* interface of *TORNADO-E2/6xxx* DSP controllers.

For more information about TMS320C6xxx DSP on-chip HPI port refer to original TI TMS320C6xxx user's guides, which are supplied in electronic form along with this user's guide.

TMS320C6xxx DSP provide on-chip 32-bit HPI port, which is used for the following purposes:

- to allow host access the DSP environment (DSP on-chip memory and registers, external SBSRAM/SDRAM/FLASH memories, DSP external control registers, etc) of on-board DSP from host application concurrently with the DSP program execution
- to generate host-to-DSP interrupt request via the *DSPINT* bit of DSP on-chip HPIC register
- to generate DSP-to-host interrupt request via the *HINT* bit of DSP on-chip HPIC register.

Host-to-DSP communication via DSP on-chip HPI port area of *HCX-ASYNC* interface typically provides 100..300 Kword/s throughoutput performance. This performance is sufficient to upload DSP executable and for general host-to-DSP communication.

TORNADO-E2/6713 with on-board TMS320C6713 DSP provides 16-bit interface to the DSP on-chip HPI port. This denotes that each of the DSP on-chip 32-bit HPI port registers (HPIC, HPIA and HPID) are splitted into two 16-bit registers (LSW and MSW) and every access cycle to the DSP on-chip HPI port must include read/write from/to the corresponding LSW register first and MSW register afterthat. The following is a list of HPI port registers for *HCX-ASYNC* interface of *TORNADO-E2/6713* controller (refer to [Table 2-25](#) for *HCX-ASYNC* interface address map):

- *HCX_AX_DSP_HPIC_LSW16_RG* and *HCX_AX_DSP_HPIC_MSW16_RG* registers, which are the LSW and MSW 16-bit words of DSP on-chip 32-bit HPI port control register (HPIC)
- *HCX_AX_DSP_HPIA_LSW16_RG* and *HCX_AX_DSP_HPIA_MSW16_RG* registers, which are the LSW and MSW 16-bit words of DSP on-chip 32-bit HPI address register (HPIA)
- *HCX_AX_DSP_HPID_AINC_LSW16_RG* and *HCX_AX_DSP_HPID_AINC_MSW16_RG* registers, which are the LSW and MSW 16-bit words of DSP on-chip 32-bit HPI data register with HPI address postincrement feature (HPID_AINC)
- *HCX_AX_DSP_HPID_LSW16_RG* and *HCX_AX_DSP_HPID_MSW16_RG* registers, which are the LSW and MSW 16-bit words of DSP on-chip 32-bit HPI data register (HPID).

NOTE

Host *HCX* controller application must use 32-bit data words to access 16-bit LSW/MSW of DSP on-chip 32-bit HPI port registers via *16-bit HPI port registers area* of *HCX-ASYNC* interface of *TORNADO-E2/6713* controller. The 16-bit LSW/MSW HPI port registers are aligned to 16-bit least significant half-words of 32-bit data words of *HCX-ASYNC* interface.

It is not allowed to access particular bytes of LSW and MSW words via *16-bit HPI port registers area*.

Timeout control for access to DSP on-chip HPI port of *HCX-ASYNC* interface

TMS320C6xxx DSP on-chip HPI port provides simple asynchronous parallel interface with input data strobe (*HPI_STB* signal at [Figure 2-4](#) and [Figure 2-5](#)) and output data ready confirmation (*HRDY* signal at [Figure 2-4](#) and [Figure 2-5](#)). Internally, the DSP on-chip HPI port request is processed via the on-chip HPI DMA controller using an bus arbitration and priority access schemes.

Maximum access time to the HPI port data registers is not guaranteed due to a complicated architecture of TMS320C6xxx DSP and a large number of internal parallel processes. This parameter is application specific and depends upon the application memory map (i.e. allocation of the code and data sections among the memories within the DSP environment).

HPI port access is completed within a minimum access times in case HPI port is addressing the DSP on-chip memory. This is a recommended configuration for user applications. Any violation of this, specifically HPI access to external SDRAM memory, may result in unpredictable delays and corresponding pending for HPI access cycles, and will therefore reduce overall host *HCX* controller performance.

As a summary, there are known conditions when HPI request cannot complete within a reasonable time by TMS320C6xxx DSP on-chip HPI DMA controller, that may result in infinite pending of host-to-HPI access, and therefore, infinite stall and unreliable operation of host *HCX* controller application. The following is the list of several most typical conditions, which result in infinite pending of host-to-HPI access for TMS320C6xxx DSP:

- Any of the DSP on-chip HPI port register is accessed while DSP is in the reset state.
- DSP has been put into either PD2 or PD3 powerdown mode via corresponding setting of PWRD bit field of DSP on-chip CSR register (refer to the TMS320C6xxx user's guide for more details).
- HPI port is accessing external memory (SBSRAM or SDRAM), which contains DSP executable code currently being executed by the DSP (this is known as the DSP EMIF access conflict).
- Sometimes when DSP is executing invalid code due to a software bug.

In order to exclude infinite stall of host *HCX* controller application caused by probable infinite pending of host-to-HPI access cycles and provide its reliable functionality, *HCX-ASYNC* interface of *TORNADO-E2/6xxx* DSP controllers include HPI access timeout controller.

HPI access timeout controller for host-to-HPI access cycles is enabled via the *HPI_TMOUT_EN* bit of [HCX_AX_CNTR2_RG](#) *HCX* control register ([Table 2-30](#)). Note, that this bit defaults to the '0' state (i.e. disabled) on

HCX-ASYNC interface reset condition. In case *HPI_TMOUT_EN* bit of [HCX_AX_CNTR2_RG](#) *HCX* control register is set into the '0' state, then the HPI access timeout controller is disabled and there is no timeout restriction applied for HPI port access cycles. This setting allows host-to-HPI access cycle to proceed infinitely long unless HPI request will be completed within DSP. This setting must be used carefully and only in case the on-board DSP is not able to complete HPI access cycle within 10 μ s time interval. This setting can result in infinite stall of *HCX* controller environment in case *TORNADO-E2/6xxx* on-board DSP will stall on any reason (typically, during software debugging when executing invalid instruction). Once occurred, infinite stall of host *HCX* controller application can be aborted by applying host *HCX* controller reset. This is completely user responsibility to guarantee that there will be no infinite stall of host *HCX* application due to the listed above conditions.

Instead, in case *HPI_TMOUT_EN* bit of [HCX_AX_CNTR2_RG](#) *HCX* control register is set into the '1' state, then HPI access timeout controller is enabled and every access from host *HCX* controller application to the DSP on-chip HPI port registers will be aborted on HPI access timeout error condition in case it cannot terminate normally within 10 μ s time interval. 10 μ s HPI port timeout interval can't be changed and meets reasonable requirements of virtually all applications. In case HPI port timeout error condition occurs, then internal *HPI_TMOUT_ERR* HPI timeout error flag is set to the '1' state.

HPI_TMOUT_ERR HPI timeout error flag is available for read via [HCX_AX_INT_STAT_RG](#) read-only *HCX* control register ([Table 2-31](#)) and can generate host *HCX* controller interrupt request in case this is configured via [HCX_AX_HIRQ0_SEL_RG](#) and [HCX_AX_HIRQ1_SEL_RG](#) *HCX* control registers ([Table 2-32](#)). Refer to subsection "[DSP-to-Host interrupt requests via HCX-ASYNC interface](#)" for more details.

Once the *HPI_TMOUT* timeout error flag has been set into the '1' state, then it remains in this state until it will be cleared by host *HCX* controller application by means of writing to the [HCX_AX_CLR_HPI_TMOUT_ERR_RG](#) write-only *HCX* control register.

NOTE

It is recommended that host software will perform periodical check of the state of *HPI_TMOUT_ERR* bit of [HCX_AX_INT_STAT_RG](#) *HCX* control register during host-to-HPI accesses in order to ensure that host-to-HPI accesses have been completed successfully.

[Figure 2-4](#) and [Figure 2-5](#) below provide timing diagrams for normal completion of host-to-HPI access cycle and termination of host-to-HPI access cycle on HPI timeout conditions correspondingly.

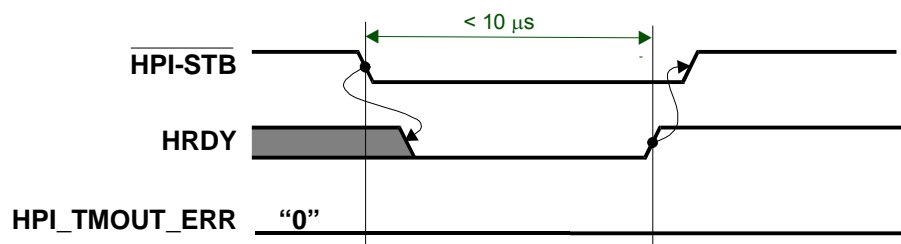


Figure 2-4. Timing diagram for normal termination of host-to-HPI access cycle.

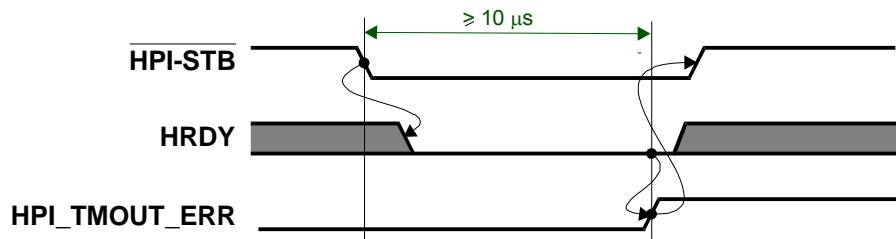


Figure 2-5. Timing diagram for termination of host-to-HPI access cycle on the timeout condition.

HCX_AX_CLR_HPI_TMOUT_ERR_RG write-only HCX control register for clearing of HPI access timeout error flag

HCX_AX_CLR_HPI_TMOUT_RG write-only *HCX* control register is used to clear *HPI_TMOUT_ERR* HPI access timeout error flag after it has been recognized and processed by host *HCX* controller application. Refer to subsection “[Timeout control for access to DSP on-chip HPI port of HCX-ASYNC interface](#)” for more details about *HPI_TMOUT_ERR* HPI access timeout error flag. Note, that when writing to the *HCX_AX_CLR_HPI_TMOUT_ERR_RG* write-only register, write data is ignored.

HCX_AX_CLR_HPI_TMOUT_ERR_RG register (w)

x	x	x	x	X	x	x	x
bit-7	bit-6	bit-5	bit-4	Bit-3	bit-2	bit-1	bit-0

Processing of DSP-to-host interrupt request via HCX-ASYNC interface

TORNADO-E2/6xxx controllers allow generation of DSP-to-Host interrupt request to *HCX* controller via any of *HCX-ASYNC* interface interrupt request outputs (*HCX_AX_HIRQ-0..1*) using *DSP_HPI_HINT* DSP-to-host interrupt request via DSP on-chip HPI port. *DSP_HPI_HINT* is actually the *HINT* bit of DSP on-chip HPI port control register (HPIC).

NOTE

This subsection provides limited information about DSP-to-host interrupt request via TMS320C6xxx DSP on-chip HPI port as far as it is required to describe operation of *HCX* DCM site interface of *TORNADO-E2/6xxx* DSP controllers.

For more information about TMS320C6xxx DSP on-chip HPI port refer to original TI TMS320C6xxx user's guides, which are supplied in electronic form along with this user's guide.

DSP_HPI_HINT DSP-to-host interrupt request can be set by DSP application only by means of writing the '1' value into the *HINT* bit of DSP on-chip HPIC register (@0x01880000).

NOTE

Writing of '0' value into the *HINT* bit of the TMS320C6xxx DSP on-chip HPIC register (@0x01880000) by on-board TMS320C6xxx DSP software has no effect.

Current state of *DSP_HPI_HINT* DSP-to-host interrupt request of DSP on-chip HPI port can be polled by host *HCX* controller application via [HCX_AX_INT_STAT_RG](#) read-only *HCX* control register (Table 2-31) and via the *HINT* bit of DSP on-chip HPIC register (refer to subsection “[DSP on-chip HPI port area of HCX-ASYNC interface](#)” for more details).

NOTE

For performance reasons, it is recommended to poll the *DSP_HPI_HINT* bit of [HCX_AX_INT_STAT_RG](#) read-only *HCX* control register rather than the *HINT* bit of the DSP on-chip HPIC register.

Once set, *DSP_HPI_HINT* DSP-to-host interrupt request via DSP on-chip HPI port can be cleared by host *HCX* controller application only by means of writing the '1' value to the *HINT* bit of DSP on-chip HPIC register.

NOTE

Writing of '0' value to the *HINT* bit of TMS320C6xxx DSP on-chip HPIC register from host *HCX* controller application has no effect.

Either [HCX_AX_HIRQ0_SEL_RG](#) or [HCX_AX_HIRQ1_SEL_RG](#) *HCX* control register shall be configured in accordance with [Table 2-32](#) to allow the *DSP_HPI_HINT* DSP-to-host interrupt request to pass to the corresponding *HCX-ASYNC_HIRQ0* or *HCX-ASYNC_HIRQ1* DSP-to-Host interrupt request output of *HCX-ASYNC* interface. Refer to subsection "[DSP-to-Host interrupt requests via HCX-ASYNC interface](#)" for more details.

Generation of Host-to-DSP interrupt request via HCX-ASYNC interface

TORNADO-E2/6xxx DSP controllers allow generation of Host-to-DSP interrupt request via DSP on-chip HPI port using *DSPINT* bit of DSP on-chip HPI port control register (HPIC).

NOTE

This subsection provides limited information about Host-to-DSP interrupt request via TMS320C6xxx DSP on-chip HPI port as far as it is required to describe the operation of *HCX-ASYNC* interface of *TORNADO-E2/6xxx* DSP controllers.

For more information about TMS320C6xxx DSP on-chip HPI port refer to original TI TMS320C6xxx user's guides, which are supplied in electronic form along with this user's guide.

Host-to-DSP interrupt request can be set by host *HCX* controller application by means of writing the '1' value to *DSPINT* bit of DSP on-chip HPIC register (refer to subsection "[DSP on-chip HPI port area of HCX-ASYNC interface](#)" for more details).

NOTE

Writing of '0' value to *DSPINT* bit of TMS320C6xxx DSP on-chip HPIC register from host *TORNADO* DSP software has no effect.

DSP application can either poll status of *DSPINT* bit via DSP on-chip HPIC register (@0x01880000), or use it to generate interrupt to the DSP core. After DSP application recognizes and processes host-to-DSP interrupt request via *DSPINT* bit of HPIC register (@0x01880000), it must clear *DSPINT* bit by means of writing the '1' value to it.

NOTE

Writing of '0' value to the *DSPIN* bit of TMS320C6xxx DSP on-chip HPIC register (@0x01880000) by DSP software has no effect.

HCX-SYNC synchronous section of HCX DCM site interface

HCX-SYNC interface of *TORNADO-E2/6xxx* DSP controllers is used for high-speed communication between DSP and *HCX* controller via shared memory or FIFO resources located at *HCX* controller DCM. *HCX-SYNC* interface is mapped into the DSP memory map (refer to [Table 2-2](#)) and is accessed by on-board DSP as just SBSRAM memory.

NOTE

HCX-SYNC interface of *TORNADO-E2/6xxx* DSP controllers is controlled exclusively by on-board DSP and appears as the DSP external memory area.

Host *HCX* controller has no access to *HCX-SYNC* interface of *TORNADO-E2/6xxx* DSP controller.

HCX-SYNC interface is 32-bit parallel interface with 24-bit addressing capabilities. Due to a limited addressing capabilities, *TORNADO-E2/6713* on-board DSP provides direct addressing to 256Kx32 page of *HCX-SYNC* interface only, whereas the addressed page is selected via [DSP_HCX_SYNC_PAGE_RG](#) DSP external control register.

HCX-SYNC interface can generate interrupt to the on-board DSP (*HCX_SYNC_IRQ* for *TORNADO-E2/6713* controller at [Figure 2-3](#)) via any of the DSP EXT_INT4..7 external interrupt requests in case this is configured via either of [DSP_EXT_INT4_SEL_RG](#), [DSP_EXT_INT5_SEL_RG](#), [DSP_EXT_INT6_SEL_RG](#), [DSP_EXT_INT7_SEL_RG](#) DSP external control registers in accordance with [Table 2-14](#).

2.5 DSP Software Development Tools

TORNADO-E2/6xxx DSP controllers have been designed to use scan-path JTAG emulation technique in order to debug application for on-board TMS320C6xxx DSP. This delivers non-intrusive debugging of on-board DSP software at full DSP speed.

Connection of external JTAG emulator to TORNADO-E2/6xxx on-board DSP

Compatible scan-path emulation tools include TI JTAG emulators and MicroLAB Systems *MIRAGE* JTAG emulators, which all connect to *TORNADO-E2/6xxx* DSP controllers on-board JTAG connector (JP3 at [Figure A-1](#)) via optional external *T/X-JTAG/C1* JTAG converter cable as shown on [Figure 2-6](#).

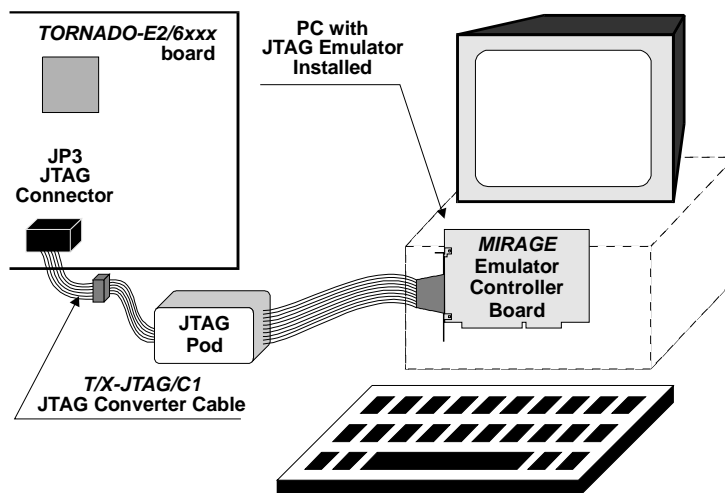


Figure 2-6. Connection of external JTAG emulator to TORNADO-E2/6xxx on-board DSP.

T/X-JTAG/C1 JTAG converter cable (refer to [Appendix B](#) for more details) comes standard with TORNADO-E2/6xxx DSP controllers and is required to connect on-board miniature JP3 JTAG connector (refer to subsection “[JP3 JTAG emulator connector](#)”) for connection to external TI and MicroLAB Systems JTAG emulators with the industry-standard 14-pin 0.1”x0.1” JTAG interface connector.

NOTE

Refer to the user’s guide for your JTAG emulator for more details about installation of your JTAG emulator.

On-board JTAG path for connection to external JTAG emulator

TORNADO-E2/6xxx DSP controllers on-board JTAG path for connection to external JTAG emulator comprises the on-board JTAG connector (JP3) and JTAG port of on-board TMS320C6xxx DSP as it is shown at [Figure 2-7](#).

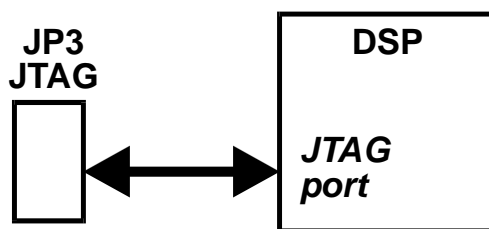


Figure 2-7. TORNADO-E2/6xxx DSP controllers on-board JTAG path for connection to external JTAG emulator.

TORNADO-E2/6xxx on-board JTAG path provides 3v/5v compatible JTAG interface signals for connection to external JTAG emulator.

Maximum JTAG clock frequency

TORNADO-E2/6xxx DSP controllers are using high-performance TMS320C6xxx DSP, which supports JTAG clock frequency (TCK) as high as 30 MHz.

Normally, JTAG emulators provide only 10 MHz JTAG clock frequency and do not allow to change it. However, in case your JTAG emulator can generate JTAG frequency 30 MHz, then you can use this selection and benefit from a high-speed JTAG communication.

NOTE

Maximum JTAG clock frequency (TCK) might be reduced if either several *TORNADO-E2/6xxx* DSP controllers or other JTAG compatible devices are connected into JTAG path along with *TORNADO-E2/6xxx* DSP controller.

NOTE

Check with your JTAG emulator documentation about support for high-speed JTAG clock.

Configuring TI Code Composer Studio TMS320C6xxx emulator drivers to debug TORNADO-E2/6xxx on-board DSP

Industry standard TI ‘C6000 Code Composer Studio (CCS) debug tools v.2.21 or later are required to debug *TORNADO-E2/6xxx* on-board DSP software via JTAG emulator.

NOTE

TORNADO-E2/6xxx on-board TMS320C6xxx DSP must be released from the reset state prior running TI CCS TMS320C6xxx software debugger (refer to sections “[DSP operation modes and DSP bootmodes](#)” and “[HCXDCM Site Interface](#)” earlier in this chapter for more details about to control the DSP reset signal for *DSP stand-alone operation mode* and *DSP host operation mode*).

It is recommended that the corresponding GEL-file, which meets configuration of your *TORNADO-E2/6xxx* on-board DSP environment, is selected and executed at debugger. The CCS GEL-files for *TORNADO-E2/6xxx* DSP controllers are included with the *TORNADO-E2/6xxx* DSP controllers software utilities (refer to [Appendix F](#) for more details).

NOTE

For more information about TI ‘C6000 CCS debug tools refer to original TI user’s guides for TI ‘C6000 CCS compiler/debug tools, which are supplied with TI ‘C6000 CCS tools.

Chapter 3. Installation and Configuration

This chapter provides general instructions for installation *TORNADO-E2/6xxx* DSP controllers.

3.1 Installation of *TORNADO-E2/6xxx* Controller in *DSP Stand-alone Operation Mode*

In case *TORNADO-E2/6xxx* DSP controller is considered to run in *DSP stand-alone operation mode* (refer to subsection “[DSP operation modes and DSP bootmodes](#)” for more details) as a stand-alone controller with external power, then it must install into custom chassis compartment of user embedded system in accordance with the user design.

In order to install *TORNADO-E2/6xxx* in DSP stand-alone operation mode with external power into the custom chassis compartment, follow the recommendations below:

1. Switch off the power of the user embedded system.
2. Pick-up the *TORNADO-E2/6xxx* board from the shipment packaging and install it into the custom chassis compartment in accordance with user design. Screw-in the *TORNADO-E2/6xxx* DSP controller board to the mounting spacers of custom chassis.
3. Connect external power supply via JP1 external power connector (refer to [Figure A-1](#)) and keep external power supply off.
4. Set TMS320C6xxx DSP bootmode configuration (switch SW1-1 for *TORNADO-E2/6713*) in accordance with [Table 2-1](#).
5. Set *TORNADO-E2/6xxx* on-board SW1-2 and SW1-3 switches for FLASH write protection in accordance with [Table 2-5](#) and [Table 2-6](#) to meet requirements of your application.
6. If required, install or change RTC controller power backup battery in BT1 on-board socket in order to ensure that RTC controller has valid backup power and real-time clock is running (refer to [Figure A-1](#)).
7. If required, plug-in RS232C cables into on-board JP8 and/or JP9 connectors (refer to [Appendix H](#)).
8. If required, connect USB type ‘A’ cable plugs of USB cables into the on-board USB mini-AB/mini-A/mini-A connectors (JP10/JP11/JP12) or USB type ‘B’ cable plug of USB cable into on-board USB mini-B connector (JP10) (refer to [Appendix I](#)).
9. If required, plug-in external general purpose I/O cable into on-board JP13 connector (refer to [Figure A-1](#)).
10. If required, plug-in external serial cables into on-board I²C JP14/JP15 connectors (refer to [Figure A-1](#)).
11. If required, install *PIOX2* DCM (refer to [Appendix D](#)) and configure installed DCM in accordance with provided documentation.
12. If required, install *SIOX* rev.B or *ASIOX* rev.D DCM onto corresponding *SIOX* DCM site interfaces (refer to [Appendix C](#)), and configure installed *SIOX* DCM in accordance with provided documentation.
13. If required, connect external DSP reset control circuit to on-board JP2 external DSP reset connector (refer to [Figure A-1](#)).
14. If required, connect external power supply control circuit to JP16 connector (refer to [Appendix J](#)).
15. If required, connect *T/X-JTAG/C1* JTAG converter cable to on-board JP3 JTAG connector (refer to [Figure A-1](#)).
16. Switch on external power supply in order to apply power to *TORNADO-E2/6xxx* DSP controller.

3.2 Installation of *TORNADO-E2/6xxx* Controller in *DSP Host Operation Mode*

In case *TORNADO-E2/6xxx* DSP controller is considered to run in *DSP host operation mode* (refer to subsection “[DSP operation modes and DSP bootmodes](#)” for more details), then *HCX* DCM must be installed into the *HCX* DCM site of *TORNADO-E2/6xxx* DSP controller.

For installation of *HCX* DCM into the *HCX* DCM site interface of *TORNADO-E2/6xxx* DSP controller follow the recommendations below:

1. Switch off power of *TORNADO-E2/6xxx* DSP controller (or of *HCX* DCM).
2. Ensure that there are four spacers installed into the mounting holes of *TORNADO-E2/6xxx* DSP controller for fixing the position of installed *HCX* DCM ([Figure 3-1](#)). Spacers are enclosed with *TORNADO-E2/6xxx* board.

- Pick-up the *TORNADO-E2/6xxx* DSP controller board and orient it parallel to *HCX DCM* above the *HCX DCM* site area. Safely plug-in *HCX DCM* into JP7-1/JP7-2 headers of *HCX DCM* site on *TORNADO-E2/6xxx* DSP controller board. Note the difference between installations of asynchronous-only *HCX DCM* and asynchronous/synchronous *HCX DCM* as it is shown at [Figure 3-1](#) and [Figure 3-2](#) correspondingly.

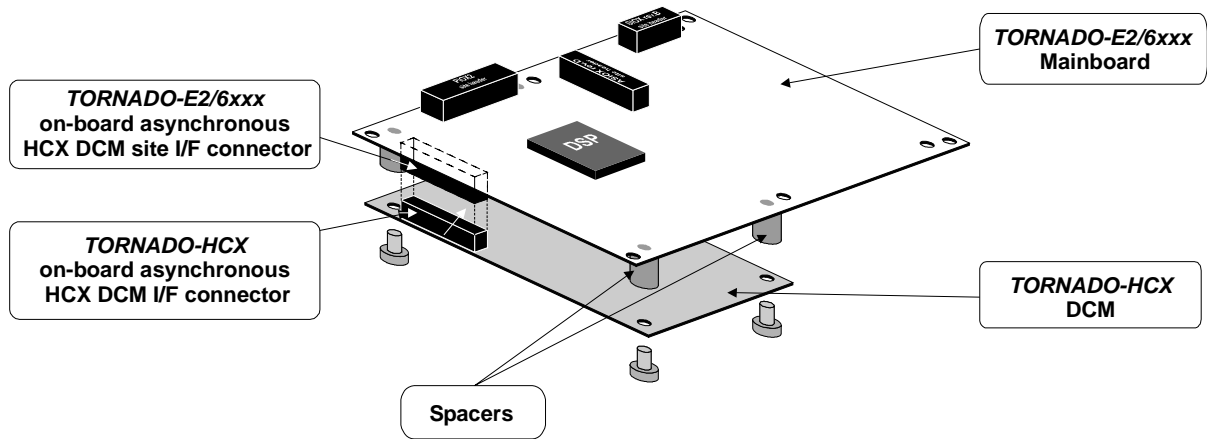


Figure 3-1. Installation of asynchronous-only *HCX DCM* into *HCX DCM* site of *TORNADO-E2/6xxx*.

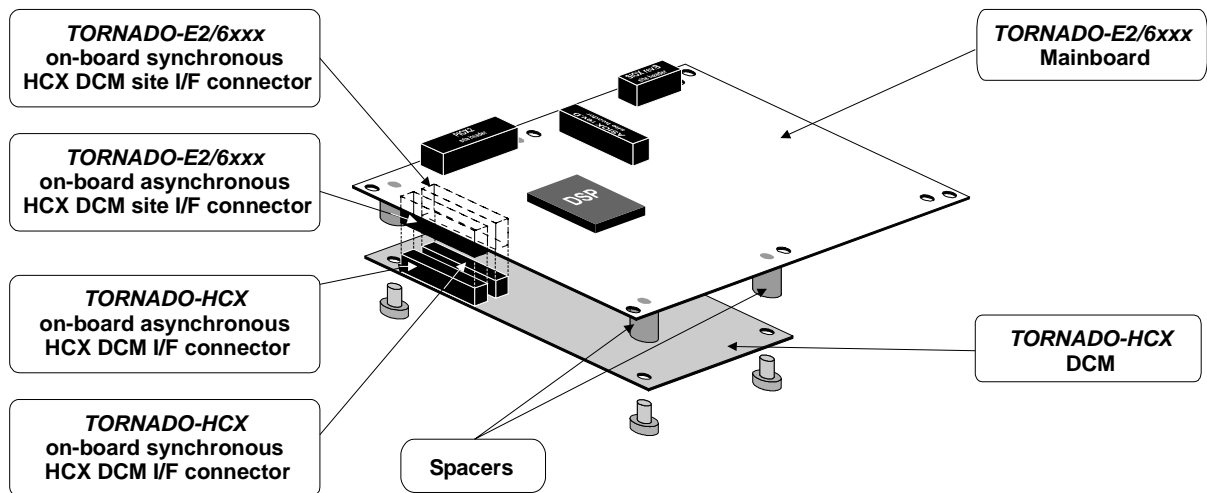


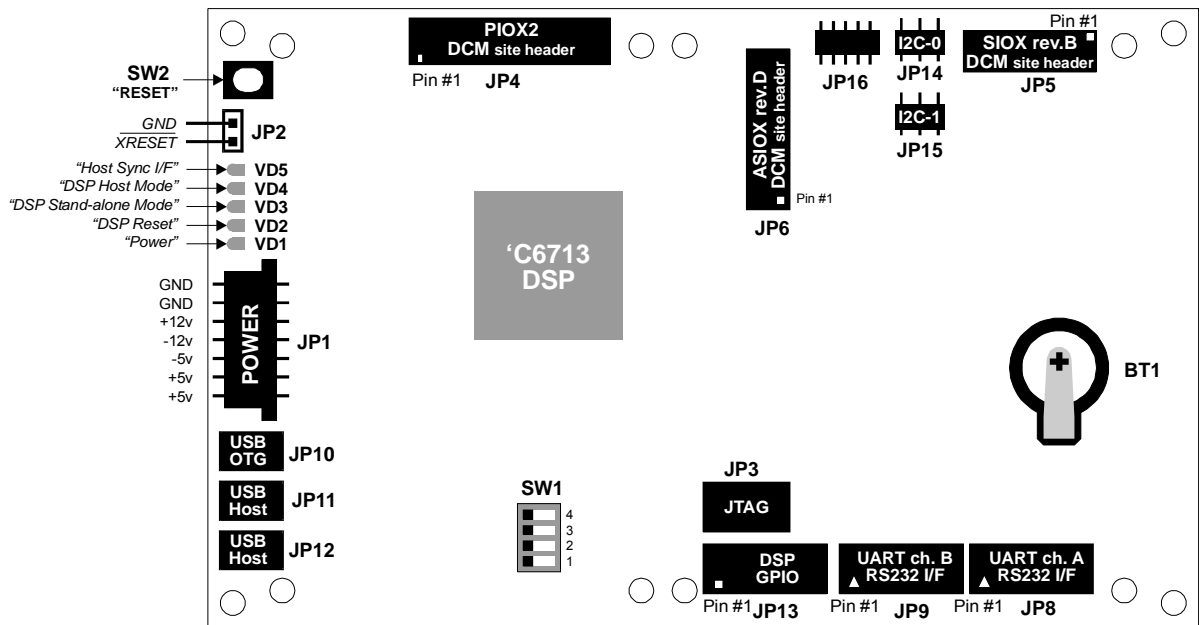
Figure 3-2. Installation of asynchronous/synchronous *HCX DCM* into *HCX DCM* site of *TORNADO-E2/6xxx*.

- Screw-in *HCX DCM* to the spacers at *TORNADO-E2/6xxx* board.
- Connect external peripherals to *TORNADO-E2/6xxx* board as it is described in items #5..12 of section 3.1.
- Switch on the power of *TORNADO-E2/6xxx* DSP controller board via JP1 external power connector or the power of *HCX DCM*.

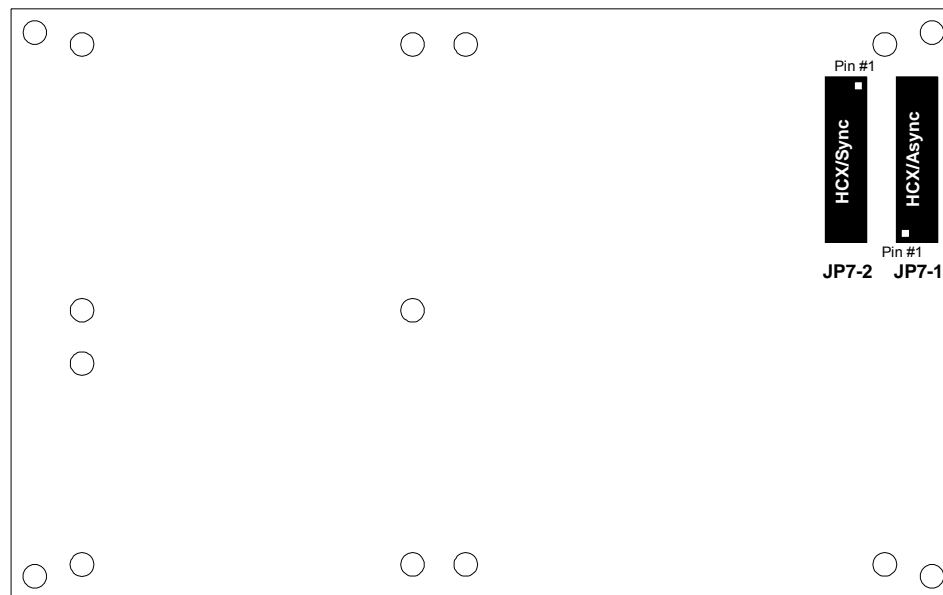
Appendix A. On-board Switches and Connectors.

This appendix provides a summary description for on-board switches, connectors and LED indicators of *TORNADO-E2/6xxx* DSP controllers.

Board layout for *TORNADO-E2/6xxx* DSP controllers is shown at [Figure A-1](#) and provides a physical allocation for on-board switches, connectors and LED indicators.



(a) Top view.



(b) Bottom view.

Figure A-1. *TORNADO-E2/6713* board layout.

Sections below in this appendix provide details about on-board switches, sockets, connectors and LED indicators.

A.1 On-board Switches

[Table A-1](#) contains a list of *TORNADO-E2/6xxx* on-board switches and the corresponding reference information.

Table A-1. On-board switches for *TORNADO-E2/6713*.

switch ID	switch button	switch function description	reference information
SW1	SW1-1	DSP Bootmode configuration for DSP stand-alone operation mode.	Table 2-1 , subsection " DSP operation modes and DSP bootmodes " of section 2.2.
	SW1-2	FLASH global write enable	Table 2-5 , subsection " FLASH memory area " of section 2.2.
	SW1-3	64Mx8 FLASH only: boot sector write enable	Table 2-6 , subsection " FLASH memory area " of section 2.2.
SW2		DSP reset pushbutton for DSP stand-alone operation mode.	Subsection " DSP operation modes and DSP bootmodes " of section 2.2.

A.2 On-board Connectors

[Table A-2](#) contains a list of *TORNADO-E2/6xxx* DSP controllers on-board connectors and the corresponding reference information.

Table A-2. *TORNADO-E2/6713* on-board connectors.

connector ID	Description	reference information
JP1	External power connector.	Figure A-2 and subsection " JP1 external power connector "
JP2	External DSP reset connector for DSP stand-alone operation mode.	Figure A-3 and subsection " JP2 external DSP reset connector "
JP3	JTAG emulator connector. External <i>T/X-JTAG/C1</i> JTAG converter cable is required to connect to external JTAG emulator. <i>T/X-JTAG/C1</i> JTAG converter cable comes standard with <i>TORNADO-E2/6xxx</i> board (refer to Appendix B).	Figure A-7 and subsection " JP3 JTAG emulator connector "
JP4	<i>PIOX2</i> DCM site interface header.	Figure D-3 and Table D-1
JP5	<i>SIOX</i> rev.B DCM site interface header.	Figure C-4 and Table C-1
JP6	<i>ASIOX</i> rev.D DCM site interface header.	Figure C-5 and Table C-2
JP7-1 JP7-2	<i>HCX</i> rev.A DCM site interface headers.	Figure E-1
JP8 JP9	RS232C interface connectors for channels "A" (JP8) and channel "B" (JP9) of UART.	Figure A-5 Appendix H

<i>JP10</i>	For single-channel USB 1.1 and USB 2.0 device controllers, this is USB device Mini-B receptacle connector. For three-channel USB 2.0 host/device controller, this is USB OTG Mini-AB receptacle connector. Industry-standard USB cables with mini-A type or mini-B type plug shall be used to connect to external host PC or device.	Appendix I
<i>JP11</i> <i>JP12</i>	USB Host Mini-A receptacle connectors. These connectors are installed for three-channel USB 2.0 host/device controller only. Industry-standard USB cables with mini-A type plug shall be used for connection to external USB devices.	Appendix I
<i>JP13</i>	GPIO connector.	Subsection “ JP13 GPIO general purpose digital I/O connector ” and subsection “ External General Purpose I/O (GPIO) ” of section 2.2
<i>JP14</i>	I ² C-0 interface connector.	Subsection “ JP14, JP15 I2C interface connectors ” and subsection “ DSP on-chip serial peripherals (McBSP, McASP, I2C ports) ” of section 2.2
<i>JP15</i>	I ² C-1 interface connector.	Subsection “ JP14, JP15 I2C interface connectors ” and subsection “ DSP on-chip serial peripherals (McBSP, McASP, I2C ports) ” of section 2.2
<i>JP16</i>	External power supply control connector.	Subsection “ JP16 external power supply control connector ” and subsection “ External power supply control ”

JP1 external power connector

TORNADO-E2/6xxx on-board JP1 external power connector is used to connect to external power supply.

NOTE

TORNADO-E2/6xxx board itself requires +5V power supply only. Other power supplies (+12V and -12V) are optional and are routed to on-board *P1OX2*, *S1OX* and *AS1OX* DCM sites and shall be used upon the requirements of particular DCM installed.

HCX DCM requires +5V power supply only.

Pinout for JP1 external power connector is shown at [Figure A-2](#). The mating plug for JP1 external power connector comes standard with *TORNADO-E2/6xxx* board. User must provide his own cable assembly for connection to external power supply upon his application requirements.

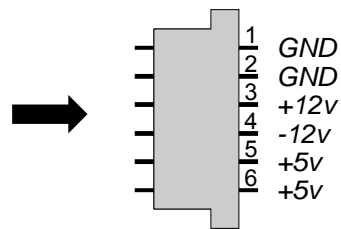


Figure A-2. Pinout of JP1 external power connector for *TORNADO-E2/6713* board.

JP2 external DSP reset connector

TORNADO-E2/6xxx on-board JP2 connector is used to provide optional external DSP reset input signal, which is valid for *DSP stand-alone operation mode* only. External DSP reset input signal can be either 3v or 5v TTL logic compliant.

Pinout for JP2 external DSP reset input connector is shown at [Figure A-3](#). The mating plug for JP2 external DSP reset input connector is an industry-standard 2-pin 0.05" miniature male plug from Molex Inc., which comes standard with *TORNADO-E2/6xxx* board. User must provide his own cable assembly for connection to external custom equipment in case this is required by application.

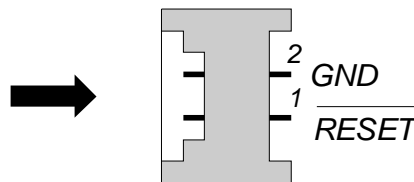


Figure A-3. Pinout of JP2 external DSP reset input connector for *TORNADO-E2/6713* board.

JP3 JTAG emulator connector

TORNADO-E2/6xxx on-board JP3 connector is used to connect to external JTAG emulator for TI TMS320 DSP. *T/X-JTAG/C1* JTAG converter cable (refer to section "[T/X-JTAG/C1 JTAG Converter Cable](#)" for more details) is required to connect between 14-pin interface connector of TI or MicroLAB Systems JTAG emulator to *TORNADO-E2/6xxx* on-board JP3 connector. *T/X-JTAG/C1* JTAG converter cable comes standard with *TORNADO-E2/6xxx* board.

Pinout for JP3 JTAG emulator connector is shown at [Figure A-4](#), which is identical to TI standard JTAG 14-pin interface connector. JP3 connector is 14-pin dual-row 2mm guarded mail header from Samtec Inc. The mating plug is Samtec p/n TCSD-07-01-N for 2mm flat cables, and it comes with *T/X-JTAG/C1* JTAG converter cable.

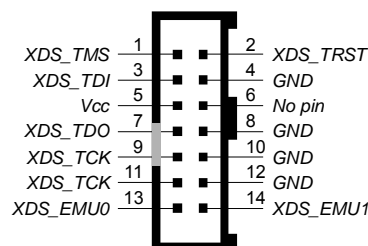


Figure A-4. Pinout of JP3 JTAG emulator connector for *TORNADO-E2/6713* board.

JP8 and JP9 RS232C interface connectors

TORNADO-E2/6xxx on-board JP8 and JP9 connector are used to connect to RS232C interfaces of channel-A and channel-B of on-board dual-channel UART correspondingly. Refer to [Appendix H](#) for more details.

Pinout for JP8 and JP9 RS232C interface connectors is shown at [Figure A-5](#). JP8 and JP9 connectors are 10-pin dual-row 2mm guarded mail headers from Samtec Inc.

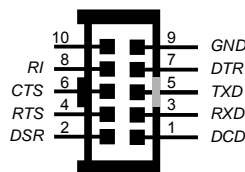


Figure A-5. Pinout of JP8 and JP9 RS232C interface connectors for *TORNADO-E2/6713* board.

The mating plugs for JP8 and JP9 RS232C interface connectors are Samtec p/n TCSD-05-01-N for 2mm flat cables. However, it is recommended to use *T/X-UART/C1* JTAG converter cables, which come standard with *TORNADO-E2/6xxx* board and provide industry-standard DB-9/male connectors for connection to PC COM ports and/or to external serial peripherals with RS232C interface using industry-standard COM-port cables. Refer to section “[T/X-UART/C1 RS232C Interface Converter Cable](#)” for more details.

JP13 GPIO general purpose digital I/O connector

TORNADO-E2/6xxx on-board *GPIO-0..7* general purpose I/O signals are available via JP13 connector (refer to [Figure A-1](#)). All *GPIO-0..7* I/O signals are 3v/5v TTL compatible.

Pinout for JP13 *GPIO* connector is shown at [Figure A-6](#). JP13 connector is 16-pin dual-row 2mm guarded mail header from Samtec Inc. The mating plug is Samtec p/n TCSD-08-01-N for 2mm flat cables, and it comes standard with *TORNADO-E2/6xxx* board. User must provide his own cable assembly for connection to custom equipment as it is required by application.

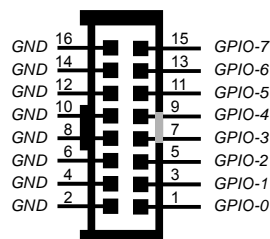


Figure A-6. Pinout of JP13 GPIO connector for *TORNADO-E2/6713* board.

JP14, JP15 I²C interface connectors

TORNADO-E2/6xxx on-board JP14 and JP15 connectors are used for DSP I²C-0 and I²C-1 interfaces correspondingly (refer to [Figure A-1](#)).

Pinout for JP14 and JP15 I²C connectors is shown at [Figure A-7](#). The mating plugs for JP14 and JP15 connectors are industry-standard 3-pin 0.05” miniature male plugs from Molex Inc., which come standard with *TORNADO-E2/6xxx* board. User must provide his own cables assembly for connection to custom equipment as it is required by application.

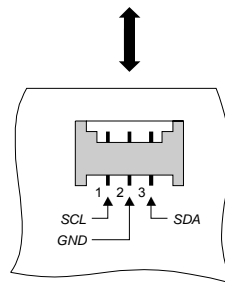


Figure A-7. Pinout of JP14 and JP15 I²C interface connectors for *TORNADO-E2/6713* board.

JP16 external power supply control connector

TORNADO-E2/6xxx on-board JP16 connector (refer to [Figure A-1](#)) is used for remote control of external power supply via on-board RTC controller. Refer to “[Appendix J. Real-time Clock \(RTC\) Controller](#)” for more details.

Pinout for JP16 connectors is shown at [Figure A-8](#). The mating plug is an industry-standard 5-pin 0.05” miniature male plug from Molex Inc., which come standard with *TORNADO-E2/6xxx* board. User must provide his own cables assembly for connection to custom equipment as it is required by application.

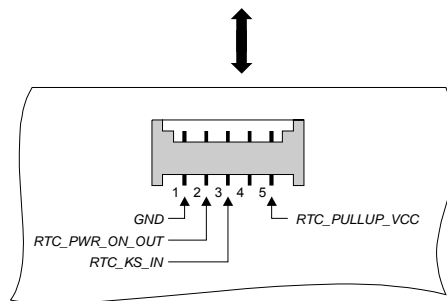


Figure A-8. Pinout of JP16 external power supply control connector for *TORNADO-E2/6713* board.

A.3 On-board Sockets

List of on-board sockets for *TORNADO-E2/6xxx* DSP controllers is presented in [Table A-3](#).

Table A-3. On-board sockets for *TORNADO-E2/6713*.

socket ID	socket function	reference information
BT1	RTC controller backup battery socket for 3V lithium 1216/1220/1225 battery.	Figure A-1 and subsection “ RTC backup battery ”

A.4 On-board LED Indicators

[Table A-4](#) contains the list of *TORNADO-E2/6xxx* DSP controllers on-board LED indicators.

Appendix B. External Cable Sets for TORNADO-E2/6xxx DSP controllers

This appendix contains information about external cable sets, which come standard with the TORNADO-E2/6xxx DSP controllers shipment package, and about the available options, which are available upon request. These options include T/X-JTAG/C1 JTAG converter cable.

B.1 T/X-JTAG/C1 JTAG Converter Cable

TORNADO-E2/6xxx on-board JP3 connector is used to connect to external JTAG emulator via the T/X-JTAG/C1 JTAG converter cable (refer to section “[DSP Software Development Tools](#)” from chapter 2 of this user’s guide for more details).

T/X-JTAG/C1 JTAG converter cable ([Figure B-1](#)) plugs into the TORNADO-E2/6xxx DSP controllers on-board JP3 connector and provides industry-standard 14-pin 0.1”x0.1” guarded keyed male header at another end for direct connection to TI and MicroLAB Systems JTAG emulators. T/X-JTAG/C1 JTAG converter cable comes standard with the TORNADO-E2/6xxx DSP controllers shipment package and has the length approximately 0.2m (8”).



Figure B-1. T/X-JTAG/C1 JTAG converter cable.

B.2 T/X-UART/C1 RS232C Interface Converter Cable

TORNADO-E2/6xxx on-board JP8 and JP9 connectors provide access to RS232C interfaces of channels “A” and “B” of on-board dual-channel UART (refer to “[Appendix H. Dual-channel UART \(DUART\)](#)” and to [Figure A-5](#) for more details).

In order to connect TORNADO-E2/6xxx on-board DUART to external PC COM ports and/or to external serial peripherals it is recommended to use T/X-UART/C1 RS232C interface JTAG converter cables ([Figure B-2](#)), which come standard with TORNADO-E2/6xxx board and provide industry-standard DB-9/male RS232C interface connectors.



Figure B-2. T/X-UART/C1 RS232C interface converter cable.

[Figure B-3](#) shows connection diagram for T/X-UART/C1 RS232C interface JTAG converter cable.

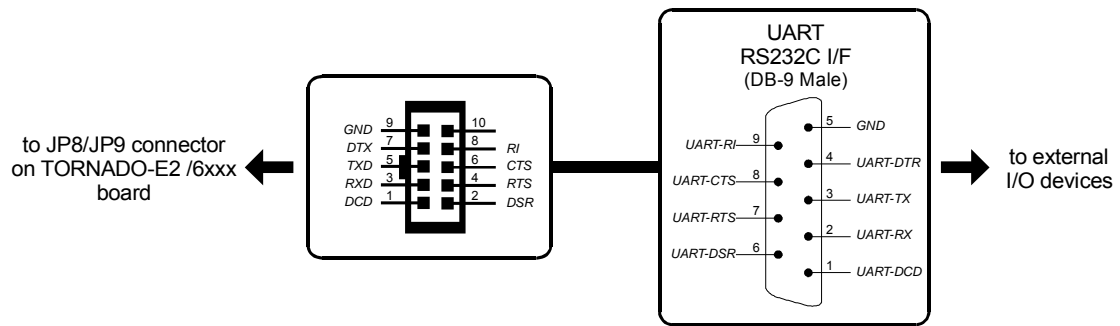


Figure B-3. Connection diagram for T/X-UART/C1 RS232C interface converter cable.

Appendix C. Serial I/O Expansion DCM Sites (SIOX and ASIOX)

This appendix contains description for *TORNADO-E2/6xxx* DSP controllers on-board *SIOX* (serial I/O expansion) and *ASIOX* (audio-*SIOX*) DCM sites (refer to [Figure 1-3](#), [Figure 2-2](#) and [Figure A-1](#)).

C.1 General Description

TORNADO-E2/6xxx system architecture allows expanding on-board I/O resources via *SIOX* DCM sites, which are designed for installation of compatible DCM.

TORNADO-E2/6xxx DSP controllers provide one on-board legacy *SIOX* rev.B DCM site, which is compatible with *SIOX* DCM sites for all previous releases of *TORNADO* PC plug-in DSP systems and *TORNADO-E* stand-alone DSP controllers, and one on-board *ASIOX* DCM site, which is a new one for *TORNADO* stand-alone DSP controllers.

TORNADO-E2/6xxx DSP controllers provide two types of on-board *SIOX* DCM sites:

- Legacy *SIOX* rev.B DCM site, which is compatible with *SIOX* DCM sites for all previous releases of *TORNADO* PC plug-in DSP systems and *TORNADO-E* stand-alone DSP controllers. *SIOX* rev.B DCM site interface allows data transfer between *TORNADO-E2/6xxx* on-board DSP and *SIOX* rev.B DCM peripherals via DSP on-chip serial McBSP port only.
- *ASIOX* rev.D DCM site, which provides an upward compatible extension of legacy *SIOX* rev.B DCM site interface and is well suited for audio, instrumentation, communication and other applications. *ASIOX* rev.D DCM site interface allows data transfer between *TORNADO-E2/6xxx* on-board DSP and *SIOX* rev.B DCM peripherals via DSP on-chip serial McBSP and McASP ports and also includes asynchronous 16-bit parallel interface for general control.

Installation of *SIOX* rev.B and *ASIOX* rev.D DCMs onto *TORNADO-E2/6xxx* board

SIOX rev.B and *ASIOX* rev.D DCMs plug into JP5 and JP6 *TORNADO-E2/6xxx* on-board DCM site connectors correspondingly. For security reasons, *TORNADO-E2/6xxx* controllers provide on-board shared area for *SIOX* rev.B and *ASIOX* rev.D DCMs and allow installation of only one DCM per instant.

NOTE

TORNADO-E2/6xxx board allows installation of either *SIOX* rev.B DCM or *ASIOX* rev.D DCM and does not allow simultaneous installation of both DCMs.

Figures below show installation different *SIOX* DCMs onto *TORNADO-E2/6713* board.



Figure C-1. *TORNADO-E2/6713* board with *SIOX* rev.B DCM installed.



Figure C-2. TORNADO-E2/6713 board with ASIOX rev.D DCM installed.

C.2 Technical Description

Figure C-3 shows connection diagram for TORNADO-E2/6xxx on-board SIOX rev.B DCM site and ASIOX rev.D DCM site interfaces.

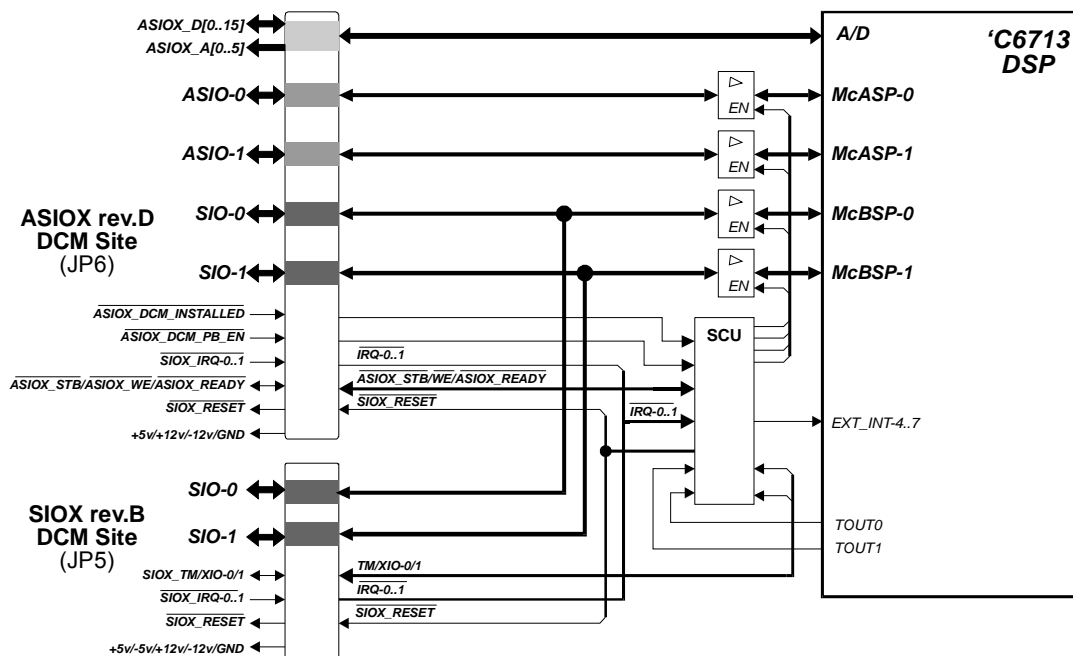


Figure C-3. Connection diagram for SIOX and ASIOX DCM site interfaces of TORNADO-E2/6713.

SIOX rev.B DCM site connector

TORNADO-E2/6xxx DSP controllers on-board SIOX rev.B DCM site header (JP5) is a dual-row 26-pin female header with 0.1"x0.1" pin pattern. Compatible plugs at installed SIOX rev.B DCM is either 26-pin 0.1"x0.1" male header (in case both SIO-0 and SIO-1 serial ports are used on SIOX plugged-in DCM) or 20-pin 0.1"x0.1" male header (in case only SIO-0 serial port is used on SIOX plugged-in DCM).

SIOX rev.B DCM site connector pinout is shown at Figure C-4 and signal description is provided in Table C-1.

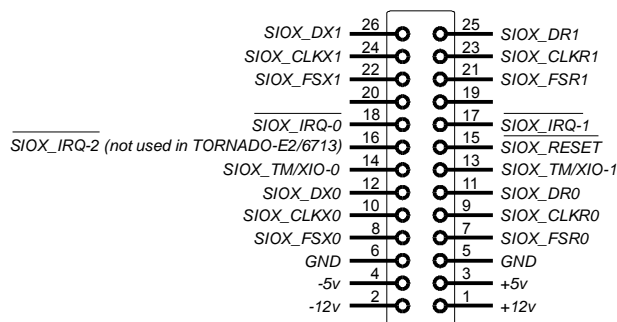


Figure C-4. Pinout for SIOX rev.B DCM site connector.

Table C-1. Signal description for SIOX rev.B DCM site interface.

SIOX signal name	signal type	Description
SIO-0 port control		
SIOX_DX0 SIOX_FSR0 SIOX_CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX rev.B DCM site. These signals correspond to TMS320C6xxx DSP on-chip McBSP-0 serial port transmitter. For TORNADO-E2/6713 controller these signals are routed through buffers, which are controlled via DSP_MCBSP0_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 . These signals have no pull-up/down resistors.
SIOX_DR0 SIOX_FSR0 SIOX_CLKR0	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX rev.B DCM site. These signals correspond to TMS320C6xxx DSP on-chip McBSP-0 serial port receiver. For TORNADO-E2/6713 controller these signals are routed through buffers, which are controlled via DSP_MCBSP0_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 . These signals have no pull-up/down resistors.
SIO-1 port control		
SIOX_DX1 SIOX_FSR1 SIOX_CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX rev.B DCM site. These signals correspond to TMS320C6xxx DSP on-chip McBSP-1 serial port transmitter. For TORNADO-E2/6713 controller these signals are routed through buffers, which are controlled via DSP_MCBSP1_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 . These signals have no pull-up/down resistors.
SIOX_DR1 SIOX_FSR1 SIOX_CLKR1	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX rev.B DCM site. These signals correspond to TMS320C6xxx DSP on-chip McBSP-1 serial port receiver. For TORNADO-E2/6713 controller these signals are routed through buffers, which are controlled via DSP_MCBSP1_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 . These signals have no pull-up/down resistors.
Timers, Reset and Interrupt Requests		
SIOX_TM/XIO-0 SIOX_TM/XIO-1	I/O/Z	DSP timer or I/O pins, which can be configured to connect to the corresponding TMS320C6xxx DSP on-chip timer outputs (TOUT0 and TOUT1), or used as general purpose I/O pins (XIO-0 and XIO-1). For TORNADO-E2/6713 controller these pins are configured via DSP_SIOX_XIO_CNFRG and DSP_SIOX_XIO_DATARG DSP external control registers. Refer to subsection " DSP on-chip timers " for more details. These signals have weak pull-up resistors.
$\overline{\text{SIOX_RESET}}$	O	Active low reset signal for SIOX rev.B DCM site, which is controlled via $\overline{\text{SIOX_RESET}}$ bit of DSP_DCM_RESET_RG DSP external control register (refer to Table 2-21 for more details)

$\overline{SIOX_IRQ-0}$, $\overline{SIOX_IRQ-1}$	I	<p>External interrupt requests from <i>SIOX</i> rev.B and <i>ASIOX</i> rev.D DCM sites. These inputs have pull-up resistors and are either falling edge sensitive or active low upon the type of <i>TORNADO-E2/xxxx</i> controller.</p> <p>$\overline{SIOX_IRQ-0}$ and $\overline{SIOX_IRQ-1}$ interrupt requests can be configured by DSP application to connect to any of DSP <i>EXT_INT4..7</i> external interrupt requests via DSP_EXT_INT4_SEL_RG..DSP_EXT_INT7_SEL_RG DSP external control registers (refer to Figure 2-3 and Table 2-14 for more details).</p>
Power Supplies		
GND		Ground.
+5v		+5v power (from on-board JP1 external power connector).
+12v		+12v power (from on-board JP1 external power connector).
-5v		-5v power (derived from -12v power).
-12v		-12v power (from on-board JP1 external power connector).

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
2. All logical signal levels and load currents correspond to that for 3v/5v CMOS/TTL logic.

ASIOX rev.D DCM site connector

TORNADO-E2/6xxx DSP controllers on-board *ASIOX* rev.D DCM site connector (JP6) is a high-density dual-row 120-pin female header with 0.50 mm pin pitch from Samtec Inc. Compatible *ASIOX* rev.D plugs (Samtec p/n BTH-060-02-L-D-A) for design of custom *ASIOX* rev.D DCM are available from MicroLAB Systems upon request.

ASIOX rev.D DCM site connector pinout is shown at [Figure C-5](#) and signal specifications are presented in [Table C-2](#).

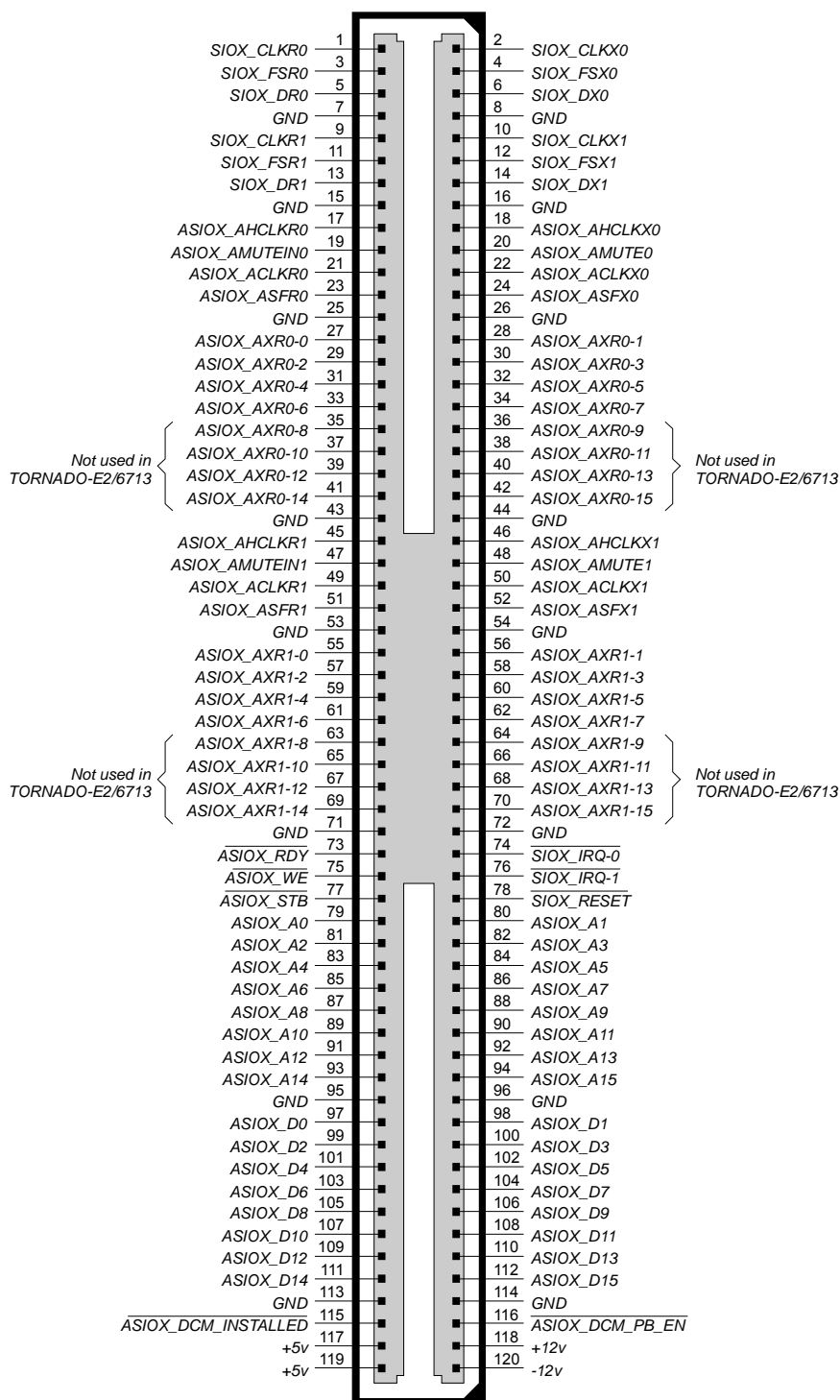


Figure C-5. ASIOX rev.D DCM site connector pinout (top view).

Table C-2. Signal description for ASIOX rev.D DCM site connector.

ASIOX rev.D connector pin	pin number	signal type	description
SIO-0 port control (common for SIOX rev.B and ASIOX rev.D DCM sites)			
SIOX_DX0 SIOX_F SX0 SIOX_CLKX0	6 4 2	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port. These signals correspond to TMS320C6xxx DSP on-chip McBSP-0 serial port transmitter. For TORNADO-E2/6713 controller these signals are routed through buffers, which are controlled via DSP_MCBSP0_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 . These signals have no pull-up/down resistors.
SIOX_DR0 SIOX_FSR0 SIOX_CLKR0	5 3 1	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port. These signals correspond to TMS320C6xxx DSP on-chip McBSP-0 serial port receiver. For TORNADO-E2/6713 controller these signals are routed through buffers, which are controlled via DSP_MCBSP0_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 . These signals have no pull-up/down resistors.
SIO-1 port control (common for SIOX rev.B and ASIOX rev.D DCM sites)			
SIOX_DX1 SIOX_F SX1 SIOX_CLKX1	14 12 10	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port. These signals correspond to TMS320C6xxx DSP on-chip McBSP-1 serial port transmitter. For TORNADO-E2/6713 controller these signals are routed through buffers, which are controlled via DSP_MCBSP1_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 . These signals have no pull-up/down resistors.
SIOX_DR1 SIOX_FSR1 SIOX_CLKR1	13 11 9	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port. These signals correspond to TMS320C6xxx DSP on-chip McBSP-1 serial port receiver. For TORNADO-E2/6713 controller these signals are routed through buffers, which are controlled via DSP_MCBSP1_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 . These signals have no pull-up/down resistors.
Reset and Interrupt Requests (common for SIOX rev.B and ASIOX rev.D DCM sites)			
$\overline{\text{SIOX_RESET}}$	78	O	Active low reset signal for ASIOX rev.D DCM site, which is controlled via $\overline{\text{SIOX_RESET}}$ bit of DSP_DCM_RESET_RG DSP external control register (refer to Table 2-21 for more details)
$\overline{\text{SIOX_IRQ}} - 0$, $\overline{\text{SIOX_IRQ}} - 1$	74 76	I	External interrupt requests from SIOX rev.B and ASIOX rev.D DCM sites. These inputs have pull-up resistors and are either falling edge sensitive or active low upon the type of TORNADO-E2/xxxx controller. $\overline{\text{SIOX_IRQ}} - 0$ and $\overline{\text{SIOX_IRQ}} - 1$ interrupt requests can be configured by DSP application to connect to any of DSP EXT_INT4..7 external interrupt requests via DSP_EXT_INT4_SEL_RG .. DSP_EXT_INT7_SEL_RG DSP external control registers (refer to Figure 2-3 and Table 2-14 for more details).

ASIO-0 port control (ASIOX rev.D DCM site only)			
ASIOX_AFSX0 ASIOX_ACLKX0 ASIOX_AHCLKX0	24 22 18	I/O/Z I/O/Z I/O/Z	Frame synchronization, bit clock and high-frequency master clock signals for transmitter of audio ASIO-0 port. These signals correspond to TMS320C6xxx DSP on-chip McASP-0 audio serial port transmitter. For <i>TORNADO-E2/6713</i> controller these signals are routed through buffers, which are controlled via {DSP_MCASP0_BUF_EN4..1} bits of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 .
ASIOX_AFSR0 ASIOX_ACLKR0 ASIOX_AHCLKR0	23 21 17	I/O/Z I/O/Z I/O/Z	Frame synchronization, bit clock and high-frequency master clock signals for receiver of ASIO-0 port. These signals correspond to TMS320C6xxx DSP on-chip McASP-0 audio serial port receiver. For <i>TORNADO-E2/6713</i> controller these signals are routed through buffers, which are controlled via {DSP_MCASP0_BUF_EN4..1} bits of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 .
ASIOX_AXR0-[0..15] ASIOX_AXR0-[0..7] (TORNADO-E2/6713 only)	27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42	I/O/Z	Data signals for ASIO-0 port. These signals correspond to TMS320C6xxx DSP on-chip McASP-0 audio serial port serializers. For <i>TORNADO-E2/6713</i> controller, only ASIOX_AXR0-[0..7] signals are valid, and these signals are routed through buffers, which are controlled via {DSP_MCASP0_BUF_EN4..1} bits of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 .
ASIOX_AMUTE0 ASIOX_AMUTEIN0	20 19	O/Z I/O/Z	Mute output and mute input signals for ASIO-0 port. These signals correspond to TMS320C6xxx DSP on-chip McASP-0 audio serial port. For <i>TORNADO-E2/6713</i> controller these signals are routed through buffers, which are controlled via {DSP_MCASP0_BUF_EN4..1} bits of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 .
ASIO-1 port control (ASIOX rev.D DCM site only)			
ASIOX_AFSX1 ASIOX_ACLKX1 ASIOX_AHCLKX1	52 50 46	I/O/Z I/O/Z I/O/Z	Frame synchronization, bit clock and high-frequency master clock signals for transmitter of ASIO-1 port. These signals correspond to TMS320C6xxx DSP on-chip McASP-1 audio serial port transmitter. For <i>TORNADO-E2/6713</i> controller these signals are routed through buffers, which are controlled via DSP_MCASP1_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 .
ASIOX_AFSR1 ASIOX_ACLKR1 ASIOX_AHCLKR1	51 49 45	I/O/Z I/O/Z I/O/Z	Frame synchronization, bit clock and high-frequency master clock signals for receiver of ASIO-1 port. These signals correspond to TMS320C6xxx DSP on-chip McASP-1 audio serial port receiver. For <i>TORNADO-E2/6713</i> controller these signals are routed through buffers, which are controlled via DSP_MCASP1_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 .
ASIOX_AXR1-[0..15] ASIOX_AXR1-[0..7] (TORNADO-E2/6713 only)	55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70	I/O/Z	Data signals for serializers of ASIO-1 port. These signals correspond to TMS320C6xxx DSP on-chip McASP-1 audio serial port serializers. For <i>TORNADO-E2/6713</i> controller only ASIOX_AXR0-[0..7] signals are valid, and these signals are routed through buffers, which are controlled DSP_MCASP1_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register.
ASIOX_AMUTE1 ASIOX_AMUTEIN1	48 47	O/Z I/O/Z	Mute output and mute input signals for ASIO-1 port. These signals correspond to TMS320C6xxx DSP on-chip McASP-1 audio serial port. For <i>TORNADO-E2/6713</i> controller these signals are routed through buffers, which are controlled via DSP_MCASP1_BUF_EN bit of DSP_PORTS_CNTR_RG DSP external control register in accordance with Table 2-7 .

Asynchronous parallel data interface (ASIOX rev.D DCM site only)			
<i>ASIOX_A[0..15]</i>	79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94	O/Z	Parallel address bus.
<i>ASIOX_D[0..15]</i>	97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112	I/O/Z	Parallel data bus.
<i>$\overline{ASIOX_STB}$</i>	77	O	Active low data transfer strobe.
<i>$\overline{ASIOX_WE}$</i>	75	O	Active low write enable signal.
<i>$\overline{ASIOX_READY}$</i>	73	I	Active low data ready signal. This signal has pull-up resistor.
DCM management signals (ASIOX rev.D DCM site only)			
<i>$\overline{ASIOX_DCM_INSTALLED}$</i>	115	I	Active low DCM installation indicator. This signal must be grounded on ASIOX rev.D DCM in order to indicate that DCM is installed. This signal has pull-up resistor.
<i>$\overline{ASIOX_DCM_PB_EN}$</i>	116	I	Active low enable signal for asynchronous parallel data interface. This signal must be grounded on ASIOX rev.D DCM in order to enable asynchronous parallel data interface. This signal has pull-up resistor.
Power Supplies			
<i>GND</i>	7, 8, 15, 16, 25, 26, 43, 44, 53, 54, 71, 72, 95, 96, 113, 114		Ground.
<i>+5v</i>	117, 119		+5v power.
<i>+12v</i>	118		+12v power.
<i>-12v</i>	120		-12v power.

- Note:
1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
 2. All logical signal levels and load currents correspond to that for 3v/5v CMOS/TTL logic.

NOTE

ASIOX_DCM_INSTALLED pin must be grounded on *ASIOX* rev.D DCM in order to indicate that *ASIOX* rev.D DCM is installed. Otherwise, *ASIOX* rev.D DCM interface will be not activated.

Maximum serial data transfer speed for SIO-0/1 serial ports of SIOX DCM sites

Maximum throughput of SIO-0/1 serial ports of *SIOX* DCM sites is 150 Mbit/s for *TORNADO-E2/6713* DSP controllers. Refer to original TI documentation for more details about programming TMS320C6xxx DSP on-chip McBSP serial ports.

DSP Timer/I/O pins

SIOX_TM/XIO-0 and *SIOX_TM/XIO-1* DSP timer/I/O pins of *TORNADO-E2/6xxx* on-board *SIOX* rev.B DCM site interface can be used as either DSP timers outputs, or general purpose I/O pins.

These pins are controlled via [DSP_SIOX_XIO_CNFG_RG](#) and [DSP_SIOX_XIO_DATA_RG](#) DSP external control registers (refer to [Table 2-22](#) and [Table 2-23](#) for more details).

When configured as DSP timer outputs, these signals connect to TMS320C6xxx DSP on-chip timers output pins TOUT0 and TOUT1 correspondingly. For *TORNADO-E2/6713*, the DSP timers output pins shall be enabled through *DEVCFG* TMS320C6713 DSP on-chip device configuration register (@0x019C0200) (refer to [Table 2-7](#)).

IMPORTANT NOTE

It is recommended, that the *DEVCFG* TMS320C6713 DSP on-chip device configuration register (@0x019C0200) bits are not directly configured from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user's guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

Maximum clock frequency for DSP timer outputs is 75 MHz for *TORNADO-E2/6713* DSP controllers. Refer to original TI documentation for more details about programming TMS320C6xxx DSP on-chip timers.

Generating Reset Signal for SIOX DCM Sites

TORNADO-E2/6xxx DSP controllers provide one common reset signal for both on-board *SIOX* rev.B and *ASIOX* rev.D DCM sites, which is controlled via *SIOX_RESET* bit of [DSP_DCM_RESET_RG](#) DSP external control register (refer to [Table 2-21](#) for more details).

Reset signal for on-board *SIOX* rev.B and *ASIOX* rev.D DCM sites allows correct initialization of installed DCM hardware and correct synchronization with DSP application.

ASIO-0/1 audio serial ports of TORNADO-E2/6713 ASIOX rev.D DCM site interface

TORNADO-E2/6713 on-board *ASIOX* rev.D DCM site interface provides ASIO-0 and ASIO-1 audio serial ports, which are connected to the DSP on-chip McASP-0 and McASP-1 audio serial ports.

Each ASIO audio serial port includes transmit and receive sections with dedicated frame synchronization, bit clock and high-frequency master clock, eight serial data bits and *ASIOX_AMUTE* and *ASIOX_AMUTEIN* pins for error-checking handling and management.

Each ASIO audio serial port DSP peripheral pins must be enabled via the corresponding bits of *DEVCFG* TMS320C6713 DSP on-chip device configuration register (@0x019C0200) (refer to [Table 2-7](#)) and [DSP_PORTS_CNTR_RG](#) DSP external control register.

ASIOX_AMUTEIN-0/1 pins also can be used for generation of DSP interrupt requests (*ASIOX_AMUTEIN-0/1*) via any of EXT_INT4..7 DSP external interrupt request selectors ([Figure 2-3](#)) as it is configured via [DSP_EXT_INT4_SEL_RG](#), [DSP_EXT_INT5_SEL_RG](#), [DSP_EXT_INT6_SEL_RG](#) and [DSP_EXT_INT7_SEL_RG](#) DSP external control registers.

NOTE

For more information about configuration of TMS320C6xxx DSP on-chip McASP serial ports control registers refer to original TI TMS320C6xxx user's guide, which is provided in electronic form along with this user's guide

IMPORTANT NOTE

It is recommended, that the *DEVCFG* TMS320C6713 DSP on-chip device configuration register (@0x019C0200) and [DSP_PORTS_CNTR_RG](#) DSP external control register bits are not directly configured from user DSP application.

Instead, the corresponding API function calls to the *TORNADO-E2/6xxx* DSP control software utilities (refer to [Appendix F](#) of this user's guide for more details) shall be used to perform this action in order to guarantee correct functionality of the on-board hardware.

Asynchronous parallel interface of ASIOX rev.D site

16-bit asynchronous parallel interface of *ASIOX* rev.D DCM site interface is mapped to the DSP external memory area (refer to [Table 2-2](#) for addressing details).

NOTE

ASIOX_DCM_PB_EN pin must be grounded on *ASIOX* rev.D DCM in order to enable asynchronous parallel interface at *ASIOX* rev.D DCM site.

NOTE

For *TORNADO-E2/6713* DSP controller, 16-bit data words of asynchronous parallel interface of *ASIOX* rev.D DCM site are allocated to least significant half-words (bits D0..D15) of 32-bit DSP EMIF data words and can be accessed using 16-bit and/or 32-bit data formats. When accessed in 32-bit data format, most significant half-words (bits 16..31) are ignored during writes and return undefined data during reads.

Data Transfer Timing for asynchronous parallel interface of ASIOX rev.D DCM Site

Timing diagram for parallel data transfer via *ASIOX* rev.D DCM site is shown at [Figure C-6](#).

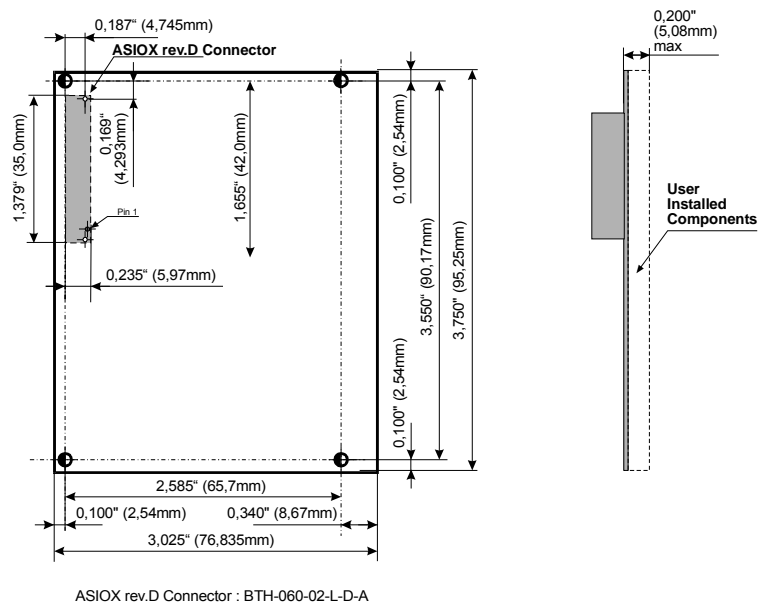


Figure C-8. Physical dimensions of AS/IOX rev.D DCM.

Appendix D. *PIOX2 DCM Site Interface*

This appendix contains information about *PIOX2* DCM site interface for *TORNADO-E2/xxxx* DSP controllers.

D.1 General Description

TORNADO-E2/xxxx DSP controllers allow expansion of on-board DSP I/O resources via 2nd generation parallel I/O expansion rev.2 DCM site (*PIOX2*). *PIOX2* is an upward compatible extension for 1st generation *PIOX* rev.1 DCM site interface providing significantly higher data transfer bandwidth.

PIOX2 DCM site interface comprises asynchronous and synchronous sections and allows installation of either asynchronous *PIOX2* DCM only or *PIOX2* DCM with both asynchronous and synchronous interfaces. ([Figure D-1](#)).

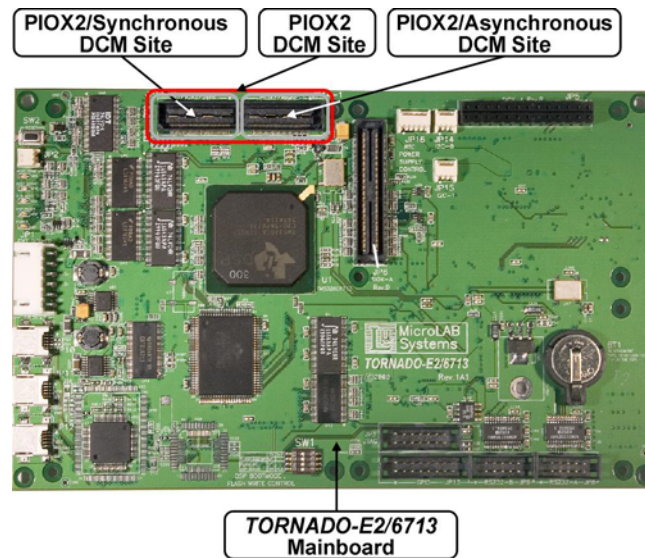


Figure D-1. *PIOX2* DCM site at *TORNADO-E2/6713* DSP controller board.

32-bit asynchronous section of *PIOX2* DCM site interface is compatible with *PIOX-32* rev.1 DCM site interface and shall be used for applications, which require medium data transfer speed up to 20 Mwords/s between DCM on-board peripherals and DSP.

32-bit synchronous section of *PIOX2* DCM site interface provides synchronous data transfer at the speed of DSP EMIF up to 133 Mwords/s and is intended for high-speed AD/DA applications.

Installation of *PIOX-16* and *PIOX-32* rev.1 DCMs into *PIOX2* rev.2 DCM site

PIOX2 DCM site interface allows installation of *PIOX-16* and 32-bit *PIOX-32* rev.1 DCMs using ‘off-the-shelf’ *PIOX2*-to-*PIOX* converter boards.

NOTE

T/X-PXA/PX2A1 converter board must be used for installation of *PIOX-16* rev.1 DCMs only.

T/X-PXA/PX2A2 converter board must be used for installation of *PIOX-32* and *PIOX-16* rev.1 DCMs.

Converter board extends the total height of *TORNADO-E2/6xxx* with *PIOX* rev.1 DCM installed by approximately 8mm.

[Figure D-2](#) below show installations of *PIOX* rev.1 DCM into *PIOX2* rev.2 DCM site of *TORNADO-E2/6713*.

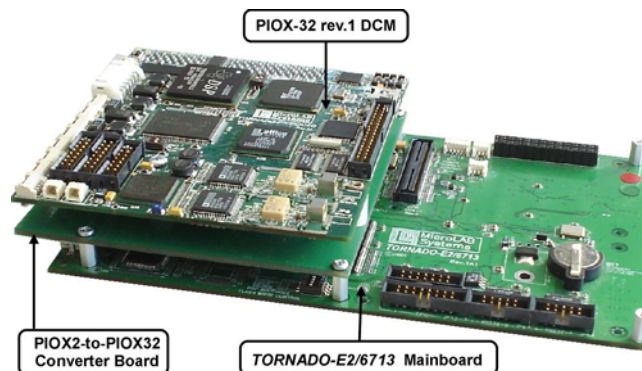


Figure D-2. *TORNADO-E2/6713* board with *PIOX-32* rev.1 DCM installed.

D.2 *PIOX2* DCM Site Interface Connector and Signals

PIOX2 DCM site interfaces comprises asynchronous and synchronous sections.

Asynchronous section of *PIOX2* DCM site interface

Asynchronous section of *PIOX2* DCM site interface is a simple asynchronous parallel interface with separate 32-bit data and 16-bit address buses, which is compatible with 16-bit *PIOX-16* and 32-bit *PIOX-32* rev.1 DCM site interfaces.

NOTE

Asynchronous section of *PIOX2* DCM site interface is mandatory and appears for all *TORNADO-E2/xxxx* boards.

Asynchronous section of *PIOX2* DCM site interface is allocated into DSP external memory area. Allocation depends upon the type of *TORNADO-E2/xxxx* board (refer to [Table 2-2](#) for more details).

Maximum data bandwidth of asynchronous section of *PIOX2* DCM site interface is about 20 Mwords/s and depends upon the type of *TORNADO-E2/xxxx* board and type of DCM installed.

Asynchronous section of *PIOX2* DCM site interface also includes two interrupt requests, DCM reset control, DCM installation ID and type ID signals, and power supplies.

Synchronous section of PIOX2 DCM site interface

32-bit synchronous section of *PIOX2* DCM site interface allows high-speed synchronous data transfer at the speed of DSP external memory interface. Particular value of data transfer speed depends upon the type of *TORNADO-E2/xxxx* board and can be up to 133 Mwords/s.

NOTE

Synchronous section of interface is optional and appears only for those *TORNADO-E2/xxxx* boards, which have the on-board DSP with synchronous memory interface (for example all *TORNADO-E2/6xxx* boards with TMS320C6xxx DSP).

Synchronous section of *PIOX2* DCM site interface does not appear for *TORNADO-E2/xxxx* boards with DSPs that have asynchronous-only external memory interface (for example *TORNADO-E2/33* boards with TMS320VC33 DSP).

Synchronous section of *PIOX2* DCM site interface includes 32-bit data bus, 16-bit address bus, data strobes, two interrupt requests, and is allocated into external synchronous DSP memory area. Allocation depends upon the type of *TORNADO-E2/xxxx* board (refer to [Table 2-2](#) for more details).

PIOX2 DCM site interface connectors and signals description

PIOX2 DCM site interface connector is a high-density high-speed dual-section connector with solid ground plane and 0.50 mm pin pitch.

Each section of *PIOX2* DCM site interface maps to individual section of connector. Standard board-to-board stacking height for *PIOX2* DCM site is 8mm. Asynchronous-only *PIOX2* DCMs provide single-section mating plug only and plugs into asynchronous section of *PIOX2* DCM site interface connector. Correspondingly, *PIOX2* DCM with full asynchronous-synchronous interface provides dual-section mating plug.

P/n for compatible *PIOX2* plugs are Samtec QTH-030-02-L-D-A for asynchronous-only *PIOX2* DCM site interface and QTH-060-02-L-D-A for full asynchronous-synchronous *PIOX2* DCM site interface. These plugs are available from MicroLAB Systems upon request for design of custom *PIOX2* DCMs.

Pinout for *PIOX2* DCM site interface connector is shown at [Figure D-3](#) and signal description is provided in [Table D-1](#).

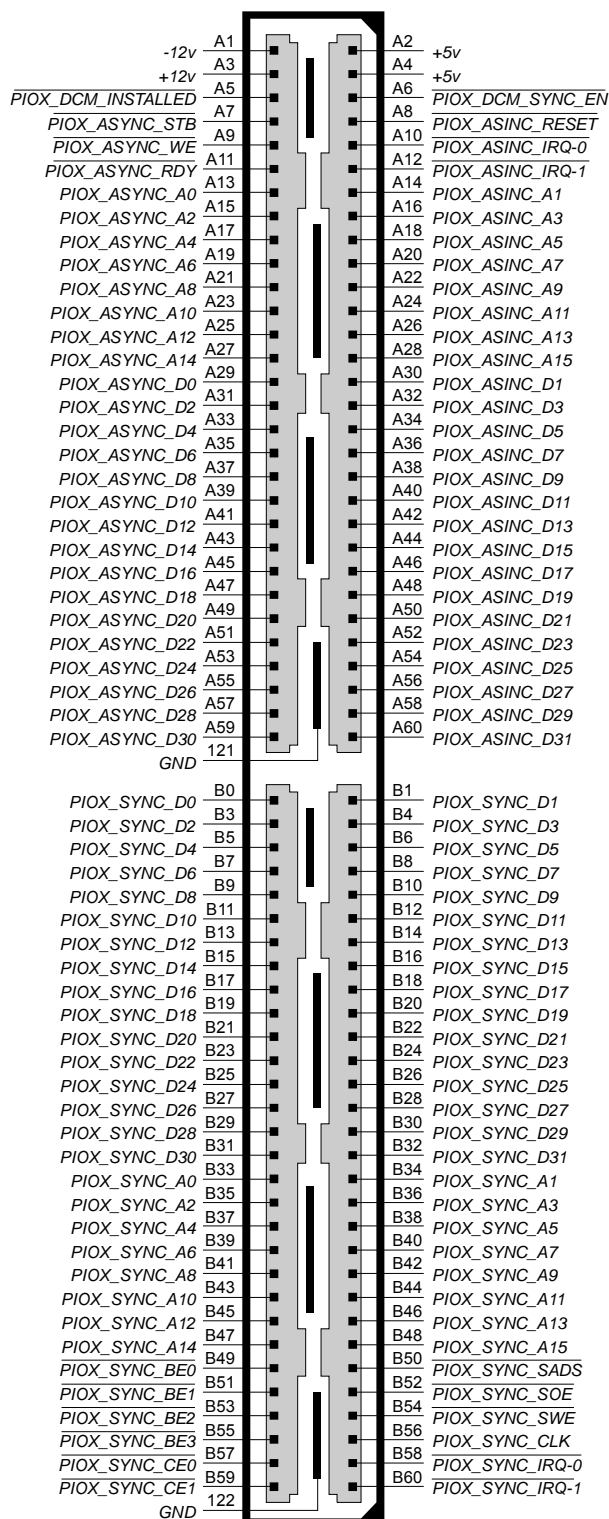


Figure D-3. Pinout of PIOX2 DCM site interface connector.

Table D-1. Signal description for *PIOX2 DCM* site interface.

Signal name	Pin number	signal type	Description
Asynchronous section of <i>PIOX2 DCM</i> site interface			
<i>PIOX_ASYNC_A</i> [0..15]	A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28	O/Z	16-bit asynchronous address bus
<i>PIOX_ASYNC_D</i> [0..31]	A29, A30, A31, A32, A33, A34, A35, A36, A37, A38, A39, A40, A41, A42, A43, A44, A45, A46, A47, A48, A49, A50, A51, A52, A53, A54, A55, A56, A57, A58, A59, A60	I/O/Z	32-bit asynchronous data bus.
<i>PIOX_ASYNC_STB</i>	A7	O	Active low asynchronous data transfer strobe.
<i>PIOX_ASYNC_WE</i>	A9	O	Active low asynchronous write enable signal.
<i>PIOX_ASYNC_READY</i>	A11	I	Active low asynchronous data ready acknowledge signal, which is generated by <i>PIOX2 DCM</i> to complete data transfer cycle in accordance with timing requirements for this DCM. This input has pull-up resistor.
<i>PIOX_ASYNC_RESET</i>	A8	O	Active low reset signal to <i>PIOX2 DCM</i> . This signal is controlled via <i>PX_RESET</i> bit of DSP DCM RESET RG DSP external control register (refer to Table 2-21 for more details)
<i>PIOX_ASYNC_IRQ - 0</i> , <i>PIOX_ASYNC_IRQ - 1</i>	A10, A12	I	Interrupt requests from asynchronous section of <i>PIOX2 DCM</i> . These interrupt request sources can be configured to route to any of DSP external interrupt requests via DSP_EXT_INT4_SEL RG ... DSP_EXT_INT7_SEL RG DSP external control registers (refer to Figure 2-3 and Table 2-14 for more details). These inputs have pull-up resistors and are either falling edge sensitive or active low upon the type of <i>TORNADO-E2/xxx</i> controller.
<i>PIOX_DCM_INSTALLED</i>	A5	I	Active low pulled-up <i>PIOX2 DCM</i> site interface installation ID. This signal must be grounded on <i>PIOX2 DCM</i> .
<i>PIOX_DCM_SYNC_EN</i>	A6	I	Active low pulled-up type ID for <i>PIOX2 DCM</i> site interface. This signal must be grounded on <i>PIOX2 DCM</i> with full asynchronous-synchronous interface and must be left unconnected for asynchronous-only <i>PIOX2 DCM</i> s.

GND	<GND>		Ground.
+5v	A2, A4		+5v power.
+12v	A3		+12v power.
-12v	A1		-12v power.
Synchronous section of PIOX2 DCM site interface			
<i>PIOX_SYNC_A[0..15]</i>	B33, B34, B35, B36, B37, B38, B39, B40, B41, B42, B43, B44, B45, B46, B47, B48	O/Z	16-bit synchronous address bus
<i>PIOX_SYNC_D[0..31]</i>	B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, B32	I/O/Z	32-bit synchronous data bus.
<i>PIOX_SYNC_BE[0..3]</i>	B49, B51, B53, B55	O/Z	Active low synchronous byte enable strobes.
<i>PIOX_SYNC_CE[0..1]</i>	B57, B59	O	Active low synchronous chip select strobes. Each strobe addresses individual 64Kx32 synchronous memory area of external DSP memory map. Refer to Table 2-2 for more details.
<i>PIOX_SYNC_SADS</i>	B50	O/Z	Active low synchronous address enable strobe.
<i>PIOX_SYNC_SOE</i>	B52	O/Z	Active low synchronous output enable signal.
<i>PIOX_SYNC_SWE</i>	B54	O/Z	Active low synchronous write enable signal.
<i>PIOX_SYNC_CLK</i>	B56	O/Z	Synchronous clock.
<i>PIOX_SYNC_IRQ-0</i> , <i>PIOX_SYNC_IRQ-1</i>	B58, B60	I	Interrupt requests from synchronous section of <i>PIOX2</i> DCM. These interrupt request sources can be configured to route to any of DSP external interrupt requests via DSP_EXT_INT4_SEL_RG...DSP_EXT_INT7_SEL_RG DSP external control registers (refer to Figure 2-3 and Table 2-14 for more details). These inputs have pull-up resistors and are either falling edge sensitive or active low upon the type of <i>TORNADO-E2/xxxx</i> controller.
GND	<GND>		Ground.

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
2. All logic I/O signal levels and load currents correspond to that for 3v/5v TTL logic.

NOTE

PIOX_DCM_INSTALLED pin must be grounded on *PIOX2* DCM in order to indicate that *PIOX2* DCM is installed, otherwise *PIOX2* DCM site interface will be not activated.

Timing diagram for data transfers cycle via asynchronous section of *PIOX2* DCM site interface

Figure D-4 shows timing diagram for data transfer cycles via asynchronous section of *PIOX2* DCM site interface of *TORNADO-E2/6713* DSP controllers.

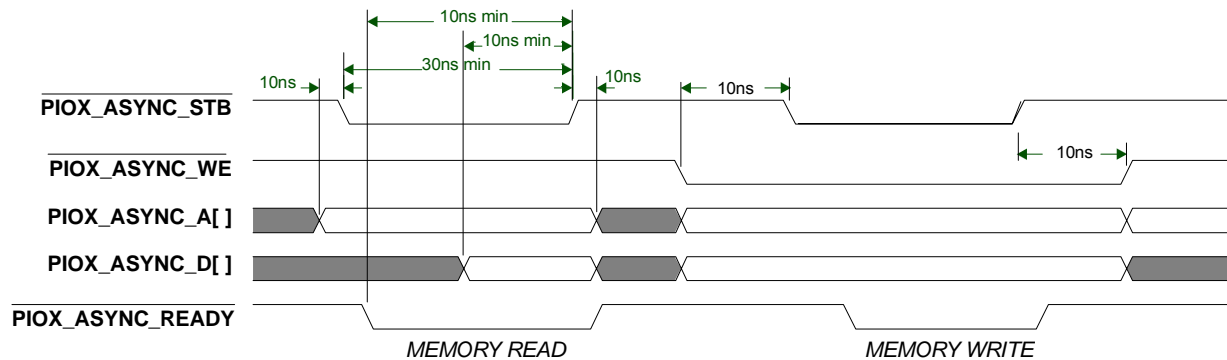


Figure D-4. Timing diagram of data transfer cycles via asynchronous section of *PIOX2* DCM site interface of *TORNADO-E2/6713*.

NOTE

Different *TORNADO-E2/xxx* boards provide different timing specification for asynchronous section of *PIOX2* DCM site interface.

Refer to documentation for your *TORNADO-E2/xxx* board for timing specification for asynchronous section *PIOX2* DCM site interface.

Timing diagram for data transfers cycle via synchronous *PIOX2* DCM site interface

Synchronous section of *PIOX2* DCM site interface uses standard synchronous burst data transfer interface, which can be found in SBSRAM and synchronous FIFO devices.

Synchronous section of *PIOX2* DCM site interface features the following configuration parameters:

- Data write latency is '0' cycles, which corresponds to single-cycle processing of data write command.
- Data read latency is either '2' or '3' cycles and depend upon the type of *TORNADO-E2/xxxx* board. Thus, for *TORNADO-E2/6713* board, data read latency is '2' cycles.

Synchronous clock for synchronous section of *PIOX2* DCM site interface is actually a synchronous clock of DSP external memory interface and its frequency varies upon the type of *TORNADO-E2/xxxx* board. Thus, for *TORNADO-E2/6713* board, frequency of synchronous clock for synchronous section of *PIOX2* DCM site interface is 100 MHz.

NOTE

Different *TORNADO-E2/xxx* boards provide different timing specification for synchronous section of *PIOX2* DCM site interface.

Refer to documentation for your *TORNADO-E2/xxx* board for timing specification for synchronous section *PIOX2* DCM site interface.

[Figure D-5](#) shows timing diagram for data transfer cycles via synchronous section of *PIOX2* DCM site interface of *TORNADO-E2/6713* DSP controllers.

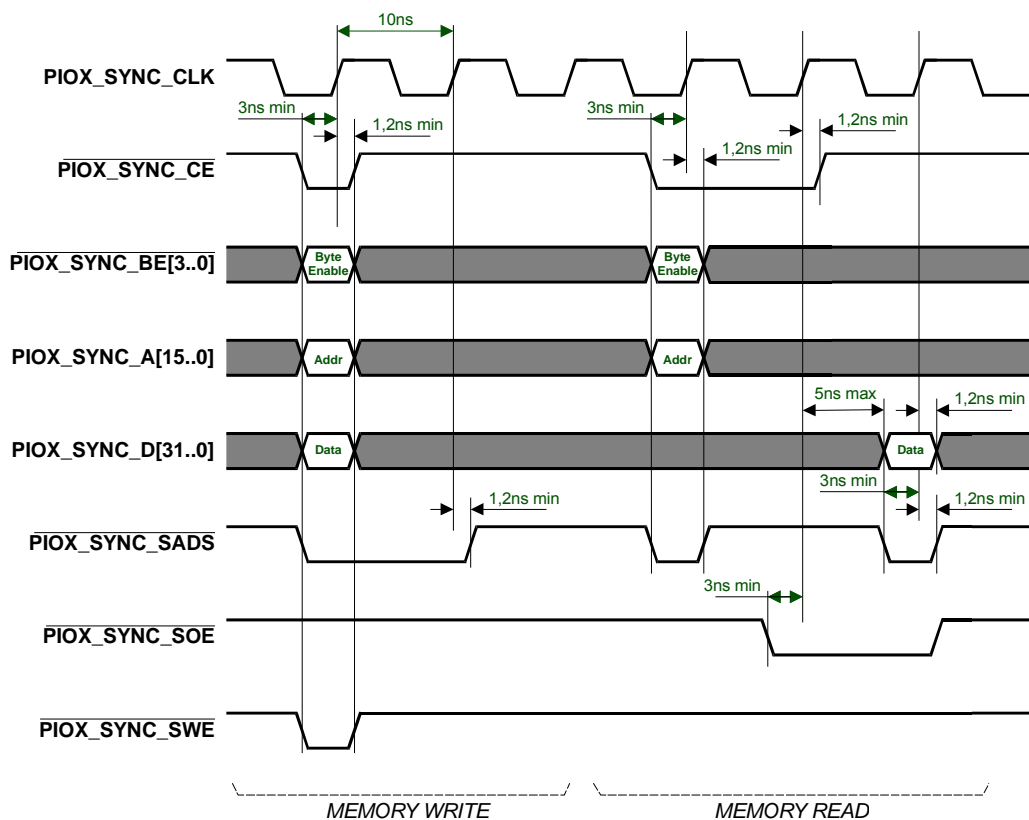


Figure D-5. Timing diagram of data transfer cycles via synchronous section of *PIOX2* DCM site interface of *TORNADO-E2/6713*.

NOTE

PIOX_DCM_SYNC_EN pin must be grounded on *PIOX2* DCM with synchronous *PIOX2* DCM site interface in order to enable synchronous section of *PIOX2* DCM site interface on *TORNADO-E2/xxxx* board.

D.3 Physical Dimensions for *PIOX2* DCM

Physical dimensions for *PIOX2* DCM are presented at [Figure D-6](#). This information is intended for those customers, who need to design custom *PIOX2* DCM.

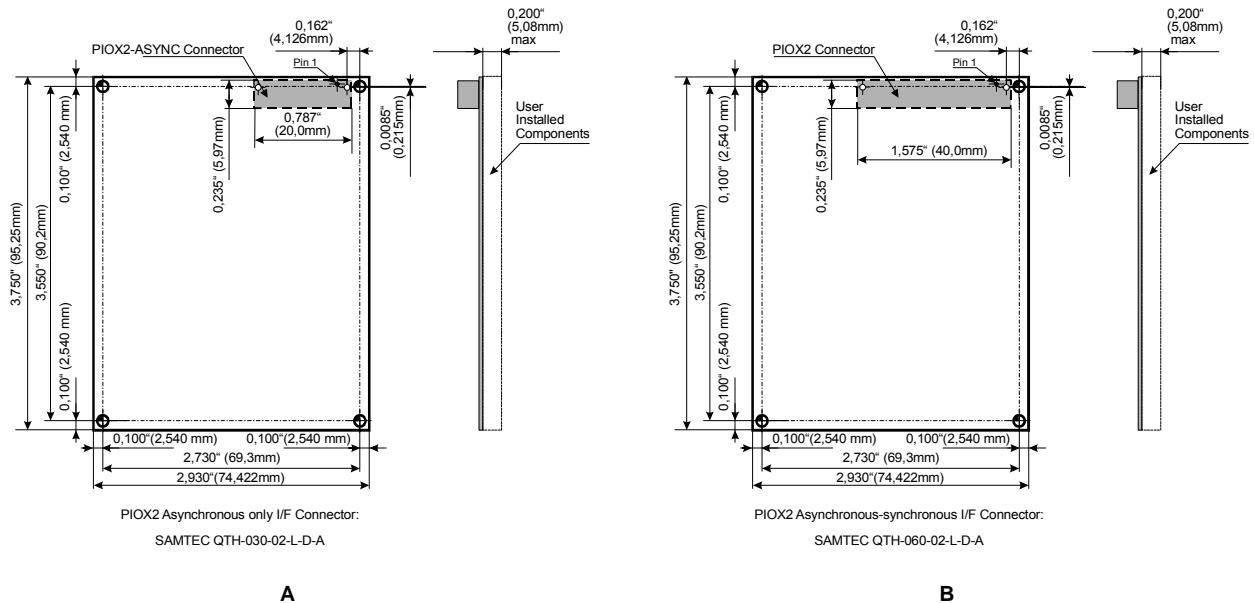


Figure D-6. Physical dimensions for *PIOX2* DCM with asynchronous-only interface (A) and *PIOX2* DCM with full asynchronous-synchronous interfaces (B).

Appendix E. *HCX DCM Site Interface*

This appendix contains information about host *HCX* rev.A DCM site interface for *TORNADO-E2/xxxx* DSP controllers.

NOTE

HCX DCM site of *TORNADO-E2/xxx* boards is intended for installation of host *HCX* controllers only, which are manufactured by MicroLAB Systems, and is not intended for installation of user designed customs DCMs.

Technical specification and detail information about *HCX* DCM site interface is proprierty of MicroLAB Systems and is not published in user's guides for *TORNADO-E2/xxxx* controllers.

This user's guide includes as much information about *HCX* DCM site interface as it is required for understanding of *HCX* DCM installation and functionality.

E.1 General Description

HCX DCM site of *TORNADO-E2/xxxx* controllers is used to install host *HCX* DCM controllers from MicroLAB Systems, which provides a set of industry-standard high-speed peripheral and network communication interfaces and high-speed memory storage, and allow to offload DSP from host communication task, which typically occupies a lot of valuable DSP performance.

HCX DCM site is located at the bottom side of *TORNADO-E2/xxxx* board ([Figure E-1](#)) and does not block installation of *PIOX2* and *SIOX/ASIOX* DCMs for expansion of DSP real-time I/O resources. *HCX* DCM site interface include two high-density connectors (i.e. JP7-1 and JP7-2 for *TORNADO-E2/xxxx* board).

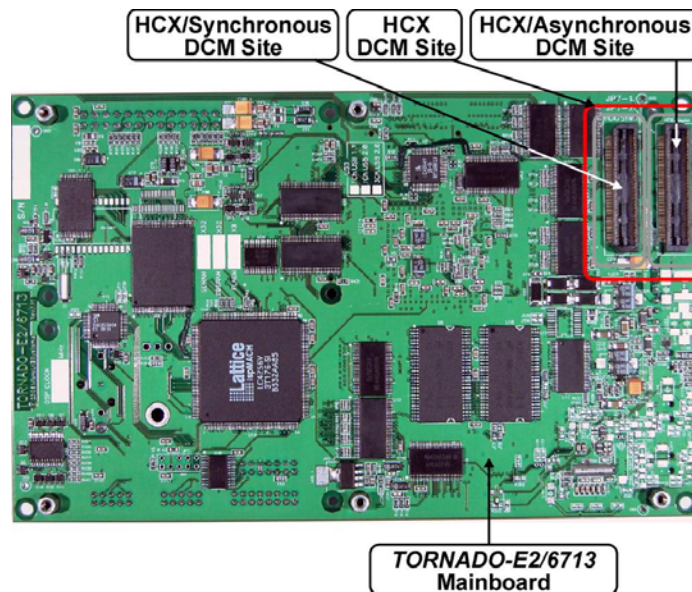


Figure E-1. *HCX* DCM site of *TORNADO-E2/6713* board.

HCX DCM site interface

Host *HCX* rev.A DCM site interface of *TORNADO-E2/6xxx* DSP controllers comprises two sections:

- Mandatory asynchronous section (*HCX-ASYNC*).

- Optional synchronous section (*HCX-SYNC*).

Asynchronous section of *HCX* rev.A DCM site interface (*HCX-ASYNC*) is mandatory and is used for general control of *TORNADO-E2/xxxx* on-board DSP from host *HCX* controller. Depending upon the type of *TORNADO-E2/xxxx* board, asynchronous section of *HCX* rev.A DCM site interface provides simple either 16-bit or 32-bit wide asynchronous data transfer interface, one to four DSP-to-host interrupt request outputs, installation ID and DCM type ID, and power supplies to *HCX* DCM. This section is always controlled by host *HCX* controller, is mapped into its external memory area, and includes a set of *HCX* control register and access to DSP on-chip HPI port in case the latter is available for particular DSP type (refer to section “[HCX DCM Site Interface](#)” in chapter 2 of this user’s guide for more details). For *TORNADO-E2/xxxx* boards, which use DSPs with asynchronous external memory interface (for example *TORNADO-E2/33* boards with TMS320VC33 DSP), asynchronous section may include dual-port memory for DSP-to-Host communication.

Typical data transfer performance between DSP and host *HCX* controller via DSP on-chip HPI port is about 100..300 Kword/s, so in most cases this path is used to upload DSP executable and for general DSP application control.

Synchronous section of *HCX* DCM site interface (*HCX-SYNC*) is optional and appears for those *TORNADO-E2/xxxx* boards only, which use DSPs with synchronous external memory interface (for example *TORNADO-E2/6xxx* boards with TMS320C6xxx DSP). *HCX-SYNC* interface has been designed for high-speed real-data transfer between DSP and host *HCX* controller applications using either shared memory or FIFO resources available at *HCX* DCM.

HCX-SYNC interface includes 32-bit wide synchronous burst memory interface and provides one to four Host-to-DSP interrupt requests (depending upon the type of *TORNADO-E2/xxxx* board), which are used for data transfer synchronization and for general purpose DSP interrupt request.

NOTE

HCX-SYNC interface of *TORNADO-E2/xxxx* DSP controllers is controlled exclusively by on-board DSP and is mapped into DSP external memory area.

Synchronous section of *HCX* DCM site interface provides highest possible data transfer performance for particular DSP type and runs at the speed of DSP EMIF and runs at the speed of DSP EMIF, i.e. at 100 Mwords/s for *TORNADO-E2/6713* controller.

HCX DCM installation

Once compatible host *HCX* DCM is installed onto *TORNADO-E2/xxxx* board, then this puts *TORNADO-E2/xxxx* on-board DSP into *DSP host operation mode* as it is listed in [Table 2-1](#). Correspondingly, in case *HCX* DCM is not installed, then this mode corresponds to the *DSP stand-alone operation mode* with host *HCX* DCM site interface disabled.

[Figure 1-2](#) shows installation of host *HCX* DCM onto *TORNADO-E2/6713* DSP controller.

Appendix F. Software Utilities for TORNADO-E2/6xxx DSP controllers

Software utilities for TORNADO-E2/6xxx DSP controllers are recommended for use to shorten DSP application development cycle and to provide compatibility between different applications.

Software utilities for TORNADO-E2/6xxx come in source code with detail comments for easy understanding and modification. The following software components are included with software utilities for TORNADO-E2/6xxx:

- Software utilities for TORNADO-E2/6xxx on-board TMS320C6xxx DSP, which come in *T2E6XXX_DSP.H* C/C++ header file and include definitions, macros and API functions for control of on-board DSP environment.
- A set of application demos, which can be used to guide through software design process for TORNADO-E2/6xxx DSP controllers and perform tests for on-board hardware.
- CCS GEL-files for automatic configuration of TORNADO-E2/6xxx on-board DSP environment from TI Code Composer Studio (CCS) debugger, which is used to debug TORNADO-E2/6xxx on-board DSP software via external TI XDS JTAG emulator or MicroLAB Systems MIRAGE JTAG emulator.

NOTE

Due to a complexity of configuration options for TORNADO-E2/6xxx DSP controller, it is highly recommended to use software utilities for TORNADO-E2/6xxx in order to configure on-board DSP environment and to access on-board peripherals in user DSP application.

F.1 Software Utilities for TORNADO-E2/6xxx on-board TMS320C6xxx DSP

Software utilities for TORNADO-E2/6xxx on-board TMS320C6xxx DSP come in well debugged and commented source code in single *T2E6XXX_DSP.H* header file for TI C6000 CCS C/C++ Compiler tools. This file must be included in user DSP application C-source code.

NOTE

C6XXX_DEF.H header file for general TMS320C6xxx DSP definitions, which is provided along with the *T2E6XXX_DSP.H* header file, is automatically included into user C-source code along with *T2E6XXX_DSP.H* header file.

The following is a list of operation that can be performed in user DSP application using macros and API functions include environment *T2E6XXX_DSP.H* header file:

- to configure TMS320C6xxx DSP on-chip PLL control registers and EMIF control registers
- to configure the on-board DSP serial ports (McBSP-0/1, McASP-0/1, I²C-1)
- to access on-board external DSP parallel peripherals (UART-A/B, USB and RTC controllers)
- to control GPIO-0..7 I/O pins
- to control on-board μ P Supervisory WDT/RTC controller
- to control reset signals and timer/IO signals for DCM sites (*SIOX*, *PIOX2*)
- to transfer data to/from DCM sites (*SIOX*, *ASIOX*, *PIOX2*, *HCX*)
- to program the on-board FLASH memory.

NOTE

For more details refer to the user's guide for software utilities for *TORNADO-E2/6xxx* DSP controller, which comes in electronic form along with software utilities.

F.2 *TORNADO-E2/6xxx* GEL-files for TI CCS TMS320C6xxx Debugger

TORNADO-E2/6xxx software utilities include CCS GEL-files for TI CCS TMS320C6xxx JTAG emulator debugger in order to automatically configure *TORNADO-E2/6xxx* DSP on-chip EMIF control registers on CCS debugger start and on software reset command.

The following CCS GEL-files are provided with the *TORNADO-E2/6xxx* software utilities:

- *T2E6713_REV1A_SDRAM4M.GEL* file, which must be used with *TORNADO-E2/6713* DSP controller rev.1A with on-board 300 MHz TMS320C6713 DSP and installed 4Mx32 SDRAM.
- *T2E6713_REV1A_SDRAM16M.GEL* file, which must be used with *TORNADO-E2/6713* DSP controller rev.1A with on-board 300 MHz TMS320C6713 and installed 16Mx32 SDRAM.

NOTE

Only one *T2E6713_REV1A_SDRAMxxM.GEL* CCS GEL-files shall be specified as a start-up CCS GEL-file in the 'Start-up GEL' folder of TI CCS debugger driver dialog of CCS SETUP utility

Refer to the user's guide for TI C6000 CCS for more details about TI CCS debugging tools and CCS GEL-files.

Appendix G. FLASH Memory Programming

This appendix contains detail information about programming procedure for *TORNADO-E2/6xxx* DSP controllers on-board FLASH memory.

NOTE

It is recommended that user DSP application will use FLASH programming utilities, which are the part of for *TORNADO-E2/6xxx* and come in *T2E6XXX_DSP.H* C/C++ header file (refer to [Appendix F](#) for more details). In this case, information provided in this appendix can be ignored.

NOTE

This appendix is provided for advanced users only, who need to design their own FLASH programming utilities for *TORNADO-E2/6xxx*.

G.1 Accessing FLASH Memory at *TORNADO-E2/6xxx* DSP controllers

TORNADO-E2/6xxx DSP controllers provide on-board either 512Kx8, or 1Mx8, or 8Mx8, or 64Mx8 in-system programmable FLASH memory, which is used as a boot source for *SA/BMODE-FLASH8* or *HOST/BMODE-FLASH8* DSP bootmodes (refer to [Table 2-1](#) and subsection “[DSP operation modes and DSP bootmodes](#)” of chapter 2 in this user’s guide for more details) and/or to save general purpose non-volatile data.

FLASH memory capacity

On the DSP side, capacity of on-board FLASH can be identified via {*FLASH_LEN-3..0*} bits of [DSP_SYS_CNF3_RG](#) DSP external control register ([Table 2-12](#)).

On the host *HCX* controller side, capacity of on-board FLASH can be identified via {*FLASH_LEN-3..0*} bits of [HCX_AX_SYS_CNF3_RG](#) *HCX* control register ([Table 2-28](#)).

All FLASH memories features identical programming algorithm and differ just in the device ID (refer to [Table G-1](#) and [Table G-2](#)) and number of sectors (8 sectors for 512Kx8 FLASH, 16 sectors for 1Mx8 FLASH, 128 sectors for 8Mx8 FLASH chip and 512 sectors for 64Mx8 FLASH chip). FLASH sector capacity is 64 kbytes for 512Kx8, 1Mx8 and 8Mx8 FLASH chips and 128 kbytes for 64Mx8 FLASH chip.

FLASH memory addressing

TORNADO-E2/6xxx on-board FLASH memory is allocated to the DSP EMIF CE-1 external data memory area (refer to [Table 2-2](#) and subsection “[FLASH memory area](#)” of chapter 2 in this user’s guide for more details).

512Kx8 and 1Mx8 FLASH directly fits into 1Mx8 address space of DSP EMIF CE-1 external data memory area, whereas 8Mx8 and 64Mx8 FLASH memories use paging technique with FLASH memory pages selected via {*FPAGE-5..0*} bits of [DSP_FLASH_PAGE_RG](#) DSP external control register. Refer to subsection “[FLASH memory area](#)” of section 2.2 of this user’s guide and for more details about FLASH memory addressing in *TORNADO-E2/6xxx* DSP controllers.

FLASH memory write protection

For *DSP stand-alone operation mode*, *TORNADO-E2/6xxx* provides user hardware and software FLASH write protection via the on-board SW1-2 and SW1-3 switches ([Figure 2-2](#) and [Figure A-1](#)) and via the *FLASH_WR_EN* and *FLASH64M_BOOT_SECTOR_WR_EN* bits of [DSP_FLASH_CNTR_RG](#) DSP external control register ([Table 2-16](#)).

G.2 FLASH Chip Description

Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. [Table G-1](#) defines the valid register command sequences for 512Kx8 and 8Mx8 FLASH memory chips and [Table G-2](#) for 64Mx8 FLASH memory chip.

Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

[illegible]

Autoselect Mode (note 7)												
Manufacturer ID	4	555	AA	2AA	55	555	90	x00	01			
Device ID (512Kx8)	4	555	AA	2AA	55	555	90	x01	4F			
Device ID (1Mx8)	4	555	AA	2AA	55	555	90	x01	38			
Device ID (8Mx8)	4	555	AA	2AA	55	555	90	x01	93			
Sector protect verify (note 8)	4	555	AA	2AA	55	555	90	SA x02	00			
									01			

Legend:

- X Don't care
- RA Address of the memory location to be read.
- RD Data read from location RA during read operation.
- PA Address of the memory location to be programmed.
- PD Data to be programmed at location PA.
- SA Address of the sector to be erased or verified. Address bits A18–A16 uniquely select any sector for 512Kx8 FLASH memory, and addresses A22–A16 for 8Mx8 FLASH memory.

Notes:

1. See AMD FLASH memory chips datasheets for descriptions of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or autoselect data, all bus cycles are write operations.
4. Address bits A22–A11 are don't care for unlock and command cycles, unless SA or PA required.
5. No unlock or command cycles required when device is in read mode.
6. The Reset command is required to return to the read mode when the device is in the autoselect mode or if DQ5 goes high.
7. The fourth cycle of the autoselect command sequence is a read cycle.
8. The data is 00h for an unprotected sector and 01h for a protected sector. The complete bus address in the fourth cycle is composed of the sector address (A22–A16), A1 = 1, and A0 = 0.
9. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
10. The Unlock Bypass Reset command is required to return to reading array data when the device is in the Unlock Bypass mode.
11. The system may read and program functions in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
12. The Erase Resume command is valid only during the Erase Suspend mode.

Table G-2. FLASH Command Definitions for 64Mx8 FLASH memory chip.

Command sequence (note 1)	Cycles	Bus cycles (note 2)											
		First		Second		Third		Fourth		Fifth		Sixth	
		addr	data	addr	data	addr	data	addr	data	addr	data	addr	data
Read (note 3)	1	RA	RD										
Reset (note 4)	1	XXX	F0										
Byte program	4	AAA	AA	555	55	AAA	A0	PA	PD				
Unlock Bypass Entry	3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program (note 7)	2	XXX	A0	PA	PD								
Unlock Bypass Reset	2	XXX	90	XXX	00								
Chip Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Erase Suspend (note 8)	1	XXX	B0										
Erase Resume (note 9)	1	XXX	30										
Autoselect Mode													
Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
Device ID (64Mx8) (note 5)	6	AAA	AA	555	55	AAA	90	X02	X7E	X1C	X23	X1E	X01
Sector protect verify (note 6)	4	AAA	AA	555	55	AAA	90	SA x04	00				
									01				

Legend:

- X Don't care
- RA Address of the memory location to be read.
- RD Data read from location RA during read operation.
- PA Address of the memory location to be programmed.
- PD Data to be programmed at location PA.
- SA Address of the sector to be erased or verified. Address bits A24–A16 uniquely select any sector for 64Mx8 FLASH memory.

- Notes:**
1. See AMD FLASH memory chips datasheets for descriptions of bus operations.
 2. All values are in hexadecimal.
 3. No unlock or command cycles required when device is in read mode.
 4. The Reset command is required to return to the read mode when the device is in the autoselect mode or if DQ5 goes high.
 5. The 4th-6th cycles of the autoselect command sequence are read cycles.
 6. The data is 00h for an unprotected sector and 01h for a protected sector.
 7. The Unlock Bypass command is required prior to the Unlock Bypass Program command. The Unlock Bypass Reset command is required to return to reading array data when the device is in the Unlock Bypass mode.
 8. The system may read and program functions in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
 9. The Erase Resume command is valid only during the Erase Suspend mode.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See “[Erase Suspend/Erase Resume Commands](#)” for more information on this mode.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the “[Reset Command](#)” section, next.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. [Table G-1](#) and [Table G-2](#) show the address and data requirements.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h for 512Kx8 and 8Mx8 FLASH memories or three read cycles at addresses XX02h, XX1Ch and XX1Eh for 64Mx8 FLASH memory return the device code. A read cycle containing a sector address (SA) and the address 02h for 512Kx8 and 8Mx8 FLASH memories or the address 04h for 64Mx8 FLASH memory returns 01h if that sector is protected, or 00h if it is unprotected. Refer to [Table G-3](#) and [Table G-4](#) for the valid sector addresses for 512Kx8 and 64Mx8 FLASH memories.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Table G-3. Uniform Sector Address Table for 512Kx8 FLASH memory.

Sector	A18	A17	A16	Address range
SA0	0	0	0	00000H-0FFFFH
SA1	0	0	1	10000H-1FFFFH
SA2	0	1	0	2000H-2FFFFH
SA3	0	1	1	30000H-3FFFFH
SA4	1	0	0	40000H-4FFFFH
SA5	1	0	1	50000H-5FFFFH
SA6	1	1	0	60000H-6FFFFH
SA7	1	1	1	70000H-7FFFFH

NOTE

For 1Mx8 and 8Mx8 FLASH memories, the A19..A16 and A22..A16 addresses correspondingly are used for sector selection and the sector addressing table is expanded.

Table G-4. Uniform Sector Address Table for 64Mx8 FLASH memory.

Sector	A24	A23	A22	A21	A20	A19	A18	A17	A16	Address range
SA0	0	0	0	0	0	0	0	0	0	00000000H-001FFFFH
SA1	0	0	0	0	0	0	0	0	1	00200000H-003FFFFH
SA2	0	0	0	0	0	0	0	1	0	00400000H-005FFFFH
SA3	0	0	0	0	0	0	0	1	1	00600000H-007FFFFH
...										
SA509	1	1	1	1	1	1	1	0	1	3FA00000H-3FBFFFFH
SA510	1	1	1	1	1	1	1	1	0	3FC00000H-3FDFFFFH
SA511	1	1	1	1	1	1	1	1	1	3FE00000H-3FFFFFFH

Byte Program Command Sequence

The device programs one byte of data for each program operation. The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verify the programmed cell margin. [Table G-1](#) and [Table G-2](#) show the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. See “[WRITE Operation Status](#)” for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries.

NOTE

A bit cannot be programmed from a “0” back to a “1”. Attempting to do so may halt the operation and set DQ5 to “1,” or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”.

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. [Table G-1](#) and [Table G-2](#) show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't cares for both cycles. The device then returns to reading array data.

[Figure G-1](#) illustrates the algorithm for the program operation.

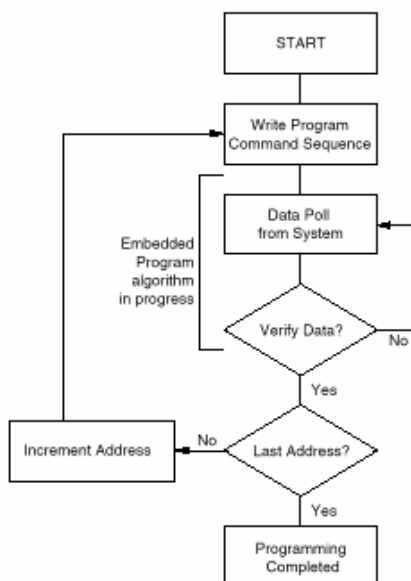


Figure G-1. Program Operation.

Note: 1. See [Table G-1](#) and [Table G-2](#) for program command sequence.

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. [Table G-1](#) and [Table G-2](#) show the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Erase algorithm are ignored. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See “[WRITE Operation Status](#)” subsection for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

[Figure G-2](#) illustrates the algorithm for the erase operation.

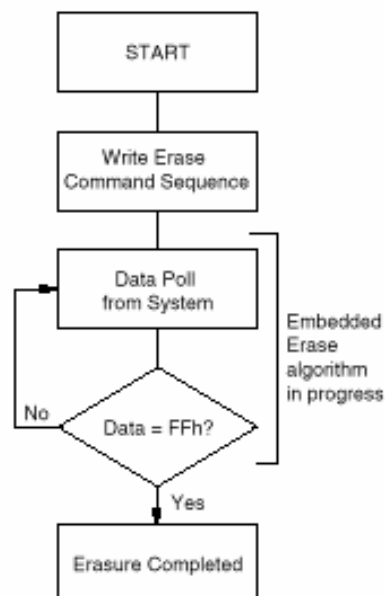


Figure G-2. Erase Operation.

Notes:

1. See [Table G-1](#) and [Table G-2](#) for erase command sequence.
2. See “[DQ3: Sector Erase Timer](#)” for more information.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. [Table G-1](#) and [Table G-2](#) show the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram the memory prior to erase. The Embedded Erase algorithm automatically programs and verifies the sector for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 μ s begins. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence,

and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 μ s, otherwise the last address and command might not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. If the time between additional sector erase commands can be assumed to be less than 50 μ s, the system need not monitor DQ3.

NOTE

Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to reading array data. The system must rewrite the command sequence and any additional sector addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out. (See the “[DQ3: Sector Erase Timer](#)” subsection.) The time-out begins from the rising edge of the final WE# pulse in the command sequence. Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. The Sector Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. (Refer to “[WRITE Operation Status](#)” for information on these status bits.)

Erase Suspend/Erase Resume Commands

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 μ s time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. Addresses are “don’t-cares” when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 μ s to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See “[WRITE Operation Status](#)” for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See “[WRITE Operation Status](#)” for more information.

The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. See “[Autoselect Command Sequence](#)” for more information.

The system must write the Erase Resume command (address bits are “don’t care”) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

WRITE Operation Status

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, and DQ7. [Table G-5](#) and the following subsections describe the functions of these bits. DQ7, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Table G-5. Write Operation Status.

operation		DQ7 (note 2)	DQ6	DQ5 (note 1)	DQ3	DQ2 (note 2)
Standard mode	Embedded Program Algorithm	DQ7	Toggle	0	N/A	No toggle
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle
Erase Suspend mode	Reading with Erase Suspended Sector	1	No Toggle	0	N/A	No toggle
	Reading with Non-Erase Suspended Sector	Data	Data	Data	Data	Data
	Erase-Suspend-Program	DQ7	Toggle	0	N/A	N/A

- Notes:**
1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See "[DQ5: Exceeded Timing Limits](#)" for more information.
 2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 μ s, then the device returns to reading array data.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. This is analogous to the complement/true datum output described for the Embedded Program algorithm: the erase function changes all the bits in a sector to "1"; prior to this, the device outputs the "complement," or "0." The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 μ s, then the device returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ7–DQ0 on the following read cycles. This is because DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. [Table G-5](#) shows the outputs for Data# Polling on DQ7. [Figure G-3](#) shows the Data# Polling algorithm.

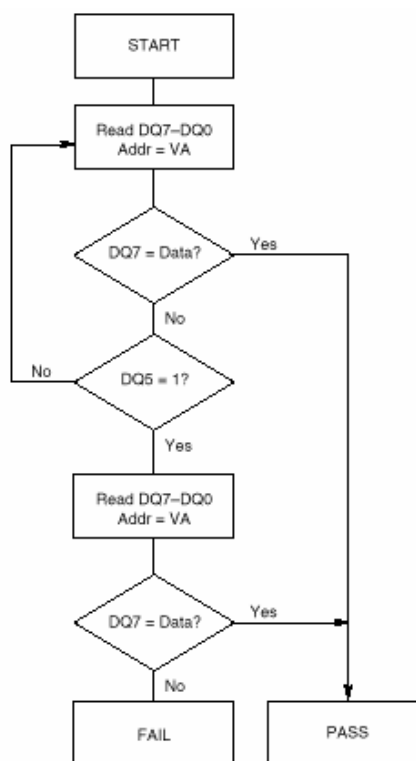


Figure G-3. Data# Polling Algorithm.

- Notes:**
1. VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.
 2. DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle (The system may use either OE# or CE# to control the read cycles). When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 μ s, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 μ s after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

[Table G-5](#) shows the outputs for Toggle Bit I on DQ6. [Figure G-4](#) shows the toggle bit algorithm in flowchart form, and the section “[Reading Toggle Bits DQ6/DQ2](#)” explains the algorithm. See also the subsection “[DQ2: Toggle Bit II](#)”.

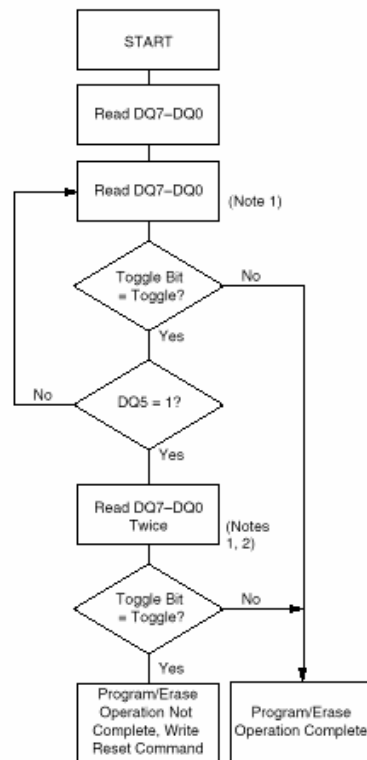


Figure G-4. Toggle Polling Algorithm.

- Notes:**
1. Read toggle bit twice to determine whether or not it is toggling. See text.
 2. Recheck toggle bit because it may stop toggling as DQ5 changes to “1”. See text.

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for era-sure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for era-sure. Thus, both status bits are required for sector and mode information. Refer to [Table G-5](#) to compare outputs for DQ2 and DQ6.

[Figure G-4](#) shows the toggle bit algorithm in flowchart form, and the section “[Reading Toggle Bits DQ6/DQ2](#)” explains the algorithm. See also the “[DQ6: Toggle Bit I](#)” subsection.

Reading Toggle Bits DQ6/DQ2

Refer to [Figure G-4](#) for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of [Figure G-4](#)).

[Table G-5](#) shows the outputs for Toggle Bit I on DQ6. [Figure G-4](#) shows the toggle bit algorithm. See also the subsection “[DQ2: Toggle Bit II](#)”.

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.”

NOTE

Only an erase operation can change a “0” back to a “1.” Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a “1.” Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out is complete, DQ3 switches from “0” to “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 μ s, the system need not monitor DQ3. See also the “[Sector Erase Command Sequence](#)” subsection.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is “1”, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0”, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. [Table G-5](#) shows the outputs for DQ3.

Appendix H. Dual-channel UART (DUART)

H.1 General Description

TORNADO-E2/6xxx DSP controllers provide on-board DUART, which is based on Exar ST16C2550 chip and comprise two independent UART channels (UART channel-A and channel-B) with external RS232C interfaces. Each UART channel is a hardware compatible superset for industry standard PC COM port.

DUART is used for communication with external computers and peripherals at speeds up to 384 kBaud for both stand-alone and host applications of *TORNADO-E2/6xxx* DSP controllers.

NOTE

This section provides only specific details about connection and programming of DUART for *TORNADO-E2/6xxx*.

Connection diagram

TORNADO-E2/6xxx on-board DUART is a part of external DSP environment ([Figure 2-1](#)). Detailed connection diagram for *TORNADO-E2/6713* on-board DUART is presented at [Figure H-1](#).

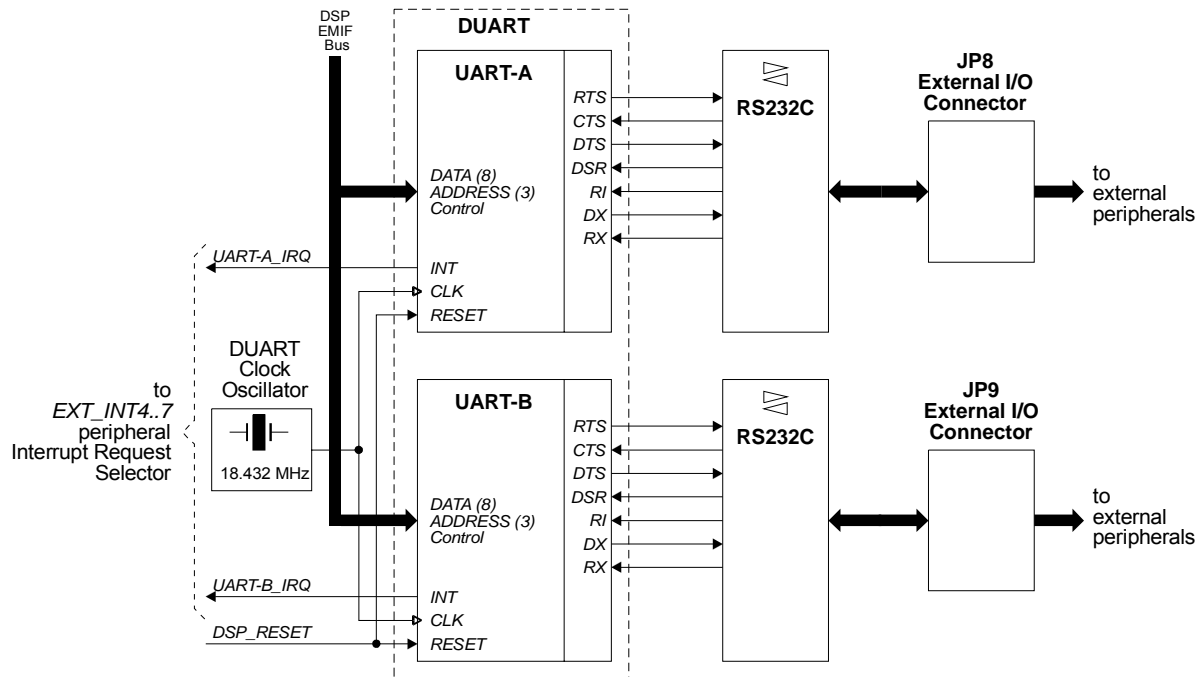


Figure H-1. Connection diagram for *TORNADO-E2/6713* on-board DUART.

Each DUART channel provides complete set of external modem control signals via on-board RS232C I/O interfaces, which are available via on-board JP8 and JP9 connectors ([Figure A-1](#)).

8-bit interface of DUART is connected to the least significant byte of 32-bit DSP EMIF data bus. Each DUART channel comprises eight control registers, which are used to configure UART channel and to receive/transmit data from/to external peripheral. Refer to subsection “[DUART control registers set](#)” later in this section for more details.

Each DUART channel generates individual interrupt request (*UART-A_IRQ* and *UART-B_IRQ*), which are used as DSP interrupt request sources for any of EXT_INT4..7 DSP external interrupt request selectors ([Figure 2-3](#)). Refer to subsection “[DUART-to-DSP interrupt requests](#)” later in this section for more details.

DUART control registers set

Each DUART channel includes eight 8-bit control registers, which are used to configure receiver/transmitter of this channel and to transfer data. Each DUART channel provides 16 bytes of receive and transmit FIFOs.

8-bit control register set for each DUART channel are mapped to DSP EMIF CE-3 external memory space as it is shown in [Table 2-2](#). [Table H-1](#) below provides details about control register address map and access mode.

NOTE

8-bit DUART registers are allocated to the least significant bytes of 32-bit data words of asynchronous EMIF CE-3 external memory space of *TORNADO-E2/6713* DSP controller at the x4 byte boundaries of 32-bit DSP data words.

Table H-1. DSP memory map for accessing DUART control registers.

UART register	DSP memory address for <i>TORNADO-E2/6713</i> DSP controller	valid bits @ EMIF area dataword format	data access formats	access condition	access mode
control registers for UART channel-A					
<i>UART-A_RHR</i> (<i>UART-A_RDATA_RG</i>)	B0040040H	D0..D7	X8	DLAB = 0 ²⁾	r
<i>UART-A_THR</i> (<i>UART-A_TDATA_RG</i>)	B0040040H	@W32	x16	DLAB = 0 ²⁾	w
<i>UART-A_DLL</i> (<i>UART-A_DIVL_RG</i>)	B0040040H		x32	DLAB = 1 ²⁾	r/w
<i>UART-A_IER</i> (<i>UART-A_IE_RG</i>)	B0040044H			DLAB = 0 ²⁾	r/w
<i>UART-A_DLM</i> (<i>UART-A_DIVH_RG</i>)	B0040044H			DLAB = 1 ²⁾	r/w
<i>UART-A_ISR</i> (<i>UART-A_IID_RG</i>)	B0040048H				r
<i>UART-A_FCR</i> (<i>UART-A_FCNTR_RG</i>)	B0040048H				w
<i>UART-A_LCR</i> (<i>UART-A_LCNTR_RG</i>)	B004004CH				r/w
<i>UART-A_MCR</i> (<i>UART-A_MCNTR_RG</i>)	B0040050H				r/w
<i>UART-A_LSR</i> (<i>UART-A_LSTAT_RG</i>)	B0040054H				r
<i>UART-A_MCR</i> (<i>UART-A_MSTAT_RG</i>)	B0040058H				r
<i>UART-A_SPR</i> (<i>UART-A_SCRPAD_RG</i>)	B004005CH				r/w
control registers for UART channel-B					
<i>UART-B_RHR</i> (<i>UART-B_RDATA_RG</i>)	B0040000H	D0..D7	X8	DLAB = 0 ²⁾	r
<i>UART-B_THR</i> (<i>UART-B_TDATA_RG</i>)	B0040000H	@W32	x16	DLAB = 0 ²⁾	w
<i>UART-B_DLL</i> (<i>UART-B_DIVL_RG</i>)	B0040000H		x32	DLAB = 1 ²⁾	r/w
<i>UART-B_IER</i> (<i>UART-B_IE_RG</i>)	B0040004H			DLAB = 0 ²⁾	r/w
<i>UART-B_DLM</i> (<i>UART-B_DIVH_RG</i>)	B0040004H			DLAB = 1 ²⁾	r/w
<i>UART-B_ISR</i> (<i>UART-B_IID_RG</i>)	B0040008H				r
<i>UART-B_FCR</i> (<i>UART-B_FCNTR_RG</i>)	B0040008H				w
<i>UART-B_LCR</i> (<i>UART-B_LCNTR_RG</i>)	B004000CH				r/w
<i>UART-B_MCR</i> (<i>UART-B_MCNTR_RG</i>)	B0040010H				r/w
<i>UART-B_LSR</i> (<i>UART-B_LSTAT_RG</i>)	B0040014H				r
<i>UART-B_MCR</i> (<i>UART-B_MSTAT_RG</i>)	B0040018H				r
<i>UART-B_SPR</i> (<i>UART-B_SCRPAD_RG</i>)	B004001CH				r/w

- Note:
- Access modes: r/w – read/write; r – read-only; w – write only.
 - 'DLAB' denotes bit #7 of the UART on-chip *UART-x_LCR* (*UART-x_LCNTR_RG*) control register for the corresponding UART channel (x = A, B).

For more details about DUART control registers formats, refer to original Exar ST16C2550 DUART documentation, which is provided in electronic form along with this user's guide.

DUART source clock and the bit rate frequency

DUART is clocked by on-board 18,432 MHz source clock ([Figure H-1](#)), which allows generating virtually all industry standard bit rate frequencies up to 1,152 Mbaud. However, for *TORNADO-E2/6xxx* boards, maximum DUART I/O baud rate is 384 kBaud, which is limited by on-board RS232C interfaces.

Baud rate frequency is programmed individually for each UART channel individually via *UART-A_DLL* (*UART-A_DIVL_RG*) and *UART-A_DLM* (*UART-A_DIVH_RG*) UART control registers ($x = A, B$).

DUART-to-DSP interrupt requests

Each DUART channel generates individual interrupt request (*UART-A_IRQ* and *UART-B_IRQ*), which are used as DSP interrupt request sources for any of the EXT_INT4..7 DSP external interrupt request selectors ([Figure 2-3](#)) controlled via [DSP_EXT_INT4_SEL_RG](#) .. [DSP_EXT_INT7_SEL_RG](#) DSP external control registers.

NOTE

DUART interrupt request outputs default to the Z-state output mode on DSP reset and power on conditions.

DSP application must set bit #3 of the *UART-x_MCR* (*UART-x_MCNTR_RG*) control register for each UART channel ([Table H-1](#)) into the '1' state in order to activate interrupt request outputs before selecting the corresponding UART interrupt requests source (*UART-A_IRQ* and *UART-B_IRQ*) via EXT_INT4..7 DSP external interrupt request selectors.

DUART-hardware reset

Hardware reset signal for DUART ([Figure H-1](#)) is generated on DSP power-on and reset conditions and applies simultaneously to both UART channels. DUART hardware reset signal is actually the DSP reset signal. When asserted, DUART hardware reset signal resets on-chip control registers for both UART channels to their default states.

RS232C interface connectors

RS232C interface assumes single-ended bipolar I/O signals. RS232C interface is an industry-standard external electrical interface for asynchronous communication.

For pinout of *TORNADO-E2/6xxx* on-board RS232C interface connectors refer to "[Appendix A. On-board Switches and Connectors.](#)" and to [Figure A-5](#).

Appendix I. USB interface

I.1 General Description

TORNADO-E2/6xxx on-board USB interface is a part of external DSP environment ([Figure 2-1](#)). *TORNADO-E2/6xxx* DSP controllers provide one of the following USB interfaces:

- 480 Mbit/s Philips ISP1761 USB rev.2.0 three-channel host/device controller with industry-standard two mini-‘A’ and one mini-‘AB’ OTG USB receptacle connectors.
- 480 Mbit/s Netchip NET2272 USB rev.2.0 single-channel device controller with industry-standard mini-‘B’ USB receptacle connector.
- Legacy 12 Mbit/s Lucent Technologies USS-820 USB rev.1.1 single-channel device controller with industry-standard mini-‘B’ USB receptacle connector.

Detailed connection diagram for all available *TORNADO-E2/6713* on-board USB controllers is provided at [Figure I-1](#), [Figure I-2](#) and [Figure I-3](#).

NOTE

This section provides only specific details about connection and programming of on-board USB controllers for *TORNADO-E2/6xxx*.

Refer to original manufacture documentation, which is provided in electronic form along with this user’s guide, for details about architecture and programming of the on-board USB controller.

I.2 Philips ISP1761 USB rev.2.0 Three-channel Host/Device Controller

Philips ISP1761 USB 2.0 controller runs in 480 Mbit/s (high-speed) and 12 Mbit/s (full-speed) modes. ISP1761 is a High-Speed USB On-Time-to-Go (OTG) Controller integrated with Advanced Philips Slave Host Controller and the Philips Peripheral Controller and provides three USB ports.

Port #1 can be configured to function as a downstream port, an upstream port or an OTG port; ports #2 and #3 are always configured as downstream host ports. The OTG port can switch its role from host to peripheral and can be used to implement a dual-role USB host or USB peripheral, depending on the cable connection. If the dual-role device is connected to a typical USB peripheral, it behaves like a typical USB host. The dual-role device can also be connected to a PC or any other USB host and behave like a typical USB peripheral.

ISP1761 internal architecture

The EHCI block and the Hi-Speed USB hub block are the main components of the Advanced Philips Slave Host Controller. The EHCI is the latest generation design, with improved data bandwidth. The EHCI in the ISP1761 is adapted from Enhanced Host Controller Interface Specification for USB Rev.1.0. The internal Hi-Speed USB hub block replaces the companion Host Controller block used in the original architecture of a Peripheral Component Interconnect (PCI) Hi-Speed USB Host Controller to handle the full-speed and low-speed modes. The hardware architecture in the ISP1761 is simplified to help reduce cost and development time, by eliminating the additional work involved in implementing the OHCI software required to support the full-speed and low-speed modes. The ISP1761 implements an EHCI that has an internal port, the Root Hub port (not available externally), on which the internal hub is connected. The three external ports are always routed to the internal hub. The internal hub is a Hi-Speed USB hub including the Integrated Transaction Translator.

The ISP1761 OTG Controller is designed to perform all the tasks specified in the OTG supplement. It supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for dual-role devices. The ISP1761 uses software implementation of HNP and SRP for maximum flexibility. A set of OTG registers provides the control and status monitoring capabilities to support software HNP and SRP.

The ISP1761 Peripheral Controller is a high-speed USB peripheral controller. It implements the Hi-Speed USB or the Original USB physical layer and the packet protocol layer. It maintains up to 16 USB endpoints concurrently (control IN and control OUT, 7 IN and 7 OUT configurable) along with endpoint EP0 setup, which accesses the setup buffer.

Connection diagram

32-bit bus interface of ISP1761 USB controller is connected to 32-bit DSP EMIF of *TORNADO-E2/6713* board ([Figure I-1](#)) and occupies 64 kB memory area (refer to [Table 2-2](#)), which includes 1 kB of registers set and 63 kB of internal memory.

A set of on-chip 256 32-bit registers includes operational registers, Host Controller-specific, OTG Controller-specific and Peripheral Controller-specific registers. ISP1761 implements 63 kB of internal memory, which consists of payload area and Philips Transfer Descriptor (PTD) area. This memory size is optimized to balance maximum USB performance with minimal system loading and cost.

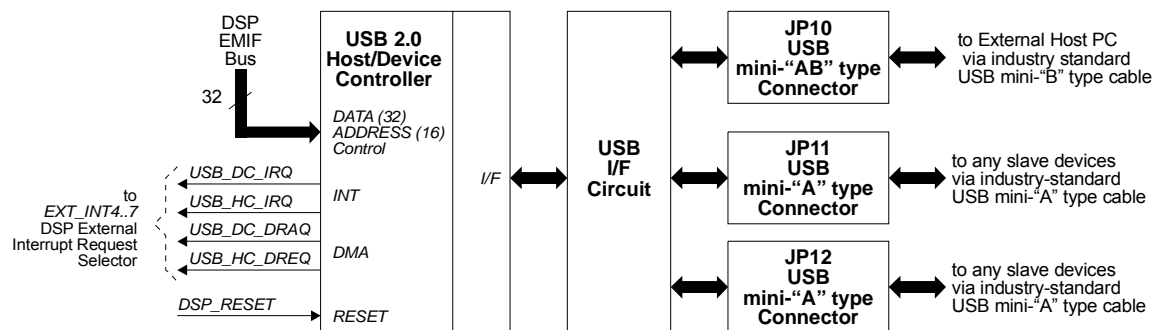


Figure I-1. Connection diagram for *TORNADO-E2/6713* on-board ISP1761 USB controller.

Data transfers between DSP and ISP1761 can be done using either Programmed I/O (PIO) or Direct Memory Access (DMA) modes. It is recommended to use DMA in order to avoid high DSP kernel utilization time.

ISP1761 on-chip DMA controller is 'slave-type' and has two independent DMA ports for the Host Controller (HC_DREQ and HC_DACK) and the Peripheral Controller (DC_DREQ and DC_DACK), that can generate DREQ requests with configurable burst size and maximum number of bytes transferred. Both DC_DREQ and HC_DREQ DMA requests can be used as DSP external interrupt request sources for synchronization with DMA channels of on-board DSP. If DREQ is not required, the ISP1761 can be accessed by system's DMA in PIO mode and the ISP1761 DMA programming is not required. Programming memory register is necessary only during memory read cycles.

Programming of ISP1761 for enumeration and data transfer involves programming of:

- CPU interface configuration registers, which define the behavior of control signals of DSP interface.
- EHCI operational registers to initialize EHCI.
- Philips Transfer Descriptors (PTDs) found in the ISP1761 memory are the dedicated memory areas.
- The payload area that contains the data to be transferred.

Refer to original manufacture documentation, which is provided in electronic form along with this user's guide, for details about architecture and programming of ISP1761 USB controller.

ISP1761 USB 2.0 controller registers set

A set of on-chip 256 32-bit registers include operational registers, Host Controller-specific, OTG Controller-specific and Peripheral Controller-specific registers. All registers range from ISP1761 USB controller start address and occupy the size of 1 kB. These registers can be read or written as 32-bit data. Operational registers range from B00C0000H to B00C01FFH, Host Controller-specific and OTG Controller-specific registers range from B00C0300H to B00C03FFH, Peripheral Controller-specific registers range from B00C0200H to B00C02FFH for *TORNADO-E2/6713* DSP controller. [Table I-1](#) below provides details about DSP memory mapping and access mode for ISP1761 on-chip control registers.

Table I-1. DSP memory map for on-chip registers of ISP1761 USB 2.0 controller for TORNADO-E2/6713 board.

ISP1761 USB 2.0 on-chip control register	DSP memory address for TORNADO-E2/6713	valid bits	data access formats
Operational registers			
<i>EHCI capability registers</i>			
USB3_CAPLENGTH_RG	B00C0000H	D0..D7	x32
USB3_HCIVERSION_RG	B00C0002H	D0..D15	x32
USB3_HCSPARAMS_RG	B00C0004H	D0..D31	x32
USB3_HCCPARAMS_RG	B00C0008H	D0..D31	x32
<i>EHCI operational registers</i>			
USB3_USBCMD_RG	B00C0020H	D0..D31	x32
USB3_USBSTS_RG	B00C0024H	D0..D31	x32
USB3_USBINTR_RG	B00C0028H	D0..D31	x32
USB3_FRINDEX_RG	B00C002CH	D0..D31	x32
USB3_CONFIGFLAG_RG	B00C0060H	D0..D31	x32
USB3_PORTSC1_RG	B00C0064H	D0..D31	x32
USB3_ISO_PTD_DONE_MAP_RG	B00C0130H	D0..D31	x32
USB3_ISO_PTD_SKIP_MAP_RG	B00C0134H	D0..D31	x32
USB3_ISO_PTD_LAST_PTD_RG	B00C0138H	D0..D31	x32
USB3_INT_PTD_DONE_MAP_RG	B00C0140H	D0..D31	x32
USB3_INT_PTD_SKIP_MAP_RG	B00C0144H	D0..D31	x32
USB3_INT_PTD_LAST_PTD_RG	B00C0148H	D0..D31	x32
USB3_ATL_PTD_DONE_MAP_RG	B00C0150H	D0..D31	x32
USB3_ATL_PTD_SKIP_MAP_RG	B00C0154H	D0..D31	x32
USB3_ATL_PTD_LAST_PTD_RG	B00C0158H	D0..D31	x32
Host controller-specific registers			
<i>Configuration registers</i>			
USB3_HW_MODE_CNTR_RG	B00C0300H	D0..D31	x32
USB3_HC_CHIP_ID_RG	B00C0304H	D0..D31	x32
USB3_HC_SCRATCH_RG	B00C0308H	D0..D31	x32
USB3_SW_RESET_RG	B00C030CH	D0..D31	x32
USB3_HC_DMA_CONFIG_RG	B00C0330H	D0..D31	x32
USB3_HC_BUFFER_STATUS_RG	B00C0334H	D0..D31	x32
USB3_ATL_DONE_TIMEOUT_RG	B00C0338H	D0..D31	x32
USB3_MEMORY_RG	B00C033CH	D0..D31	x32
USB3_EDGE_INTERRUPT_CNT_RG	B00C0340H	D0..D31	x32
USB3_DMA_START_ADDR_RG	B00C0344H	D0..D31	x32
USB3_PWR_DOWN_CNTR_RG	B00C0354H	D0..D31	x32
<i>Interrupt registers</i>			
USB3_HC_INT_RG	B00C0310H	D0..D31	x32
USB3_HC_INT_EN_RG	B00C0314H	D0..D31	x32
USB3_ISO_IRQ_MASK_OR_RG	B00C0318H	D0..D31	x32
USB3_INT_IRQ_MASK_OR_RG	B00C031CH	D0..D31	x32
USB3_ATL_IRQ_MASK_OR_RG	B00C0320H	D0..D31	x32
USB3_ISO_IRQ_MASK_AND_RG	B00C0324H	D0..D31	x32
USB3_INT_IRQ_MASK_AND_RG	B00C0328H	D0..D31	x32
USB3_ATL_IRQ_MASK_AND_RG	B00C032CH	D0..D31	x32

OTG controller-specific registers			
USB3_PRODUCT_ID_RG	B00C0370H	D0..D31	x32
USB3_OTG_CNTR_RG	B00C0374H	D0..D31	x32
USB3_OTG_STAT_RG	B00C0378H	D0..D15	x32
USB3_OTG_INT_LATCH_RG	B00C037CH	D0..D31	x32
USB3_OTG_INT_EN_FALL_RG	B00C0380H	D0..D31	x32
USB3_OTG_INT_EN_RISE_RG	B00C0384H	D0..D31	x32
USB3_OTG_TIMER_LW_RG	B00C0388H	D0..D31	x32
USB3_OTG_TIMER_HW_RG	B00C038CH	D0..D31	x32
Peripheral controller-specific registers			
<i>Initialization registers</i>			
USB3_ADDR_RG	B00C0200H	D0..D7	x32
USB3_MODE_RG	B00C020CH	D0..D15	x32
USB3_INT_CNF_RG	B00C0210H	D0..D7	x32
USB3_DEBUG_RG	B00C0212H	D0..D15	x32
USB3_DC_INT_EN_RG	B00C0214H	D0..D31	x32
<i>Data flow registers</i>			
USB3_ENDPNT_INDEX_RG	B00C022CH	D0..D7	x32
USB3_CNTR_FUNC_RG	B00C0224H	D0..D7	x32
USB3_DATA_PORT_RG	B00C0220H	D0..D15	x32
USB3_BUF_LEN_RG	B00C021CH	D0..D15	x32
USB3_DC_BUF_STAT_RG	B00C021EH	D0..D7	x32
USB3_ENDPNT_MAX_PACK_SIZE_RG	B00C0204H	D0..D15	x32
USB3_ENDPNT_TYPE_RG	B00C0208H	D0..D15	x32
<i>DMA registers</i>			
USB3_DMA_CMD_RG	B00C0230H	D0..D7	x32
USB3_DMA_TRANSFER_CNT_RG	B00C0234H	D0..D31	x32
USB3_DC_DMA_CNF_RG	B00C0238H	D0..D15	x32
USB3_DMA_HARDWARE_RG	B00C023CH	D0..D7	x32
USB3_DMA_INT_SRC_RG	B00C0250H	D0..D15	x32
USB3_DMA_INT_EN_RG	B00C0254H	D0..D15	x32
USB3_DMA_ENDPNT_RG	B00C0258H	D0..D7	x32
USB3_DMA_BURST_CNT_RG	B00C0264H	D0..D15	x32
<i>General registers</i>			
USB3_DC_INT_RG	B00C0218H	D0..D31	x32
USB3_DC_CHIP_ID_RG	B00C0270H	D0..D31	x32
USB3_FRAME_NUM_RG	B00C0274H	D0..D15	x32
USB3_DC_SCRATCH_RG	B00C0278H	D0..D15	x32
USB3_UNLOCK_DEV_RG	B00C027CH	D0..D15	x32
USB3_INT_PULSE_WIDTH_RG	B00C0280H	D0..D15	x32
USB3_TEST_MODE_RG	B00C0284H	D0..D7	x32

USB-to-DSP interrupt and DMA requests

ISP1761 USB controller generates dedicated interrupt requests from Host Controller and Peripheral Controller (*USB_DC_IRQ* and *USB_HC_IRQ*) and corresponding DMA requests (*USB_DC_DREQ* and *USB_HC_DREQ*) to TORNADO-E2/6xxx on-board DSP via the DSP EXT_INT4..7 external interrupt requests ([Figure 2-3](#)), which are controlled via the [DSP_EXT_INT4_SEL_RG](#), [DSP_EXT_INT5_SEL_RG](#), [DSP_EXT_INT6_SEL_RG](#) and [DSP_EXT_INT7_SEL_RG](#) DSP external control registers.

TORNADO-E2/6xxx on-board USB receptacle connectors

TORNADO-E2/6xxx board with ISP1761 USB controller provides JP11 and JP12 industry-standard mini-‘A’ USB host connectors and JP10 mini-‘AB’ USB OTG host/device connector ([Figure A-1](#)), which allow connection to one host computer or two USB devices.

Hardware reset for USB controller

Hardware reset signal for ISP1761 USB controller is generated on the power-on and DSP reset conditions and is actually a DSP reset signal. When asserted, USB hardware reset signal resets ISP1761 on-chip control registers to their default state.

I.3 PLX/NetChip NET2272 USB 2.0 One-channel Device Controller

PLX/NetChip NET2272 USB 2.0 device controller provides USB device interface and supports industry-standard USB rev.2.0 and rev.1.1 protocols at 480 Mbit/s (high-speed) and 12 Mbit/s (full-speed). NET2272 USB 2.0 device controller is a flexible programmable device with build-in programmable high-density data FIFO, support for four physical and 30 virtual endpoints, 16-bit and 8-bit DSP-to-USB data format, and many more features.

NOTE

TORNADO-E2/6xxx on-board NET2272 USB 2.0 device interface does not provide host controller functionality for the USB bus and can communicate with the USB host controller of host PC only.

Connection diagram

16-bit microprocessor interface of NET2272 USB 2.0 device controller is connected to 32-bit DSP EMIF of TORNADO-E2/6713 ([Figure I-2](#)). On-chip control registers of NET2272 controller are mapped to DSP EMIF CE-3 external memory space (refer to [Table 2-2](#)).

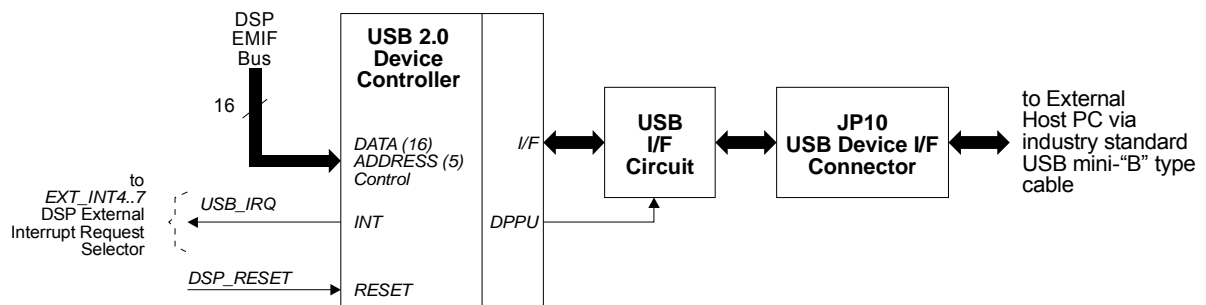


Figure I-2. Connection diagram for TORNADO-E2/6713 on-board NET2272 USB controller.

NET2272 USB 2.0 device controller registers set

NET2272 USB 2.0 device controller registers set comprises 51 on-chip control registers, which are used to configure USB controller and to transfer data over the USB bus. 22 on-chip registers are accessed directly by DSP and the remaining 29 registers are accessed via indirect addressing. [Table I-2](#) below provides details about mapping and access mode for every on-chip control register of the NET2272 USB 2.0 device controller.

NOTE

For *TORNADO-E2/6713* board, 16-bit control registers of the NET2272 USB 2.0 device controller are allocated to the least significant halfwords of DSP 32-bit data words at the x4 byte boundaries

Table I-2. DSP memory map for on-chip registers of NET2272 USB 2.0 controller for *TORNADO-E2/6713* board.

NET2272 USB 2.0 on-chip control register	DSP memory address for <i>TORNADO-E2/6713</i>	Indirect register address via the <i>USB2_REGADDRPTR_RG</i> register	valid bits	data access formats
Directly accessed control registers				
<i>USB2_REGADDRPTR_RG</i>	B00C0000H	-	D0..D7	x8
<i>USB2_REGDATA_RG</i>	B00C0004H		D0..D7/D15	x8/x16
<i>USB2_IRQSTAT0_RG</i>	B00C0008H		D0..D7	x8
<i>USB2_IRQSTAT1_RG</i>	B00C000CH		D0..D7	x8
<i>USB2_PAGESEL_RG</i>	B00C0010H		D0..D7	x8
<i>USB2_EPDATA_RG</i>	B00C0014H		D0..D7/D15	x8/x16
<i>USB2_EPSTAT0_RG</i>	B00C0018H		D0..D7	x8
<i>USB2_EPSTAT1_RG</i>	B00C001CH		D0..D7	x8
<i>USB2_EPTRANSFER0_RG</i>	B00C0020H		D0..D7	x8
<i>USB2_EPTRANSFER1_RG</i>	B00C0024H		D0..D7	x8
<i>USB2_EPTRANSFER2_RG</i>	B00C0028H		D0..D7	x8
<i>USB2_EPIRQENB_RG</i>	B00C002CH		D0..D7	x8
<i>USB2_EPAVAIL0_RG</i>	B00C0030H		D0..D7	x8
<i>USB2_EPAVAIL1_RG</i>	B00C0034H		D0..D7	x8
<i>USB2_RSPCLR_RG</i>	B00C0038H		D0..D7	x8
<i>USB2_RSPSET_RG</i>	B00C003CH		D0..D7	x8
<i>USB2_USBCTL0_RG</i>	B00C0060H		D0..D7	x8
<i>USB2_USBCTL1_RG</i>	B00C0064H		D0..D7	x8
<i>USB2_FRAME0_RG</i>	B00C0068H		D0..D7	x8
<i>USB2_FRAME1_RG</i>	B00C006CH		D0..D7	x8
<i>USB2_DMAREQ_RG</i>	B00C0070H		D0..D7	x8
<i>USB2_SCRATCH_RG</i>	B00C0074H		D0..D7	x8

Indirectly accessed control registers (register address is written into the <i>USB2_REGADDRPTR_RG</i> register and data is accessed via the <i>USB2_REGDATA_RG</i> register)				
<i>USB2_IRQENB0_RG</i>	-	20H	D0..D7	x8
<i>USB2_IRQENB1_RG</i>		21H	D0..D7	x8
<i>USB2_LOCCTL_RG</i>		22H	D0..D7	x8
<i>USB2_CHIPREVLEGACY_RG</i>		23H	D0..D7	x8
<i>USB2_LOCCTL1_RG</i>		24H	D0..D7	x8
<i>USB2_CHIPREV2272_RG</i>		25H	D0..D7	x8
<i>USB2_EPMAXPKT0_RG</i>		28H	D0..D7	x8
<i>USB2_EPMAXPKT1_RG</i>		29H	D0..D7	x8
<i>USB2_EPCFG_RG</i>		2AH	D0..D7	x8
<i>USB2_EPHBW_RG</i>		2BH	D0..D7	x8
<i>USB2_EBBUFFSTATES_RG</i>		2CH	D0..D7	x8
<i>USB2_OURADDR_RG</i>		30H	D0..D7	x8
<i>USB2_USBDIAG_RG</i>		31H	D0..D7	x8
<i>USB2_USBTEST_RG</i>		32H	D0..D7	x8
<i>USB2_XCVRDIAG_RG</i>		33H	D0..D7	x8
<i>USB2_VIRTOUT0_RG</i>		34H	D0..D7	x8
<i>USB2_VIRTOUT1_RG</i>		35H	D0..D7	x8
<i>USB2_VIRTIN0_RG</i>		36H	D0..D7	x8
<i>USB2_VIRTIN1_RG</i>		37H	D0..D7	x8
<i>USB2_SETUP0_RG</i>		40H	D0..D7	x8
<i>USB2_SETUP1_RG</i>		41H	D0..D7	x8
<i>USB2_SETUP2_RG</i>		42H	D0..D7	x8
<i>USB2_SETUP3_RG</i>		43H	D0..D7	x8
<i>USB2_SETUP4_RG</i>		44H	D0..D7	x8
<i>USB2_SETUP5_RG</i>		45H	D0..D7	x8
<i>USB2_SETUP6_RG</i>		46H	D0..D7	x8
<i>USB2_SETUP7_RG</i>		47H	D0..D7	x8

USB-to-DSP interrupt request

NET2272 USB 2.0 controller generates interrupt request to on-board DSP (*USB_IRQ*), which is used as DSP interrupt request source for any of the EXT_INT4..7 DSP external interrupt request selectors ([Figure 2-3](#)) controlled via [DSP_EXT_INT4_SEL_RG](#) .. [DSP_EXT_INT7_SEL_RG](#) DSP external control registers.

TORNADO-E2/6xxx on-board USB receptacle connector

NET2272 USB 2.0 device controller connects to host PC USB interface via JP10 industry-standard mini-‘B’ USB device connector ([Figure A-1](#)).

Hardware reset for NET2272 USB controller

Hardware reset signal for NET2272 USB controller is generated on the power-on and DSP reset conditions and is actually a DSP reset signal. When asserted, USB hardware reset signal resets NET2272 on-chip control registers to their default state.

I.4 Lucent Technologies USS-820 USB 1.1 One-channel Device Controller

Lucent Technologies USS-820 USB 1.1 device controller is used as a legacy USB controller for backward compatibility with *TORNADO-E6x* boards. USS-820 USB controller supports industry-standard USB.1.1 protocol at up to 12 Mbit/s data transfer rate.

NOTE

TORNADO-E2/6xxx on-board USS-820 USB 1.1 device interface does not provide host controller functionality for the USB bus and can communicate with the USB host controller of host PC only.

Connection diagram

USS-820 USB controller is flexible programmable device with build-in programmable FIFO for transmitter and receiver, dual-packet support, support for 16 USB endpoints, integrated USB transceivers, and many more features.

USB 1.1 device controller features 8-bit data bus, which is connected to the lowest significant byte of 32-bit *TORNADO-E2/6713* DSP data bus ([Figure I-3](#)).

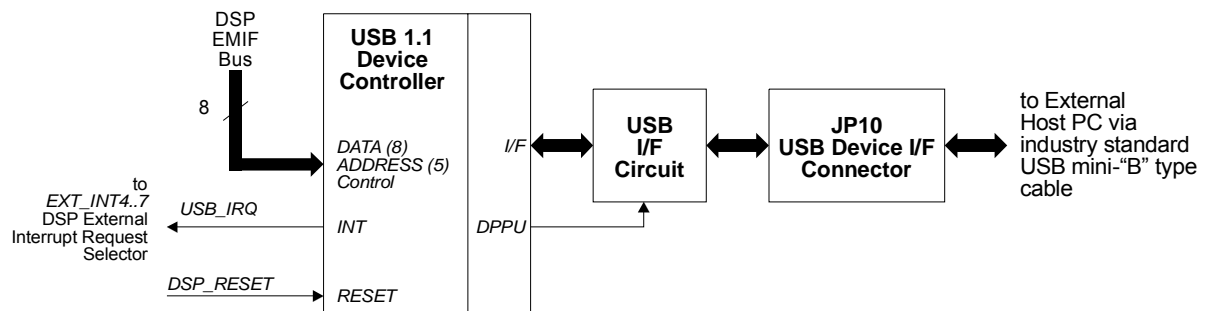


Figure I-3. Connection diagram for *TORNADO-E2/6713* on-board USS820 USB controller.

USS-820 USB 1.1 device controller registers set

USS-820 USB 1.1 device controller register set comprises of 32 8-bit registers (refer to [Table I-3](#)) and is allocated into EMIF CE-3 memory space of on-board DSP (refer to [Table 2-2](#)).

NOTE

For *TORNADO-E2/6713* boards, 8-bit control registers of the USS-820 USB 1.1 device controller are allocated to the least significant bytes of DSP 32-bit data words at the x4 byte boundaries.

Table I-3. DSP memory map for on-chip registers of USS-820 USB 1.1 controller for *TORNADO-E2/6713* board.

USS-820 USB 1.1 on-chip control register	DSP memory address for <i>TORNADO-E2/6713</i> DSP controller	valid bits	data access formats
<i>USB1_TXDAT_RG</i>	B00C0000H	D0..D7	x8
<i>USB1_TXCNTL_RG</i>	B00C0004H	D0..D7	x8
<i>USB1_TXCNTH_RG</i>	B00C0008H	D0..D7	x8
<i>USB1_TXCON_RG</i>	B00C000CH	D0..D7	x8
<i>USB1_TXFLG_RG</i>	B00C0010H	D0..D7	x8
<i>USB1_RXDAT_RG</i>	B00C0014H	D0..D7	x8
<i>USB1_RXCNTL_RG</i>	B00C0018H	D0..D7	x8
<i>USB1_RXCNTH_RG</i>	B00C001CH	D0..D7	x8
<i>USB1_RXCON_RG</i>	B00C0020H	D0..D7	x8
<i>USB1_RXFLG_RG</i>	B00C0024H	D0..D7	x8
<i>USB1_EPINDEX_RG</i>	B00C0028H	D0..D7	x8
<i>USB1_EPCON_RG</i>	B00C002CH	D0..D7	x8
<i>USB1_TXSTAT_RG</i>	B00C0030H	D0..D7	x8
<i>USB1_RXSTAT_RG</i>	B00C0034H	D0..D7	x8
<i>USB1_SOFL_RG</i>	B00C0038H	D0..D7	x8
<i>USB1_SOFH_RG</i>	B00C003CH	D0..D7	x8
<i>USB1_FADDR_RG</i>	B00C0040H	D0..D7	x8
<i>USB1_SCR_RG</i>	B00C0044H	D0..D7	x8
<i>USB1_SSR_RG</i>	B00C0048H	D0..D7	x8
<i>USB1_SBI_RG</i>	B00C0050H	D0..D7	x8
<i>USB1_SBI1_RG</i>	B00C0054H	D0..D7	x8
<i>USB1_SBIE_RG</i>	B00C0058H	D0..D7	x8
<i>USB1_SBIE1_RG</i>	B00C005CH	D0..D7	x8
<i>USB1_REV_RG</i>	B00C0060H	D0..D7	x8
<i>USB1_LOCK_RG</i>	B00C0064H	D0..D7	x8
<i>USB1_PEND_RG</i>	B00C0068H	D0..D7	x8
<i>USB1_SCRATCH_RG</i>	B00C006CH	D0..D7	x8
<i>USB1_MCSR_RG</i>	B00C0070H	D0..D7	x8

USB-to-DSP interrupt request

USS-820 USB 1.1 device controller generates interrupt request to on-board DSP (*USB_IRQ*), which is used as DSP interrupt request source for any of the EXT_INT4..7 DSP external interrupt request selectors ([Figure 2-3](#)) controlled via [DSP_EXT_INT4_SEL_RG](#) .. [DSP_EXT_INT7_SEL_RG](#) DSP external control registers.

TORNADO-E2/6xxx on-board USB receptacle connector

USS-820 USB 1.1 device controller connects to host PC USB interface via JP10 industry-standard mini-‘B’ USB device connector ([Figure A-1](#)).

Hardware reset for USS-820 USB controller

Hardware reset signal for USS-820 USB controller is generated on the power-on and DSP reset conditions and is actually a DSP reset signal. When asserted, USB hardware reset signal resets USS-820 on-chip control registers to their default state.

Appendix J. Real-time Clock (RTC) Controller

J.1 General Description

TORNADO-E2/6xxx DSP controllers provide on-board battery backup RTC controller, which is used for time keeping, saving non-volatile data, and allows remote control of external power supply for automatic system wake-up on programmable time instant.

RTC controller features 2100 year calendar, on-board battery back-up, programmable alarm, programmable watchdog timer (WDT). RTC controller also provides 256 bytes NvRAM for non-volatile data. Programmable is used to generate DSP interrupt request and/or to activate external power supply in case the latter supports this feature.

TORNADO-E2/6xxx on-board RTC controller is based around the Dallas Semiconductor DS1501 RTC chip with external back-up battery. Connection diagram for on-board DS1501 RTC controller is shown at [Figure J-1](#).

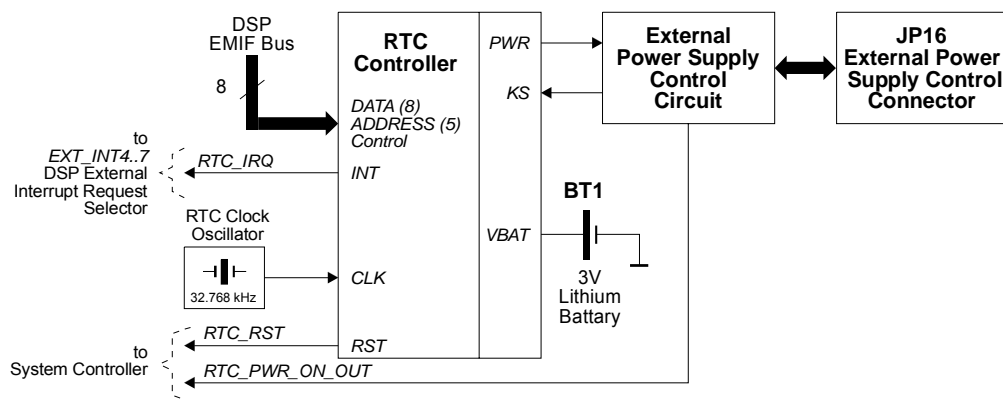


Figure J-1. Connection diagram for *TORNADO-E2/6713* DSP controller on-board RTC.

RTC backup battery

TORNADO-E2/6xxx boards use 3V lithium battery type 1216, 1220, or 1225 to backup RTC/NvRAM data, which plugs into on-board BT1 socket ([Figure 2-2](#) and [Figure A-1](#)). Typically, new Duracell 3V lithium type 1216 battery will safely maintain RTC on-chip data within 2..3 years.

IMPORTANT NOTE

Installation of other than 3V lithium battery type 1216/1220/1225 is prohibited and can result in damage of *TORNADO-E2/6xxx* on-board hardware.

RTC control register set

DS1501 RTC controller provides a set of on-chip 8-bit control registers, which are accessed via DSP EMIF CE-3 external memory space (refer to [Table 2-2](#)).

NOTE

DS1501 RTC on-chip 8-bit control registers are allocated into least significant bytes of DSP 32-bit data words at x4 byte boundaries.

TORNADO-E2/6xxx features hardware protection of RTC contents in order to exclude accidental access to RTC and to increase RTC data security. *RTC_EN* bit of [DSP_WDT_RTC_CNTR_RG](#) DSP external control register is used to enable/disable access to RTC from DSP application (refer to [Table 2-18](#)).

NOTE

RTC_EN bit of [DSP_WDT_RTC_CNTR_RG](#) DSP external control register defaults to the '0' state on DSP power on and disables access to RTC controller.

In order to enable access to RTC, DSP application must set *RTC_EN* bit into the '1' state.

DS1501 RTC on-chip control register set comprises 16 8-bit registers. [Table J-1](#) below provides details about mapping and access mode for control registers of the DS1501 RTC.

Table J-1. Control register list for DS1501 RTC controller for *TORNADO-E2/6713*.

DS1501 RTC on-chip control register	DSP memory address for <i>TORNADO-E2/6713</i>	valid data bits or DSP 32-bit dataword	data access format
<i>RTC_CLK_SECONDS_RG</i>	B0080000H	D0..D7	x8
<i>RTC_CLK_MINUTES_RG</i>	B0080004H	D0..D7	x8
<i>RTC_CLK_HOURS_RG</i>	B0080008H	D0..D7	x8
<i>RTC_CLK_DAY_OF_WEEK_RG</i>	B008000CH	D0..D7	x8
<i>RTC_CLK_DATE_RG</i>	B0080010H	D0..D7	x8
<i>RTC_CLK_MONTH_RG</i>	B0080014H	D0..D7	x8
<i>RTC_CLK_YEAR_RG</i>	B0080018H	D0..D7	x8
<i>RTC_CLK_CENTURY_RG</i>	B008001CH	D0..D7	x8
<i>RTC_ALARM_SECONDS_RG</i>	B0080020H	D0..D7	x8
<i>RTC_ALARM_MINUTES_RG</i>	B0080024H	D0..D7	x8
<i>RTC_ALARM_HOURS_RG</i>	B0080028H	D0..D7	x8
<i>RTC_ALARM_DAY_DATE_RG</i>	B008002CH	D0..D7	x8
<i>RTC_WDT_SEC_FRACTION_RG</i>	B0080030H	D0..D7	x8
<i>RTC_WDT_SECONDS_RG</i>	B0080034H	D0..D7	x8
<i>RTC_CNTRA_RG</i>	B0080038H	D0..D7	x8
<i>RTC_CNTRB_RG</i>	B008003CH	D0..D7	x8
<i>RTC_USER_RAM_ADDR_RG</i>	B0080040H	D0..D7	x8
<i>RTC_USER_RAM_DATA_RG</i>	B008004CH	D0..D7	x8

For more details about on-chip control registers for DS1501 RTC refer to original manufacturer documentation, which is provided in electronic form along with this user's guide.

RTC clock oscillator control

DS1501 RTC allows to enable/disable on-chip clock oscillator in order to start/stop real-time clock and to reduce power consumption from back-up battery.

RTC on-chip clock oscillator is controlled via EOSC bit (D7) of register #5. When this bit is set to the '0' state, then RTC clock oscillator is enabled and real-time clock data and calendar are updated. When this bit is set to the '1' state, then RTC clock is disabled, and real-time clock data and calendar are not updated, however, in this case RTC controller consumes significantly lower power from backup battery when *TORNADO-E2/6xxx* DSP controller power is off.

IMPORTANT NOTE

RTC controller on-chip clock oscillator is enabled (bit EOSC of register #5 is set to the '0' state) upon *TORNADO-E2/6xxx* power-up.

RTC-to-DSP interrupts

RTC provides programmable interrupt output (*RTC_IRQ*), which is used to generate DSP interrupt on programmable alarm event, on kickstart/wakeup events or on WDT expiration event.

RTC *RTC_IRQ* interrupt request output is used as DSP interrupt request source for EXT_INT4..7 DSP external interrupt request selectors ([Figure 2-3](#)), which are controlled via the [DSP_EXT_INT4_SEL_RG](#), [DSP_EXT_INT5_SEL_RG](#), [DSP_EXT_INT6_SEL_RG](#) and [DSP_EXT_INT7_SEL_RG](#) DSP external control registers.

DSP reset control by RTC

DS1501 RTC always generates DSP reset signal via *RTC_RST* RTC output signal (refer to [Figure J-1](#)) on power-on and power-off conditions, and can be configured to generate DSP reset on programmable RTC WDT expiration event. DS1501 on-chip WDT can generate WDT expiration event within 0.01..99.99 sec time interval with resolution 0.01 sec, which is important for DSP applications with reduced system restore latency.

DS1501 RTC on-chip WDT is enabled by DSP application via WDE and WDS bits of *RTC_CNTRB_RG* RTC on-chip control register. These bits default to the '0' state of power-on condition and disable RTC on-chip WDT. In order to configure WDT to activate DSP reset on WDT expiration event, bits WDE and WDS shall be both set to the '1' state. Refer to DS1501 user's guide for more details.

External power supply control

TORNADO-E2/6xxx supports remote control of external power supply control in order to perform system wakeup at programmable time instant and/or on kickstart condition. These features are provided via on-board DS1501 RTC controller ([Figure J-1](#)). External power supply used must support remote control and provide compatible I/O interface.

TORNADO-E2/6xxx on-board JP16 connector ([Figure A-1](#) and [Figure A-8](#)) is used to control external power supply via *RTC_PWR_ON_OUT* active low open drain output signal and *RTC_KS_IN* active low input signal.

RTC_PWR_ON_OUT output is typically used to drive internal opto-relay inside external power supply and actually enables/disable main power input to external power supply. This output can sink 0.5A and provides 20V maximum applied voltage. As an option, *RTC_PULLUP_VCC* pull-up resistor output at JP16 connector can be used to provide +3V@30mA power from *TORNADO-E2/6xxx* on-board battery to activate opto-relay of external power supply. In this case, caution must be taken to exclude continuous power-on fault of external power supply in order to exclude discharge of backup battery.

RTC_PWR_ON_OUT output is controlled via PAB bit of *RTC_CNTRA_RG* RTC on-chip control register and via TPE bit of *RTC_CNTRB_RG* RTC on-chip control register. Refer to DS1501 user's guide for more details.

Read-only *RTC_XPS_EN* bit of [DSP_WDT_RTC_CNTR_RG](#) DSP external control register (refer to [Table 2-18](#)) shall be used by DSP application to read current state of *RTC_PWR_ON_OUT* output signal at JP16 connector.

RTC_KS_IN input is optional and normally connects to external kickstart switch, which is used to manually activate external power supply on kickstart condition. Refer to DS1501 user's guide for more details.

Glossary of Terms

This Glossary contains definition for terms and other synchronisms used along in this user's guide.

A

ASIOX

Audio Serial I/O eXpansion DCM site interface, which is used to install compatible DCM. *TORNADO-E2/6713* provides one ASIOX rev.D. Refer to [Appendix C](#) for more details.

ASIO-0, ASIO-1

Audio serial ports of *TORNADO-E2/6713* ASIOX rev.D DCM site interface. Refer to [Appendix C](#) for more details.

B

C

D

DCM

Daughter-card module. *TORNADO-E2/6xxx* provide several on-board DCM sites for optional I/O expansion using compatible DCMs.

DSP

On-board TI TMS320C6xxx Digital Signal Processor.

DSP bootmode

Bootmode configuration for *TORNADO-E2/6xxx* on-board DSP. Refer to subsection “[DSP operation modes and DSP bootmodes](#)” and [Table 2-1](#) for more details.

DSP operation modes

Either *DSP stand-alone operation mode* or *DSP host operation mode* for *TORNADO-E2/6xxx* on-board DSP. Refer to subsection “[DSP operation modes and DSP bootmodes](#)” and [Table 2-1](#) for more details.

DSP external control registers

On-board control registers, which are implemented in FPGA and are mapped into DSP external memory space. Refer to section “[DSP external control registers area](#)” for more details.

DSP_DCM_CNF_RG

Read-only DSP external control register, which is used to identify the installed DCMs from DSP application. Refer to subsection “[DSP_DCM_CNF_RG DSP external control register for identification of installed DCM](#)” for more details.

DSP_DCM_RESET_RG

DSP external control register, which is used to generate individual reset signals for on-board SIOX/ASIOX and PIOX2 DCM sites. Refer to subsection “[DSP_DCM_RESET_RG DSP external control register for reset control of PIOX2/SIOX/ASIOX DCM sites](#)”, [Appendix C](#) and [Appendix D](#) for more details.

DSP_DSP_CNF_RG

Read-only DSP external control register, which is used to identify the DSP bootmode configuration, DSP operation mode and HPI enable status of *TORNADO-E2/6xxx* DSP controller from DSP application. Refer to subsection [“DSP_DSP_CNF_RG DSP external control register for identification of the DSP start-up configuration”](#) for more details.

DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG, DSP_EXT_INT7_SEL_RG

DSP external control registers, which are used to select interrupt request source for DSP EXT_INT4..7 external interrupt request inputs correspondingly. Refer to subsections [“DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG, DSP_EXT_INT7_SEL_RG and DSP_NMI_SEL_RG DSP external control registers for selection of interrupt request source for DSP_EXT_INT4..7 and NMI external interrupt requests”](#) and [“DSP external interrupt requests”](#) for more details.

DSP_FLASH_PAGE_RG

DSP external control register, which is used to select accessed FLASH memory page for 8Mx8 or 64Mx8 FLASH memories. Refer to subsections [“DSP_FLASH_PAGE_RG DSP external FLASH memory page control register”](#) and [“FLASH memory area”](#) for more details.

DSP_FLASH_CNTR_RG

DSP external control register, which is used to control write protection feature for on-board FLASH memory. Refer to subsections [“DSP_FLASH_CNTR_RG DSP external FLASH memory control register”](#) and [“FLASH memory area”](#) for more details.

DSP_GPIO_DIR_RG, DSP_GPIO_DATA_RG

DSP external control registers, which are used for direction and data control for external general purpose I/O (GPIO) pins. Refer to subsections [“DSP_GPIO_DIR_RG and DSP_GPIO_DATA_RG DSP external control registers for GPIO pins”](#) and [“External General Purpose I/O \(GPIO\)”](#) for more details.

DSP_HCX_SYNC_PAGE_RG

DSP external control register, which is used to set memory page accessed via *HCX-SYNC* interface. Refer to subsections [“DSP_HCX_SYNC_PAGE_RG DSP external control register for address extension of synchronous HCX DCM site interface”](#) and [“HCX-SYNC synchronous section of HCX DCM site interface”](#) for more details.

DSP_NMI_SEL_RG

DSP external control register, which is used to select interrupt request source for DSP NMI external interrupt request input. Refer to subsections [“DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG, DSP_EXT_INT7_SEL_RG and DSP_NMI_SEL_RG DSP external control registers for selection of interrupt request source for DSP_EXT_INT4..7 and NMI external interrupt requests”](#) and [“DSP external interrupt requests”](#) for more details.

DSP_PORTS_CNTR_RG

DSP external control register, which is used for general configuration of *TORNADO-E2/6xxx* on-board McBSP-0/1, McASP-0/1, I²C-1 serial ports buffers. Refer to subsections [“DSP_PORTS_CNTR_RG DSP external control register for on-board serial ports buffers configuration”](#), [“DSP on-chip serial peripherals \(McBSP, McASP, I2C ports\)”](#) and [Appendix C](#) for more details.

DSP_SIOX_XIO_CNF_RG, DSP_SIOX_XIO_DATA_RG

DSP external control registers, which are used for direction and data control of legacy *SIOX* rev.B I/O pins (*SIOX_TM/XIO-0/1*). Refer to subsections [“DSP_SIOX_XIO_CNF_RG and DSP_SIOX_XIO_DATA_RG DSP external control registers for configuring DSP Timers/XIO pins”](#), [“DSP on-chip timers”](#) and [Appendix C](#) for more details.

DSP_SYS_CNF1_RG

Read-only DSP external control register, which is used to identify type of *TORNADO-E2/6xxx* DSP controller. Refer to subsection “[DSP_SYS_CNF1_RG DSP external control register for identification of TORNADO-E2/6xxx DSP controller](#)” for more details.

DSP_SYS_CNF2_RG

Read-only DSP external control register, which is used to read board revision ID, to identify DSP clock frequency and presence of *SSCLK* clock option. Refer to subsection “[DSP_SYS_CNF2_RG DSP external control register for identification of board revision, DSP clock frequency and EMIF spread spectrum clock presence](#)” for more details.

DSP_SYS_CNF3_RG

Read-only DSP external control register, which is used to identify length of on-board SBSRAM, SDRAM and FLASH memories. Refer to subsection “[DSP_SYS_CNF3_RG DSP external control register for identification of on-board external DSP memories](#)” for more details.

DSP_SYS_CNF4_RG

Read-only DSP external control register, which is used to identify on-board parallel peripherals (USB, RTC controllers). Refer to subsection “[DSP_SYS_CNF4_RG DSP external control register for identification of on-board external parallel peripherals](#)” for more details.

DSP_WDT_RTC_CNTR_RG, DSP_WDT_RESET_RG

DSP external control registers, which are used to enable WDT feature (i.e. automatic DSP reset on WDT expiration event), to enable access to on-board RTC controller and to reset on-board watch-dog timer (WDT). Refer to subsections “[DSP_WDT_RTC_CNTR_RG DSP external control register for WDT and RTC control](#)”, “[On-board watch-dog timer \(WDT\)](#)” and [Appendix J](#) for more details.

DSPINT

Host-to-DSP interrupt request via TMS320C6xxx DSP on-chip HPI port, which appears as the *DSPINT* bit of TMS320C6xxx DSP on-chip HPIC register. Refer to subsection “[Generation of Host-to-DSP interrupt request via HCX-ASYNC interface](#)” for more details.

DUART

Dual-channel universal asynchronous receiver/transmitter comprising the channels UART-A and UART-B. The RS232C compatible I/O control signal for on-board UART-A and UART-B controllers are available via on-board JP8 and JP9 connectors. Refer to subsection “[Dual-channel UART](#)” and [Appendix H](#) for more details.

E**EMIF**

TMS320C6xxxx DSP external memory interface, which is used to connect to on-board SDRAM, SDRAM, FLASH memories, parallel peripherals, DCM sites interfaces and DSP external control registers. Refer to section “[TMS320C6xxx DSP Environment](#)” and to TI TMS320C6xxx documentation for more details.

EXT_INT4..EXT_INT7

TMS320C6xxx DSP external interrupt request inputs, which are used for generation the DSP interrupts via *DSP_EXT_INT4_SEL_RG..DSP_EXT_INT7_SEL_RG* interrupt selector registers. Refer to subsections “[DSP_EXT_INT4_SEL_RG, DSP_EXT_INT5_SEL_RG, DSP_EXT_INT6_SEL_RG, DSP_EXT_INT7_SEL_RG and DSP_NMI_SEL_RG DSP external control registers for selection of interrupt request source for DSP_EXT_INT4..7 and NMI external interrupt requests](#)” and “[DSP external interrupt requests](#)” for more details.

F

FLASH

TORNADO-E2/6xxx on-board non-volatile FLASH memory, which is local for on-board TMS320C6xxx DSP and which is used to keep non-volatile data and DSP start-up code. Refer to subsection “[FLASH memory area](#)” for more details.

G

GPIO

General purpose I/O pins (*GPIO-0..7*), which are available via on-board JP13 connector. Refer to subsection “[External General Purpose I/O \(GPIO\)](#)” for more details.

H

HCX

Host Control eXpansion DCM site interface, which is used to install compatible host *HCX* DCM. *TORNADO-E2/6713* provides one *HCX* rev.A DCM site. Refer to section “[HCX DCM Site Interface](#)” and [Appendix E](#) for more details.

HINT

DSP-to-host interrupt request via TMS320C6xxx DSP on-chip HPI port, which appears as the *HINT* bit of TMS320C6xxx DSP on-chip HPIC register. Refer to subsection “[Processing of DSP-to-host interrupt request via HCX-ASYNC interface](#)” for more details.

HCX_AX_CLR_HPI_TMOUT_RG

Write-only *HCX* control register, which is used to clear timeout error flag for host-to-HPI access cycles. Refer to subsections “[HCX AX CLR HPI TMOUT ERR RG write-only HCX control register for clearing of HPI access timeout error flag](#)” and “[Timeout control for access to DSP on-chip HPI port of HCX-ASYNC interface](#)” for more details.

HCX_AX_CNTR1_RG

HCX control register, which is used to control DSP reset signal. Refer to subsection “[HCX AX CNTR1 RG HCX control register for DSP reset control](#)” for more details.

HCX_AX_CNTR2_RG

HCX control register, which is used to read-back DSP operation mode, to set DSP bootmode, to set DSP FLASH write protection bits, enable DSP HPI port and to enable timeout control for host-to-HPI access cycles. Refer to subsection “[HCX AX CNTR2 RG HCX control register for DSP start-up configuration control](#)” for more details.

HCX_AX_HIRQ0_SEL_RG, HCX_AX_HIRQ1_SEL_RG, HCX_AX_HIRQ2_SEL_RG, HCX_AX_HIRQ3_SEL_RG

HCX control registers, which are used to configure DSP-to-host interrupt selectors. Refer to subsections “[HCX AX HIRQ0 SEL RG and HCX AX HIRQ1 SEL RG registers for configuration of 32-bit asynchronous HCX DCM site interface interrupt request outputs](#)” and “[DSP-to-Host interrupt requests via HCX-ASYNC interface](#)” for more details.

HCX_AX_DSP_HPIC_LSW_RG, HCX_AX_DSP_HPIC_MSW_RG, HCX_AX_DSP_HPIA_LSW_RG, HCX_AX_DSP_HPIA_MSW_RG, HCX_AX_DSP_HPID_LSW_RG, HCX_AX_DSP_HPID_MSW_RG, HCX_AX_DSP_HPID_AINC_LSW_RG, HCX_AX_DSP_HPID_AINC_MSW_RG

DSP on-chip 16-bit HPI port registers. Refer to subsection “[DSP on-chip HPI port area of HCX-ASYNC interface](#)” for more details.

HCX_AX_INT_STAT_RG

Read-only *HCX* control register, which is used to read status of *HCX* interrupt request source flags. Refer to subsections “[HCX_AX_INT_STAT_RG read-only HCX control register for status information of DSP-to-Host interrupt request sources](#)” and “[DSP-to-Host interrupt requests via HCX-ASYNC interface](#)” for more details.

HCX_AX_SYS_CNF1_RG, HCX_AX_SYS_CNF2_RG, HCX_AX_SYS_CNF3_RG

Read-only *HCX* control registers, which are used to identify type of *TORNADO-E2/6xxx* DSP controller, to read board revision ID, to identify the DSP clock frequency, identify presence of *SSCLK*, and to identify length of on-board *SBSRAM*, *SDRAM* and *FLASH* memories. Refer to subsection “[HCX_AX_SYS_CNF1_RG, HCX_AX_SYS_CNF2_RG, and HCX_AX_SYS_CNF3_RG read-only HCX control registers for board configuration information](#)” for more details.

HPI

TMS320C6xxx DSP on-chip host port interface, which is used to access DSP environment from host *HCX* application. Refer to subsection “[DSP on-chip HPI port area of HCX-ASYNC interface](#)” for more details.

HPI access timeout error flag

Error flag, which is set in case of timeout condition for host-to-HPI access cycles. HPI access timeout flag can be read via *DSP_HPI_ERR* bit of *HCX_AX_INT_STAT_RG* read-only *HCX* control register. Refer to subsections “[HCX_AX_INT_STAT_RG read-only HCX control register for status information of DSP-to-Host interrupt request sources](#)” and “[DSP-to-Host interrupt requests via HCX-ASYNC interface](#)” for more details.

I

I²C

Inter-Integrated Circuit Bus serial ports. *TMS320C6713* DSP provides two on-chip *I²C* serial ports which are available via on-board *JP14* and *JP15* connectors. Refer to subsection “[DSP on-chip serial peripherals \(McBSP, McASP, I²C ports\)](#)” for more details.

J

JTAG

Joint Test Action Group interface, which is a part of the *TMS320C2xx/VC33/C4x/C5x/C54xx/C55xx/C6xxx/C8x* DSP silicon, and is used to debug on-board *TMS320C6xxx* DSP application using external JTAG emulator (*TI XDS* and *MicroLAB Systems MIRAGE*). Refer to section “[DSP Software Development Tools](#)” for more details.

K

L

LED

Light emitting diode indicator. Refer to [Appendix A](#) for more details.

M

McASP

TMS320C6713 DSP on-chip multichannel audio serial ports, which are optimized for the needs of multichannel audio applications. McASP ports are available via *ASIOX* rev.D DCM site. Refer to subsection “[DSP on-chip serial peripherals \(McBSP, McASP, I2C ports\)](#)” and [Appendix C](#) for more details.

McBSP

TMS320C6xxx DSP on-chip multichannel serial ports, which are standard serial ports used on TMS320C6xxx DSP. McBSP ports are available via *SIOX* rev.B and *ASIOX* rev.D DCM sites. Refer to subsection “[DSP on-chip serial peripherals \(McBSP, McASP, I2C ports\)](#)” and [Appendix C](#) for more details.

N

NMI

TMS320C6xxx DSP external non-maskable interrupt request input, which are used for generation the DSP non-maskable interrupt via *DSP_NMI_SEL_RG* interrupt selector register. Refer to subsections “[DSP_EXT_INT4_SEL_RG](#), [DSP_EXT_INT5_SEL_RG](#), [DSP_EXT_INT6_SEL_RG](#), [DSP_EXT_INT7_SEL_RG](#) and [DSP_NMI_SEL_RG DSP external control registers for selection of interrupt request source for DSP_EXT_INT4..7 and NMI external interrupt requests](#)” and “[DSP external interrupt requests](#)” for more details.

O

P

PIOX

Legacy 1st generation either 16-bit or 32-bit Parallel I/O eXpansion DCM site interface for compatible DCM, which was available at *TORNADO-E* controllers and 1st *TORNADO* DSP systems for ISA/PCI-bus. Not available at *TORNADO-E2/6xxx* DSP controllers. *PIOX2* to *PIOX* converter boards (*T/X-PXA/PX2A1* and *T/X-PXA/PX2A2*) shall be used to install *PIOX* DCMs onto *TORNADO-E2/6xxx* boards.

PIOX2

2nd generation Parallel I/O eXpansion DCM site interface, which is used to install compatible DCM. *TORNADO-E2/6713* DSP controller provides one *PIOX2* DCM site. Refer to [Appendix D](#) for more details.

Pod

External pod, which is used to connect external JTAG emulator to *TORNADO-E2/6xxx* on-board JTAG connector for debug purposes. Refer to section “[DSP Software Development Tools](#)” for more details.

Q

R

RS232C

External I/O signal interfaces for on-board UART-A and UART-B, which are available via on-board JP8 and JP9 connectors. Refer to subsection “[Dual-channel UART](#)” and [Appendix H](#) for more details.

RTC

TORNADO-E2/6xxx on-board real-time clock controller. Refer to subsection “[Real-time clock \(RTC\) controller](#)” and [Appendix J](#) for more details.

S**SBSRAM**

TORNADO-E2/6xxx on-board synchronous static burst RAM (SBSRAM), which is local for on-board TMS320C6xxx DSP. Refer to subsection for “[Synchronous burst static RAM \(SBSRAM\) memory area](#)” more details.

SCU

On-board system controller unit, which is implemented using FPGA chip.

SDRAM

TORNADO-E2/6xxx on-board synchronous dynamic RAM, which is local for on-board TMS320C6xxx DSP and which is used to store large run-time data arrays. Refer to subsection “[Synchronous dynamic RAM \(SDRAM\) memory area](#)” for more details.

SIO-0, SIO-1

Serial ports of legacy *SIOX* rev.B DCM site interface, which are connected to the corresponding DSP on-chip serial ports. Refer to [Appendix C](#) for more details.

SIOX rev.B

Serial I/O eXpansion DCM rev.B site interface, which is used to install compatible DCM. *TORNADO-E2/6713* DSP controller provides one *SIOX* rev.B DCM site. Refer to [Appendix C](#) for more details.

T**T/X-JTAG/C1**

A connection cable, which is used to connect *TORNADO-E2/6xxx* DSP controllers on-board JTAG connector to external JTAG emulator. Refer to section “[DSP Software Development Tools](#)” and [Appendix B](#) for more details.

TM/XIO

DSP Timer/IO pins of *SIOX* rev.B DCM site interface. Refer to subsection “[DSP on-chip timers](#)” and [Appendix C](#) for more details.

U**UART-A, UART-B**

Channels #A and #B of dual-channel universal asynchronous receiver/transmitter (DUART).. Refer to subsection “[Dual-channel UART](#)” and [Appendix H](#) for more details.

USB

Universal serial bus interface. *TORNADO-E2/6xxx* provide different USB interface controller options. Refer to subsection “[USB interface](#)” and [Appendix I](#) for more details.

V

W

WDT

Watch-dog timer, which is used to reset (restart) DSP in case of the DSP application stall. WDT is enabled in the *DSP stand-alone operation mode* only. Refer to subsection “[On-board watch-dog timer \(WDT\)](#)” for more details.

X

Y

Z

Index

This Index contains a list of subject specific keywords and their important references in this user's guide.

A

ASIOX, [3](#), [11](#), [42](#), [54](#), [89](#)
connector, [92](#)

D

DCM, [2](#), [3](#)
DSP, [10](#), [12](#), [40](#), [43](#), [63](#), [64](#)
bootmodes, [13](#), [15](#), [64](#)
external interrupt requests, [38](#), [46](#)
on-chip timers, [31](#), [55](#), [97](#)
operation modes, [12](#)
DSP_DCM_CNF_RG, [41](#)
DSP_DCM_RESET_RG, [54](#)
DSP_DSP_CNF_RG, [40](#)
DSP_EXT_INT4_SEL_RG, [46](#)
DSP_EXT_INT5_SEL_RG, [46](#)
DSP_EXT_INT6_SEL_RG, [46](#)
DSP_EXT_INT7_SEL_RG, [46](#)
DSP_FLASH_CNTR_RG, [50](#), [52](#)
DSP_FLASH_PAGE_RG, [49](#), [50](#)
DSP_GPIO_DATA_RG, [53](#)
DSP_GPIO_DIR_RG, [53](#)
DSP_HCX_SYNC_PAGE_RG, [56](#)
DSP_NMI_SEL_RG, [46](#)
DSP_PORTS_CNTR_RG, [48](#)
DSP_SIOX_XIO_CNF_RG, [55](#), [56](#)
DSP_SIOX_XIO_DATA_RG, [55](#)
DSP_SYS_CNF1_RG, [42](#)
DSP_SYS_CNF2_RG, [43](#)
DSP_SYS_CNF3_RG, [44](#)
DSP_SYS_CNF4_RG, [45](#)
DSP_WDT_RESET_RG, [31](#), [40](#), [53](#)
DSP_WDT_RTC_CNTR_RG, [52](#)
DUART, [10](#), [29](#), [129](#)

F

FLASH, [10](#), [25](#), [44](#), [115](#)

G

GPIO, [10](#), [37](#), [53](#), [83](#)

H

HCX, [3](#), [11](#), [29](#), [42](#), [56](#), [57](#), [111](#)
HCX_AX_CLR_HPI_TMOUT_RG, [71](#)
HCX_AX_CNTR1_RG, [63](#)
HCX_AX_CNTR2_RG, [64](#)
HCX_AX_HIRQ0_SEL_RG, [67](#)
HCX_AX_HIRQ1_SEL_RG, [67](#)
HCX_AX_HIRQ2_SEL_RG, [67](#)
HCX_AX_HIRQ3_SEL_RG, [67](#)
HCX_AX_INT_STAT_RG, [67](#)
HCX_AX_SYS_CNF1_RG, [61](#)
HCX_AX_SYS_CNF2_RG, [61](#)
HCX_AX_SYS_CNF3_RG, [61](#)

I

I2C, [10](#), [32](#), [48](#)

J

JTAG, [73](#), [82](#), [87](#)

M

McASP, [32](#), [48](#)
McBSP, [32](#), [48](#)

P

PIOX2, [3](#), [11](#), [29](#), [42](#), [54](#), [101](#)
connector, [103](#)

R

RTC, [11](#), [30](#), [45](#), [52](#), [143](#)

S

SBSRAM, [10](#), [23](#), [44](#)
SCU, [12](#)
SDRAM, [10](#), [24](#), [44](#)
SIOX, [3](#), [11](#), [54](#), [55](#), [89](#)
connector, [90](#)

U

USB, [10](#), [30](#), [45](#), [133](#)

W

WDT, [11](#), [31](#), [52](#)