MicroLAB Systems

Ultimate DSP Development Solutions

DIGITAL SIGNAL PROCESSING

T/SDAS-DDC1

Digital Radio Receiver SIOX Daughter-card Module
for *TORNADO* DSP Systems, Controllers and Coprocessors

User's Guide

covers:
T/SDAS-DDC1 rev.2D/2E/2F

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About this Document

This user's guide contains description for *T/SDAS-DDC1* single-channel digital radio receiver (DRR) SIOX daughter-card DCM (DCM) for *TORNADO* DSP systems/controllers/coprocessors from MicroLAB Systems Ltd.

This document does not include detail description neither for *TORNADO* systems, nor for TI DSP and on-board components. To get the corresponding information please refer to the following documentation:

1. ***HSP50214 Programmable Down Converter.*** Intersil Inc, 1999.
2. ***TL16C450 UART.*** Texas Instruments Inc, 1989.

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Chapter 1. Introduction

This chapter contains general description for *T/SDAS-DDC1* SIOX DCM for *TORNADO* DSP systems/controllers/coprocessors.

1.1 General Information

T/SDAS-DDC1 is a single-channel digital radio receiver SIOX (serial I/O expansion) DCM (fig.1-1) for *TORNADO* DSP systems, *TORNADO-E* stand-alone DSP controllers and *TORNADO-PX/SX* DSP coprocessors from MicroLAB Systems Ltd.

T/SDAS-DDC1 DCM has been designed for high-frequency digital radio receiver (DRR) telecom applications, however it can be used for many other applications with similar signal processing algorithm.

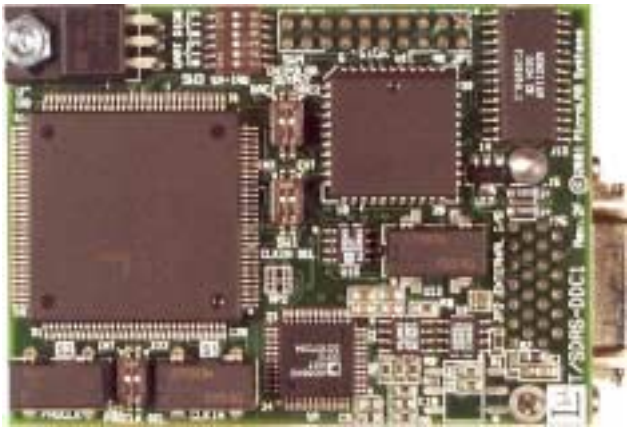


Fig. 1-1. T/SDAS-DDC1 DCM.

Installation

T/SDAS-DDC1 DCM installs as SIOX DCM (fig.1-2) into the SIOX site onto *TORNADO* DSP mainboard. If required, the *T/SU-X* SIOX extender can be used for remote connection to SIOX interface of *TORNADO* mainboard.

Fig. 1-2. T/SDAS-DDC1 DCM installed onto *TORNADO-54x* mainboard.

Overview

T/SDAS-DDC1 DCM provides single-channel DRR facility and features:

- 12-bit 65 MSPS ADC
- 65 MSPS programmable down converter (PDC)
- programmable peripherals
- control unit.

On-board ADC features 12-bit resolution at 65 MHz sampling frequency and excellent linearity, which guarantee minimum signal distortion during RF signal sampling. Input analog circuit and ADC also allows undersampling of RF input signal. Input analog circuit can be factory installed as either RF amplifier (default for all RF applications), or balanced RF transformer (recommended for high-frequency RF applications with low signal distortion).

The ADC output stream is routed to Intersil HSP50214 programmable down converter (PDC), which is the 'heart' of *T/SDAS-DDC1* DCM. Intersil HSP50214 PDC is extremely flexible telecom oriented PDC chip, which provides high-resolution tuning and mixing of input digital stream with further decimation, filtering, resampling and demodulation of. The PDC serial output might be software configured to comprise of different output data and is directly routed to the SIO-0 serial port of host SIOX site for direct routing to the DSP serial port of host *TORNADO* DSP system/controller/coprocessor. The ADC/PDC sampling frequency can be user modified by replacing the on-board sampling frequency generator, which is plugged to on-board socket.

T/SDAS-DDC1 DCM also contains a set of on-board peripherals, which are required for design a complete single-channel programmable DRR system with a minimum of external components. On-board peripherals comprise of UART with RS232C interface for external tuner/peripheral control, two 12-bit DACs for analog gain control of external RF amplifier and connection to phones, two external serial links for external gain control of external RF amplifier, and general purpose digital I/O.

External signal I/O

Connection of *T/SDAS-DDC1* DCM to external analog I/O world is performed via the on-board I/O JP2 connector, which is available via rear panel of host PC (if *T/SDAS-DDC1* DCM is installed onto *TORNADO* DSP system for PC).

External options

T/SDAS-DDC1 DCM provides several I/O options when connecting to external signal I/O equipment:

- *T/X-DDC1/C* external cable set, which comes standard with *T/SDAS-DDC1* DCM and provides separate industry standard connectors for RF analog input, analog outputs, RS232C interface and auxiliary I/O (refer to Appendix C for more details)
- *T/X-DDC/AFE-xx* external RF amplifier, which is optional for *T/SDAS-DDC1* DCM.

T/X-DDC1/C external cable set (Appendix C) comes standard with *T/SDAS-DDC1* DCM and provides direct connection to any external RF signal source, however this external signal source must match input signal range of *T/SDAS-DDC1* DCM. The RS232C interface I/O, dual-channel analog I/O and auxiliary I/O are also available via separate industry-standard connectors.

T/X-DDC/AFE-xx external RF amplifier (fig.1-3) is optional for *T/SDAS-DDC1* DCM and provides software programmable gain at particular RF signal bandwidth. *T/X-DDC/AFE-xx* option is useful in case external tuner provides small output RF output signal, which is a typical situation with the most industry standard tuners. *T/X-DDC/AFE-xx* option is available with different bandwidth and gain parameters, and it is also possible to customize the bandwidth and gain parameters of this option in order to meet requirements of customer application. The RS232C interface I/O, analog output and auxiliary I/O are available on separate connectors at the *T/X-DDC/AFE-xx* device package.

Fig. 1-3. T/SDAS-DDC1 DCM with *T/X-DDC/AFE-xx* external RF amplifier.

Applications

T/SDAS-DDC1 DCM has been designed for high-frequency digital radio receiver (DRR) telecommunication applications as well as for other general signal processing applications, which assume similar signal processing and demodulation technique within similar signal bandwidth.

1.2 Technical Specifications

The following are technical specifications for *T/SDAS-DDC1* DCM for temperature of external environment +25°C.

parameter description	*parameter value*
Analog input circuit and ADC	
input signal range	± (1 VAC ± 80 mVAC)
input impedance for analog input	50 Ohm
resolution	12 bits
input signal bandwidth	with input RF amplifier circuit: 5 kHz .. 220 MHz with input balance RF transformer circuit: 70 kHz .. 280 MHz
SNR (Fs=31MHz)	with input RF amplifier circuit: 63 dB (typ) with input balance RF transformer circuit: 67 dB (typ)
sampling frequency (Fs)	5..65 MHz
input DC bias	± 30 VDC max
PDC	
PDC type	Intersil HSP50214 PDC
maximum Fs/CLKIN sampling frequency	65 MHz (factory default as 60MHz)
maximum PROCLK frequency	55 MHz (factory default as 50MHz)

user supplied Fs/CLKIN and PROCLK plug-in oscillator chips, which can be installed into on0board S1 and S2 sockets	DIP-4 package (0.3”x0.3”) with +5v power supply (compatible with EPSON SG531 crystal oscillators)
input logical signal level for external XF frequency input (user selected as external Fs/CLKIN or PROCLK)	3v/5v TTL
input impedance for external XF frequency input (user selected as external Fs/CLKIN or PROCLK)	50 Ohm
decimation factor	4..16384
hardware demodulators	AM, FM, ASK, FSK ready for PM/PSK
output signal bandwidth	≤ 982 kHz

Analog outputs

number of DAC channels	2
resolution	12 bits
output signal range	0..4.096 V (DC output) ± 2 Vp-p (AC output)
minimum load resistance	≥ 600 Ohm
settling time	≤ 16 uS
Output high-pass filter cutoff for DAC/AC output mode	≤ 20 Hz

External Serial Link (XSL)

number of XSL channels	2
number of programmable output data bits	14, 22 or 30
Output serial clock features	programmable polarity programmable framing
Output signals level	3v/5v TTL @ 3.2mA

UART

UART chip	16C450/16C550 (PC COM-port compatible)
external I/O interface	RS232C
maximum communication speed	115 kBaud

External Digital I/O

number of programmable digital I/O bits	2 bits
I/O signal level	3v/5v TTL @3.2mA

Host SIOX Interface

number of bits in data packet via SIO-port	16/24/32 bits
serial clock frequency for transmitter of host SIO-port	15 MHz
SIOX logical I/O signal level	3v/5v TTL

physical and power:

Dimensions	55mm (2.14") x 77mm (3") (full size SIOX rev.B DCM)
Power consumption via host SIOX I/F	+5v @ 500mA +12v @ 250mA -12v @ 60 mA

Chapter 2. Technical Description

This chapter contains detail technical description for architecture and construction of *T/SDAS-DDC1* SIOX DCM.

2.1 Block Diagram

Basic configuration and connectivity of *T/SDAS-DDC1* DCM is presented at fig.2-1.

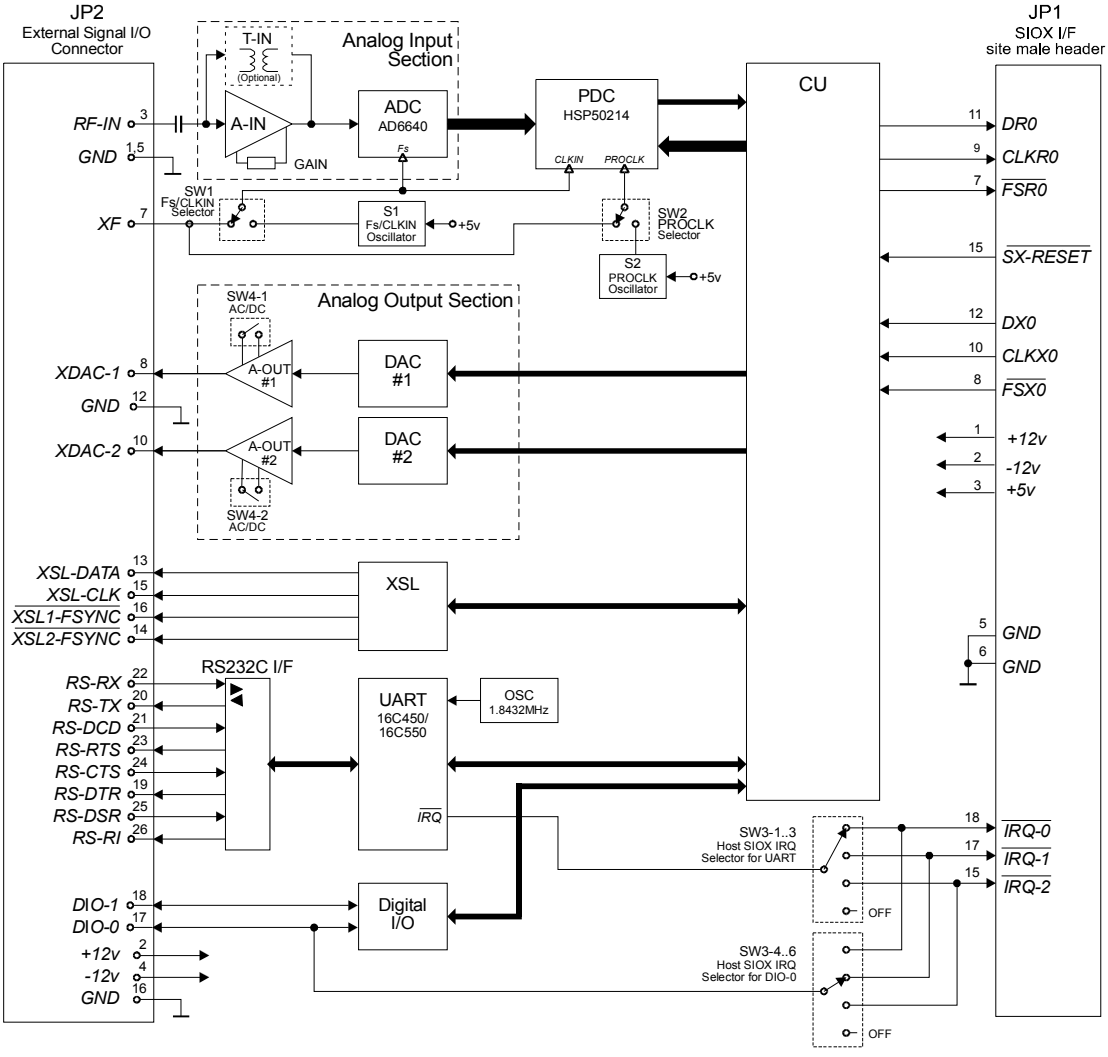


Fig. 2-1. Block diagram of *T/SDAS-DDC1* DCM.

T/SDAS-DDC1 DCM installs into a SIOX site onto *TORNADO* mainboard and assumes that communication with *TORNADO* on-board DSP is provided via the DSP on-chip serial port.

T/SDAS-DDC1 DCM comprises of the following components:

- analog input section, which contains 12-bit 65 Msps ADCs and either input RF amplifier (A-IN) or input RF transformer (T-IN)
- Intersil HSP50214 programmable down-converter (PDC) chip
- ADC/PDC sampling frequency (Fs/CLKIN) selector (SW1)
- PDC PROCLK frequency selector (SW2)
- S1 and S2 on-board sockets for Fs/CLKIN and PDC PROCLK oscillators
- analog output section, which comprises of two 12-bit 60 ksps DAC for analog gain control of external RF amplifier, connection to phones or general purpose analog output
- two programmable external serial output links (XSL-1/2) for digital gain control of external RF amplifier, or general purpose serial output
- 115 kBaud UART with RS232C interface for external tuner control or communication with general purpose external peripherals using industry standard asynchronous serial protocol
- 2-bit general purpose digital I/O (DIO)
- external signal I/O connector (JP2)
- synchronization and control unit (CU)
- host SIOX interrupt request selector (switch SW3)
- host SIOX interface header (JP1) for installation onto *TORNADO* DSP systems.

analog input section

Analog input section of *T/SDAS-DDC1* DCM is designed for input RF analog signal acquisition and analog-to-digital conversion with further routing of ADC parallel output digital code to the PDC chip. Analog input section comprises of the following components:

- either input RF analog input amplifier (A-IN) or input RF transformer (T-IN), which are installed alternatively upon the customer specification
- high-speed 12-bit analog-to-digital converter (ADC).

CAUTION

T/SDAS-DDC1 DCM comes with either installed A-IN RF analog input amplifier (factory default), or with alternative T-IN RF input transformer (installed on customer request).

Default A-IN input analog buffer is used for interfacing to external low- and high-frequency general purpose RF signal source, and features 50 Ohm input impedance with input over-voltage protection at ±5.5 V signal level.

CAUTION

Input of A-IN amplifier is AC-coupled at the frequency higher than 5kHz (typical) in order to exclude conversion of any undesired external DC drift. AC coupling at the different frequency is available on request from MicroLAB Systems.

CAUTION

Default factory setting for the gain factor of A-IN input RF amplifier is 0dB. Different gain factor for A-IN input RF amplifier is available upon request from MicroLAB Systems.

Alternative T-IN balanced RF-input transformer is recommended for interfacing to external high-frequency RF signal source with low signal distortions, and features 50 Ohm input impedance with input over-voltage protection at ±5.5 V signal level. The gain factor of installed T-IN balance RF-input transformer is always 0dB and cannot be changed.

CAUTION

Input of T-IN transformer is AC-coupled at the frequency higher than 75kHz in order to exclude conversion of any undesired external DC drift. AC coupling at the higher frequency is available upon request from MicroLAB Systems.

The on-board 12-bit 65 Msps ADC is based on AD6640 chip from Analog Devices Inc, which features excellent linearity and high-accuracy at ultra-high conversion rates.

CAUTION

The output ADC stream is directly routed to the PDC inputs with the alignment at the most significant bit and four lower bits of PDC input being ‘zeroed’.

The analog input channel does not provide any low-pass filtering of RF input in order to allow undersampling of higher bandwidth signals.

PDC

On-board Intersil HSP50214 PDC chip is the ‘heart’ of *T/SDAS-DDC1* DCM and provides digital down conversion of high-bandwidth parallel ADC output stream to the low-band output serial stream, which can be further routed directly to the SIO-0 port of host *TORNADO* SIOX interface.

HSP50214 PDC chip is the industry most flexible and powerful 16-bit 65 Msps PDC chip, which is oriented for telecommunication applications. It features on-chip digital mixer/NCO, digital filters/decimators, resampler, automatic digital gain control, and output digital demodulator. It provides up to 16384 decimation factor, built-in AM/FM/ASK/FSK demodulator (ready for PH/PSK demodulation), and programmable serial output formatter in order to meet requirements of different telecommunication applications. The SEROUTA serial output of PDC can be routed to the received of SIO-0 port of host SIOX interface.

CAUTION

T/SDAS-DDC1 user's guide does not provide detail information about architecture and programming of Intersil HSP50214 PDC chip.

For more details about Intersil HSP50214 PDC chip refer to original datasheet, which is supplied in either electronic or paper form with this user's guide.

ADC/PDC sampling frequency selector

The Fs/CLKIN sampling frequency for the on-board ADC and PDC chips (also known as the CLKIN input clock for HSP50214 PDC chip) can be selected from any of the following sources:

- on-board sampling frequency (Fs/CLKIN) crystal oscillator, which is installed into the on-board S1 socket
- external XF frequency input via on-board JP2 connector.

Selection of particular clock source for ADC/PDC sampling frequency is performed by the on-board SW1 switch (refer to fig.2-1 and A-1) in accordance with table 2-1.

Table 2-1. ADC/PDC sampling frequency (Fs/CLKIN) selector.

SW1 switch		**description**
SW1-1	**SW1-2**	
ON	*OFF*	ADC/PDC sampling frequency (Fs/CLKIN) is sourced from on-board Fs/CLKIN oscillator, which is installed into S1 socket.
OFF	*ON*	ADC/PDC sampling frequency (Fs/CLKIN) is sourced from external XF input via JP2 external I/O connector.

Notes:
1. Highlighted configuration corresponds to default factory setting.
2. Other not shown configurations are reserved and cannot be used.

CAUTION

Maximum Fs/CLKCIN sampling frequency value for on-board ADC and Intersil HSP50214 PDC is 65 MHz.

Default frequency value for installed Fs/CLKIN sampling frequency oscillator, which is installed into the on-board S1 socket, is 60 MHz.

Most of applications do not require to change default value of installed Fs/CLKIN sampling frequency oscillator due to flexible programmable design of HSP50214 PDC, which allows to program any desired NCO frequency and decimation factor. However, low-frequency applications may require reduced Fs/CLKIN sampling frequency value.

CAUTION

User can customize the sampling frequency for any particular application and can install any desired crystal oscillator with the frequency below 65MHz into the on-board S1 socket.

User supplied crystal oscillator must be in the DIP-4 (0.3”x0.3”) package with 5V power supply (similar to EPSON SG-531 series crystal oscillators). Call MicroLAB Systems for available plug-in crystal oscillators.

PDC PROCLK input clock selector

HSP50214 PDC chip requires PROCLK input clock in order to provide normal operation of serial output section.

PDC PROCLK input clock for on-board HSP50214 PDC chip can be selected from any of the following sources:

- on-board PDC PROCLK crystal oscillator, which is installed into the on-board S2 socket
- external XF frequency input via on-board JP2 connector.

Selection of particular clock source for PDC PROCLK input clock is performed by the on-board SW2 switch (refer to fig.2-1 and A-1) in accordance with table 2-2.

Table 2-2. PDC PROCLK input clock selector.

SW2 switch		description
SW2-1	**SW2-2**	
ON	*OFF*	PDC PROCLK input clock is sourced from on-board PROCLK oscillator, which is installed into S2 socket.
OFF	*ON*	ADC/PDC sampling frequency (Fs/CLKIN) is sourced from external XF input via JP2 external I/O connector.

Notes:
1. Highlighted configuration corresponds to default factory setting.
2. Other not shown configurations are reserved and cannot be used.

CAUTION

Maximum PROCLK clock frequency value for on-board Intersil HSP50214 PDC is 55 MHz.

Default frequency value for installed PROCLK oscillator, which is installed into the on-board S2 socket, is 50 MHz.

Most of applications do not require to change default value of installed Fs/CLKIN sampling frequency oscillator due to flexible programmable design of HSP50214 PDC. However, in case *T/SDAS-DDC1* DCM is used with low-performance DSP, then this may require different PDC PROCLK frequency.

CAUTION

User can customize PROCLK clock frequency value for any particular application and can install any crystal oscillator with the frequency below 55MHz into the on-board S2 socket.

User supplied crystal oscillator must be in the DIP-4 (0.3"x0.3") package with 5V power supply (similar to EPSON SG-531 series crystal oscillators).

analog output section

Analog output section of *T/SDAS-DDC1* DCM comprises of two identical D/A channels (#1 and #2), and is designed for conversion of digital code from serial transmitter of SIO-0 port of host SIOX interface of *TORNADO* DSP system into analog output signals (XDAC-1 and XDAC-2) for external gain control, phone output or general purpose analog output.

Each D/A channel of analog output section comprises of the following components:

- unipolar 12-bit digital-to-analog converter (DAC)
- output analog buffer with gain factor 0dB and user configurable AC coupling.

Each D/A channel of *T/SDAS-DDC1* DCM is based around 12-bit DAC with 16 uS settling time (60 ksps), which can be individually loaded by DSP of host *TORNADO* DSP system/controller via SIOX interface using *DAC-1_WR_CMND* and *DAC-2_WR_CMND* commands (refer to section "Software Control" later in this chapter). Both DAC provide unipolar 0 VDC .. 4.096 VDC output.

Analog output buffers are used for interfacing to external low-impedance loads and provide minimum signal distortions. Output buffers also provide optional AC coupling feature in order to remove DC component from the DAC output to the XDAC-1/2 analog output of the corresponding D/A channel. This feature is useful when connecting to external phones and similar analog equipment, which do not allow DC component. The AC coupling feature is performed by means of 1st-order high-pass filter with cut-off frequency about 20Hz.

The AC coupling feature of the output buffers can be enabled by the on-board SW4-1 switch for D/A-1 channel and SW4-2 switch for D/A-2 channel (refer to fig.2-1 and A-1) in accordance with tables 2-3 and 2-4.

Table 2-3. AC coupling for XDAC-1 analog output.

SW4-1 switch	**Description**
ON	XDAC-1 analog output is DC coupled and provides 0 VDC .. 4.096 VDC output signal range.
OFF	XDAC-1 analog output is AC coupled and provides 1.4 Vrms output signal range

Notes: 1. Highlighted configuration corresponds to default factory setting.

Table 2-4. AC coupling for XDAC-2 analog output.

SW4-2 switch	**Description**
ON	AOUT-2 analog output is DC coupled and provides 0 VDC .. 4.096 VDC output signal range.
OFF	AOUT-2 analog output is AC coupled and provides 1.4 Vrms output signal range

Notes: 1. Highlighted configuration corresponds to default factory setting.

External serial links (XSL)

Two external programmable serial links (XSL-1 and XSL-2) of *T/SDAS-DDC1* DCM are designed for either control of programmable digital gain of external RF amplifier or for general purpose serial data output. XSL feature programmable data format (14/22/30 data bits), programmable serial clock polarity, and programmable serial clock framing feature.

CAUTION

External serial links (XSL-1 and XSL-2) of *T/SDAS-DDC1* DCM share common serial clock (XSL-CLK) and serial data (XSL-DATA) pins at JP2 external I/O connector.

External hardware must recognize between transmissions over XSL-1 and XSL-2 by means of different frame synchronization pulses (XSL1-FSYNC and XSL2-FSYNC).

UART and RS232C interface

On-board UART (universal asynchronous receiver/transceiver) with RS232 external interface is designed for external digital RF tuner control or for interfacing to any general purpose external peripheral, which allows host control using the industry standard serial asynchronous protocol with RS232C interface. Most of the industry standard digital RF tuners (AOR, ICOM, etc), which can be used with the *T/SDAS-DDC1* DCM, provide RS232C input port for remote control.

On-board UART is the industry standard 16C450 (or 16C550) UART chip, which is hardware and software compatible with PC COM port, and provides up to 115 kBaud communication via RS232C interface. The UART is sourced by the 1.8432 MHz clock, which allows communication at all industry standard baud rates up to 115 kBaud.

CAUTION

T/SDAS-DDC1 user's guide does not provide detail information about architecture and programming of 16C450 and 16C550 UART chips.

For more details about 16C450 and 16C550 UART chips refer to the corresponding datasheet, which is enclosed in either electronic or paper form with this user's guide

UART can generate interrupt request to the DSP of host *TORNADO* DSP system/controller via IRQ-0..2 interrupt request inputs of SIOX interface. The particular interrupt request input of SIOX interface is selected via the on-board SW3-1..3 switches (refer to fig.2-1 and A-1) in accordance with table 2-5.

Table 2-5. SIOX interrupt line selector for UART output interrupt.

SW3-1..3 switch			description
SW3-1	**SW3-2**	**SW3-3**	
ON	*OFF*	*OFF*	UART interrupt request output is connected to the *IRQ-0* interrupt input of host SIOX interface.
OFF	*ON*	*OFF*	UART interrupt request output is connected to the *IRQ-1* interrupt input of host SIOX interface.
OFF	*OFF*	*ON*	UART interrupt request output is connected to the *IRQ-2* interrupt input of host SIOX interface.
OFF	*OFF*	*OFF*	UART interrupt request is not used.

Notes:
1. Highlighted configuration corresponds to default factory setting.
2. Other not shown configurations are reserved and cannot be used.

Programmable digital I/O

T/SDAS-DDC1 DCM provides 2-bit programmable digital I/O DIO-0/1, which are wired to the DIO-0 and DIO-1 pins of JP2 external I/O connector. DIO-0/1 I/O pins are 3v/5v TTL compatible and can be used as general purpose I/O with individual direction control for control and interfacing to external peripherals.

Direction and output data values for DIO-0/1 pins can be programmed via the *DIO_WR_CMND* command, whereas the read-back direction and data status are available via the *DIO_RD_CMND* command.

DIO-0 I/O pin can also generate interrupt request to the DSP of host *TORNADO* DSP system/controller via IRQ-0..2 interrupt request inputs of SIOX interface. The particular interrupt request input of SIOX interface is selected via the on-board SW3-4..6 switches (refer to fig.2-1 and A-1) in accordance with table 2-6.

CAUTION

SIOX interrupt request is generated on the falling edge of the DIO-0 I/O pin. Refer to documentation for your *TORNADO* DSP system/controller for more details.

Table 2-6. SIOX interrupt line selector for DIO-0 I/O pin.

SW3-4..6 switch			description
SW3-4	**SW3-5**	**SW3-6**	
ON	*OFF*	*OFF*	DIO-0 interrupt request is connected to the *IRQ-0* interrupt input of host SIOX interface.
OFF	*ON*	*OFF*	DIO-0 interrupt request is connected to the *IRQ-1* interrupt input of host SIOX interface.
OFF	*OFF*	*ON*	DIO-0 interrupt request is connected to the *IRQ-2* interrupt input of host SIOX interface.
OFF	*OFF*	*OFF*	DIO-0 interrupt request is not used.

Notes:
1. Highlighted configuration corresponds to default factory setting.
2. Other not shown configurations are reserved and cannot be used.

control unit (CU)

On-board Control Unit (CU) of *T/SDAS-DDC1* DCM decodes the incoming commands from the DSP of host *TORNADO* DSP system/controller, provides control of the on-board hardware and synchronization with SIOX SIO-0 port receiver/transmitter serial data streams.

receiver data output mode

Serial data, which is transmitted from *T/SDAS-DDC1* DCM to the receiver of SIO-0 port of host SIOX interface, can be originated from different sources:

- read-back data requested by the read commands (*UART_RD_CMND, PDC_RD_CMND,* etc), which is permitted in the receiver *RCV_AUX_DATA_MODE* data output mode only
- PDC real-time output data stream, which is permitted in the receiver *RCV_PDC_DATA_MODE* data output mode only.

CAUTION

In case the on-board Control Unit (CU) is configured in the *RCV_AUX_DATA_MODE* mode (which is also default mode on SIOX DCM reset condition), then UART, PDC, DIO and XSL data format are available for both read/write operations.

In case the on-board Control Unit (CU) is configured in the *RCV_PDC_DATA_MODE* mode, then UART, PDC, DIO and XSL data format are available for write-only operation. Although the UART and PDC read commands will be executed and the corresponding device will be actually read, these read-back data will be not available at the receiver of SIO-0 port of host SIOX interface in order to provide continuous PDC real-time output data stream..

Setting of particular receiver data output mode is performed by means of *SET_RCV_AUX_DATA_MODE_CMND* and *SET_RCV_PDC_DATA_MODE_CMND* software commands.

2.2 Software Control

T/SDAS-DDC1 DCM operation is controlled by host *TORNADO* DSP software using the set of commands transmitted via the DSP on-chip serial port transmitter, which is wired to the SIO-0 port of the corresponding SIOX interface site. The software command set for *T/SDAS-DDC1* DCM comprises of commands for write/read to DAC, UART, PDC, DIO and XSL.

Receiver of SIO-0 port of host SIOX interface is used either to receive PDC real-time output data stream (*RCV_PDC_DATA_MODE* receiver data mode), or to receive data from different on-board resources after receiving the corresponding read data command (*RCV_AUX_DATA_MODE* receiver data mode).

DAC write commands

On-board 12-bit DAC of D/A-1/2 analog output channels can be loaded using the following commands:

DAC-1_WR_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*0*	*0*	*0*	*DAC11*	*DAC10*	*DAC9*	*DAC8*	*DAC7*	*DAC6*	*DAC5*	*DAC4*	*DAC3*	*DAC2*	*DAC1*	*DAC0*

DAC-2_WR_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*0*	*0*	*1*	*DAC11*	*DAC10*	*DAC9*	*DAC8*	*DAC7*	*DAC6*	*DAC5*	*DAC4*	*DAC3*	*DAC2*	*DAC1*	*DAC0*

UART commands

The following commands perform write and read of 8-bit data to/from 16C450/16C550 UART in order to configure UART and to communicate with external peripherals:

UART_WR_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*0*	*1*	*0*	*1*	*A2*	*A1*	*A0*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*

Notes:
1. *A2..A0* denotes address of the UART register to be written to.
2. *D7..D0* denotes data to be written to the UART register.

UART_RD_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*0*	*1*	*0*	*0*	*A2*	*A1*	*A0*	*X*	*x*	*x*	*x*	*x*	*x*	*x*	*x*

Notes:
1. *A2..A0* denotes address of the UART register to be read from.

Format of UART read-back data, which is sent to the receiver of SIO-0 port during execution of *UART_RD_CMND* command is as the following:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	*x*	*x*	*x*	*x*	*x*	*x*	*x*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*

PDC configuration commands

The following commands provide write and read of 8-bit data to/from Intersil HSP50214 PDC in order to configure PDC:

PDC_WR_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*0*	*1*	*1*	*1*	*A2*	*A1*	*A0*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*

Notes:
1. *A2..A0* denotes address of the PDC register to be written to.
2. *D7..D0* denotes data to be written to the PDC register.

PDC_RD_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*0*	*1*	*1*	*0*	*A2*	*A1*	*A0*	*X*	*x*	*x*	*x*	*x*	*x*	*x*	*x*

Notes:
1. *A2..A0* denotes the address of the PDC register to be read from.

Format of PDC read-back data, which is sent to the receiver of SIO-0 port during execution of *PDC_RD_CMND* command is as the following:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	*x*	*x*	*x*	*x*	*x*	*x*	*x*	*D7*	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*

Digital I/O (DIO) commands

The following commands configure direction and write/read to the DIO-0/1 I/O facility:

DIO_WR_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*1*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*DIR-1*	*DIR-0*	*DIO-1*	*DIO-0*

Notes:
1. *DIR-0/1* denote direction of the corresponding DIO-0/1 I/O pin: 0 - input, 1 - output.
2. *DIO-0/1* denote data to be written to the DIO-0/1 outputs.

CAUTION

Default direction of the DIO-0/1 I/O pins, which is set on the SIOX DCM reset condition, is the 'input' direction, which corresponds to *DIR-0/1* bits equal to '0'.

DIO_RD_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*X*	*x*	*x*	*x*	*x*	*X*	*x*	*x*

Format of DIO read-back data, which is sent to the receiver of SIO-0 port during execution of *DIO_RD_CMND* command is as the following:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	*x*	*x*	*x*	*x*	*x*	*x*	*x*	*x*	*x*	*x*	*x*	*DIR-1*	*DIR-0*	*DIO-1*	*DIO-0*

Setting data format for the XSL write command

Data transmission over XSL-1 and XSL-2 serial links to external peripherals using XSL-1/2 write commands (*XSL1_WR_CMND* and *XSL2_WR_CMND*) can be performed with different data formats, serial clock polarity, and serial clock framing.

CAUTION

Both XSL-1 and XSL-2 external serial links of *T/SDAS-DDC1* DCM feature common data format, common serial clock polarity and common serial clock framing feature for data transmission over XSL-1 and XSL-2.

XSL data formats, serial clock polarity, and serial clock framing can be programmed using the *XSL_SET_FMT_CMND* command:

XSL_SET_FMT_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*1*	*0*	*0*	*1*	*0*	*0*	*1*	*0*	*0*	*0*	*0*	*XSL-CLK_FRM*	*XSL-CLK_POL*	*XSL-DF1*	*XSL-DF0*

The {*XSL-DF1,XSL-DF0*} bits of *XSL_SET_FMT_CMND* command define the data format (length in bits) of the XSL-0/1 write command (*XSL_WR_CMND*) as the following:

- {*XSL-DF1,XSL-DF0*} = {0,0} condition sets 16-bit data format for the XSL-0/1 write command, i.e. 14-bit actual XSL data transmission format. This data format is also set as default on the SIOX DCM reset condition.
- {*XSL-DF1,XSL-DF0*} = {0,1} condition sets 24-bit data format for the XSL-0/1 write command, i.e. 22-bit actual XSL data transmission format.
- {*XSL-DF1,XSL-DF0*} = {1,0} condition sets 32-bit data format for the XSL-0/1 write command, i.e. 30-bit actual XSL data transmission format.
- {*XSL-DF1,XSL-DF0*} = {1,1} condition is reserved and is not recommended for use.

The *XSL-CLK_POL* bit of *XSL_SET_FMT_CMND* command defines polarity of output XSL serial clock as the following:

- *XSL-CLK_POL* = 0 condition sets negative polarity of output XSL serial clock, i.e. data and frame sync pulse are updated on the falling edge of output XSL serial clock. This XSL output clock polarity is also the default value on the SIOX DCM reset condition.

- *XSL-CLK_POL* = 1 condition sets positive polarity of output XSL serial clock, i.e. data and frame sync pulse are updated on the rising edge of output XSL serial clock.

The *XSL-CLK_FRM* bit of *XSL_SET_FMT_CMND* command defines the framing feature for the output XSL serial clock as the following:

- *XSL-CLK_FRM* = 0 disables framing of output XSL serial clock, i.e. output XSL serial clock is continuous and is not effected by the XSL-1/2 frame synchronization pulses. This setting is also the default value on the SIOX DCM reset condition.
- *XSL-CLK_FRM* = 1 enables framing of output XSL serial clock, i.e. output XSL serial clock is enabled only during active XSL-1/2 frame synchronization pulses. This feature is useful in case XSL is used for gain control of external RF amplifier and it is desirable to reduce the digital noise.

CAUTION

In case the framing feature for XSL serial clock is enabled and the XSL serial clock polarity is set to active falling edge of XSL serial clock, then XSL serial clock defaults to the logical '0' value outside active XSL frame sync pulse.

In case the framing feature for XSL serial clock is enabled and the XSL serial clock polarity is set to active rising edge of XSL serial clock, then XSL serial clock defaults to the logical '1' value outside active XSL frame sync pulse.

For more details about timing diagram for transmission data over XSL-0/1 external serial links refer to the 'XSL Timing' section later in this chapter and figures 2-5 and 2-6.

In order to read-back current data format for the XSL-0/1 write commands, the following command can be used:

XSL_FMT_RD_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*1*	*0*	*0*	*0*	*0*	*0*	*1*	*X*	*x*	*x*	*x*	*x*	*x*	*x*	*x*

Format of read-back data, which is sent to the receiver of SIO-0 port during execution of *XSL_FMT_RD_CMND* command is as the following:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	*x*	*x*	*x*	*x*	*x*	*x*	*X*	*x*	*X*	*x*	*x*	*XSL-CLK_FRM*	*XSL-CLK_POL*	*XSL-DF1*	*XSL-DF0*

XSL-1/2 write commands

The following are the XSL-1/2 write data commands, which are used to initialize transmission over XSL-1/2. Note, that particular data format for the XSL-1/2 write command is set by *XSL_SET_FMT_CMND* command.

XSL1_WR_CMND command with 16-bit data format

D15	D14	D13..D0
1	*0*	*XSL-D13..XSL-D0*

XSL2_WR_CMND command with 16-bit data format

D15	D14	D13..D0
1	*1*	*XSL-D13..XSL-D0*

XSL1_WR_CMND command with 24-bit data format

D23	D22	D21..D0
1	*0*	*XSL-D21..XSL-D0*

XSL2_WR_CMND command with 24-bit data format

D23	D22	D21..D0
1	*1*	*XSL-D21..XSL-D0*

XSL1_WR_CMND command with 32-bit data format

D31	D30	D29..D0
1	*0*	*XSL-D29..XSL-D0*

XSL2_WR_CMND command with 32-bit data format

D31	D30	D29..D0
1	*1*	*XSL-D29..XSL-D0*

Setting receiver data mode

In order to set the receiver *RCV_AUX_DATA_MODE* or *RCV_PDC_DATA_MODE* the following commands shall be used:

SET_RCV_AUX_DATA_MODE_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*1*	*0*	*0*	*1*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*

SET_RCV_PDC_DATA_MODE_CMND command

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	*1*	*0*	*0*	*1*	*0*	*1*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*

2.3 Host SIOX Configuration

Transmitter of SIO-0 port of host SIOX interface is used to transmit software commands to *T/SDAS-DDC1* DCM, whereas the receiver of SIO-0 port of host SIOX interface is used either to receive PDC real-time output data stream in the *RCV_PDC_DATA_MODE* receiver data mode, or to receive read-back data during execution of read data command in the *RCV_AUX_DATA_MODE* receiver data mode.

SIOX SIO-0 port transmitter timing

Timing diagram for communication between the *T/SDAS-DDC1* DCM and host DSP via transmitter of SIO-0 port of host *TORNADO* SIOX interface is defined by the *T/SDAS-DDC1* DCM hardware. Both frame sync pulse (FSX) and serial clock (CLKX) for transmitter of DSP on-chip serial port, which is wired to SIO-0 port of host SIOX interface on *TORNADO* board, shall be generated by the DSP on-chip serial port, and must be configured for active high data, internal active low serial clock and internal active low frame sync strobe pulse.

Transmitted data format depends upon the command, which is being transmitted to the *T/SDAS-DDC1* DCM:

- data format must be set to 16-bit for all commands except for the *XSL_WR_CMND* command
- data format must be set to 16 bits for the *XSL_WR_CMND* command after SIOX DCM reset condition or after execution of *XSL_SET_FMT_CMND* command, which sets the 16-bit data format
- data format must be set to 24 bits for the *XSL_WR_CMND* command after execution of *XSL_SET_FMT_CMND* command, which sets the 24-bit data format
- data format must be set to 32 bits for the *XSL_WR_CMND* command after execution of *XSL_SET_FMT_CMND* command, which sets the 32-bit data format.

Timing diagram for communication between the *T/SDAS-DDC1* DCM and host DSP via transmitter of SIO-0 port of host *TORNADO* SIOX interface is presented at figure 2-2.

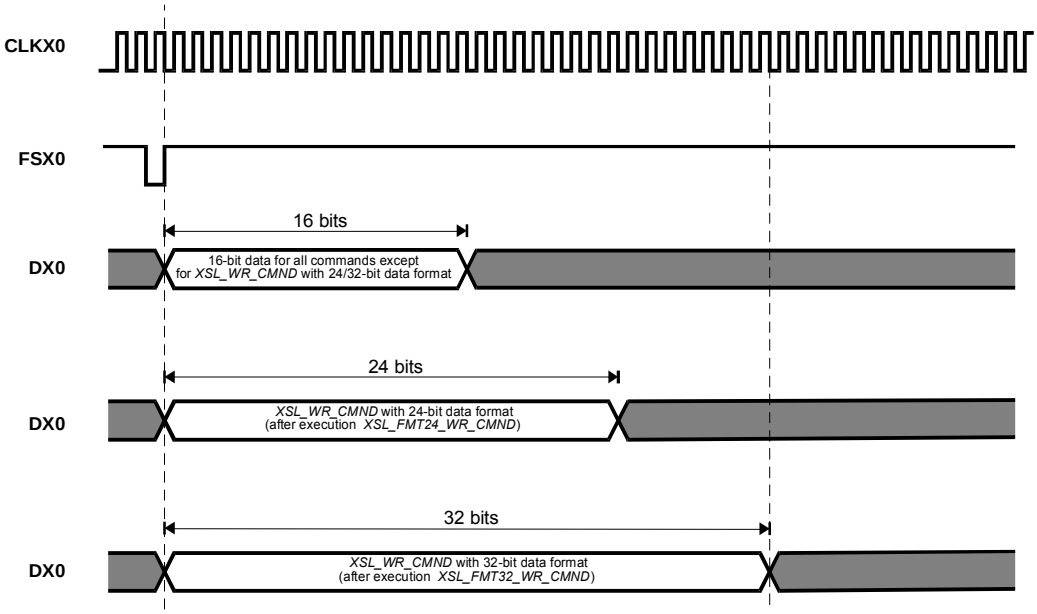


Fig. 2-2. Timing diagram for sending command via transmitter of SIOX SIO-0 port.

CAUTION

Maximum serial clock frequency for transmitter of SIO-0 port of host SIOX interface is 15 MHz. The higher transmitter serial clock values will result in incorrect functionality for on-board UART and PDC.

Transmitter of SIO-0 port of host SIOX interface must provide data transmission with the most significant bit first.

SIOX SIO-0 port receiver timing for RCV_AUX_DATA_MODE receiver data mode

In case the *T/SDAS-DDC1* DCM is configured for operation in the *RCV_AUX_DATA_MODE* receiver data mode (read-back commands), then the receiver frame sync (FSR), serial clock (CLKR) and serial data (DR) are generated by the CU of *T/SDAS-DDC1* DCM. Note, that the receiver serial clock for *RCV_AUX_DATA_MODE* receiver data mode is routed from the input transmitter serial clock (CLKX) of SIOX SIO-0 port, which is generated by the DSP on-chip transmitter, whereas the receiver frame sync pulse and serial data are generated by CU during the read-back command execution.

For the *RCV_AUX_DATA_MODE* receiver data mode the receiver of DSP on-chip serial port, which is wired to SIO-0 port of host SIOX interface on *TORNADO* board, must be configured for active high data, external active high serial clock, external active low frame sync strobe pulse and 16-bit data format.

Timing diagram for communication between the *T/SDAS-DDC1* DCM and host DSP via receiver of SIO-0 port of host *TORNADO* SIOX interface for *RCV_AUX_DATA_MODE* receiver data mode is presented at figure 2-3.

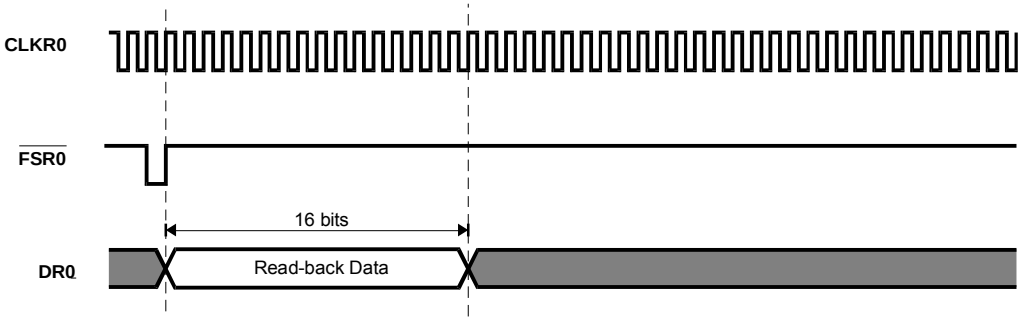


Fig. 2-3. Timing diagram for receiving data via receiver of SIOX/SIO-0 port for *RCV_AUX_DATA_MODE* receiver data mode (for read-back commands).

CAUTION

Receiver of SIO-0 port of host SIOX interface must provide data reception with the most significant bit first.

SIOX SIO-0 port receiver timing for RCV_PDC_DATA_MODE receiver data mode

In case the *T/SDAS-DDC1* DCM is configured for operation in the *RCV_PDC_DATA_MODE* receiver data mode (download PDC real-time data), then the receiver frame sync (FSR), serial clock (CLKR) and serial data (DR) are generated by Intersil HSP50214 PDC chip of *T/SDAS-DDC1* DCM. Output serial data correspond to the PDC SEROUTA serial output.

The polarities of receiver frame sync pulse and of serial clock the *RCV_PDC_DATA_MODE* receiver data mode are defined by the Intersil HSP50214 PDC, and can be software configured via PDC on-chip Control Word #20 register.

CAUTION

In order to obtain complete compatibility with the *RCV_PDC_DATA_MODE* receiver data mode, we highly recommend to configure PDC via Control Word #20 register to the early inverse frame sync pulse and rising edge serial clock polarity. This will eliminate reconfiguration of the DSP on-chip receiver when switching between the *RCV_AUX_DATA_MODE* and *RCV_PDC_DATA_MODE* receiver data modes.

Correspondingly, the receiver of DSP on-chip serial port, which is wired to SIO-0 port of host SIOX interface on *TORNADO* board, must be configured for active high data, external active high serial clock and external active low frame sync strobe pulse.

Receiver data format for *RCV_PDC_DATA_MODE* receiver data mode (real-time PDC output data stream) must be set either to 16 bits or 32 bits depending upon the programming of the PDC output serial data formatter via PDC on-chip Control Word #19 register.

Timing diagram for communication between the *T/SDAS-DDC1* DCM and host DSP via receiver of SIO-0 port of host *TORNADO* SIOX interface for *RCV_PDC_DATA_MODE* receiver data mode is presented at figure 2-4. This figure corresponds to the PDC serial formatter configuration with early inverse FSX, rising edge CLKX polarity, and 32-bit serial data format.

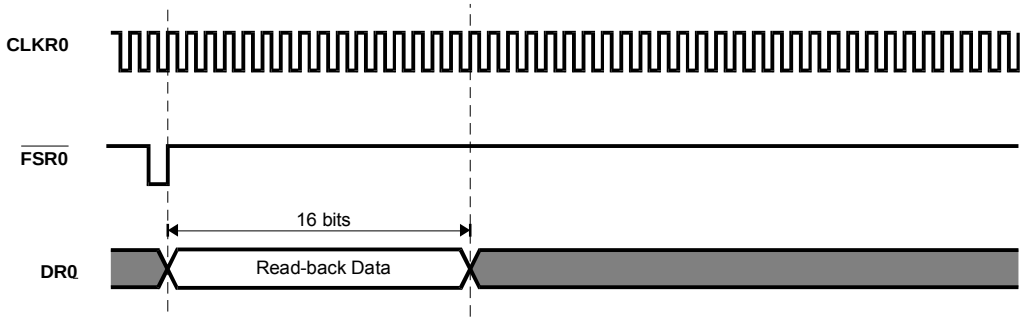


Fig. 2-4. Timing diagram for receiving data via receiver of SIOX SIO-0 port for *RCV_PDC_DATA_MODE* receiver data mode (for PDC real-time data output).

CAUTION

Receiver of SIO-0 port of host SIOX interface must provide data reception with the most significant bit first.

2.4 XSL Timing

XSL feature programmable serial clock polarity, programmable framing feature, and programmable data bit length via the *XSL_SET_FMT_CMND* command (refer to the 'Software Control' section earlier in this chapter). The above programmable features allow to use XSL-1 and XSL-2 external serial links for programming external RF gain amplifier with low digital noise, as general purpose serial output, and many more.

XSL serial clock

The polarity and framing feature of XSL output serial clock are programmable via bits *XSL-CLK_POL* and *XSL-CLK_FRM* of *XSL_SET_FMT_CMND* command (refer to the 'Software Control' section earlier in this chapter) as shown at figure 2-5.

CAUTION

Serial clock (*XSL-CLK*) for XSL-1 and XSL-2 external serial links is sourced from the input transmitter clock (*CLKX0*) of SIO-0 port transmitter of host SIOX interface.

CAUTION

In case the framing feature for XSL serial clock is enabled and the XSL serial clock polarity is set to active falling edge of XSL serial clock, then XSL serial clock defaults to the logical '0' value outside active XSL frame sync pulse.

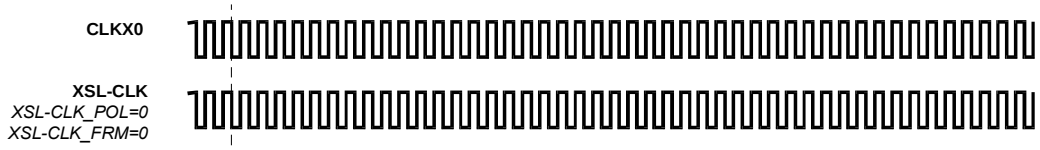
In case the framing feature for XSL serial clock is enabled and the XSL serial clock polarity is set to active rising edge of XSL serial clock, then XSL serial clock defaults to the logical '1' value outside active XSL frame sync pulse.

XSL data format and frame sync

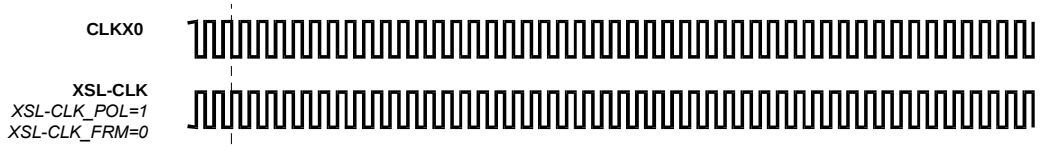
The XSL data format (data bit length of output XSL packet) can be programmable to either 14-bit, or 22-bit, or 30-bit via the {*XSL-DF1,XSL-DF0*} bits of *XSL_SET_FMT_CMND* command (refer to the 'Software Control' section earlier in this chapter). Figure 2-6 presents XSL timing diagrams for different XSL data formats and continuous serial clock with active falling edge.

CAUTION

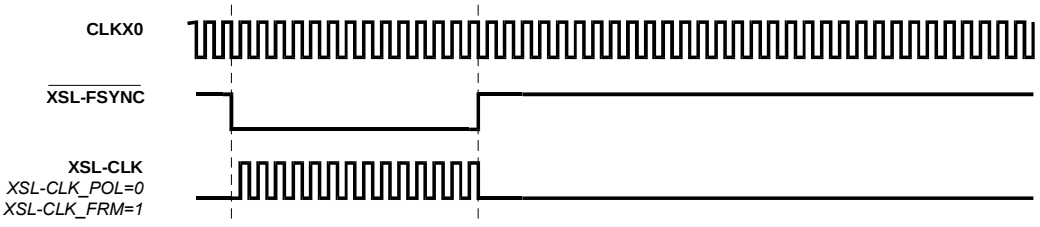
XSL provides active low output frame sync pulse (*XSL-FSYNC*), which frames the entire transmitted XSL data packet.



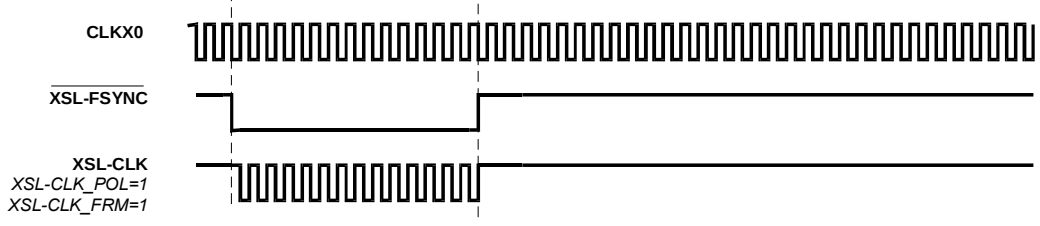
A) Continuous XSL serial clock with active falling edge polarity.



B) Continuous XSL serial clock with active rising edge polarity.

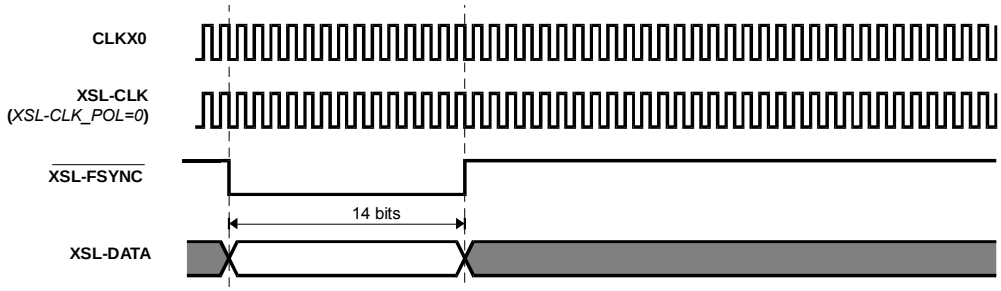


C) Framed XSL serial clock with active falling edge polarity.

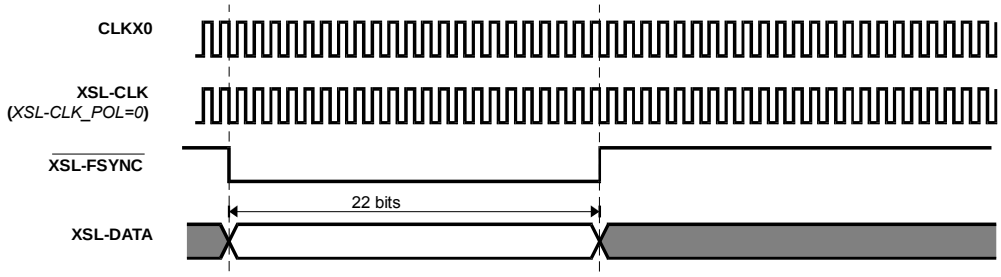


D) Framed XSL serial clock with active rising edge polarity.

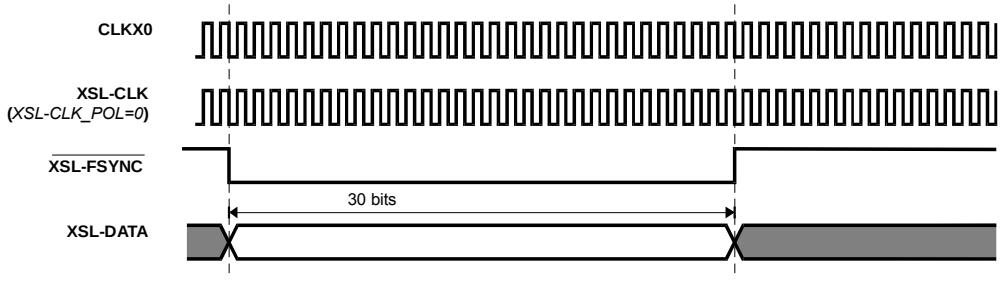
Fig. 2-5. Polarity and framing of output XSL serial clock.



A) 14-bit output *XSL-DATA* format



B) 22-bit output *XSL-DATA* format



C) 30-bit output *XSL-DATA* format

Fig. 2-6. Timing diagram for XSL transmission.

2.5 Construction

T/SDAS-DDC1 DCM (fig.1-1, fig.A-1) meets standard SIOX rev.B daughter-card form-factor. Construction of *T/SDAS-DDC1* DCM assumes that host *TORNADO* DSP system with *T/SDAS-DDC1* DCM installed fits into one ISA-bus slot of PC chassis.

Connection of *T/SDAS-DDC1* DCM to external analog I/O world is performed via the on-board JP2 connector, which is available via rear panel of host PC (if *T/SDAS-DDC1* is installed onto *TORNADO* DSP system for

PC). Compatible *T/X-DDC1/C* cable is provided as standard with *T/SDAS-DDC1* DCM. Optional external RF amplifier *T/X-DDC/AFE-xx* DCM can be connected directly to the JP2 connector of *T/SDAS-DDC1* DCM.

Chapter 3. Installation

This chapter contains information for installation and configuration of *T/SDAS-DDC1* DCM.

3.1 Installation

T/SDAS-DDC1 DCM installs as SIOX daughter-card DCM onto *TORNADO* DSP system mainboard.

For installation of *T/SDAS-DDC1* DCM into SIOX site of *TORNADO* DSP system follow the recommendations below (fig.3-1):

1. Switch off the power of host PC.
2. Remove *TORNADO* mainboard from PC slot.
3. Take *T/SDAS-DDC1* DCM and slant it for about 30°..40° degrees refer to *TORNADO* mainboard. Insert JP2 external I/O connector of *T/SDAS-DDC1* DCM into the corresponding hole of mounting bracket of *TORNADO* DSP system.

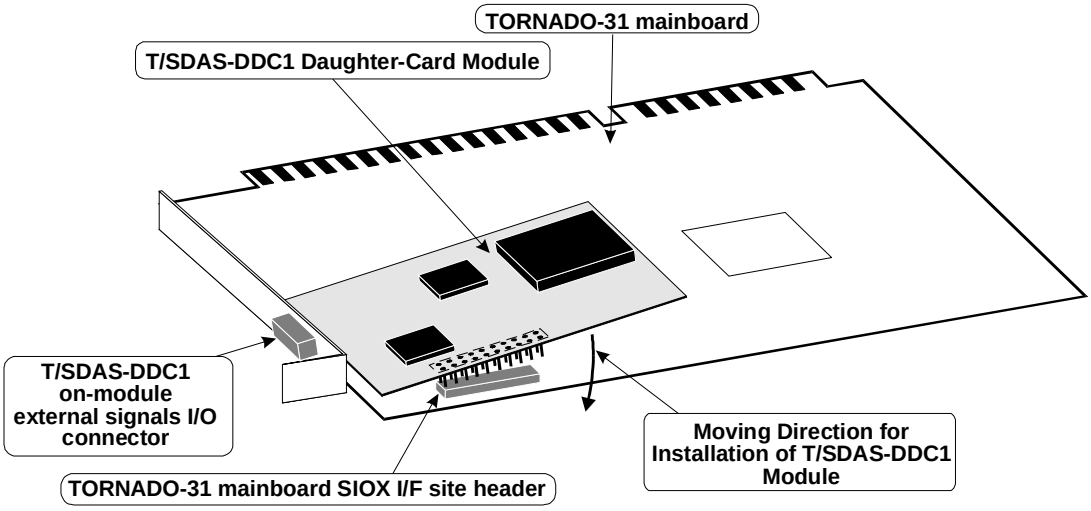


Fig. 3-1. Installation of *T/SDAS-DDC1* DCM into SIOX site of *TORNADO* DSP system.

4. Rotate *T/SDAS-DDC1* DCM around mounting bracket and allocate pin #1 of JP1 host SIOX connector of *T/SDAS-DDC1* DCM against pin #1 of SIOX interface header on *TORNADO* mainboard.

CAUTION

TORNADO on-board SIOX female connector site has 20 pins for *TORNADO-31/31Z/31M/32L/32LX/33/P33/E31/E33* DSP systems and controllers and 26 pins for *TORNADO-30/54x/6x/E6x/E54x* DSP systems and controllers. Pin #1 of host SIOX site connectors always fit into the same physical position on *TORNADO* DSP systems and controllers.

Pin #1 of SIOX connector of *T/SDAS-DDC1* DCM must always plug into pin #1 of host SIOX site connector not regarding type of host *TORNADO* DSP systems or controller.

Missing doing this will result in damage of *T/SDAS-DDC1* DCM and/or host *TORNADO* hardware.

5. Safely plug-in SIOX male header of *T/SDAS-DDC1* DCM into SIOX female header of *TORNADO* DSP system.
6. Screw external analog I/O connector shell of *T/SDAS-DDC1* DCM to the mounting bracket of *TORNADO* DSP system.
7. If required, configure on-board SW3 switch for selection of desired host SIOX interrupts for DIO-0 and UART (refer to tables 2-5 and 2-6).
8. If required, install desired Fs/CLKIN and PDC PROCLK crystal oscillators to on-board S1 and S2 sockets and configure on-board SW1 and SW2 clock selector switches (refer to tables 2-1 and 2-2).
9. Configure on-board SW4 switch in accordance with desired AC-coupling feature for D/A-1/2 analog output channels (refer to tables 2-3 and 2-4).
10. Install *TORNADO* board into PC slot and screw it to rear panel of PC.
11. Connect I/O cable to JP2 external analog I/O connector of *T/SDAS-DDC1* DCM.
12. Switch on power of host PC.

3.2 Connection to external signal I/O equipment

Connection of *T/SDAS-DDC1* DCM to external analog I/O equipment is performed by means of on-board JP2 connector (fig.A-1) and external I/O cable set (Appendix C).

CAUTION

It is highly recommended to plug-in and unplug external I/O cable set into/from on-board JP2 connector of *T/SDAS-DDC1* DCM when host *TORNADO* power is switched off.

The ground signal of *T/SDAS-DDC1* DCM has no galvanic isolation from host *TORNADO* and/or PC ground signal and chassis.

CAUTION

When connecting external analog I/O equipment to *T/SDAS-DDC1* DCM you should be aware that AIN analog input and AOUT-0/1 analog outputs of *T/SDAS-DDC1* DCM are DC coupled. If required, external DC isolation capacitors should be used.

Appendix A. On-board Connectors and Switches

This appendix contains a summary for the on-board connectors, configuration jumpers and configuration switches for *T/SDAS-DDC1* DCM.

The on-board sockets, connectors and configuration jumpers are presented at fig.A-1.

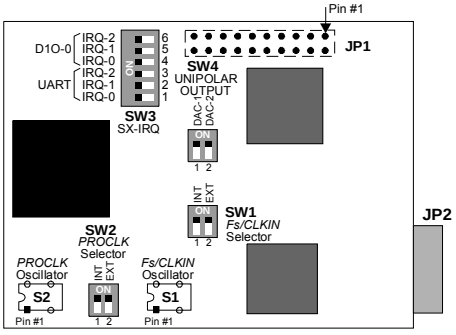


Fig. A-1. On-board sockets, connectors and configuration jumpers for *T/SDAS-DDC1* DCM.

A.1 Configuration Switches

Table A-1 specifies how to set on-board configuration switches.

Table A-1. Configuration jumpers for *T/SDAS-DDC1* DCM.

Switch	Description	Reference
SW1	ADC/PDC sampling frequency (Fs/CLKIN) clock selector.	table 2-1
SW2	PDC PROCLK input clock selector.	table 2-2
SW3-1..3	Host SIOX interrupt line selector for interrupt on UART request.	table 2-5
SW3-4..6	Host SIOX interrupt line selector for interrupt on DIO-0 I/O event.	table 2-6
SW4-1 *SW4-1*	AC coupling for XDAC-1 and XDAC-2 analog outputs.	tables 2-3 and 2-4

A.2 On-board Connectors

Table A-2 contain the list of on-board connectors.

Table A-2. On-board connectors of *T/SDAS-DDC1* DCM.

Connector	Description
JP1	SIOX interface site male header. Pinout of JP1 host SIOX connector is presented in the user's guide of host *TORNADO* DSP system or controller, which is used for installation of *T/SDAS-DDC1* DCM, and in Appendix B of this *T/SDAS-DDC1* DCM user's guide.
JP2	External analog I/O connector.

Pinout for external I/O connector

Pinout of JP2 external I/O connector for *T/SDAS-DDC1* DCM is presented at fig.A-2, and description of signals is presented in table A-3.

The connector p/n for JP2 is DHA-RA26 female half-pitch connector from DDK Ltd manufacturer (www.ddkconectors.com) . P/n for compatible plug-in connector is DHA-PC26. In case customer needs to design his own application specific cable for connection to *T/SDAS-DDC1* DCM, then compatible plug-in connectors for JP2 are available from MicroLAB Systems upon request.

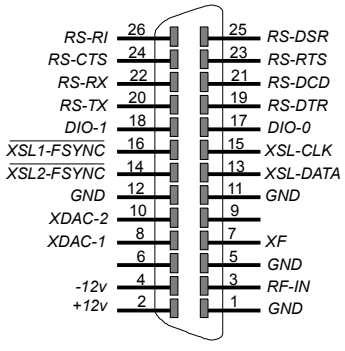


Fig. A-2. Pinout for JP2 external I/O connector of *T/SDAS-DDC1* DCM.

Table A-3. Signal description for JP2 external I/O connector of *T/SDAS-DDC1* DCM.

Signal name	type	description
RF-IN	AI	RF analog input
XDAC-1 *XDAC-2*	AO	Analog outputs from channels D/A-1 and D/A-2.
XF	3v/5v TTL/IN	External frequency input for either ADC/PDC sampling frequency (Fs/CLKIN), or PDC PROCLK.

XSL-DATA *XSL-CLK* *XSL1-FSYNC* *XSL2-FSYNC*	3v/5v TTL/OUT	Serial data, clock and frame sync correspondingly for XSL-1 and XSL-2 external serial output links.
DIO-0 *DIO-1*	3v/5v TTL/IO	General purpose programmable digital I/O DIO-0/1.
RS-TX *RS-RX* *RS-RTS* *RS-CTS* *RS-DTR* *RS-DSR* *RS-RI* *RS-DCD*	RS/OUT RS/IN RS/OUT RS/IN RS/OUT RS/IN RS/IN RS/IN	RS232C I/O pins from UART.
+12V, -12V	-	Power supply outputs.
GND	-	Ground.

Notes: 1. Signal types: *AI* - analog input; *AO* - analog output; *TTL/IN* - TTL compatible digital input; *TTL/OUT* - TTL compatible digital output; *TTL/IO* - TTL compatible digital input/output; *RS/IN* - RS232C compatible digital input; *RS/OUT* - RS232C compatible digital output.

A.3 On-board Sockets

Table A-4 contain the list of on-board sockets.

Table A-4. On-board sockets of *T/SDAS-DDC1* DCM.

Socket	description
S1	DIP-4 socket for installation of ADC/PDC Fs/CLKIN sampling frequency crystal oscillator. Refer to section 2-1 for more details.
S2	DIP-4 socket for installation of PDC PROCLK crystal oscillator. Refer to section 2-1 for more details.

Appendix B. SIOX Rev.B Interface Site

This appendix contains information about *TORNADO* SIOX rev.B interface site specifications. This description is general to all *TORNADO* DSP systems/controllers/coprocessors, whereas different *TORNADO* boards with different DSP platforms may differ in the number and in the on-board routing of SIOX serial ports, timer/IO pin specifications. Refer to your particular *TORNADO* user's guide for more details.

B.1 General Description

TORNADO architecture provides expansion of the on-board DSP I/O resources via on-board serial I/O expansion interface sites (SIOX-A and SIOX-B) (fig.B-1), which are designed to carry compatible DCM (DCM).

Fig.B-1. TORNADO-54x board with two SIOX sites.

Some *TORNADO* boards (typically *TORNADO* DSP systems for PC) provide two SIOX interface sites, whereas other *TORNADO* boards (typically *TORNADO* stand-alone DSP controllers and DSP coprocessors) provide only one SIOX site.

TORNADO SIOX rev.B interface site comprises of signals for one or two SIO-0/SIO-1 logical serial ports, timers/IO pins, DSP interrupts, and host power supplies.

CAUTION

In case *TORNADO* on-board DSP features two or more on-chip serial ports (TMS320C30, TMS320C54x, TMS320C6x), then *TORNADO* on-board SIOX sites provides two SIO-0 and SIO-1 serial ports and the SIOX site headers are 26-pin headers.

In case *TORNADO* on-board DSP features only one on-chip serial ports (TMS320C31, TMS320C32), then *TORNADO* on-board SIOX sites provides only one SIO-0 serial port and the SIOX site headers are 20-pin headers.

Both *TORNADO* on-board SIOX-A and SIOX-B interface sites feature identical pinout control and may only differ in the routing of DSP physical serial ports to SIO-0 and SIO-1 logical serial ports. If *TORNADO* on-board DSP features two or more on-chip serial ports (TMS320C30, TMS320C54x, TMS320C6x), then DSP serial ports routing is performed on *TORNADO* mainboard, and allows simultaneous operation of two or more SIOX DCM, which are routed to different DSP serial ports.

B.2 SIOX Site Connector and Signals

TORNADO SIOX rev.B interface site comprises of signals for SIO-0 and SIO-1 logical serial ports, DSP on-chip TM/XIO-0/1 timers/IO pins, three DSP interrupts, SIOX reset control, and power ±5V/±12V host power supplies.

TORNADO on-board SIOX site connector with two serial ports

TORNADO on-board SIOX site connector with two serial ports is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM should be the industry standard either 26-pin 0.1"x0.1"male header (in case both SIO-0 and SIO-1 serial ports are utilized on SIOX plugged-in DCM) or 20-pin 0.1"x0.1"male header (in case only SIO-0 serial port is utilized on SIOX plugged-in DCM).

SIOX site connector pinout with two serial ports is shown at fig.B-2 and signal specifications are listed in table B-1.

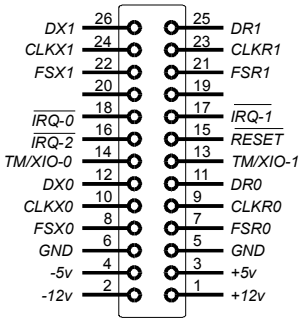


Fig.B-2. TORNADO on-board SIOX connector pinout with two serial ports (top view).

TORNADO on-board SIOX site connector with one serial port

TORNADO on-board SIOX site connector with one serial port is an industry standard dual-row 20-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM should be the industry standard 20-pin 0.1"x0.1"male header.

SIOX site connector pinout with one serial ports is shown at fig.B-3 and signal specifications are listed in table B-1.

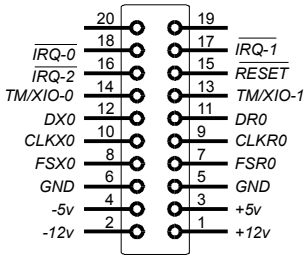


Fig.B-3. TORNADO on-board SIOX connector pinout with one serial port (top view).

SIOX site signal description

Description for SIOX interface site signals is presented in table B-1.

Table B-1. SIOX interface signal description.

SIOX signal name	signal type	description
	SIO-0 port control	
DX0 *FSX0* *CLKX0*	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX site..
DR0 *FSR0* *CLKR0*	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX site..
	SIO-1 port control *(available in SIOX site connector with two serial ports only)*	
DX1 *FSX1* *CLKX1*	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX site..
DR1 *FSR1* *CLKR1*	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX site..

DSP Timers/IO, DSP Interrupt Requests and SIOX Reset		
TM/XIO-0	I/O/Z	This signal is typically connected to the DSP on-chip timer-0 I/O pin and can be software configured by DSP as either timer or I/O pin.
TM/XIO-1	I/O/Z	This signal is typically connected to the DSP on-chip timer-1 I/O pin and can be software configured by DSP as either timer or I/O pin.
$\overline{RESET}$	O	Active low SIOX reset signal. Some *TORNADO* boards (for example *TORNADO-3x* boards) wires this signal directly from the DSP reset signal and SIOX plugged-in DCM reset is performed simultaneously with *TORNADO* on-board DSP reset, however other *TORNADO* boards (for example *TORNADO-54x/6x* etc. boards) features dedicated SIOX site reset signal, which is controlled by TORNADO on-board DSP for better synchronization between the DSP software and SIOX DCM operation.
$\overline{IRQ-0}$, $\overline{IRQ-1}$, $\overline{IRQ-2}$	I	Active low external interrupt request lines for TORNADO on-board DSP. These line are pulled up.
Power Supplies		
GND		Ground.
+5v		+5v
+12v		+12v
-5v		-5v
-12v		-12v

Note:
1. Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
1. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

SIOX site signal levels

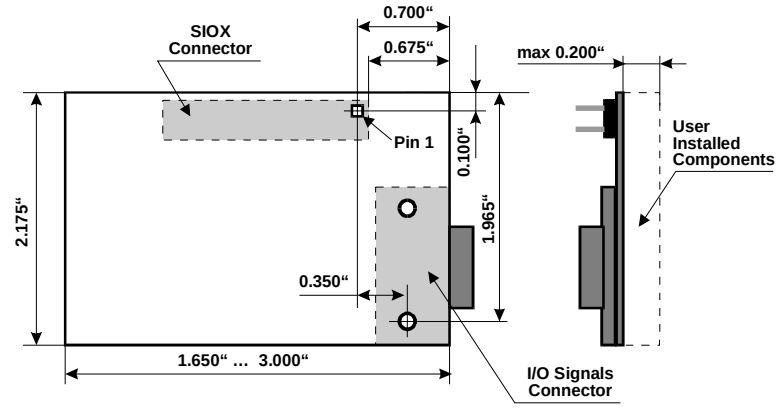
Signal levels for SIOX interface signals correspond to that for the CMOS/TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

CAUTION

Some *TORNADO* boards (*TORNADO-3x/542L/E31*) provide SIOX interface signal levels for CMOS/TTL only, whereas other *TORNADO* boards (*TORNADO-54xx/6x/E6x/P6x*) provide SIOX interface signal levels universal for both 3V TLL and standard TTL. Refer to documentation for your particular *TORNADO* board for information about SIOX interface signal levels.

B.3 Physical Dimensions for SIOX DCM

Physical dimensions for SIOX DCM are presented at fig.B-4. This information is intended for those customers, who need to design customized SIOX DCM.



SIOX connector: 20-pin or 26-pin straight dual-row mail header (0.025“ Sq., 0.1“x0.1” pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.B-4. Physical dimensions for SIOX DCM.

Appendix C. T/X-DDC1/C Cable

This appendix contains description for ***T/X-DDC1/C*** cable set (fig.C-1), which comes standard with ***T/SDAS-DDC1*** DCM and is used for connection to external signal sources and peripherals using industry standard end connectors.

Fig.C-1. T/SDAS-DDC1 DCM with *T/X-DDC1/C* cable.

T/X-DDC1/C external I/O cable set for ***T/SDAS-DDC1*** DCM plugs into the JP2 connector of ***T/SDAS-DDC1*** DCM and splits I/O signals of JP2 external I/O connector into several functional groups via industry-standard end connectors in order to simplify connection to external analog I/O equipment. ***T/X-DDC1/C*** cable set comprises of the following end connectors (refer to Appendix C for more details):

- RF-IN BNC coax connector for RF analog signal input
- RCA jack XDAC-1 analog output for external gain control, phones, and general purpose analog output (recommended usage is to connect to external RF amplifier for gain control)
- 3.5mm mini jack at the XDAC-2 analog output for external gain control, phones, and general purpose analog output (recommended usage is to connect to headphones)
- D-Sub DB-9 male 9-pins connector for RS232C interface, which meets the industry-standard pinout for PC COM ports
- high-density D-Sub DBH-15 female 15-pins connector (compatible with connectors for PC VGA monitors) for auxiliary signal I/O and power output.

Fig.C-2 shows generic schematic diagram of ***T/X-DDC1/C*** cable for ***T/SDAS-DDC1*** DCM. Signal description is provided in table A-3 for JP2 external I/O connector of ***T/SDAS-DDC1*** DCM.

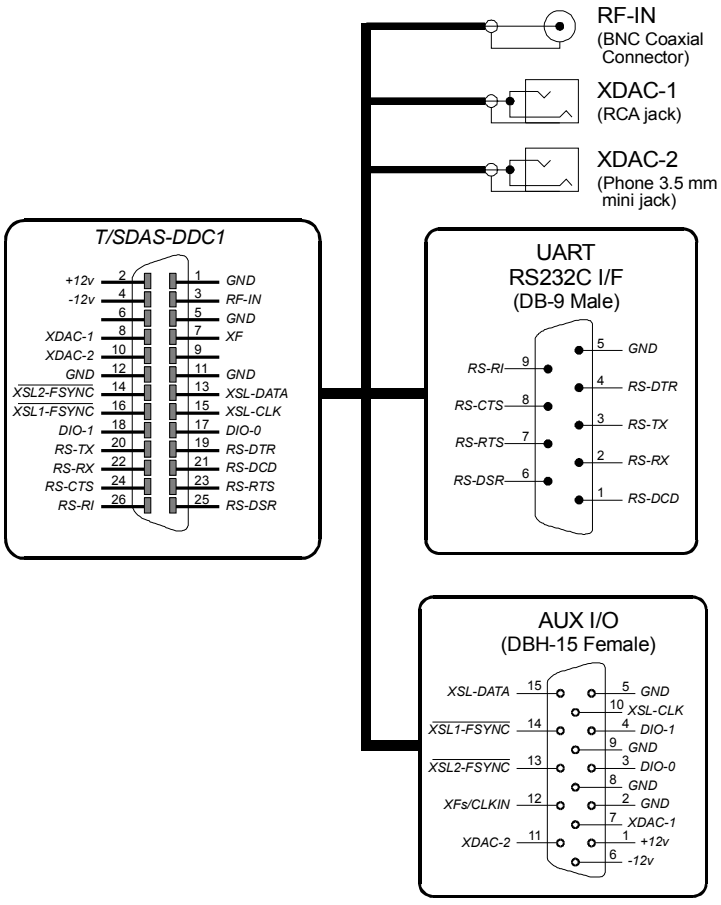


Fig.C-2. Schematic diagram of *T/X-DDC1/C* cable.