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DIGITAL SIGNAL PROCESSING

T/SDAS-ADDA4/16Q/200K

Quad-channel 16-bit AD/DA Instrumentation SIOX DCM
for *TORNADO* DSP Systems, Controllers and Coprocessors

User's Guide

covers:
T/SDAS-ADDA4/16Q/200K rev.1A

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About this Document

This user's guide contains description for *T/SDAS-ADDA4/16Q/200K* AD/DA SIOX daughter-card DCM (DCM) for *TORNADO* DSP systems/controllers/coprocessors from MicroLAB Systems Ltd.

This document does not include detail description neither for *TORNADO* systems, nor for TI DSP and corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C3x User's Guide.*** Texas Instruments Inc, SPRU031C, USA, 1992.
2. ***TMS320C54x. CPU and Peripherals. Reference Guide.*** Texas Instruments Inc, SPRU131D, USA, 1997.
3. ***TMS320C6x. CPU and Instruction Set. Reference Guide.*** Texas Instruments Inc, SPRU189C, USA, 1998.
4. ***TORNADO-3x. User's Guide.*** MicroLAB Systems, 1998.
5. ***TORNADO-P33. User's Guide.*** MicroLAB Systems, 2000.
6. ***TORNADO-54x. User's Guide.*** MicroLAB Systems, 1998.
7. ***TORNADO-6x. User's Guide.*** MicroLAB Systems, 1998.
8. ***TORNADO-P6x. User's Guide.*** MicroLAB Systems, 1999.
9. ***TORNADO-PX31DP. User's Guide.*** MicroLAB Systems, 1996.
10. ***TORNADO-SX30. User's Guide.*** MicroLAB Systems, 1996.
11. ***TORNADO-E31. User's Guide.*** MicroLAB Systems, 1996.
12. ***TORNADO-E33. User's Guide.*** MicroLAB Systems, 2000.
13. ***TORNADO-EL31. User's Guide.*** MicroLAB Systems, 1996.
14. ***TORNADO-E6x. User's Guide.*** MicroLAB Systems, 1998.

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Chapter 1. Introduction

This chapter contains general description for *T/SDAS-ADDA4/16Q/200K* SIOX daughter-card module (DCM) for *TORNADO* DSP systems/controllers/coprocessors.

1.1   General Information

T/SDAS-ADDA4/16Q/200K (fig.1-1) is quad-channel AD/DA SIOX (serial I/O expansion) DCM for *TORNADO* DSP systems (*TORNADO-3x/54x/6x/P6x/P33/etc*), *TORNADO-E/EL* stand-alone DSP controllers (*TORNADO-E3x/E54x/E6x/etc*) and *TORNADO-PX/SX* DSP coprocessors (*TORNADO-PX31DP/SX30/etc*) from MicroLAB Systems Ltd.

T/SDAS-ADDA4/16Q/200K DCM has been designed for high-accuracy high-speed and multi-channel instrumentation applications, however it can be used for many other applications with similar requirements for the AD/DA front-end.
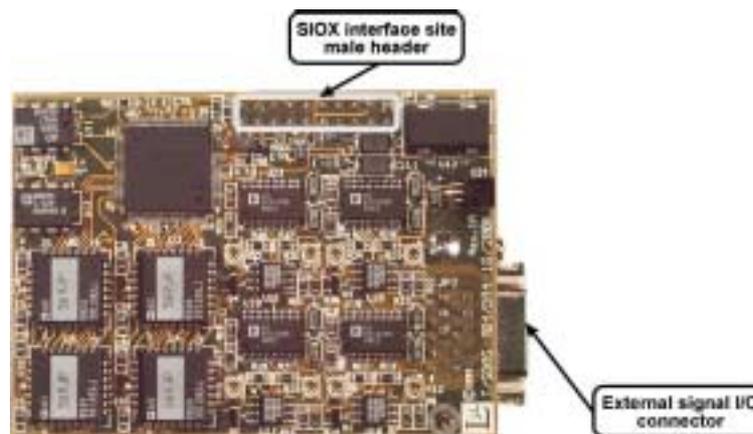
Fig. 1-1.   T/SDAS-ADDA4/16Q/200K DCM.

Installation

T/SDAS-ADDA4/16Q/200K DCM installs as SIOX DCM (fig.1-2) into the SIOX site onto *TORNADO* DSP mainboard. If required, the *T/SU-X* SIOX extender can be used for remote connection to SIOX interface of *TORNADO* mainboard.
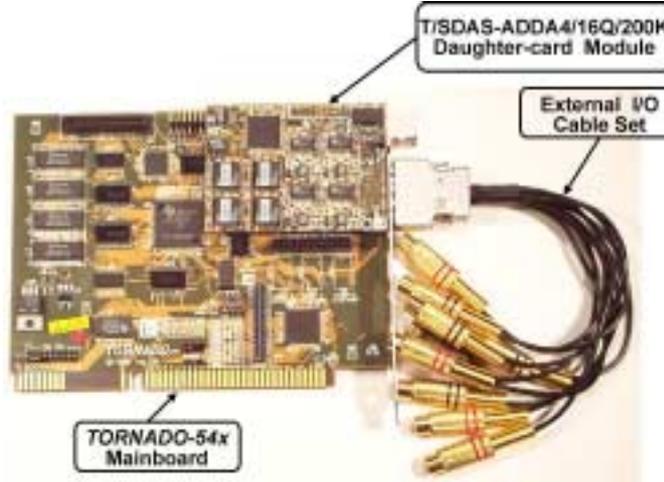
Fig. 1-2.   T/SDAS-ADDA4/16Q/200K DCM installed onto TORNADO-54x mainboard.

Overview

T/SDAS-ADDA4/16Q/200K DCM comprises of four AD/DA channels of instrumentation quality and features:
- four 16-bit 200ksps ADCs with synchronous sampling
- four 16-bit 200ksps DACs with synchronous sampling
- programmable sampling frequency generator
- control unit.

On-board AD/DA channels feature 16-bit resolution, excellent linearity, low THD and synchronous sampling of all AD/DA channels.

On-board sampling frequency (period) generator of *T/SDAS-ADDA4/16Q/200K* DCM can be software programmed to any value in the range 0.6 Hz .. 200 kHz with 100 ns sampling period resolution. Also, external sampling frequency input or output of any host SIOX interface timers can be software selected as the sampling frequency event.

T/SDAS-ADDA4/16Q/200K DCM operates in "CONTROL", "ASYNC-DATA" and "SYNC-DATA" modes, allows individual programmable enable for every A/D and D/A channels, and features software programmable serial data word format.

External signal I/O

Connection of *T/SDAS-ADDA4/16Q/200K* DCM to external analog I/O world is performed via the on-board I/O JP2 connector, which is available via rear panel of host PC (if *T/SDAS-ADDA4/16Q/200K* DCM is installed onto *TORNADO* DSP system for PC).

Applications

T/SDAS-ADDA4/16Q/200K AD/DA DCM has been designed for high-accuracy high-speed multi-channel instrumentation applications as well as for other general signal processing applications (biomedical, speech/audio, etc), which feature similar AD/DA requirements.

1.2   Technical Specifications

The following are technical specifications for *T/SDAS-ADDA4/16Q/200K* AD/DA DCM for temperature of external environment +25°C.

parameter description	*parameter value*
A/D channel:	
ADC type	AD677A from Analog Devices Inc
number of channels (ADCs)	4
input signal range	$\pm$ (5 V $\pm$ 50 mV (typ))
input impedance for analog inputs	1 MOhm
settling time for input analog buffers	2 us (typ) to 0.01%
resolution	16 bits
zero offset error	$\pm$10 mV max
differential nonlinearity	$\pm$1.5 LSB (typ)
integral nonlinearity	$\pm$2 LSB (typ)
THD	-92 dB (typ)
signal sampling method	synchronous sampling of all A/D channel
D/A channel	
DAC type	AD569 from Analog Devices Inc
number of channels (DACs)	4
output signal range for LINE-OUT output	$\pm$ (5 V $\pm$ 3 mV) @ 5 kOhm

resolution	16 bits
zero offset error	±1 mV max
differential nonlinearity	±1/2 LSB (typ)
integral nonlinearity	±0.02% FSR (typ)
output voltage settling time	4.5 us (typ) after Fs
signal sampling method	synchronous sampling of all D/A channel

common parameters:

output frequency range for sampling frequency (period) generator	0.6 Hz .. 200 kHz
sampling period resolution for sampling frequency (period) generator	100 ns
external sampling frequency or output frequency of SIOX I/F TM/XIO (timer) pin when used as sampling frequency source	≤ 200 kHz
number of bits in data packet via SIO-port in CONTROL mode	16 bits
external serial clock frequency via SIO-port in CONTROL mode	≤ 100 MHz
number of bits in data packet via SIO-port in data acquisition modes	16/32/64 bits
serial clock frequency for transmitter of SIO-port, when it is used as source synchro-clock for on-board timing	15 MHz ± 1%
logical low level for external clock frequency input	≤ 0.6 V
logical high level for external clock frequency input	≥ 2.4 V

physical and power:

dimensions	55mm (2.14") x 77mm (3") (full size SIOX rev.B DCM)
power consumption via SIOX I/F	+5v @ 600mA +12v @ 150mA -12v @ 50 mA -5v @ 5mA

Chapter 2. Technical Description

This chapter contains detail technical description for architecture and construction of *T/SDAS-ADDA4/16Q/200K* SIOX DCM.

2.1 Block Diagram

Basic configuration and connectivity of *T/SDAS-ADDA4/16Q/200K* DCM is presented at fig.2-1.
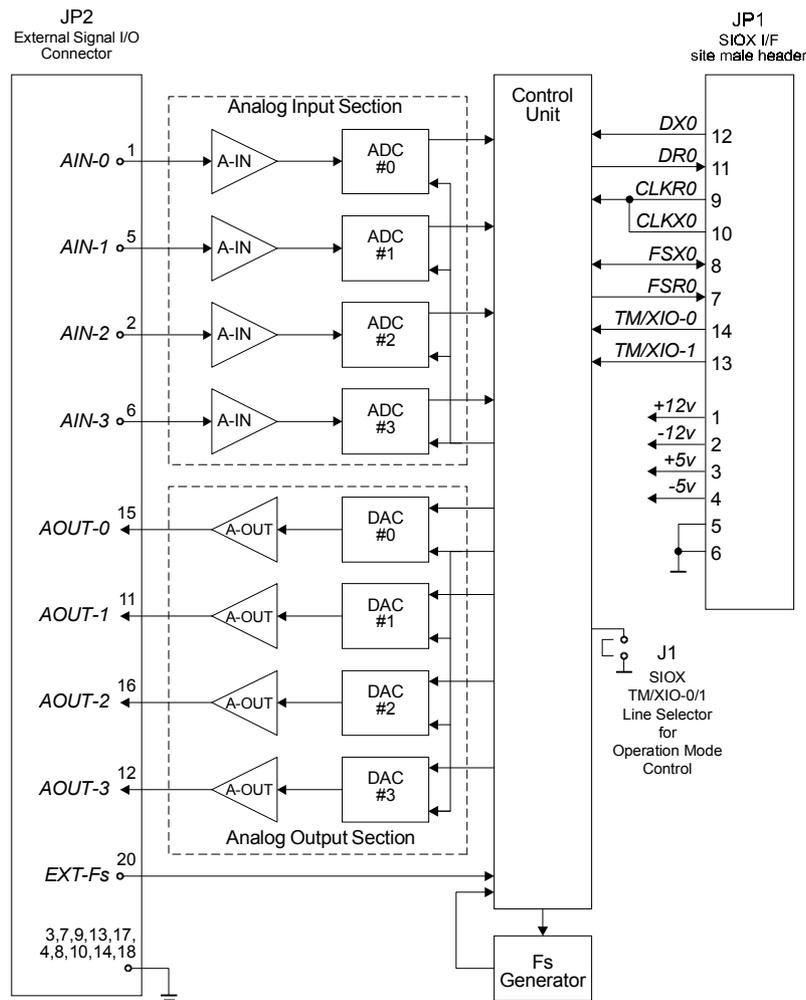

Fig. 2-1. Block diagram of *T/SDAS-ADDA4/16Q/200K* DCM.

T/SDAS-ADDA4/16Q/200K DCM installs as SIOX (serial I/O expansion interface) DCM onto *TORNADO* mainboard and assumes that communication with *TORNADO* on-board DSP is provided via the DSP on-chip serial port.

T/SDAS-ADDA4/16Q/200K DCM comprises of:
- analog input section, which contains four 16-bit 200ksps ADCs with synchronous sampling and input analog buffers
- analog output section, which contains four 16-bit 200ksps DACs with synchronous sampling and output analog buffers
- programmable sampling frequency generator (FSG)
- control unit (CU)
- host SIOX interface header for installation onto *TORNADO* DSP systems.

analog input section

Analog input section of *T/SDAS-ADDA4/16Q/200K* DCM comprises of four identical A/D channels (#0..#3), and is designed for analog-to-digital conversion of input analog signals from AIN-0..AIN-3 analog inputs and further transmission of digital code to the receiver of SIO-0 port of host SIOX interface of *TORNADO* DSP system.

Each A/D channel of analog input section comprises of the following components:
- input analog buffer (A-IN)
- 16-bit analog-to-digital converter (ADC) AD677A from Analog Devices Inc.

The A-IN input analog buffers are designed for interfacing to external analog input signals and feature high input impedance 1 MOhm and over-voltage protection at ±5.5 V signal level. The settling time for input buffers is typically 2 us to 0.01% accuracy. The A-IN input of every A/D channel is DC coupled and can process external DC/AC analog signals.

Every A/D channel of *T/SDAS-ADDA4/16Q/200K* DCM contains 16-bit 200ksps AD677A ADC from Analog Devices Inc, which features excellent linearity and high-accuracy at high conversion rates. All four ADCs feature synchronous sampling and transfer data in serial format via CU to the receiver of SIO-0 port of host SIOX interface of *TORNADO* DSP system. Each ADC can be individually enabled via the corresponding enable bit of *CONTROL REGISTER* in CU.

analog output section

Analog output section of *T/SDAS-ADDA4/16Q/200K* DCM comprises of four identical D/A channels (#0..#3), and is designed for conversion of digital code from transmitter of SIO-0 port of host SIOX interface of *TORNADO* DSP system into output analog signals (AOUT-0..AOUT-3).

Each D/A channel of analog output section comprises of the following components:
- 16-bit digital-to-digital converter (DAC) AD569 from Analog Devices Inc.
- output analog buffers (A-OUT) with gain factor 0dB

Every A/D channel of *T/SDAS-ADDA4/16Q/200K* DCM contains 16-bit 200ksps AD569 DAC from Analog Devices Inc, which features excellent linearity and high-accuracy at high conversion rates. Each DAC can be individually enabled via the corresponding enable bit of *CONTROL REGISTER* in CU, and all enabled DACs feature synchronous sampling. Data for DACs is unpacked by CU from the serial data stream from the transmitter of SIO-0 port of host SIOX interface of *TORNADO* DSP system.

A-OUT analog output buffers are used for interfacing to external low-impedance loads and provide minimum signal distortions.

sampling frequency generator (FSG) and sampling frequency selector

T/SDAS-ADDA4/16Q/200K DCM features programmable AD/DA sampling frequency selector from the following sources:

- 24-bit software programmable sampling frequency (period) generator (FSG) with 100 ns sampling period resolution, which allows on-board generation of 0.6 Hz .. 200 kHz sampling frequency. FSG is programmed by means of *FSG PERIOD REGISTER* in CU.
- external sampling frequency input (Ext-Fs)
- TM/XIO-0/1 pin (host DSP timer output) of host SIOX interface of *TORNADO* DSP system
- FSX strobe (SIO-0 port transmitter frame synch strobe) of host SIOX interface of *TORNADO* DSP system ("ASYNC-DATA" mode only).

Particular sampling frequency source selection is performed by the {*FS_SEL-1, FS_SEL-0*} bits of *CONTROL REGISTER* in CU.

operation modes

T/SDAS-ADDA4/16Q/200K DCM can operate in the following modes:

- "CONTROL" mode, which is used for configuring the *T/SDAS-ADDA4/16Q/200K* DCM by means of programming *CONTROL REGISTER* and *FSG PERIOD REGISTERs #0..#2* in CU
- data acquisition mode, which can be selected from one of the following modes:
  - ÿ "ASYNC-DATA" mode, which provides AD/DA signal acquisition with simplified timing and no pipelining at reduced maximum sampling rate. This mode does not offer synchronous sampling of both A/D and D/A channels, it provides synchronous sampling separately for all enabled A/D and all enable D/A channels instead.
  - ÿ "SYNC-DATA" mode, which provides AD/DA signal acquisition with pipelining at full sampling rate and synchronous sampling of all A/D and D/A channels.

CAUTION

Software selection between the "CONTROL" mode and any of the "ASYNC-DATA" or "SYNC-DATA" data acquisition modes is performed by means of TM/XIO-0/1 pin of host SIOX interface of *TORNADO* DSP system, which should be configured by *TORNADO* on-board DSP as software programmable I/O pin.

The particular selection of the TM/XIO-0/1 pin of host SIOX interface, which is used for selection between "CONTROL" mode and either "ASYNC-DATA" or "SYNC-DATA" data acquisition mode, is performed by means of on-board J1 jumper in accordance with table 2-1.

> **CAUTION**
>
> Software selection between the "ASYNC-DATA" and "SYNC-DATA" data acquisition modes
> is performed by the *MODE_SEL* bit of *CONTROL REGISTER* in CU. Both "ASYNC-
> DATA" and "SYNC-DATA" modes correspond to AD/DA signal acquisition.

Table 2-1.   Operation mode programming for *T/SDAS-ADDA4/16Q/200K* DCM.

J1 jumper state	TM/XIO-0 output pin of host SIOX I/F	TM/XIO-1 output pin of host SIOX I/F	*MODE_SEL* bit of *CONTROL_REGISTER*	TM/XIO output pin of host SIOX I/F, which can be used as Sampling Frequency source	operation mode
1-2	*0*	*x*	*x*	*TM/XIO-1*	"CONTROL" mode
1-2	*1*	*x*	*0*	*TM/XIO-1*	"ASYNC-DATA" mode
1-2	*1*	*x*	*1*	*TM/XIO-1*	"SYNC-DATA" mode
2-3	*x*	*0*	*x*	*TM/XIO-0*	"CONTROL" mode
2-3	*x*	*1*	*0*	*TM/XIO-0*	"ASYNC-DATA" mode
2-3	*x*	*1*	*1*	*TM/XIO-0*	"SYNC-DATA" mode

Notes: 1. Logical states: '0' - logical '0'; '1' - logical '1'; 'x' - don't care.

control unit (CU)

On-board Control Unit (CU) of *T/SDAS-ADDA4/16Q/200K* DCM is implemented with the FPGA chips and provides software DCM configuring via *CONTROL REGISTER* and *FSG PERIOD REGISTERs #0..#2* in "CONTROL" mode, as well as generates corresponding timing and provides data-path handling during either "ASYNC-DATA" or "SYNC-DATA" mode.

2.2   "CONTROL" Mode

"CONTROL" mode of *T/SDAS-ADDA4/16Q/200K* DCM must be used for configuring the DCM by means of programming the *CONTROL REGISTER* and *FSG PERIOD REGISTERs #0..#2*.

CAUTION

In "CONTROL" mode the transmitter of SIO-0 port of host SIOX interface is used for programming the *CONTROL REGISTER* and *FSG PERIOD REGISTERs* #0..#2 of *T/SDAS-ADDA4/16Q/200K* DCM from host DSP.

The receiver of SIO-0 port of host SIOX interface in "CONTROL" mode can be used for read-back verification of the contents of *CONTROL REGISTER* and *FSG PERIOD REGISTERs #0..#2*. While transmitter of SIO-0 port of host SIOX interface is sending new contents for either *CONTROL REGISTER* or *FSG PERIOD REGISTERs #0..#2*, the serial data, which is transmitted back by *T/SDAS-ADDA4/16Q/200K* DCM to the receiver of SIO-0 port of host SIOX interface, corresponds to the new programmed contents of either *CONTROL REGISTER* or *FSG PERIOD REGISTERs #0..#2*.

In "CONTROL" mode the transmitter of DSP on-chip serial port, which is wired to SIO-0 port of host SIOX interface on *TORNADO* board must be configured to 16-bit data format (active high), internally generated active high serial clock and internally generated active low frame sync strobe pulse (refer to table 2-3).

In "CONTROL" mode the receiver of DSP on-chip serial port, which is wired to SIO-0 port of host SIOX interface on *TORNADO* board must be configured to 16-bit data format (active high), external active high serial clock and external active low frame sync strobe pulse (refer to table 2-3).

Timing diagram for programming *T/SDAS-ADDA4/16Q/200K* DCM in "CONTROL" mode from host DSP via transmitter of SIO-0 port of host *TORNADO* SIOX interface is presented at figure 2-2.
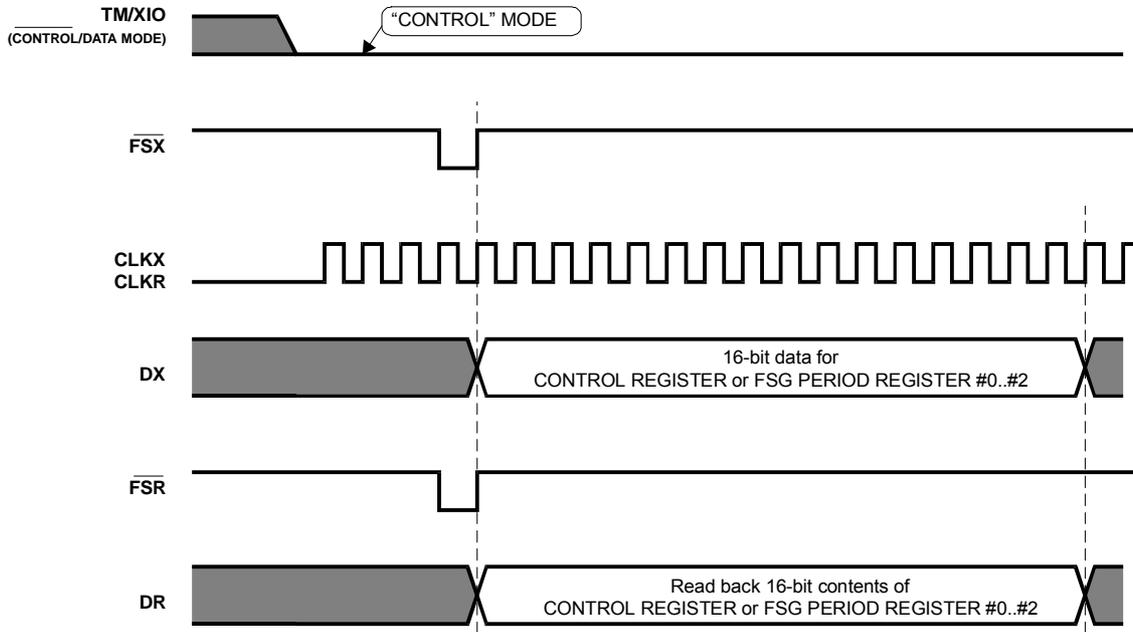
Fig. 2-2. Serial data communication for "CONTROL" mode.

CONTROL REGISTER

Data word format for programming *CONTROL REGISTER* of *T/SDAS-ADDA4/16Q/200K* DCM via transmitter of SIO-0 SIOX port is presented below and data bits description is presented in table 2-2:

Transmitter data word for programming CONTROL REGISTER

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	CLK_ SEL (0+)	SDW_ FMT-1 (0+)	SDW_ FMT-0 (0+)	FS_ SEL-1 (0+)	FS_ SEL-0 (0+)	MODE _SEL (0+)	DAC3 _EN (0+)	DAC2 _EN (0+)	DAC1 _EN (0+)	DAC0 _EN (0+)	ADC3 _EN (0+)	ADC2 _EN (0+)	ADC1 _EN (0+)	ADC0 _EN (0+)

Table 2-2. Data bits description for *CONTROL REGISTER*.

register bit(s)	default value on SIOX I//F reset	description
ADC3_EN .. ADC0_EN	{0,0,0,0}	Individual ADC-3..ADC-0 enable bits for data acquisition mode: 0 – disabled 1 – enabled
DAC3_EN .. DAC0_EN	{0,0,0,0}	Individual DAC-3..DAC-0 enable bits for data acquisition mode: 0 – disabled 1 – enabled
MODE_SEL	0	Data acquisition mode selector: 0 - "ASYNC-DATA" mode 1 - "SYNC-DATA" mode
FS_SEL1, FS_SEL-0	{0,0}	Sampling Frequency source selector for data acquisition mode: {0,0} - on-board sampling frequency generator (FSG) {0,1} - external sampling frequency input {1,0} - output of host SIOX interface timer (see table 2-1) {1,1} - data transmission event (FSX transmitter frame sync) over SIO-0 port from host of host SIOX interface
SDW_FMT-1..SDW_FMT-0	{0,0}	Serial transmitter/receiver data word format for data acquisition mode: {0,0} - 64 bits {0,1} - 32 bits {1,0} - 16 bits {1,1} - reserved, do not use
CLK_SEL	0	Source timing clock selector for data acquisition mode: 0 - on-board 15 MHz clock oscillator is used 1 - 15 MHz (±1%.) on-board clock is transmitter serial clock input (CLKX0) of SIO-0 port of host SIOX interface

For more details about *CONTROL REGISTER* data bits refer to section "DATA ACQUISITION MODES" later in this chapter.

FSG PERIOD REGISTER

24-bits period register for on-board sampling frequency (period) generator of *T/SDAS-ADDA4/16Q/200K* DCM comprises of three byte-wide registers (*FSG PERIOD REGISTER #0 ..#2)* . Data word formats for programming *FSG PERIOD REGISTERs #0..#2* registers via transmitter of SIO-0 SIOX port are presented below:

Transmitter data word for programming FSG PERIOD REGISTER #0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0	FSG_ PER-7 (0+)	FSG_ PER-6 (0+)	FSG_ PER-5 (1+)	FSG_ PER-4 (1+)	FSG_ PER-3 (0+)	FSG_ PER-2 (0+)	FSG_ PER-1 (0+)	FSG_ PER-0 (1+)

Transmitter data word for programming FSG PERIOD REGISTER #1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	1	FSG_ PER-15 (0+)	FSG_ PER-14 (0+)	FSG_ PER-13 (0+)	FSG_ PER-12 (0+)	FSG_ PER-11 (0+)	FSG_ PER-10 (0+)	FSG_ PER-9 (0+)	FSG_ PER-8 (0+)

Transmitter data word for programming FSG PERIOD REGISTER #2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	1	0	FSG_ PER-23 (0+)	FSG_ PER-22 (0+)	FSG_ PER-21 (0+)	FSG_ PER-20 (0+)	FSG_ PER-19 (0+)	FSG_ PER-18 (0+)	FSG_ PER-17 (0+)	FSG_ PER-16 (0+)

For more details about FSG and *FSG PERIOD REGISTERs #0..#2* refer to section "DATA ACQUISITION MODES" later in this chapter.

CAUTION

Default reset value for 24-bit combined FSG register is 000031H (decimal '49'), which corresponds to the FSG sampling frequency 200 kHz.

2.3   Data Acquisition Modes

Data acquisition modes for *T/SDAS-ADDA4/16Q/200K* DCM provide AD/DA signal acquisition and real-time digital data transfer to/from SIO-0 port of host *TORNADO* SIOX interface via on-board CU.

T/SDAS-ADDA4/16Q/200K DCM can operate either in the "ASYNC-DATA" or "SYNC-DATA" data acquisition modes. Particular data acquisition mode is selected by *MODE_SEL* bit of *CONTROL REGISTER* in accordance with table 2-1, which can be programmed during "CONTROL" mode.

Selected data acquisition mode is enabled by setting the corresponding TM/XIO output line of host *TORNADO* SIOX interface to logical '1' (refer to table 2-1 for details).

enabling individual A/D and D/A channels for signal acquisition

T/SDAS-ADDA4/16Q/200K DCM allows individual enable for every A/D and D/A channel to be involved into analog I/O signal acquisition. This is done via the corresponding bits of *CONTROL REGISTER* as the following:

- Bits *ADC0_EN..ADC3_EN* of *CONTROL REGISTER* individually enables A/D channels for input analog signal acquisition. Setting any of this bits to logical '0' disables the corresponding A/D channel and setting to '1' enables the corresponding A/D channel.
- Bits *DAC0_EN..DAC3_EN* of *CONTROL REGISTER* individually enables D/A channels for input analog signal acquisition. Setting any of this bits to logical '0' disables the corresponding D/A channel and setting to '1' enables the corresponding D/A channel.

sampling frequency selector

T/SDAS-ADDA4/16Q/200K DCM features programmable sampling frequency selector from different sources in accordance with the state of bits {*FS_SEL-1, FS_SEL-0*} of *CONTROL REGISTER*:

- 24-bit software programmable sampling frequency (period) generator (FSG) with 100 ns sampling period resolution, which allows on-board generation of 0.6 Hz .. 200 kHz sampling frequency
- external sampling frequency input (Ext-Fs)
- TM/XIO-0/1 timer output pin (host DSP timer output) of host SIOX interface of *TORNADO* DSP system (refer to table 2-1 for details how to select the TM/XIO timer output pin of host SIOX interface)
- FSX-0 strobe pulse (SIO-0 port transmitter frame synch strobe pulse, which appears on every transmission via SIO-0 port from host DSP) of host SIOX interface of *TORNADO* DSP system ("ASYNC-DATA" mode only).

CAUTION

Sampling frequency event for data acquisition modes is detected on the rising edge of selected sampling frequency source.

---

sampling frequency generator (FSG)

T/SDAS-ADDA4/16Q/200K DCM features programmable 24-bit sampling frequency (period) generator (FSG), which can generate sampling frequency within the 0.6 Hz .. 200 kHz frequency range with 100ns sampling period resolution.

The 24-bit sampling period {*FSG_PER-23..FSG_PER-0*} for FSG might be software programmed in "CONTROL" mode via three byte-wide *FSG PERIOD REGISTERs #0..#2* (refer to section "CONTROL MODE" earlier in this chapter).

> **CAUTION**
>
> Actual sampling period, which is generated by FSG, is defined as the following:
> *FSG_PER* = 100ns * [1+{*FSG_PER-23..FSG_PER-0*}]

> **CAUTION**
>
> The 24-bit {*FSG_PER-23..FSG_PER-0*} value, which is loaded to *FSG PERIOD REGISTER #0..#2*, should be equal or larger than decimal '49' value (i.e. sampling frequency should be 200 kHz or less).

> **CAUTION**
>
> Default reset value for 24-bit combined FSG register is decimal '49', which corresponds to sampling frequency 200 kHz, which can be generated by FSG.

Internal synchro-clock

T/SDAS-ADDA4/16Q/200K DCM allows software selection of source for internal synchro-clock, which is used for clocking on-board logic and for generation of CLKR0/CLKX0 serial receiver/transmitter clocks for SIO-0 port of host *TORNADO* SIOX interface.

> **CAUTION**
>
> In order to provide maximum 200 ksps sampling frequency for *T/SDAS-ADDA4/16Q/200K* DCM, the internal synchro-clock of *T/SDAS-ADDA4/16Q/200K* DCM must be 15 MHz ± 1%. However, in case maximum conversion rate is not a point, whereas interfacing to slow external DSP is most important, then the reduced internal synchro-clock may be used.

Selection of source for internal synchro-clock is performed by means of *CLK_SEL* bit of *CONTROL REGISTER*, and the following options are available:
- on-board 15 MHz crystal generator, which allows maximum 200 ksps analog I/O signal conversion rate (recommended default selection for *TORNADO-54x/6x/33/P6x/P33* boards)
- CLKX0 clock (SIO-0 port transmitter clock) of host SIOX interface of *TORNADO* DSP system (recommended selection for *TORNADO-31/E31* boards with 60 MHz TMS320C31 DSP).

For example, the CLKX0 clock source selection for internal synchro-clock is required for all *TORNADO-3x* boards with 60 MHz TMS320C31 DSP, since TMS320C31 DSP allows 15 MHz serial receiver/transmitter clock for DSP serial port only in case the DSP is used to generate this serial clock.

ASYNC-DATA mode

"ASYNC-DATA" mode features simple timing diagram, no-pipeline operation, and reduced maximum data acquisition rate. Timing diagram for "ASYNC-DATA" mode is presented at fig.2-3.
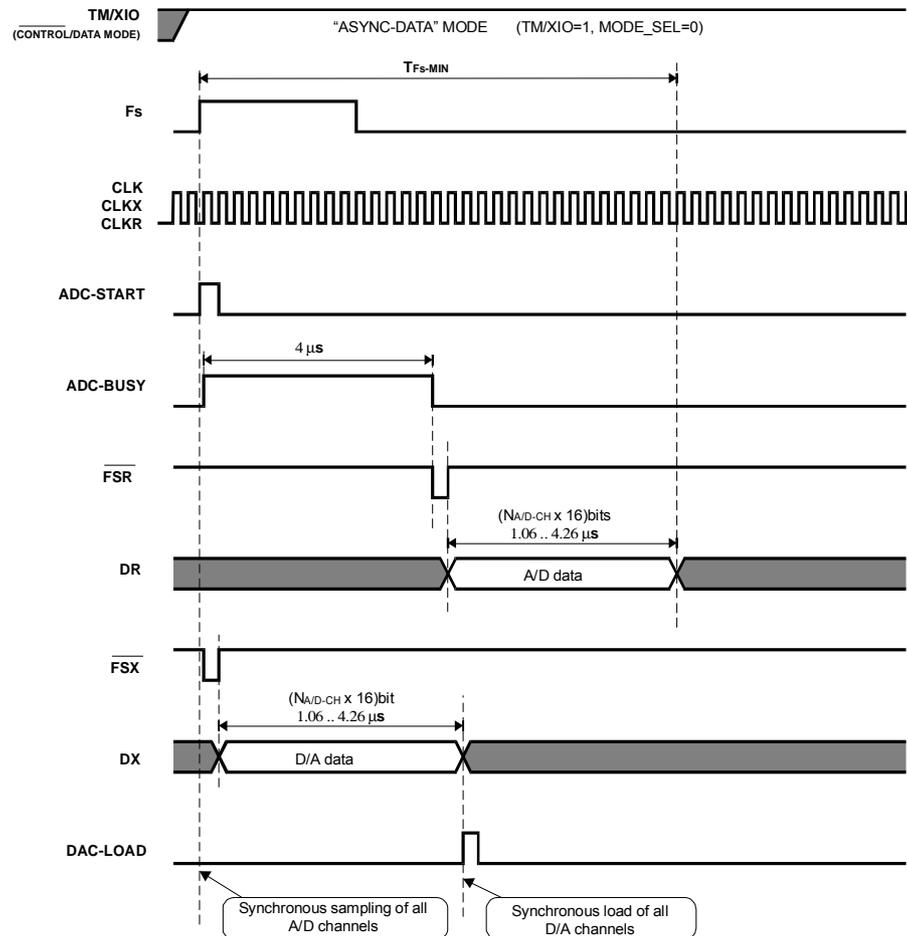
Fig. 2-3. Timing diagram for "ASYNC-DATA" mode.

Input analog signal acquisition in "ASYNC-DATA" mode is provided on sampling frequency event for all enabled A/D channels simultaneously with immediate A/D digital data transfer to SIO-0 port of host *TORNADO* SIOX interface via on-board CU. All sampling frequency events during A/D conversion and digital data transmission are ignored until transmission will be completed. Number of data bits, transmitted to the receiver of SIO-0 port of host *TORNADO* SIOX interface depends upon the number of enabled A/D channels, whereas the number of generated FSR strobe pulses (frame sync strobe pulses for receiver of SIO-0 port)

depends upon the number of enabled A/D channels and programmed serial data word length (see section "SERIAL DATA WORD FORMATS" later in this chapter).

Output analog signal acquisition in "ASYNC-DATA" mode is performed after all D/A digital input data from transmitter of SIO-0 port of host *TORNADO* SIOX interface will be received. The first FSX strobe pulse (frame synch strobe pulse for transmitter of SIO-0 port) is generated immediately after the sampling frequency event has been recognized, i.e. the transmission via transmitter of SIO-0 port is initiated immediately of the sampling frequency event. Number of data bits, transmitted from the SIO-0 port of host *TORNADO* SIOX interface depends upon the number of enabled D/A channels, whereas the number of generated FSR strobe pulses (frame sync strobe pulses for receiver of SIO-0 port) depends upon the number of enabled D/A channels and programmed serial data word length (see section "SERIAL DATA WORD FORMATS" later in this chapter).

CAUTION

The signal acquisition events for enabled A/D and D/A channels do not match each other
for "ASYNC-DATA" mode.

The sampling frequency event source for "ASYNC-DATA" mode can be either the output of the on-board FSG, or external sampling frequency input, or the TM/XIO timer output of host *TORNADO* SIOX interface, or the input FSX strobe pulse (frame synch strobe pulse for transmitter of SIO-0 port), as it is defined by bits {*FS_SEL-1, FS_SEL-0*} of *CONTROL REGISTER.* Note, that different sampling frequency source configurations require different serial port configuration for host *TORNADO* on-board DSP.

CAUTION

In case the sampling frequency source for "ASYNC-DATA" mode is configured as either output of on-board FSG, or external sampling frequency input, or the TM/XIO timer output of host *TORNADO* SIOX interface, then the FSX strobe pulse (frame synch strobe pulse for transmitter of SIO-0 port) is generated by *T/SDAS-ADDA4/16Q/200K* DCM, i.e. the serial port of host *TORNADO* on-board DSP must be configured for externally generated active low FSX/FSR, active high serial clock, and active high serial data.

In case the sampling frequency source for "ASYNC-DATA" mode is configured as the FSX strobe pulse (frame synch strobe pulse for transmitter of SIO-0 port), then the FSX strobe pulse must be generated by transmitter of SIO-0 port of host *TORNADO* SIOX interface, i.e. the serial port of host *TORNADO* on-board DSP must be configured for internally generated active low FSX, externally generated active low FSR, active high serial clock, and active high serial data.

The minimum sampling period (i.e. the maximum sampling frequency) for the "ASYNC-DATA" mode depends upon the number of enabled A/D channels and the frequency of synchro-clock. There is no effect on the number of enabled D/A channels.

Thus, with all A/D channels enabled and internally generated 15 MHz synchro-clock the minimum sampling period for the "ASYNC-DATA" mode is defined as the following:

$$4 \text{ us } + 66\text{ns} * (3+64) = 8.4 \text{ us}$$

which corresponds to 118 ksps maximum sampling rate.

Also, with one A/D channel enabled and internally generated 15 MHz synchro-clock the minimum sampling period for the "ASYNC-DATA" mode is defined as the following:

$$4 \text{ us } + 66\text{ns} * (3+16) = 5.25 \text{ us}$$

which corresponds to 190 ksps maximum sampling rate.

SYNC-DATA mode

"SYNC-DATA" mode features pipeline operation and delivers maximum available data acquisition rate. Timing diagram for "SYNC-DATA" mode is presented at fig.2-4.
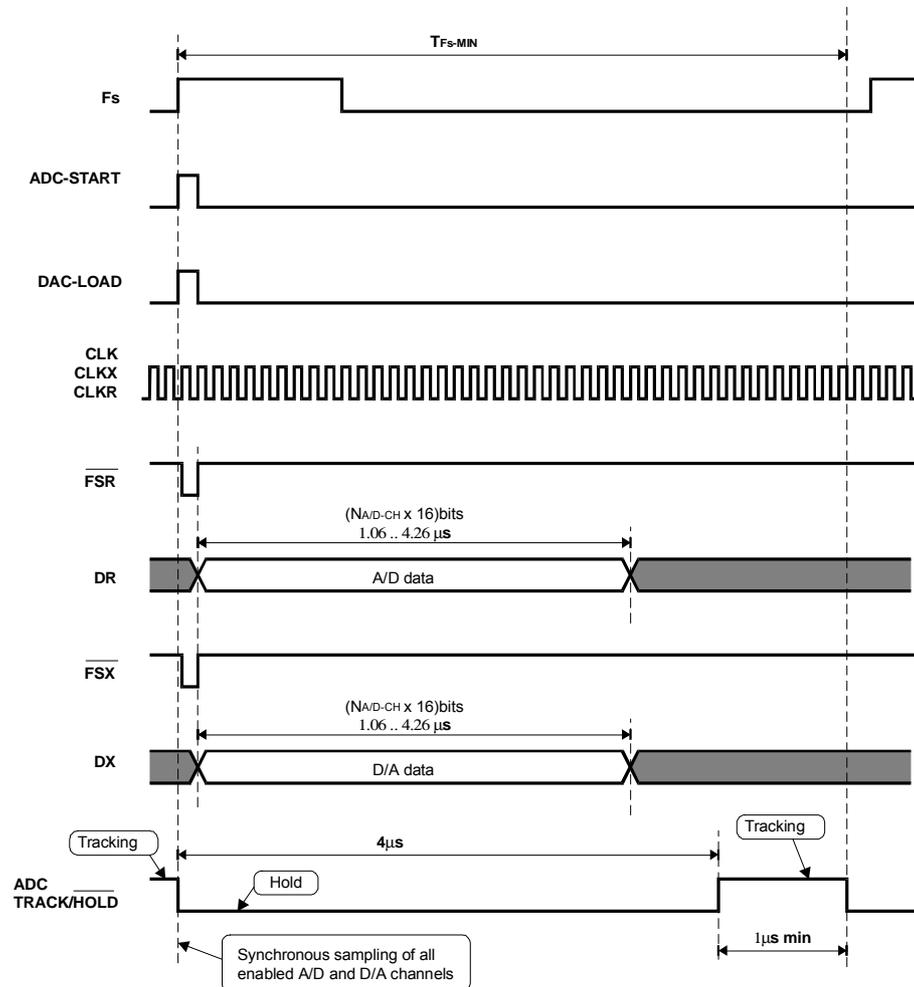

Fig. 2-4. Timing diagram for "SYNC-DATA" mode.

Both transmission and reception of data from/for ADC/DAC channels via receiver/transmitter of SIO-0 port of host *TORNADO* SIOX interface are initialized on the sampling frequency event.

Digital data, which is transmitted by *T/SDAS-ADDA4/16Q/200K* DCM to the receiver of SIO-0 port of host *TORNADO* SIOX interface, corresponds to enabled A/D channels, which have been acquired on the previous sampling frequency event. Number of data bits, transmitted to the receiver of SIO-0 port of host *TORNADO* SIOX interface depends upon the number of enabled A/D channels, whereas the number of generated FSR strobe pulses (frame sync strobe pulses for receiver of SIO-0 port) depends upon the number of enabled A/D channels and programmed serial data word length (see section "SERIAL DATA WORD FORMATS" later in this chapter).

Digital data, which is being received by *T/SDAS-ADDA4/16Q/200K* DCM from the transmitter of SIO-0 port of host *TORNADO* SIOX interface, corresponds to enabled D/A channels, which will be acquired on the next sampling frequency event. Number of data bits, transmitted from the SIO-0 port of host *TORNADO* SIOX interface depends upon the number of enabled D/A channels, whereas the number of generated FSR strobe pulses (frame sync strobe pulses for receiver of SIO-0 port) depends upon the number of enabled D/A channels and programmed serial data word length (see section "SERIAL DATA WORD FORMATS" later in this chapter).

CAUTION

Both input and output analog signal acquisitions in "SYNC-DATA" mode are performed on the sampling frequency event for all enabled A/D and D/A channels simultaneously.

The pipelined operation provides transmission of A/D data, which has been acquired on the previous sampling frequency event to SIO-0 port of host *TORNADO* SIOX interface, and provides reception of D/A data from SIO-0 port of host *TORNADO* SIOX interface, which will be loaded to D/A channels on the next sampling frequency event.

CAUTION

The minimum sampling period (i.e. the maximum sampling frequency) for the "SYNC-DATA" mode is defined by the frequency of internal synchro-clock and does not depend upon the number of enabled A/D and D/A channels.

With internally enabled 15 MHz synchro-clock or external 15MHz synchro-clock, the minimum sampling period is 5 us, which corresponds to 200 ksps maximum sampling rate.

The sampling frequency event source for "SYNC-DATA" mode can be either the output of on-board FSG, or external sampling frequency input, or the TM/XIO timer output of host *TORNADO* SIOX interface as it is defined by bits {*FS_SEL-1, FS_SEL-0*} of *CONTROL REGISTER.*

> **CAUTION**
>
> Both FSX strobe pulse (frame synch strobe pulse for transmitter of SIO-0 port) and FSR strobe pulse (frame synch strobe pulse for receiver of SIO-0 port) for "SYNC-DATA" mode are generated by *T/SDAS-ADDA4/16Q/200K* DCM, i.e. the serial port of host *TORNADO* on-board DSP must be configured for externally generated active low FSX/FSR, active high serial clock, and active high serial data.

2.3 Serial Data Word Formats and DSP Serial Port Configuration

T/SDAS-ADDA4/16Q/200K DCM is designed to install into SIOX site onto any *TORNADO* DSP system/controller/coprocessor with either 16-bit TMS320C54x DSP or 32-bit TMS320C3x/C6x DSP, and transmits digital AD/DA data over host *TORNADO* SIOX interface in serial format. Each received/transmitted serial data word is preceded by active low frame sync strobe pulse.

> **CAUTION**
>
> All serial data transfers (both for receiver and transmitter) via host *TORNADO* SIOX interface for *T/SDAS-ADDA4/16Q/200K* DCM for all operation modes are performed with active low frame synch strobe pulse, active high clock and active high data bits.

> **CAUTION**
>
> All serial data words (both for receiver and transmitter) via host *TORNADO* SIOX interface for *T/SDAS-ADDA4/16Q/200K* DCM are transmitted/received the MSB first.

DSP serial port configuration

Table 2-3 shows how to configure the corresponding serial port of *TORNADO* on-board DSP, which is routed to SIO-0 port of *TORNADO* on-board SIOX interface, for communication with *T/SDAS-ADDA4/16Q/200K* DCM in different operation modes.

Table 2-3. Host DSP on-chip serial port configuration for communication with *T/SDAS-ADDA4/16Q/200K* DCM in different operation modes.

Operation mode and specific condition	DSP FSX (transmitter frame sync strobe)	DSP CLKX (transmitter serial clock)	DSP transmitter data bits	DSP FSR (receiver frame sync strobe)	DSP CLKR (receiver serial clock)	DSP receiver data bits
"CONTROL" mode	active low internal	active high internal	16 active high	active low external	active high external	16
"ASYNC-DATA" mode with CLK_SEL=0 Fs_SEL= { {0,0} or {0,1} or {1,0} }	active low external	active high external	16/32/64 active high	active low external	active high external	16/32/64 active high
"ASYNC-DATA" mode with CLK_SEL=1 Fs_SEL= { {0,0} or {0,1} or {1,0} }	active low external	active high internal	16/32/64 active high	active low external	active high external	16/32/64 active high
"ASYNC-DATA" mode with CLK_SEL=0 Fs_SEL= {1,1}	active low internal	active high external	16/32/64 active high	active low external	active high external	16/32/64 active high
"ASYNC-DATA" mode with CLK_SEL=1 Fs_SEL= {1,1}	active low internal	active high internal	16/32/64 active high	active low external	active high external	16/32/64 active high
"SYNC-DATA" mode with CLK_SEL=0	active low external	active high external	16/32/64 active high	active low external	active high external	16/32/64 active high
"SYNC-DATA" mode with CLK_SEL=1	active low external	active high internal	16/32/64 active high	active low external	active high external	16/32/64 active high

Notes: 1. *CLK_SEL* is internal synchro-clock selector bit of *CONTROL REGISTER*.
2. *Fs_SEL* is the sampling frequency selector bit field ({*Fs_SEL-1, Fs_SEL-0* }) of *CONTROL REGISTER*.

serial data communication format for "CONTROL" mode

When *T/SDAS-ADDA4/16Q/200K* DCM operates in "CONTROL" mode, then transmitter of SIO-0 port of host *TORNADO* SIOX interface is used for programming the on-board *CONTROL REGISTER* and *FSR PERIOD REGISTER #0..#2*. Meanwhile, the receiver of SIO-0 port of host *TORNADO* SIOX interface can

be used for verification of the programmed contents of *CONTROL REGISTER* and *FSR PERIOD REGISTER #0..#2* (refer to section "CONTROL MODE" earlier in this chapter).

Serial data words, which are transmitted and received by *TORNADO* on-board DSP via SIO-0 port of SIOX interface, shall be 16-bit long, and are not software configurable.

> **CAUTION**
>
> In "CONTROL" mode the transmitter of DSP on-chip serial port, which is wired to SIO-0 port of host SIOX interface on *TORNADO* board, must be configured to 16-bit data format (active high), internally generated active high serial clock and internally generated active low frame sync strobe pulse (refer to table 2-3).
>
> In "CONTROL" mode the receiver of DSP on-chip serial port, which is wired to SIO-0 port of host SIOX interface on *TORNADO* board, must be configured to 16-bit data format (active high), external active high serial clock and external active low frame sync strobe pulse (refer to table 2-3).

serial data communication for data acquisition modes

When *T/SDAS-ADDA4/16Q/200K* DCM operates in either "ASYNC-DATA" or "SYNC-DATA" data acquisition mode, then transmitter and receiver of SIO-0 port of host *TORNADO* SIOX interface are used for real-time AD/DA digital data transfers (refer to section "DATA ACQUISITION MODES" earlier in this chapter).

> **CAUTION**
>
> For data acquisition modes the frame sync strobe pulse and serial clock for transmitter of DSP on-chip serial port, which is routed to SIO-0 serial port of host SIOX interface on *TORNADO* board., shall be configured to either external or internal source depending upon the operation mode and synchro-clock source as shown in table 2-3.
>
> For data acquisition modes the frame sync strobe and serial clock for receiver of DSP on-chip serial port, which is routed to SIO-0 serial port of host SIOX interface on *TORNADO* board., shall always be configured to external sources as shown in table 2-3.

The receiver of SIO-0 port of host *TORNADO* SIOX interface is used for real-time A/D digital data transfers, whereas transmitter of SIO-0 port of host *TORNADO* SIOX interface is used for real-time D/A digital data transfers. Number of received and transmitted data bits per every sampling frequency event depends upon the number of enabled A/D and D/A channels, as it is defined in *CONTROL REGISTER*.

CAUTION

Total number of data bits, transmitted by *T/SDAS-ADDA4/16Q/200K* DCM to the receiver of SIO-0 port of host *TORNADO* SIOX interface in data acquisition modes, is defined by the number of enabled A/D channels multiplied by 16 per one A/D channel, and can be either 0 bits, or 16 bits, or 32 bits, or 48 bits or 64 bits. Transmitted data for all enabled A/D channels is grouped into continuous stream.

The transmit sequence for A/D channels is defined by the sorted up-growing row of numbers of enabled A/D channels, i.e.:
if enabled, the A/D-0 channel is always transmitted first
if enabled, the A/D-1 channel is always transmitted prior A/D-2 and A/D-3 channels
if enabled, the A/D-2 channel is always transmitted prior A/D-3 channel
if enabled, the A/D-3 channel is always transmitted last.

CAUTION

Total number of data bits, received by *T/SDAS-ADDA4/16Q/200K* DCM from the transmitter of SIO-0 port of host *TORNADO* SIOX interface in data acquisition modes, is defined by the number of enabled D/A channels multiplied by 16 per one D/A channel, and can be either 0 bits, or 16 bits, or 32 bits, or 48 bits or 64 bits. Received data for all enabled A/D channels shall be grouped into continuous stream.

The receive sequence of D/A channels is defined by the sorted up-growing row of numbers of enabled D/A channels, i.e.:
if enabled, the D/A-0 channel is always received first
if enabled, the D/A-1 channel is always received prior D/A-2 and D/A-3 channels
if enabled, the D/A-2 channel is always received prior D/A-3 channel
if enabled, the D/A-3 channel is always received last.

Fig.2-5 shows several examples of serial port receiver timing diagrams, which correspond to real-time transmission or different configurations of enabled A/D channels.
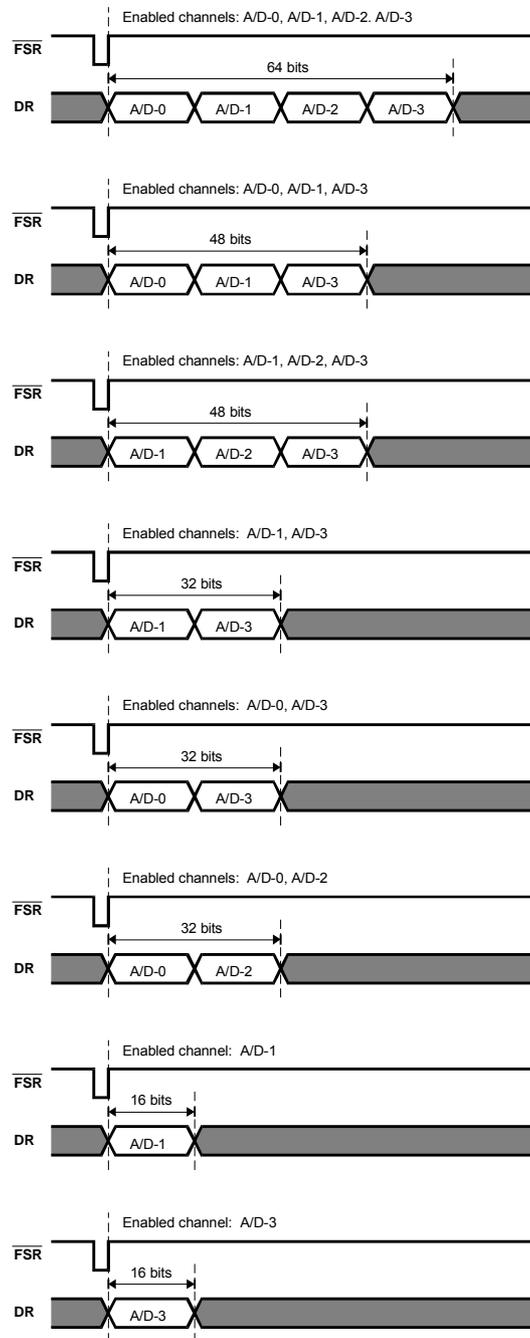
Fig. 2-5. Examples of timing diagram for transmission of A/D channels to the SIO-0 port receiver for data acquisition modes.

serial data word formats for data acquisition modes

T/SDAS-ADDA4/16Q/200K DCM offers software programmable selection of serial data words format for "ASYNC-DATA" and "SYNC-DATA" data acquisition modes.

This feature allows to adjust the number of generated frame sync pulses per serial data transmission for every sampling frequency event, and allows easy interfacing with different host *TORNADO* on-board DSPs, delivers optimal serial port transfer timing in accordance with the number of enabled AD/DA channels, and allows perfect synchronization between the DSP software and serial data transfer events.

Software programmable selection of serial data words format, which are received and transmitted by *T/SDAS-ADDA4/16Q/200K* DCM in "ASYNC-DATA" and "SYNC-DATA" data acquisition modes, is performed by means of {*SDW_FMT-1, SDW_FMT-0*} bits of *CONTROL REGISTER*. The following options are available:

- 64-bit serial data word with one receiver/transmitter frame sync strobe pulse (recommended default selection for *TORNADO-54x/6x* boards with TMS320C5402/C5410/C5416/C6x DSP with 32-bit McBSP multi-channel serial ports)
- 32-bit serial data word with one receiver/transmitter frame sync strobe pulse per every 32-bit serial data word (recommended selection for *TORNADO-3x* boards with 32-bit TMS320C3x DSP)
- 16-bit serial data word with one receiver/transmitter frame sync strobe pulse per every 16-bit serial data word (recommended selection for *TORNADO-542L/548/549* boards with TMS320C542/C548/C549 DSP with 16-bit BSP/TDM serial ports).

<div style="border:2px solid black; padding:10px;">

CAUTION

Selected serial data word format is used for both transmitted and received serial data streams, which are transferred over SIO-0 port of host *TORNADO* SIOX interface.

</div>

Correct selection of serial data word format for every particular DSP excludes incorrect serial data processing situations for DSP that might occur due to discontinued serial data transmission between two neighbour serial data packets, which correspond to neighbour sampling events.

Also, since *T/SDAS-ADDA4/16Q/200K* DCM allows software programmable individual enable bits for each of A/D and D/A channels, then the length of transmitted serial package must be configured depending upon the number of particular enabled A/D and D/A channels. For example, if all ADC-0..ADC-3 channels are enabled, then the number of transmitted data bits will be 4x16=64 bits. Also, if only ADC-1 and ADC-3 channels are enabled, then the number of transmitted data bits will be 2x16=32 bits.

64-bit serial data word format for data acquisition modes

The 64-bit serial data word format can be used with *TORNADO-54x/6x* boards only with TMS320C5402/C5410/C5416 and TMS320C6x DSP with McBSP multi-channel serial ports.

The 64-bit serial data word format is a recommended selection when three or four A/D and/or D/A channels are enabled simultaneously via the *CONTROL REGISTER*.

CAUTION

When the 64-bit serial data word format is selected, then only one transmit (FSX) and one receive (FSR) frame sync pulses are generated in every sampling frequency period.

64-bit serial data word format allows transmission of any number (1..4) of AD/DA channels in one serial data word.

Examples of timing diagram for transmission serial data via the receiver of SIO-0 port of host *TORNADO* SIOX interface for 64-bit serial data word format is shown at fig.2-6.
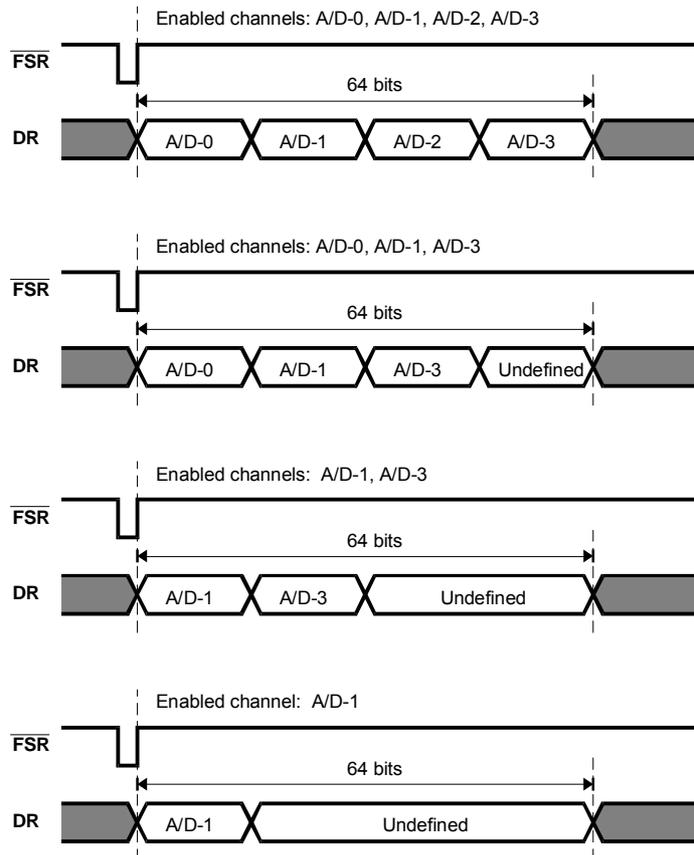

Fig. 2-6. Timing diagram for transmission serial data via the serial port receiver for 64-bit serial data word format.

32-bit serial data word format for data acquisition modes

The 32-bit serial data word format can be used with *TORNADO-3x/54x/6x* boards with TMS320C3x DSP and with TMS320C5402/C5410/C5416 and TMS320C6x DSP with McBSP multi-channel serial ports.

The 32-bit serial data word format is the recommended selection for *TORNADO-3x* boards in case two or more A/D and/or D/A channels are enabled simultaneously via the *CONTROL REGISTER*.

Also, the 32-bit serial data word format is the recommended selection for *TORNADO-54x/6x* boards with DSP on-chip McBSP serial ports in case two A/D and/or D/A channels are enabled simultaneously via the *CONTROL REGISTER*.

CAUTION

When the 32-bit serial data word format is selected, then one or two transmit (FSX) and one or two receive (FSR) frame sync pulses are generated in every sampling frequency period depending upon the number of enabled A/D and D/A channels correspondingly.

In case one or two A/D (D/A) channels are enabled, then only one FSX (FSR) pulse is generated and 32 bits are being transmitted.

In case three or four A/D (D/A) channels are enabled, then two FSX (FSR) pulses are generated and 64 bits are being transmitted.

Examples of timing diagram for transmission serial data via the receiver of SIO-0 port of host *TORNADO* SIOX interface for 32-bit serial data word format is shown at fig.2-7.
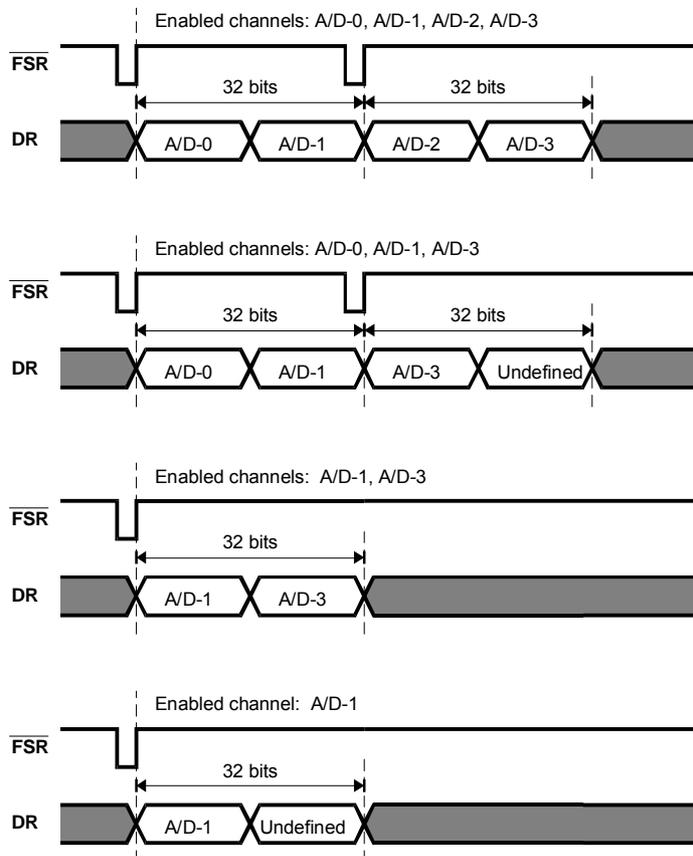
Fig. 2-7.   Timing diagram for transmission serial data via the serial port receiver for 32-bit serial data word format.

16-bit serial data word format for data acquisition modes

The 16-bit serial data word format can be used with *TORNADO-3x/54x/6x* boards only with TMS320C3x DSP, all TMS320C54x DSP and with TMS320C6x DSP.

The 16-bit serial data word format is the only allowed selection for *TORNADO-542L/548/549* boards with TMS320C542/C548/C549 DSP with 16-bit BSP/TDM serial ports.

Also, the 16-bit serial data word format is the recommended selection for *TORNADO-3x* boards and for *TORNADO-54x/6x* boards with DSP on-chip McBSP serial ports in case only one A/D and/or one D/A channels are enabled via the *CONTROL REGISTER*.

CAUTION

When the 16-bit serial data word format is selected, then 1..4 transmit (FSX) and 1..4 receive (FSR) frame sync pulses are generated in every sampling frequency period depending upon the number of enabled A/D and D/A channels correspondingly.

In case one A/D (D/A) channel is enabled, then only one FSX (FSR) pulse is generated and 16 bits are being transmitted.

In case two A/D (D/A) channels are enabled, then two FSX (FSR) pulse are generated and 32 bits are being transmitted.

In case three A/D (D/A) channels are enabled, then three FSX (FSR) pulse are generated and 48 bits are being transmitted.

In case all four A/D (D/A) channels are enabled, then four FSX (FSR) pulse are generated and 64 bits are being transmitted.

Examples of timing diagram for transmission serial data via the receiver of SIO-0 port of host *TORNADO* SIOX interface for 16-bit serial data word format is shown at fig.2-8.

Enabled channels: A/D-0, A/D-1, A/D-2, A/D-3

FSR

16 bits | 16 bits | 16 bits | 16 bits

DR | A/D-0 | A/D-1 | A/D-2 | A/D-3

Enabled channels: A/D-0, A/D-1, A/D-3

FSR

16 bits | 16 bits | 16 bits

DR | A/D-0 | A/D-1 | A/D-3

Enabled channels: A/D-1, A/D-3

FSR

16 bits | 16 bits

DR | A/D-1 | A/D-3

Enabled channel: A/D-1

FSR

16 bits

DR | A/D-1
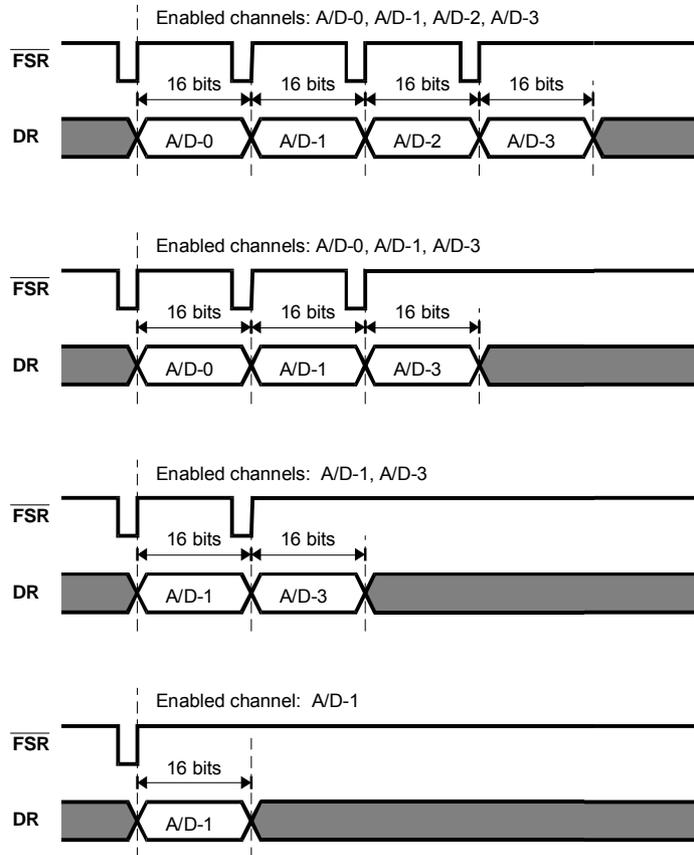
Fig. 2-8. Timing diagram for transmission serial data via the serial port receiver for 16-bit serial data word format.

2.4 Construction

T/SDAS-ADDA4/16Q/200K DCM (fig.1-1, fig.A-1) meets standard SIOX rev.B daughter-card form-factor. Construction of *T/SDAS-ADDA4/16Q/200K* DCM assumes that host *TORNADO* DSP system with *T/SDAS-ADDA4/16Q/200K* DCM installed fits into one ISA-bus slot of PC chassis.

Connection of *T/SDAS-ADDA4/16Q/200K* DCM to external analog I/O world is performed via the on-board JP2 connector, which is available via rear panel of host PC (if *T/SDAS-ADDA4/16Q/200K* is installed onto *TORNADO* DSP system for PC). Compatible cable with eight analog I/O RCA jacks and one external sampling frequency RCA jack is provided as standard with *T/SDAS-ADDA4/16Q/200K* DCM.

Chapter 3. Installation

This chapter contains information for installation and configuration of *T/SDAS-ADDA4/16Q/200K* DCM.

3.1   Installation

T/SDAS-ADDA4/16Q/200K DCM installs as SIOX daughter-card DCM onto *TORNADO* DSP system mainboard.

For installation of *T/SDAS-ADDA4/16Q/200K* DCM into SIOX site of *TORNADO* DSP system follow the recommendations below (fig.3-1):
1. Switch off the power of host PC.
2. Remove *TORNADO* mainboard from PC slot.
3. Take *T/SDAS-ADDA4/16Q/200K* DCM and slant it for about 30°..40° degrees refer to *TORNADO* mainboard. Insert JP2 external I/O connector of *T/SDAS-ADDA4/16Q/200K* DCM into the corresponding hole of mounting bracket of *TORNADO* DSP system.
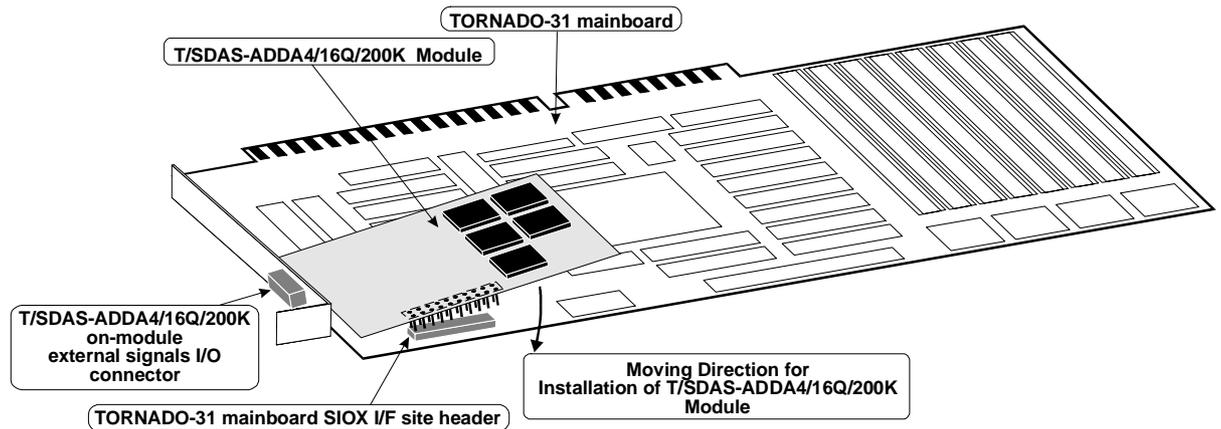

Fig. 3-1.   Installation of *T/SDAS-ADDA4/16Q/200K* DCM into SIOX site of *TORNADO* DSP system.

4. Rotate *T/SDAS-ADDA4/16Q/200K* DCM around mounting bracket and allocate pin #1 of JP1 connector of *T/SDAS-ADDA4/16Q/200K* DCM against pin #1 of SIOX interface header on *TORNADO* mainboard.

> **CAUTION**
>
> Female connector of host SIOX interface has 20 pins for *TORNADO-31/31Z/31M/32L/32LX/E31* DSP systems and controllers and 26 pins for *TORNADO-30/54x/6x/E6x/E54x* DSP systems and controllers. Pin #1 of host SIOX site connectors always fit into the same physical position on *TORNADO* DSP systems and controllers.
>
> Pin #1 of SIOX connector of *T/SDAS-ADDA4/16Q/200K* DCM must always plug into pin #1 of host SIOX site connector not regarding type of host *TORNADO* DSP systems or controller.
>
> Missing doing this will result in damage of *T/SDAS-ADDA4/16Q/200K* DCM and/or host *TORNADO* hardware.

5. Safely plug-in SIOX male header of *T/SDAS-ADDA4/16Q/200K* DCM into SIOX female header of *TORNADO* DSP system.
6. Screw external analog I/O connector shell of *T/SDAS-ADDA4/16Q/200K* DCM to the mounting bracket of *TORNADO* DSP system.
7. Configure on-board jumper J1 for selection the TM/XIO output of host SIOX interface, which will select between the "CONTROL" and data acquisition modes (see table 2-1).
8. Install *TORNADO* board into PC slot and screw it to rear panel of PC.
9. Connect the plug to external analog I/O connector of *T/SDAS-ADDA4/16Q/200K* DCM.
10. Switch on power of host PC.

3.2   Connection to external signal I/O equipment

Connection of *T/SDAS-ADDA4/16Q/200K* DCM to external analog I/O equipment is performed by means of on-board JP2 connector (fig.A-1) and external I/O cable set.

> **CAUTION**
>
> It is highly recommended to plug-in and unplug external I/O cable set into/from on-board JP2 connector of *T/SDAS-ADDA4/16Q/200K* DCM when host *TORNADO* power is switched off.
>
> The ground signal of *T/SDAS-ADDA4/16Q/200K* DCM has no halvanic isolation from host *TORNADO* and/or PC ground signal and chassis.

CAUTION

When connecting external analog I/O equipment to *T/SDAS-ADDA4/16Q/200K* DCM you should be aware that AIN-0..3 analog inputs and AOUT-0..3 analog outputs of *T/SDAS-ADDA4/16Q/200K* DCM are DC coupled. If required, external DC isolation capacitors should be used.

External I/O cable set for *T/SDAS-ADDA4/16Q/200K* DCM uses standard miniature banana jacks for connection to external analog I/O equipment with single-ended I/O signals. This set comprises of 8 jacks:

- AIN-0..3 analog in channels #0..#3
- AOUT-0..3 analog out channels #0..#3
- EXT-Fs external sampling frequency input

Appendix A.   On-board Connectors and Jumpers

This appendix contains a summary for the on-board connectors, configuration jumpers and configuration switches for *T/SDAS-ADDA4/16Q/200K* DCM.

The on-board connectors and configuration jumpers are presented at fig.A-1.
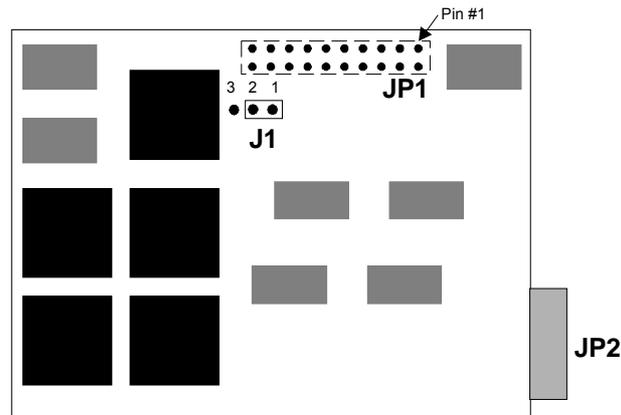
Fig. A-1.   On-board connectors and configuration jumpers for *T/SDAS-ADDA4/16Q/200K* DCM*.*

A.1   Configuration Jumpers

Table A-1 specifies how to set on-board configuration jumpers.

Table A-1.   Configuration jumpers for *T/SDAS-ADDA4/16Q/200K* DCM.

Jumper	Description
J1	Host SIOX TM/XIO output line selector, which is used for selection between "CONTROL" and data acquisition modes (see table 2-1 for more details):
1-2	- TM/XIO-0 output of host SIOX interface is used
2-3	- TM/XIO-1 output of host SIOX interface is used

Notes: 1. Highlighted configurations correspond to the factory setting.

A.2   On-board Connectors

Table A-2 contain the list of on-board connectors.

Table A-2.   On-board connectors of *T/SDAS-ADDA4/16Q/200K* DCM.

Connector	description
JP1	SIOX interface site male header.
JP2	External analog I/O connector.

Pinout of JP1 host SIOX connector is presented in the user's guide of host *TORNADO* DSP system or controller, which is used for installation of *T/SDAS-ADDA4/16Q/200K* DCM.

Pinout for external I/O connector

Pinout of JP2 external I/O connector for *T/SDAS-ADDA4/16Q/200K* DCM is presented at fig.A-2, and description of signals is presented in table A-3.

The connector p/n for JP2 is DHA-RA20 female half-pitch connector from DDK Ltd manufacturer. P/n for compatible plug-in connector is DHA-PC20. In case customer needs to design his own application specific cable for connection to *T/SDAS-ADDA4/16Q/200K* DCM, then compatible plug-in connectors for JP2 are available from MicroLAB Systems upon request.
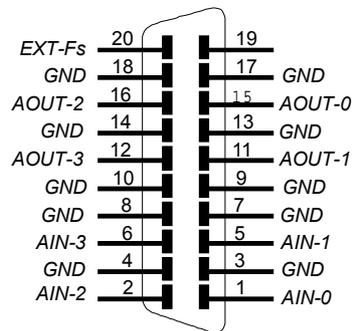

Fig. A-2.   Pinout for JP2 external I/O connector of *T/SDAS-ADDA4/16Q/200K* DCM.

Table A-3.   Signal description for JP2 external I/O connector of *T/SDAS-ADDA4/16Q/200K* DCM.

Signal name	type	description
AIN-0 AIN-1 AIN-2 AIN-3	AI	Analog input channels A/D-0..A/D-3.

AOUT-0 AOUT-1 AOUT-2 AOUT-3	AO	Analog output channels A/D-0..A/D-3.
EXT-Fs	TTL/IN	External sampling frequency input.
GND	-	Ground.

Notes: 1. Signal types: *AI* - analog input; *AO* - analog output; *TTL/IN* - TTL compatible digital input.

Appendix B. SIOX Rev.B Interface Site

This appendix contains information about *TORNADO* SIOX rev.B interface site specifications. This description is general to all *TORNADO* DSP systems/controllers/coprocessors, whereas different *TORNADO* boards with different DSP platforms may differ in the number and in the on-board routing of SIOX serial ports, timer/IO pin specifications. Refer to your particular *TORNADO* user's guide for more details.

B.1   General Description

TORNADO architecture provides expansion of the on-board DSP I/O resources via on-board serial I/O expansion interface sites (SIOX-A and SIOX-B) (fig.B-1), which are designed to carry compatible DCMs (DCM).

Fig.B-1.   *TORNADO-54x* board with two SIOX sites.

Some *TORNADO* boards (typically *TORNADO* DSP systems for PC) provide two SIOX interface sites, whereas other *TORNADO* boards (typically *TORNADO* stand-alone DSP controllers and DSP coprocessors) provide only one SIOX site.

TORNADO SIOX rev.B interface site comprises of signals for one or two SIO-0/SIO-1 logical serial ports, timers/IO pins, DSP interrupts, and host power supplies.

CAUTION

In case *TORNADO* on-board DSP features two or more on-chip serial ports (TMS320C30, TMS320C54x, TMS320C6x), then *TORNADO* on-board SIOX sites provides two SIO-0 and SIO-1 serial ports and the SIOX site headers are 26-pin headers.

In case *TORNADO* on-board DSP features only one on-chip serial ports (TMS320C31, TMS320C32), then *TORNADO* on-board SIOX sites provides only one SIO-0 serial port and the SIOX site headers are 20-pin headers.

Both *TORNADO* on-board SIOX-A and SIOX-B interface sites feature identical pinout control and may only differ in the routing of DSP physical serial ports to SIO-0 and SIO-1 logical serial ports. If *TORNADO* on-board DSP features two or more on-chip serial ports (TMS320C30, TMS320C54x, TMS320C6x), then DSP serial ports routing is performed on *TORNADO* mainboard, and allows simultaneous operation of two or more SIOX DCM, which are routed to different DSP serial ports.

B.2   SIOX Site Connector and Signals

TORNADO SIOX rev.B interface site comprises of signals for SIO-0 and SIO-1 logical serial ports, DSP on-chip TM/XIO-0/1 timers/IO pins, three DSP interrupts, SIOX reset control, and power ±5V/±12V host power supplies.

TORNADO on-board SIOX site connector with two serial ports

TORNADO on-board SIOX site connector with two serial ports is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM should be the industry standard either 26-pin 0.1"x0.1"male header (in case both SIO-0 and SIO-1 serial ports are utilized on SIOX plugged-in DCM) or 20-pin 0.1"x0.1"male header (in case only SIO-0 serial port is utilized on SIOX plugged-in DCM).

SIOX site connector pinout with two serial ports is shown at fig.B-2 and signal specifications are listed in table B-1.
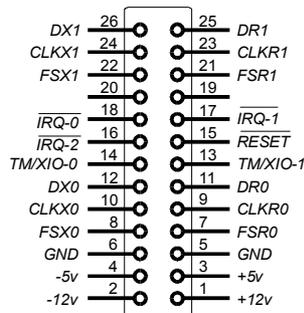

Fig.B-2.   TORNADO on-board SIOX connector pinout with two serial ports (top view).

TORNADO on-board SIOX site connector with one serial port

TORNADO on-board SIOX site connector with one serial port is an industry standard dual-row 20-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM should be the industry standard 20-pin 0.1"x0.1"male header.

SIOX site connector pinout with one serial ports is shown at fig.B-3 and signal specifications are listed in table B-1.
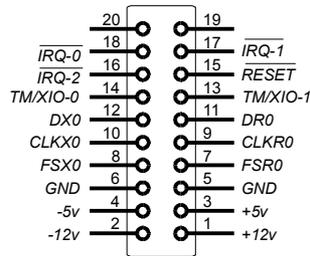

Fig.B-3. TORNADO on-board SIOX connector pinout with one serial port (top view).

SIOX site signal description

Description for SIOX interface site signals is presented in table B-1.

Table B-1.   SIOX interface signal description.

SIOX signal name	signal type	description
*SIO-0 port control*		
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX site..
DR0 FSR0 CLKR0	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX site..
SIO-1 port control *(available in SIOX site connector with two serial ports only)*		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX site..
DR1 FSR1 CLKR1	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX site..

DSP Timers/IO, DSP Interrupt Requests and SIOX Reset		
TM/XIO-0	I/O/Z	This signal is typically connected to the DSP on-chip timer-0 I/O pin and can be software configured by DSP as either timer or I/O pin.
TM/XIO-1	I/O/Z	This signal is typically connected to the DSP on-chip timer-1 I/O pin and can be software configured by DSP as either timer or I/O pin.
$\overline{RESET}$	O	Active low SIOX reset signal. Some *TORNADO* boards (for example *TORNADO-3x* boards) wires this signal directly from the DSP reset signal and SIOX plugged-in DCM reset is performed simultaneously with *TORNADO* on-board DSP reset, however other *TORNADO* boards (for example *TORNADO-54x/6x* etc. boards) features dedicated SIOX site reset signal, which is controlled by TORNADO on-board DSP for better synchronization between the DSP software and SIOX DCM operation.
$\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, $\overline{IRQ\text{-}2}$	I	Active low external interrupt request lines for TORNADO on-board DSP. These line are pulled up.
Power Supplies		
GND		Ground.
+5v		+5v
+12v		+12v
-5v		-5v
-12v		-12v

Note:
1.   Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
1.   All logical signal levels and load currents correspond to that for CMOS/TTL signals.

SIOX site signal levels

Signal levels for SIOX interface signals correspond to that for the CMOS/TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

CAUTION

Some *TORNADO* boards (*TORNADO-3x/542L/E31*) provide SIOX interface signal levels for CMOS/TTL only, whereas other *TORNADO* boards (*TORNADO-54xx/6x/E6x/P6x*) provide SIOX interface signal levels universal for both 3V TLL and standard TTL. Refer to documentation for your particular *TORNADO* board for information about SIOX interface signal levels.

B.3   Physical Dimensions for SIOX DCM

Physical dimensions for SIOX DCM are presented at fig.B-4. This information is intended for those customers, who need to design customized SIOX DCMs.
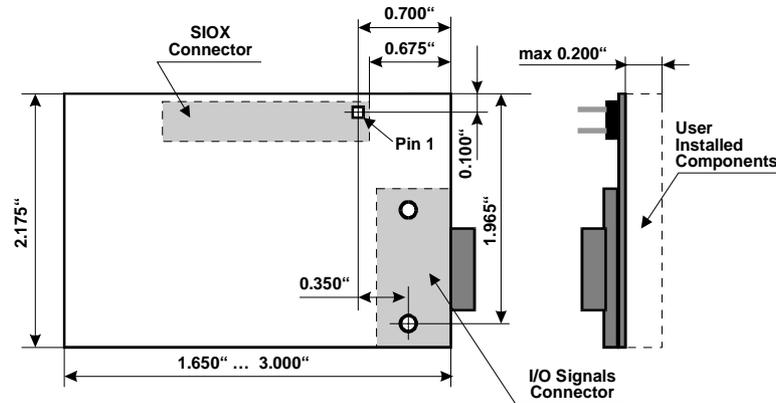
SIOX connector: 20-pin or 26-pin straight dual-row mail header
(0.025" Sq., 0.1"x0.1" pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.B-4.   Physical dimensions for SIOX DCM.