

T/SDAS-AD1/14/300K-DA1/16/300K

14/16-bit AD/DA Instrumentation SIOX rev.B DCM
for *TORNADO* DSP Systems, Controllers and Coprocessors

User's Guide

covers:
T/SDAS-AD1/14/300K-DA1/16/300K rev.2A

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About this Document

This user's guide contains description for *T/SDAS-AD1/14/300K-DA1/16/300K* AD/DA SIOX daughter-card DCM (DCM) for *TORNADO* DSP systems/controllers/coprocessors from MicroLAB Systems Ltd.

This document does not include detail description neither for *TORNADO* systems, nor for TI DSP and corresponding software and hardware applications. To get the corresponding information refer to the following documentation:

1. ***TMS320C3x User's Guide.*** Texas Instruments Inc, SPRU031C, USA, 1992.
2. ***TMS320C54x. CPU and Peripherals. Reference Guide.*** Texas Instruments Inc, SPRU131D, USA, 1997.
3. ***TMS320C6x. CPU and Instruction Set. Reference Guide.*** Texas Instruments Inc, SPRU189C, USA, 1998.
4. ***TORNADO-3x. User's Guide.*** MicroLAB Systems, 1998.
5. ***TORNADO-P33. User's Guide.*** MicroLAB Systems, 2000.
6. ***TORNADO-54x. User's Guide.*** MicroLAB Systems, 1998.
7. ***TORNADO-6x. User's Guide.*** MicroLAB Systems, 1998.
8. ***TORNADO-P6x. User's Guide.*** MicroLAB Systems, 1999.
9. ***TORNADO-PX31DP. User's Guide.*** MicroLAB Systems, 1996.
10. ***TORNADO-SX30. User's Guide.*** MicroLAB Systems, 1996.
11. ***TORNADO-E31. User's Guide.*** MicroLAB Systems, 1996.
12. ***TORNADO-E33. User's Guide.*** MicroLAB Systems, 2000.
13. ***TORNADO-EL31. User's Guide.*** MicroLAB Systems, 1996.
14. ***TORNADO-E6x. User's Guide.*** MicroLAB Systems, 1998.

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Chapter 1. Introduction

This chapter contains general description for *T/SDAS-AD1/14/300K-DA1/16/300K* SIOX daughter-card module (DCM) for *TORNADO* DSP systems/controllers/coprocessors.

1.1 General Information

T/SDAS-AD1/14/300K-DA1/16/300K DCM (fig.1-1) is a high-accuracy and high-speed AD/DA instrumentation SIOX (serial I/O expansion) DCM with one A/D channel and one D/A channel, which can be used with *TORNADO* DSP systems, *TORNADO-E* stand-alone DSP controllers and *TORNADO-PX/SX* DSP coprocessors from MicroLAB Systems Ltd.

Although *T/SDAS-AD1/14/300K-DA1/16/300K* DCM has been designed for high-accuracy high-speed single-channel AD/DA instrumentation applications, it can be used for many other applications with similar requirements for the AD/DA front-end.



Fig. 1-1. *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

Installation

T/SDAS-AD1/14/300K-DA1/16/300K DCM installs as SIOX DCM (fig.1-2) into the SIOX site onto *TORNADO* DSP mainboard. If required, the *T/SU-X* SIOX extender can be used for remote connection to SIOX interface of *TORNADO* mainboard.



Fig. 1-2. T/SDAS-AD1/14/300K-DA1/16/300K DCM installed onto TORNADO-54x mainboard with external I/O cable set.

Overview

T/SDAS-AD1/14/300K-DA1/16/300K DCM comprises of one A/D and one D/A channels of instrumentation quality and features:

- one 14-bit 300ksps ADC
- four 16-bit 300ksps DAC
- programmable high-resolution sampling frequency generator
- control unit.

On-board A/D and D/A channels feature 14-bit and 16-bit resolution correspondingly, excellent linearity, low THD, and up to 300ksps sampling frequency.

On-board sampling frequency (period) generator of T/SDAS-AD1/14/300K-DA1/16/300K DCM can be software programmed to any value in the range 47 Hz .. 300 kHz with high sampling period resolution. Also, either external sampling frequency input or output of any host SIOX interface timers can be selected as the sampling frequency source.

T/SDAS-AD1/14/300K-DA1/16/300K DCM operates in “ASYNC” and “SYNC” modes, allows individual programmable enable for A/D and D/A channels in “ASYNC” mode, and features synchronous sampling of A/D and D/A channels in “SYNC” mode.

External signal I/O

Connection of T/SDAS-AD1/14/300K-DA1/16/300K DCM to external analog I/O world is performed via the on-board I/O JP2 connector, which is available via rear panel of host PC (if T/SDAS-AD1/14/300K-DA1/16/300K DCM is installed onto TORNADO DSP system for PC).

Applications

T/SDAS-AD1/14/300K-DA1/16/300K AD/DA DCM has been designed for high-accuracy high-speed single-channel instrumentation applications as well as for other general signal processing applications (biomedical, speech/audio, etc), which feature similar AD/DA requirements.

1.2 Technical Specifications

The following are technical specifications for T/SDAS-AD1/14/300K-DA1/16/300K AD/DA DCM for temperature of external environment +25°C.

<u>parameter description</u>	<u>parameter value</u>
<i>A/D channel:</i>	
number of ADC channels	1
input signal range	$\pm 5\text{ V} \pm 0.2\%$
input impedance for analog inputs	1 MOhm
resolution	14 bits
zero offset error	$\pm 10\text{ mV max}$
differential nonlinearity	$\pm 1.5\text{ LSB (typ)}$
integral nonlinearity	$\pm 2\text{ LSB (typ)}$
THD	-85 dB (typ)
A/D conversion time	2.8 μS
A/D input tracking time	400 nS min
analog input buffer settling time	2 $\mu\text{s (typ)}$
<i>D/A channel</i>	
number of DAC channels	1
output signal range for LINE-OUT output	$\pm (5\text{ V} \pm 3\text{ mV}) @ 5\text{ kOhm}$
resolution	16 bits
zero offset error	$\pm 1\text{ mV max}$
differential nonlinearity	$\pm 1/2\text{ LSB (typ)}$

integral nonlinearity	$\pm 0.02\%$ FSR (typ)
output voltage settling time	2 μ s (typ)

Programmable Sampling Frequency Generator (PFG)

output frequency range for sampling frequency generator	47 Hz .. 300 kHz
reference clock frequency	10 MHz
stability of reference clock frequency	± 50 ppm
PLL lock time to 0.1% of output clock frequency	< 200 μ s
period jitter	± 40 pS (MSV) ± 120 pS (absolute)

common parameters:

AD/DA conversion time in "ASYNC" mode	3.2 μ s (D/A) 3.4 μ s (A/D)
AD/DA conversion time in "SYNC" mode	3.2 μ s
sampling frequency synchronization jitter in "SYNC" mode	200 nS max
maximum clock frequency at external sampling frequency input and at the SIOX TM/XIO (timer) output pin when those are configured as sampling frequency source in "SYNC" mode	≤ 294 kHz
number of bits in SIO-0 transmitter data packet	32 bits @ "ASYNC" mode 16 bits @ "SYNC" mode
number of bits in SIO-0 receiver data packet	16 bits
serial clock for SIO-0 transmitter (generated by DCM)	10 MHz
serial clock for SIO-0 receiver (generated by DCM)	5 MHz
logical low level for external clock frequency input	≤ 0.6 V
logical high level for external clock frequency input	≥ 2.4 V

physical and power:

Dimensions	55mm x 58mm (SIOX rev.B DCM)
power consumption via SIOX I/F	+5v @ 100mA +12v @ 50mA -12v @ 35 mA

Chapter 2. Technical Description

This chapter contains detail technical description for architecture and construction of *T/SDAS-AD1/14/300K-DA1/16/300K* SIOX AD/DA DCM.

2.1 Block Diagram

Basic configuration and connectivity of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM is presented at fig.2-1.

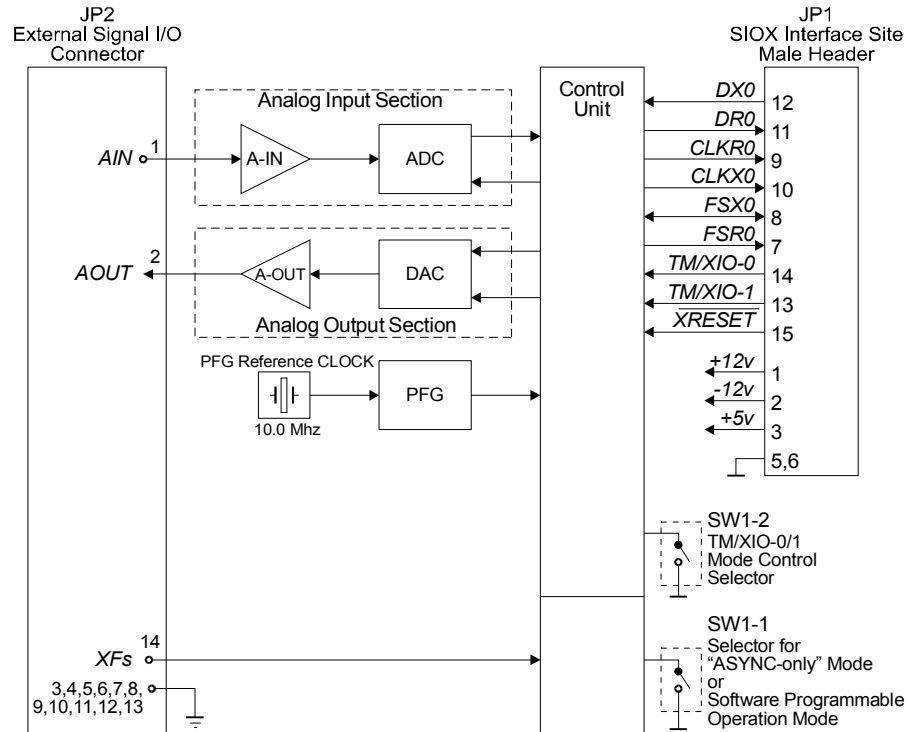


Fig. 2-1. Block diagram of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

T/SDAS-AD1/14/300K-DA1/16/300K DCM installs as SIOX (serial I/O expansion interface) DCM onto *TORNADO* mainboard and assumes that communication with *TORNADO* on-board DSP is provided via the DSP on-chip serial port.

T/SDAS-AD1/14/300K-DA1/16/300K DCM comprises of:

- analog input section, which includes 14-bit 300ksps ADC and input analog buffer
- analog output section, which includes 16-bit 300ksps DAC and output analog buffer
- programmable sampling frequency generator (PFG)
- control unit (CU)
- host SIOX interface header for installation onto *TORNADO* DSP systems.

analog input section

Analog input section of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM includes one A/D channel, and is designed for analog-to-digital conversion of input analog signal from analog input (AIN) and further transmission of digital code to the receiver of SIO-0 port of host SIOX interface of *TORNADO* DSP system.

Analog input section comprises of the following components:

- input analog buffer (A-IN)
- 14-bit 300ksps analog-to-digital converter (ADC).

The A-IN input analog buffer is designed for interfacing to external ± 5 V analog input signals and feature high input impedance 1 MOhm and over-voltage protection at ± 12.5 V signal level. The settling time for analog input buffer is typically 2 μ s to 0.01% accuracy. The AIN analog input is DC coupled with the ADC input and can process external DC/AC analog signals.

The ADC chip of analog input section of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM is 14-bit 300ksps ADC, which features excellent linearity and high-accuracy at high conversion rates. ADC transfers data in serial format via CU to the receiver of SIO-0 port of host SIOX interface of *TORNADO* DSP system.

analog output section

Analog output section of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM includes one D/A channel, and is designed for conversion of digital code from transmitter of SIO-0 port of host SIOX interface of *TORNADO* DSP system into output analog signal (AOUT)).

Analog output section comprises of the following components:

- 16-bit digital-to-digital converter (DAC)
- output analog buffer (A-OUT)

The analog output section of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM includes 16-bit 300ksps DAC, which features excellent linearity and high-accuracy at high conversion rates. Input data for DAC is unpacked by CU from the serial data stream from the transmitter of SIO-0 port of host SIOX interface of *TORNADO* DSP system.

A-OUT analog output buffer provides ± 5 V analog output and is used for interfacing to external low-impedance loads with minimum signal distortions.

operation modes

T/SDAS-AD1/14/300K-DA1/16/300K DCM can operate in the following modes:

- “ASYNC” (asynchronous) mode, which can be used for asynchronous software initialized A/D and D/A conversions at reduced data rate, and to configure *T/SDAS-AD1/14/300K-DA1/16/300K* DCM for operation in “SYNC” mode
- “SYNC” mode, which provides AD/DA signal acquisition at full sampling rate and synchronous sampling of A/D and D/A channels, and with hardware generated sampling frequency with low sampling period jitter.

Setting of particular operation mode can be done by means of on-board SW1-1 and SW1-2 switches and software programmable TM/XIO-0/1 SIOX timer output pins in accordance with table 2-1.

Table 2-1. Operation mode programming.

SW1-1 switch state		TM/XIO-0 output pin of host SIOX I/F	TM/XIO-1 output pin of host SIOX I/F	TM/XIO timer output of host SIOX I/F, which can be used as sampling frequency source in “SYNC” mode in case {FS_SEL1, FS_SEL0} bits of CNTR_RG_WR_CMND command are set to the {0,1} state	operation mode
SW1-1	SW1-2				
“ASYNC”-only operation mode					
OFF	X	x	x	-	“ASYNC”
Software programmable operation mode					
ON	OFF	0 ²⁾	x	TM/XIO-1	“ASYNC”
		1 ²⁾	x	TM/XIO-1	“SYNC”
ON	ON	x	0 ³⁾	TM/XIO-0	“ASYNC”
		x	1 ³⁾	TM/XIO-0	“SYNC”

Notes:

1. Logical states: '0' - logical '0'; '1' - logical '1'; 'x' - don't care.
2. SIOX TM/XIO-0 pin must be configured as output pin.
3. SIOX TM/XIO-1 pin must be configured as output pin.
4. Highlighted configuration corresponds to default factory setting and is set on SIOX reset condition.

SW1-1 is used to select between either “ASYNC”-only operation mode (SW1-1 is in the OFF state) and software programmable operation mode (SW1-1 is in the ON state). SW1-2 is used only in case SW1-1 is in the ON state, and defines SIOX TM/XIO pin (#0 or #1), which will be used for software selection between “ASYNC” and “SYNC” mode.

CAUTION

In case SW1-1 is set in the ON state and SW1-2 is in the OFF state, which corresponds to software programmable “ASYNC”/“SYNC” mode via SIOX TM/XIO-0 pin signal, then TM/XIO-0 pin must be configured as output pin by host **TORNADO** on-board DSP.

In case SW1-1 is set in the ON state and SW1-2 is in the ON state, which corresponds to software programmable “ASYNC”/“SYNC” mode via SIOX TM/XIO-1 pin signal, then TM/XIO-1 pin must be configured as output pin by host **TORNADO** on-board DSP.

“ASYNC” mode must be used for those DSP applications, which either require eventual A/D and D/A conversions only, or do not require stable hardware defined sampling frequency with low sampling period jitter.

The A/D and D/A sampling event for “ASYNC” mode is defined by the DSP generated active FSX condition, i.e. by transmission of *DAC_WR_CMND* and *ADC_RD_CMND* software commands over SIO-0 port of SIOX interface, which simplifies programming of DSP software applications. Refer to the corresponding section below in this chapter for more details.

“SYNC” mode must be used for those DSP applications, which require stable sampling frequency with low sampling period jitter. The sampling frequency for “SYNC” mode can be defined from different hardware sources. Programming of DSP software applications for “SYNC” mode typically requires either interrupts or DMA programming, and is more complicated than that for “ASYNC” mode. Refer to the corresponding section below in this chapter for more details.

sampling frequency generator (PFG) and sampling frequency selector for “SYNC” mode

T/SDAS-AD1/14/300K-DA1/16/300K DCM features programmable AD/DA sampling frequency source selector, which allows to select the source for sampling frequency clock in “SYNC” mode from the following sources:

- software programmable sampling frequency generator (PFG), which allows to set output sampling frequency clock within the 47 Hz .. 300 kHz range with high resolution. PFG can be programmed via *PFG_WR_CMND* command in “ASYNC” mode.
- external sampling frequency input (XFs), which is available via JP2 external signal I/O connector
- TM/XIO-0/1 pin (host DSP timer output) of host SIOX interface of *TORNADO* DSP system.

Particular sampling frequency source selection for “SYNC” mode is performed by the {*FS_SEL-1*, *FS_SEL-0*} bits of *CNTR_RG_WR_CMND* command in “ASYNC” mode.

control unit (CU)

On-board Control Unit (CU) of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM provides DCM configuration via a set of commands in “ASYNC” mode and generates corresponding timing and provides serial data-path handling during “ASYNC” and “SYNC” operation modes.

2.2 “ASYNC” Operation Mode

“ASYNC” mode of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM must be used for asynchronous software initialized A/D and D/A conversions at reduced data rate and to configure DCM for operation in “SYNC” mode.

setting “ASYNC” operation mode

“ASYNC” mode can be set either in case on-board SW1-1 switch is set to the “ASYNC”-only mode state (table 2-1), or in case on-board SW1-1 switch is set to the software programmable operation mode state and the corresponding TM/XIO line, which is selected via SW1-2 switch, is set to the ‘0’ state.

general description

When configured in “ASYNC” mode, *T/SDAS-AD1/14/300K-DA1/16/300K* DCM interprets incoming data from the transmitter of SIOX SIO-0 port as commands, and decodes and executes received command during its reception.

The following is the list of commands for “ASYNC” mode, which are described in details in the corresponding subsections later in this section:

- *DAC_WR_CMND* command, which is used to write data to DAC
- *CNTR_RG_WR_CMND* command, which is used to write control register
- *PFG_WR_CMND* command, which is used to configure on-board PFG
- *ADC_RD_CMND* command, which is used to initialize A/D conversion and to transmit ADC data to the receiver of SIOX SIO-0 port. This command can be a part of (ORed with) any of the above commands.

Transmitted command is decoded using bits D31, D30 and D29 of command data word. Bit D31 corresponds to the *ADC_RD_CMND* command and allows to initialize A/D conversion and to transmit ADC output data back to host DSP via the receiver of SIOX SIO-0 port. Bits D30 and D29 are used to decode other commands (*DAC_WR_CMND*, *CNTR_RG_WR_CMND* and *PFG_WR_CMND*), which are used to load incoming data to the on-board DCM resources, i.e. to load DAC data and to configure DCM for operation in “SYNC” mode. Therefore, A/D conversion can be performed in parallel with reception and execution of other commands.

There is no hardware generated sampling frequency source for “ASYNC” mode. Data transmission in “ASYNC” mode over transmitter of SIOX SIO-0 port can be initiated by host DSP only, and active frame synchronization pulse (FSX) denotes transmission of new command. ADC sampling period is defined as the time interval between sequential A/D conversion cycles, whereas DAC sampling period is defined as the time interval between sequential D/A conversion cycles.

serial data word formats for “ASYNC” mode

When configured in “ASYNC” mode, *T/SDAS-AD1/14/300K-DA1/16/300K* DCM requires that incoming command, which is transmitted over transmitter of SIOX SIO-0 port, has 32-bit data format.

ADC data, which is transmitted from *T/SDAS-AD1/14/300K-DA1/16/300K* DCM to the receiver of SIOX SIO-0 port during execution of *ADC_RD_CMND* command, has 16-bit data format.

DAC_WR_CMND command for writing to DAC

DAC_WR_CMND command must be used for writing to DAC and to start D/A conversion in “ASYNC” mode of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

DAC_WR_CMND command can also include *ADC_RD_CMND* command in order to initialize A/D conversion and transmit ADC data to the receiver of SIOX SIO-0 port in “ASYNC” mode during command reception.

Transmitter data word format for *DAC_WR_CMND* command is presented below and data bits description is presented in table 2-2.

Transmitter data word format for *DAC_WR_CMND* command

D31	D30	D29	D28	D27..D16	D15..D0
<i>ADC_EN</i>	0	1	0	0	<i>DAC-15 .. DAC-0</i>

Table 2-2. Data bits description for *DAC_WR_CMND* command.

bit(s)	Description
<i>ADC_EN</i>	Denotes active <i>ADC_RD_CMND</i> command, i.e. initialize A/D conversion enable during reception of this command. ADC output data will be transmitted to the receiver of SIOX SIO-0 port. Refer to the description of <i>ADC_RD_CMND</i> command below for more details.
{ <i>DAC-15..DAC-0</i> }	16-bit DAC input data in 2's complement binary code.

***CNTR_RG_WR_CMND* command for writing to CONTROL REGISTER**

CNTR_RG_WR_CMND command must be used for programming sampling frequency source selector in order to select particular sampling frequency source during “SYNC” mode of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

CNTR_RG_WR_CMND command can also include *ADC_RD_CMND* command in order to initialize A/D conversion and transmit ADC data to the receiver of SIOX SIO-0 port in “ASYNCR” mode during command reception.

Transmitter data word format for *CNTR_RG_WR_CMND* command is presented below and data bits description is presented in table 2-3.

Transmitter data word format for *CNTR_RG_WR_CMND* command

D31	D30	D29	D28	D27..D16	D15..D2	D1	D0
<i>ADC_EN</i>	1	0	0	0	0	<i>FS_SEL-1</i> (0+)	<i>FS_SEL-0</i> (0+)

Table 2-3. Data bits description for *CNTR_RG_WR_CMND* command.

bit(s)	default value on SIOX reset	Description
<i>ADC_EN</i>	-	Denotes active <i>ADC_RD_CMND</i> command, i.e. initialize A/D conversion enable during reception of this command. ADC output data will be transmitted to the receiver of SIOX SIO-0 port. Refer to the description of <i>ADC_RD_CMND</i> command below for more details.
{ <i>FS_SEL-1, FS_SEL-0</i> }	{0,0}	Sampling frequency source selector for “SYNC” mode. Refer to table 2-4 for details how to set this bit field.

Table 2-4. Sampling frequency source selection for “SYNC” mode.

{FS_SEL-1, FS_SEL-0} bits of CNTR_RG_WR_CMND command	Description
{0,0}	Selects on-board PFG output as sampling frequency source for “SYNC” mode.
{0,1}	Selects TM/XIO timer output of SIOX interface as sampling frequency source for “SYNC” mode. Refer to table 2-1 for details about which particular TM/XIO-0 or TM/XIO-1 timer is used as sampling frequency source.
{1,0}	Selects external XFs input from JP2 external I/O connector as sampling frequency source for “SYNC” mode.
{1,1}	Reserved. Do not use.

Notes: 1. Highlighted configuration is set on SIOX reset condition.

PFG_WR_CMND command for programming on-board PFG

PFG_WR_CMND command must be used for programming on-board high-resolution PFG in case PFG will be used as sampling frequency source in “SYNC” mode of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

PFG_WR_CMND command can also include *ADC_RD_CMND* command in order to initialize A/D conversion and transmit ADC data to the receiver of SIOX SIO-0 port in “ASYNC” mode during command reception.

Transmitter data word format for *PFG_WR_CMND* command is presented below and data bits description is presented in table 2-5.

Transmitter data word format for *PFG_WR_CMND* command

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
<i>ADC_EN</i>	1	1	0	0	0	Z1	Z0	N0	N1	N2	N3	N4	N5	N6	M0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
<i>M1</i>	<i>M2</i>	<i>M3</i>	<i>M4</i>	<i>M5</i>	<i>M6</i>	V	X1	X0	R1	R0	0	1	1	0	1

Table 2-5. Data bits description for *PFG_WR_CMND* command.

bit(s)	Description
<i>ADC_EN</i>	Denotes active <i>ADC_RD_CMND</i> command, i.e. initialize A/D conversion enable during reception of this command. ADC output data will be transmitted to the receiver of SIOX SIO-0 port. Refer to the description of <i>ADC_RD_CMND</i> command below for more details.
<i>{M0..M6}</i> <i>{N0..N6}</i> <i>V</i> <i>{R1..R0}</i> <i>{X1, X0}</i> <i>{Z1, Z0}</i>	<i>M, N, V, R, X</i> and <i>Z</i> bit fields for programming on-board high-resolution PFG. Refer to section “PFG Programming” later in this chapter for details how to program PFG.

ADC_RD_CMND command for initializing A/D conversion

ADC_WR_CMND command must be used to initialize A/D conversion and transmit ADC data to the receiver of SIOX SIO-0 port in “ASYNC” mode.

Transmitter data word format for *ADC_RD_CMND* command

D31	D30	D29	D28	D27..D0
<i>ADC_EN</i>	x	x	x	x

ADC_RD_CMND command appears as bit D31 of command data word and can be a part of any of the *DAC_WR_CMND*, *CNTR_RG_WR_CMND*, and *PFG_WR_CMND* commands in order to execute during reception of these commands in “ASYNC” mode of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM. Refer to the corresponding subsections above for more details about these commands.

14-bit ADC output data appear in 2’s complement binary code and are MSB aligned when transmitted to the receiver of SIOX SIO-0 port using 16-bit serial data word format:

Receiver data word format for *ADC Output Data*

D15..D2	D1	D0
<i>ADC-13 .. ADC-0</i>	0	0

Table 2-6. Data bits description for ADC output data.

bit(s)	Description
{ADC-13..ADC-0}	14-bit ADC output data in 2's complement binary code.

timing diagram for serial data communication in “ASYNC” mode

Timing diagram for transmission and execution of *DAC_WR_CMND* command with active *ADC_RD_CMND* command (*ADC_EN* bit set to the ‘1’ state) in “ASYNC” mode is presented at figure 2-2.

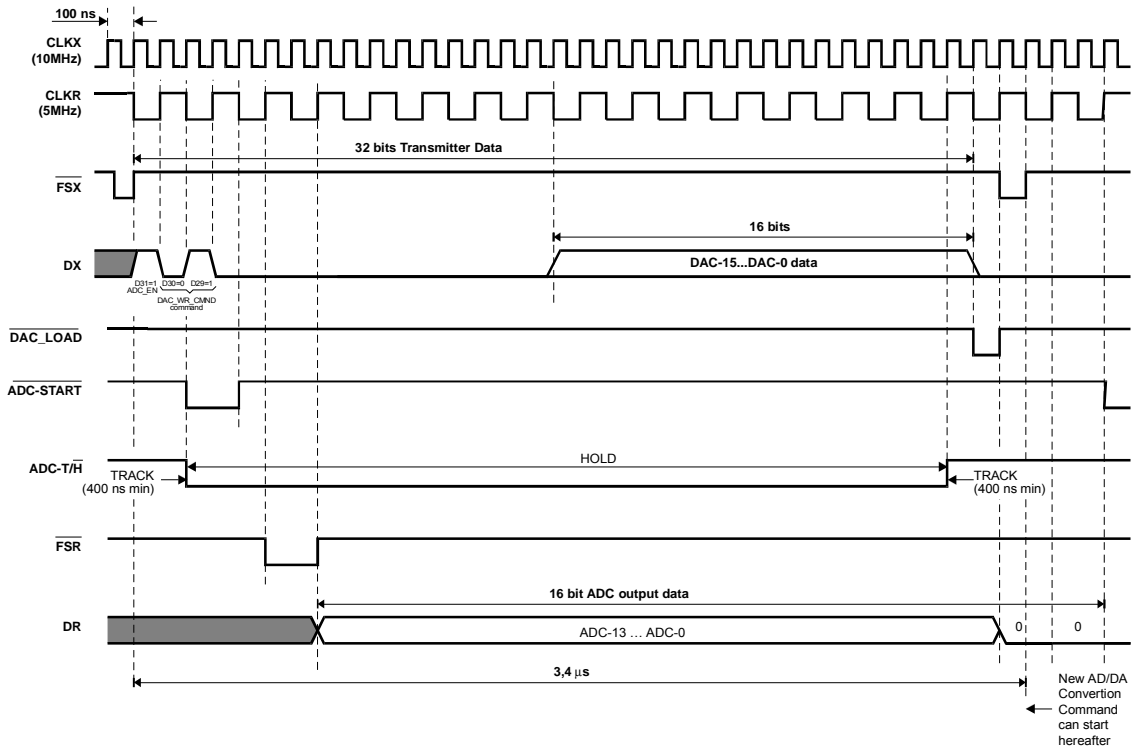


Fig. 2-2. Timing diagram for *DAC_WR_CMND* command with active *ADC_RD_CMND* command in “ASYNC” mode.

Command reception cycle in “ASYNC” mode is initialized by transmitter frame synchronization signal (FSX), which must be generated by DSP via SIOX SIO-0 port. FSX signal must appear at the rising edge of transmitter serial clock (CLKX) and must be generated as one CLKX period in advance of transmitter 32-bit serial data (DX) packet.

CAUTION

Transmitter serial clock (CLKX) and receiver serial clock (CLKR) are both generated by
T/SDAS-AD1/14/300K-DA1/16/300K DCM.

The frequency of CLKR clock (5 MHz) is half of the frequency of CLKX clock (10 MHz) and
is generated at the rising edge of CLKX clock.

The state of CLKR clock is not known during reception of FSX signal
in “ASYNC” mode.

The first received DX data bit is *ADC_EN* bit, which controls initialization of A/D conversion. In case of *ADC_EN*=1 condition, ADC will be started at the first falling edge of CLKR clock after reception of *ADC_EN* bit at the rising edge of CLKX clock. Since CLKR clock is not synchronized to the FSX signal in “ASYNC” mode, then the time instant of ADC start can vary within one CLKX period referenced to the received *ADC_EN* bit timing. Figure 2-2 illustrates the worst case for relative position of FSX signal and CLKR clock.

The on-board input ADC track and hold circuit will be put into the ‘HOLD’ state immediately on active ADC start signal.

CAUTION

Input ADC track and hold circuit must stay in the ‘TRACKING’ state at least 400 nS prior
active ADC start signal.

Once initialized, A/D conversion procedure will proceed within 14 CLKR clock cycles (2.8 μ S) starting from the first rising edge of CLKR clock after active ADC start signal. Next A/D conversion can be started only after the minimum 400 nS of input ADC tracking time will expire, i.e. after at least 3.4 μ S starting from beginning of reception of current command data word. This limits maximum A/D sampling frequency in “ASYNC” mode to 294 kHz.

14-bit ADC output data are transmitted as MSB first and are aligned to the MSB of 16-bit receiver serial data (DR) packet. Two least significant bits of 16-bit receiver data packet are logical ‘0’. Receiver data packet is accompanied by active receiver frame synchronization signal (FSR), which is generated by *T/SDAS-AD1/14/300K-DA1/16/300K* DCM as one CLKR clock period in advance of receiver data packet. Both DR and FSR signals are generated at the rising edge of CLKR clock.

DAC data are recognized as last 16 bits of 32-bit transmitter data packet. DAC data is latched at the next CLKX clock cycle after the end of transmitter data packet. This limits maximum D/A sampling frequency in “ASYNC” mode to 312.5 kHz.

DSP serial port configuration for “ASYNC” mode

In case *T/SDAS-AD1/14/300K-DA1/16/300K* DCM is configured in “ASYNC” mode, then *TORNADO* DSP on-chip serial port, which is routed to the SIO-0 port of SIOX interface, must be configured as the following:

- CLKX and CLKR clock pins shall be configured as external active high clock

- DX and DR serial data pins shall be configured as active high
- DX transmitter data word format must be configured to 32-bit data word
- DR transmitter data word format must be configured to 16-bit data word
- FSX transmitter frame synchronization pin must be configured as active low, internally generated at the rising edge of CLKX, and generated at one advanced CLKX clock period
- FSX transmitter frame synchronization pin must be configured as active low, externally generated at the rising edge of CLKR, and generated at one advanced CLKR clock period.

When configured in “ASYNC” mode, *T/SDAS-AD1/14/300K-DA1/16/300K* DCM is compliant with *TORNADO* DSP systems, controllers, and coprocessors with TMS320C3x DSP, TMS320C54x DSP with McBSP serial ports (TMS320C5402, TMS320C5410, TMS320C5416, etc), and with TMS320C6x DSP.

2.3 “SYNC” Operation Mode

“SYNC” mode of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM must be used with hardware generated sampling frequency clock in case low sampling period jitter is an important issue for user application. “SYNC” mode is ideal selection for high-speed and high-accuracy instrumentation applications.

selecting “SYNC” operation mode

“SYNC” mode can be set by DSP software only (table 2-1) in case on-board SW1-1 switch is set to the software programmable operation mode state and the corresponding TM/XIO line, which is selected via SW1-2 switch, is set to the ‘1’ state.

general description

When configured in “SYNC” mode, *T/SDAS-AD1/14/300K-DA1/16/300K* DCM can accept hardware generated sampling frequency clock from different sources and starts data conversion procedure on active sampling event. “SYNC” mode features low sampling period jitter and each sampling cycle includes A/D and D/A conversion procedures.

The hardware generated sampling frequency source for “SYNC” mode is selected via bits {*FS_SEL-1*, *FS_SEL-0*} of *CNTR_RG_WR_CMND* command, which must be preliminary issued in “ASYNC” mode. Refer to table 2-4 for more details.

serial data word formats for “SYNC” mode

When configured in “SYNC” mode, *T/SDAS-AD1/14/300K-DA1/16/300K* DCM assumes that transmitter and receiver serial data packets, which are transmitted over transmitter and receiver of SIOX SIO-0 port, contain DAC input data and ADC output data correspondingly and have 16-bit data format. Both DAC input data and ADC output data appear in 2’s complement binary code.

Transmitter data word format for “SYNC” mode

D15..D0
DAC-15 .. DAC-0

Receiver data word format for “SYNC” mode

D15..D2	D1	D0
ADC-13 .. ADC-0	0	0

timing diagram for serial data communication in “SYNC” mode

Timing diagram for operation of T/SDAS-AD1/14/300K-DA1/16/300K DCM in “SYNC” mode is presented at figure 2-3.

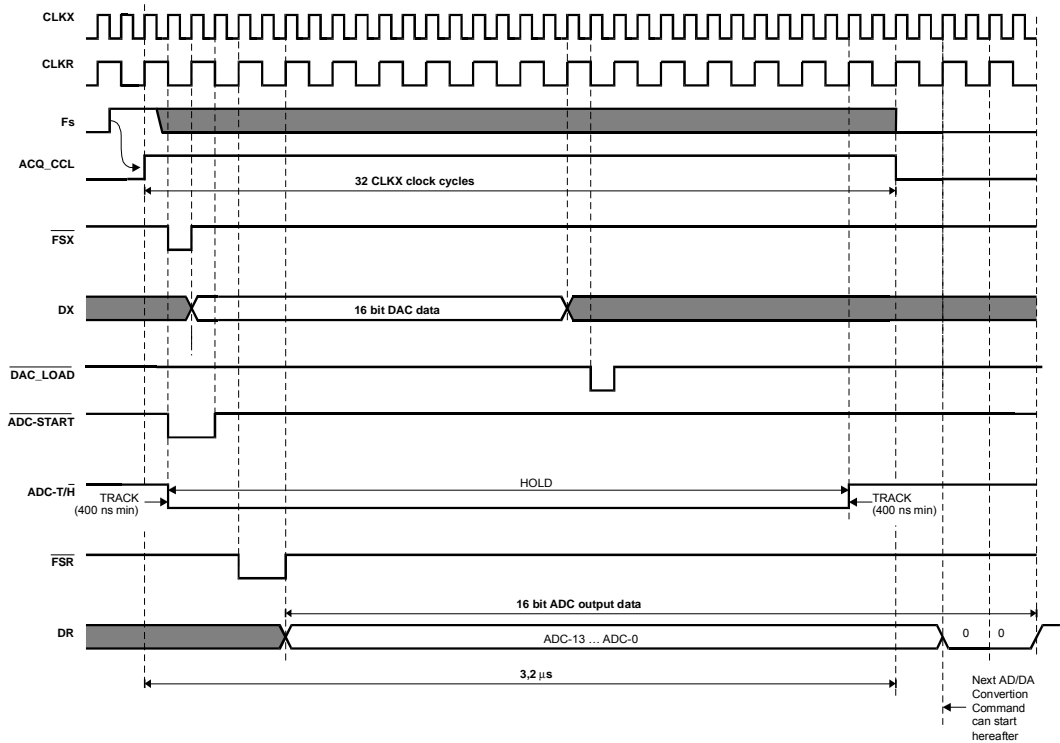


Fig. 2-3. Timing diagram for operation of T/SDAS-AD1/14/300K-DA1/16/300K DCM in “SYNC” mode.

Data acquisition cycle in “SYNC” mode is initialized by detection of sampling event at the output of sampling frequency clock selector, which is controlled by bits {FS_SEL-1, FS_SEL-0} of CNTR_RG_WR_CMND

command in accordance with table 2-4. *CNTR_RG_WR_CMND* command must be preliminary issued in “ASYNC” mode.

CAUTION

Sampling event in “SYNC” mode is detected at the rising edge of selected sampling frequency clock.

Active sampling event is synchronized to the rising edge of receiver serial clock (CLKR) and starts new data acquisition cycle.

CAUTION

Transmitter serial clock (CLKX) and receiver serial clock (CLKR) are both generated by *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

The frequency of CLKR clock (5 MHz) is half of the frequency of CLKX clock (10 MHz) and is generated at the rising edge of CLKX clock.

Active transmitter frame synchronization (FSX) signal is generated by *T/SDAS-AD1/14/300K-DA1/16/300K* DCM immediately at the beginning of new data acquisition cycle in “SYNC” mode, and is used to download 16-bit DAC data from DSP via transmitter of SIOX SIO-0 port. DAC data is latched at the next CLKX clock cycle after the end of transmitter data packet. There is no jitter for the DAC latch instant if referenced to the beginning of data acquisition cycle.

A/D conversion is started immediately at the at the beginning of new data acquisition cycle in “SYNC” mode. There is no jitter for the A/D conversion start instant if referenced to the beginning of data acquisition cycle. The on-board input ADC track and hold circuit will be put into the ‘HOLD’ state immediately on active ADC start signal.

CAUTION

Input ADC track and hold circuit must stay in the ‘TRACKING’ state at least 400 nS prior active ADC start signal.

Once initialized, A/D conversion procedure will proceed within 14 CLKR clock cycles (2.8 μ S) starting from the first rising edge of CLKR clock after active ADC start signal. Next A/D conversion can be started only after the minimum 400 nS of input ADC tracking time will expire, i.e. after at least 3.4 μ S starting from beginning of reception of current command data word.

14-bit ADC output data are transmitted as MSB first and are aligned to the MSB of 16-bit receiver serial data (DR) packet. Two least significant bits of 16-bit receiver data packet are logical ‘0’. Receiver data packet is accompanied by active receiver frame synchronization signal (FSR), which is generated by *T/SDAS-*

AD1/14/300K-DA1/16/300K DCM as one CLKR clock period in advance of receiver data packet. Both DR and FSR signals are generated at the rising edge of CLKR clock.

Duration of data acquisition cycle in “SYNC” mode is 3.2 uS, which corresponds to 294 kHz maximum A/D sampling frequency.

DSP serial port configuration for “ASYNC” mode

In case T/SDAS-AD1/14/300K-DA1/16/300K DCM is configured in “SYNC” mode, then *TORNADO* DSP on-chip serial port, which is routed to the SIO-0 port of SIOX interface, must be configured as the following:

- CLKX and CLKR clock pins shall be configured as external active high clock
- DX and DR serial data pins shall be configured as active high
- DX transmitter data word format must be configured to 16-bit data word
- DR transmitter data word format must be configured to 16-bit data word
- FSX transmitter frame synchronization pin must be configured as active low, externally generated at the rising edge of CLKX, and generated at one advanced CLKX clock period
- FSX transmitter frame synchronization pin must be configured as active low, externally generated at the rising edge of CLKR, and generated at one advanced CLKR clock period.

When configured in “SYNC” mode, T/SDAS-AD1/14/300K-DA1/16/300K DCM is compliant with *TORNADO* DSP systems, controllers, and coprocessors with TMS320C3x DSP, TMS320C54x DSP with McBSP serial ports (TMS320C5402, TMS320C5410, TMS320C5416, etc), and with TMS320C6x DSP.

2.4 PFG Programming

On-board programmable sampling frequency generator (PFG) of T/SDAS-AD1/14/300K-DA1/16/300K DCM allows to set output sampling frequency clock within 47 Hz .. 300 kHz with very high resolution.

PFG is based on the phased locked loop (PLL) technique and can be programmed in “ASYNC” mode by means of *PFG_WR_CMND* command (refer to section ““ASYNC” mode” earlier in this chapter for more details), which comprises of the 7-bit *M*-field, 7-bit *N*-field, 1-bit *V*-field, and 2-bit *R*-field, *X*-field and *Z*-field. PLL reference clock is 10 MHz.

CAUTION

PFG_WR_CMND command requires the inversed order of data bits for *M*-field and *N*-field, i.e. least significant bits for these fields shall be transmitted first.

Host DSP software must reverse order of data bits for *M*-field and *N*-field, which are used to program the PFG output frequency value.

PFG output frequency value

PFG output frequency value can be programmed within the 47 Hz .. 300 kHz frequency range via *M*, *N*, *V*, *R*, *X* and *Z* fields of the *PFG_WR_CMND* command as the following:

$$F_{out} = \frac{10MHz * N * V_v}{M * R_v * X_v * Z_v}$$

where:

- F_{out}* output frequency value (MHz)
- N* is defined by the *N*-field of *PFG_WR_CMND* command
- M* is defined by the *M*-field of *PFG_WR_CMND* command
- V_v* value of *V*-multiplier, which is defined by the *V*-field of *PFG_WR_CMND* command in accordance with table 2-7a
- R_v* value of *R*-divider, which is defined by the *R*-field of *PFG_WR_CMND* command in accordance with table 2-7b
- X_v* value of *X*-divider, which is defined by the *X*-field of *PFG_WR_CMND* command in accordance with table 2-7c
- Z_v* value of *Z*-divider, which is defined by the *Z*-field of *PFG_WR_CMND* command in accordance with table 2-7d

Table 2-7a. V-multiplier programming for PFG.

value of the <i>V</i> -field of <i>PFG_WR_CMND</i> command	value of the <i>V</i> -multiplier (<i>V_v</i>)
0	X1
1	X8

Table 2-7b. R-divider programming for PFG.

value of the R-field of PFG_WR_CMND command		value of the R-divider (Rv)
R1	R0	
0	0	:1
1	0	:2
0	1	:4
1	1	:8

Table 2-7c. X-divider programming for PFG.

value of the X-field of PFG_WR_CMND command		value of the X-divider (Xv)
X1	X0	
0	0	:1
1	0	:2
0	1	:4
1	1	:8

Table 2-7d. Z-divider programming for PFG.

value of the Z-field of PFG_WR_CMND command		value of the X-divider (Xv)
Z1	Z0	
0	0	:1
1	0	:256
0	1	:2048
1	1	:16384

restrictions

The following restrictions are applicable for N , M and V -fields of *PFG_WR_CMND* command when programming PFG output frequency value:

$$3 \leq N \leq 75$$

$$3 \leq M \leq 50$$

$$50\text{MHz} \leq \frac{10\text{MHz} * N * V_V}{M} \leq 250\text{MHz}$$

CAUTION

The time period between succeeding transmissions of *PFG_WR_CMND* command must be 200 uS or greater in order to meet lock time specification for PFG on-chip PLL.

2.5 Construction

T/SDAS-AD1/14/300K-DA1/16/300K DCM (fig.1-1, fig.A-1) meets standard SIOX rev.B daughter-card form-factor. Construction of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM assumes that host *TORNADO* DSP system with *T/SDAS-AD1/14/300K-DA1/16/300K* DCM installed fits into one ISA or PCI-bus slot of PC chassis.

Connection of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM to external analog I/O world is performed via the on-board JP2 connector, which is available via rear panel of host PC (if *T/SDAS-AD1/14/300K-DA1/16/300K* is installed onto *TORNADO* DSP system for PC). Compatible cable with two analog I/O RCA jacks and one external sampling frequency RCA jack is provided as standard with *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

Chapter 3. Installation

This chapter contains information for installation and configuration of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

3.1 Installation

T/SDAS-AD1/14/300K-DA1/16/300K DCM installs as SIOX daughter-card DCM onto *TORNADO* DSP system mainboard.

For installation of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM into SIOX site of *TORNADO* DSP system follow the recommendations below (fig.3-1):

1. Switch off the power of host PC.
2. Remove *TORNADO* mainboard from PC slot.
3. Take *T/SDAS-AD1/14/300K-DA1/16/300K* DCM and slant it for about 30°..40° degrees refer to *TORNADO* mainboard. Insert JP2 external I/O connector of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM into the corresponding hole of mounting bracket of *TORNADO* DSP system.

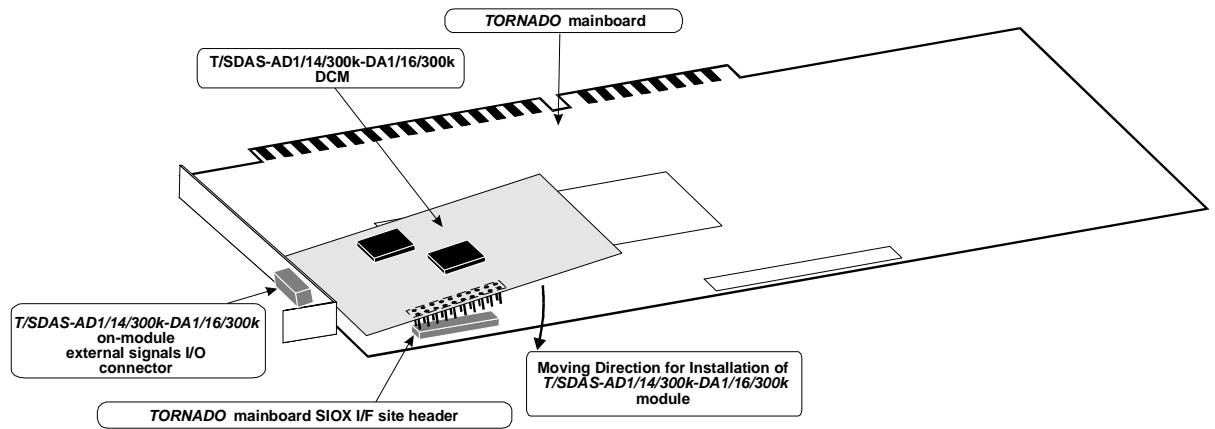


Fig. 3-1. Installation of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM into SIOX site of *TORNADO* DSP system.

4. Rotate *T/SDAS-AD1/14/300K-DA1/16/300K* DCM around mounting bracket and allocate pin #1 of JP1 connector of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM against pin #1 of SIOX interface header on *TORNADO* mainboard.

CAUTION

Female connector of host SIOX interface has 20 pins for *TORNADO-31/31Z/31M/32L/32LX/33/P33/E31/E33* DSP systems and controllers and 26 pins for *TORNADO-30/54x/6x/E6x/E54x* DSP systems and controllers. Pin #1 of host SIOX site connectors always fit into the same physical position on *TORNADO* DSP systems and controllers.

Pin #1 of SIOX connector of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM must always plug into pin #1 of host SIOX site connector not regarding type of host *TORNADO* DSP systems or controller.

Missing doing this will result in damage of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM and/or host *TORNADO* hardware.

5. Safely plug-in SIOX male header of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM into SIOX female header of *TORNADO* DSP system.
6. Screw external analog I/O connector shell of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM to the mounting bracket of *TORNADO* DSP system.
7. Configure on-board SW1-1 switch to set either “ASYNC” mode or software programmable operation mode in order to meet requirements of your application (refer to table 2-1).
8. Configure on-board SW1-2 switch for selection the TM/XIO output line of host SIOX interface, which will select between the “ASYNC” and “SYNC” mode in case software programmable operation mode is set via SW1-1 switch (refer to table 2-1).
9. Install *TORNADO* board into PC slot and screw it to rear panel of PC.
10. Connect the plug to external analog I/O connector of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.
11. Switch on power of host PC.

3.2 Connection to external signal I/O equipment

Connection of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM to external analog I/O equipment is performed by means of on-board JP2 connector (fig.A-1) and external I/O cable set.

CAUTION

It is highly recommended to plug-in and unplug external I/O cable set into/from on-board JP2 connector of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM when host *TORNADO* power is switched off.

The ground signal of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM has no galvanic isolation from host *TORNADO* and/or PC ground signal and chassis.

CAUTION

When connecting external analog I/O equipment to *T/SDAS-AD1/14/300K-DA1/16/300K* DCM you should be aware that AIN-0..3 analog inputs and AOOUT-0..3 analog outputs of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM are DC coupled. If required, external DC isolation capacitors should be used.

External I/O cable set for *T/SDAS-AD1/14/300K-DA1/16/300K* DCM uses standard miniature banana jacks for connection to external analog I/O equipment with single-ended I/O signals. This set comprises of 3 RCA jacks:

- AIN analog input
- AOOUT analog output
- XFs external sampling frequency input.

Appendix A. On-board Connectors and Switches

This appendix contains a summary for the on-board connectors, configuration jumpers and configuration switches for *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

The on-board connectors and configuration jumpers are presented at fig.A-1.

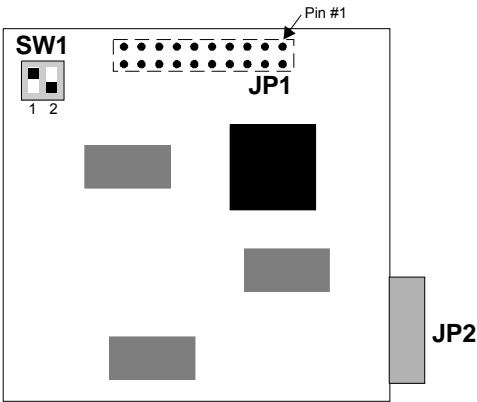


Fig. A-1. On-board connectors and configuration switches for *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

A.1 Configuration Switches

Table A-1 specifies a list of on0board configuration switches.

Table A-1. Configuration switches.

Switch	Description	References
SW1-1	Selection of either "ASYNC"-only mode or software programmable operation mode.	Table 2-1
SW1-2	Selection of SIOX TM/XIO output line, which will be used for selection between "ASYNC" and "SYNC" mode in case SW1-1 is set to the software programmable operation mode.	Table 2-1

A.2 On-board Connectors

Table A-2 contain the list of on-board connectors.

Table A-2. On-board connectors of T/SDAS-AD1/14/300K-DA1/16/300K DCM.

Connector	description
JP1	SIOX interface site male header.
JP2	External analog I/O connector.

Pinout of JP1 host SIOX connector is presented in the user’s guide of host *TORNADO* DSP system or controller, which is used for installation of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

Pinout for external I/O connector

Pinout of JP2 external I/O connector for *T/SDAS-AD1/14/300K-DA1/16/300K* DCM is presented at fig.A-2, and description of signals is presented in table A-3.

The connector p/n for JP2 is DHA-RA14 female half-pitch connector from DDK Ltd manufacturer. P/n for compatible plug-in connector is DHA-PC14. In case customer needs to design his own application specific cable for connection to *T/SDAS-AD1/14/300K-DA1/16/300K* DCM, then compatible plug-in connectors for JP2 are available from MicroLAB Systems upon request.

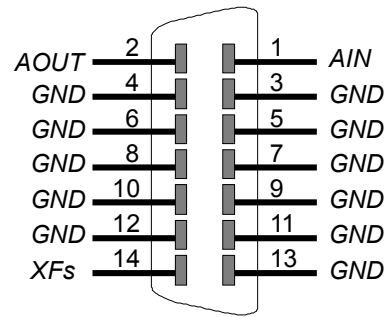


Fig. A-2. Pinout for JP2 external I/O connector of T/SDAS-AD1/14/300K-DA1/16/300K DCM.

Table A-3. Signal description for JP2 external I/O connector of *T/SDAS-AD1/14/300K-DA1/16/300K* DCM.

Signal name	type	description
<i>AIN</i>	AI	Analog input.
<i>AOUT</i>	AO	Analog output.
<i>XF_s</i>	TTL/IN	External sampling frequency input.
<i>GND</i>	-	Ground.

Notes: 1. Signal types: *AI* - analog input; *AO* - analog output; *TTL/IN* - TTL compatible digital input.

Appendix B. SIOX Rev.B Interface Site

This appendix contains information about *TORNADO* SIOX rev.B interface site specifications. This description is general to all *TORNADO* DSP systems/controllers/coprocessors, whereas different *TORNADO* boards with different DSP platforms may differ in the number and in the on-board routing of SIOX serial ports, timer/IO pin specifications. Refer to your particular *TORNADO* user's guide for more details.

B.1 General Description

TORNADO architecture provides expansion of the on-board DSP I/O resources via on-board serial I/O expansion interface sites (SIOX-A and SIOX-B) (fig.B-1), which are designed to carry compatible DCMs (DCM).



Fig.B-1. *TORNADO*-54x board with two SIOX sites.

Some *TORNADO* boards (typically *TORNADO* DSP systems for PC) provide two SIOX interface sites, whereas other *TORNADO* boards (typically *TORNADO* stand-alone DSP controllers and DSP coprocessors) provide only one SIOX site.

TORNADO SIOX rev.B interface site comprises of signals for one or two SIO-0/SIO-1 logical serial ports, timers/IO pins, DSP interrupts, and host power supplies.

CAUTION

In case *TORNADO* on-board DSP features two or more on-chip serial ports (TMS320C30, TMS320C54x, TMS320C6x), then *TORNADO* on-board SIOX sites provides two SIO-0 and SIO-1 serial ports and the SIOX site headers are 26-pin headers.

In case *TORNADO* on-board DSP features only one on-chip serial ports (TMS320C31, TMS320C32), then *TORNADO* on-board SIOX sites provides only one SIO-0 serial port and the SIOX site headers are 20-pin headers.

Both *TORNADO* on-board SIOX-A and SIOX-B interface sites feature identical pinout control and may only differ in the routing of DSP physical serial ports to SIO-0 and SIO-1 logical serial ports. If *TORNADO* on-board DSP features two or more on-chip serial ports (TMS320C30, TMS320C54x, TMS320C6x), then DSP serial ports routing is performed on *TORNADO* mainboard, and allows simultaneous operation of two or more SIOX DCM, which are routed to different DSP serial ports.

B.2 SIOX Site Connector and Signals

TORNADO SIOX rev.B interface site comprises of signals for SIO-0 and SIO-1 logical serial ports, DSP on-chip TM/XIO-0/1 timers/IO pins, three DSP interrupts, SIOX reset control, and power $\pm 5V/\pm 12V$ host power supplies.

TORNADO on-board SIOX site connector with two serial ports

TORNADO on-board SIOX site connector with two serial ports is an industry standard dual-row 26-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM should be the industry standard either 26-pin 0.1"x0.1" male header (in case both SIO-0 and SIO-1 serial ports are utilized on SIOX plugged-in DCM) or 20-pin 0.1"x0.1" male header (in case only SIO-0 serial port is utilized on SIOX plugged-in DCM).

SIOX site connector pinout with two serial ports is shown at fig.B-2 and signal specifications are listed in table B-1.

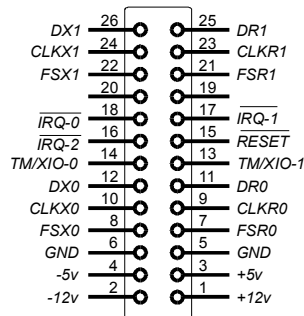


Fig.B-2. *TORNADO* on-board SIOX connector pinout with two serial ports (top view).

TORNADO on-board SIOX site connector with one serial port

TORNADO on-board SIOX site connector with one serial port is an industry standard dual-row 20-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM should be the industry standard 20-pin 0.1"x0.1"male header.

SIOX site connector pinout with one serial ports is shown at fig.B-3 and signal specifications are listed in table B-1.

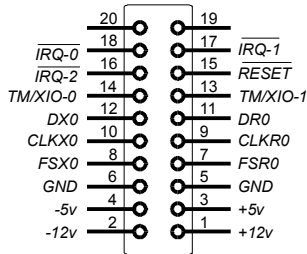


Fig.B-3. TORNADO on-board SIOX connector pinout with one serial port (top view).

SIOX site signal description

Description for SIOX interface site signals is presented in table B-1.

Table B-1. SIOX interface signal description.

SIOX signal name	signal type	description
SIO-0 port control		
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX site..
DR0 FSR0 CLKR0	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX site..
SIO-1 port control (available in SIOX site connector with two serial ports only)		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX site..
DR1 FSR1 CLKR1	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX site..

DSP Timers/IO, DSP Interrupt Requests and SIOX Reset		
<i>TM/XIO-0</i>	I/O/Z	This signal is typically connected to the DSP on-chip timer-0 I/O pin and can be software configured by DSP as either timer or I/O pin.
<i>TM/XIO-1</i>	I/O/Z	This signal is typically connected to the DSP on-chip timer-1 I/O pin and can be software configured by DSP as either timer or I/O pin.
\overline{RESET}	O	Active low SIOX reset signal. Some <i>TORNADO</i> boards (for example <i>TORNADO-3x</i> boards) wires this signal directly from the DSP reset signal and SIOX plugged-in DCM reset is performed simultaneously with <i>TORNADO</i> on-board DSP reset, however other <i>TORNADO</i> boards (for example <i>TORNADO-54x/6x</i> etc. boards) features dedicated SIOX site reset signal, which is controlled by <i>TORNADO</i> on-board DSP for better synchronization between the DSP software and SIOX DCM operation.
$\overline{IRQ-0}$, $\overline{IRQ-1}$, $\overline{IRQ-2}$	I	Active low external interrupt request lines for <i>TORNADO</i> on-board DSP. These line are pulled up.
Power Supplies		
<i>GND</i>		Ground.
<i>+5v</i>		+5v
<i>+12v</i>		+12v
<i>-5v</i>		-5v
<i>-12v</i>		-12v

Note:

1. Signal type is denoted as the following: I - input, O - output, Z - high impedance.
1. All logical signal levels and load currents correspond to that for CMOS/TTL signals.

SIOX site signal levels

Signal levels for SIOX interface signals correspond to that for the CMOS/TTL signals with $I_{OL}=2\text{ma}$ and $I_{OH}=-0.3\text{ma}$ load currents.

CAUTION

Some *TORNADO* boards (*TORNADO-3x/542L/E31*) provide SIOX interface signal levels for CMOS/TTL only, whereas other *TORNADO* boards (*TORNADO-54xx/6x/E6x/P6x*) provide SIOX interface signal levels universal for both 3V TTL and standard 5V TTL. Refer to documentation for your particular *TORNADO* board for information about SIOX interface signal levels.

B.3 Physical Dimensions for SIOX DCM

Physical dimensions for SIOX DCM are presented at fig.B-4. This information is intended for those customers, who need to design customized SIOX DCMs.

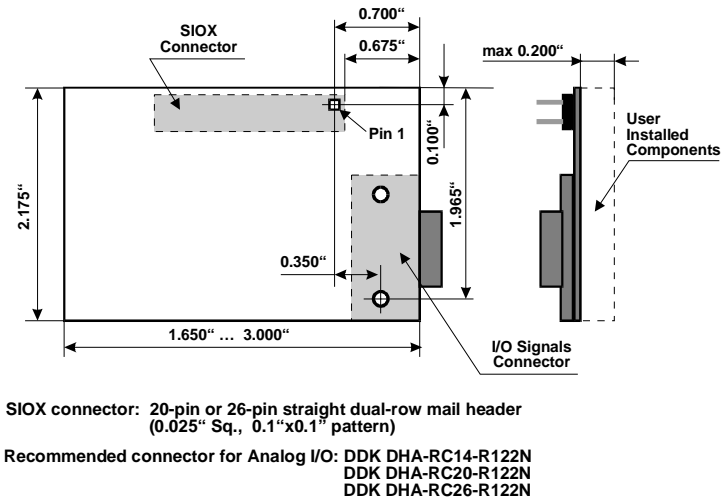


Fig.B-4. Physical dimensions for SIOX DCM.