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DSP
TEXAS INSTRUMENTS

DIGITAL SIGNAL PROCESSING

T/SBDAS-7890/8420

Octal-channel 12-bit AD/DA Instrumentation SIOX-Bus DCM
for *TORNADO* DSP Systems, Controllers and Coprocessors

User's Guide

covers:
T/SBDAS-7890/8420 rev.1B

CAUTION

Ôèðì à ÌèêðîËÀÁ Ñèñòåìñ Ëòä (ÌËÑ) îñòàâëÿåò çà ñîáîé ï ðàâî âíîñèòü ëþáûåèçì åíåíèÿ ï ðåæðûáòþ âûï óñê è ï îîäàæðåêó ëþáûõ èçäåëèé è ï ðîãðàì ìíîî îáñï å÷åíÿ, óÿ ïî ìíåíûõ â íàñòîÿùå äîêîì åíòà áåç êàêîã-ëèáî ï ðåäâàðèòåëüíîãî óáåäî ëåíÿ, ãñëè èíîå íñî àðåëèûîí íà îãîâàðèâàåòñÿ. ÌËÑ ðêîî äàãóàð ñàáìèî ï íêïîî àîãéåì ï íëüçîâàòüñÿ ï îäîÿííûï è íñàûè è íñîåäèíè è âåðñèÿ è ðèõí àíûõ êíîîòð äëèîíûõ äîêòî åòäî è íñóãàñòîèêÿòü ï ðåàâåäèòåëüíîå êîîîîéöèòèðîâàíèå ñ ðèõò íîï àíîä ðãç àåãäåí çàèçà, ÷îòûõ áûûòü óáåàýðûò, ÷îò íàñòîÿùÿ åíîîð äëèÿ äïîîíîñàíûí ï ðïè ñëåï à íàñåìóòñûé ì îì åò.

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ï ðîãóòöèÿ ÌËÑ íå ï ðåäíàçíà-åíà äëÿ ï ðèì åäåíÿ â ä ì àðàóðå ñèñòåàõ èëè çäàíèÿõ äëÿ ï îääàðãêè æçèíåäÿòäëüíîñòè. Ï ðèì åäå ï ðîãóòöèè ÌËÑ â ýèõ íàîîäàîäàäåí êîàäîî÷ñêè çíÿ ðàåì áåç íñî ðèõèëüíîì ï åñüï åííîì ï îòàâåäàÿäåíèÿ îò ÌËÑ èëè îòðåäãîíîìüíîîî ôèðìåííîî ñðòòèêôèêôàòà ÌËÑ.

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About this Document

This user's guide contains description for *T/SBDAS-7890/8420* AD/DA SIOX daughter-card DCM (DCM) for *TORNADO* DSP systems/controllers/coprocessors from MicroLAB Systems Ltd.

This document does not include detail description neither for *TORNADO* systems, nor for TI DSP and corresponding software and hardware applications. To get the corresponding information please refer to the following documentation:

1. ***TMS320C3x User's Guide.*** Texas Instruments Inc, SPRU031C, USA, 1992.
2. ***TMS320C54x. CPU and Peripherals. Reference Guide.*** Texas Instruments Inc, SPRU131D, USA, 1997.
3. ***TMS320C6x. CPU and Instruction Set. Reference Guide.*** Texas Instruments Inc, SPRU189C, USA, 1998.
4. ***TORNADO-3x. User's Guide.*** MicroLAB Systems, 1998.
5. ***TORNADO-P33. User's Guide.*** MicroLAB Systems, 2000.
6. ***TORNADO-54x. User's Guide.*** MicroLAB Systems, 1998.
7. ***TORNADO-6x. User's Guide.*** MicroLAB Systems, 1998.
8. ***TORNADO-P6x. User's Guide.*** MicroLAB Systems, 1999.
9. ***TORNADO-PX31DP. User's Guide.*** MicroLAB Systems, 1996.
10. ***TORNADO-SX30. User's Guide.*** MicroLAB Systems, 1996.
11. ***TORNADO-E31. User's Guide.*** MicroLAB Systems, 1996.
12. ***TORNADO-E33. User's Guide.*** MicroLAB Systems, 2000.
13. ***TORNADO-EL31. User's Guide.*** MicroLAB Systems, 1996.
14. ***TORNADO-E6x. User's Guide.*** MicroLAB Systems, 1998.

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Chapter 1. Introduction

This chapter contains general description for *T/SBDAS-7890/8420* SIOX daughter-card module (DCM) for *TORNADO* DSP systems/controllers/coprocessors.

1.1   General Information

T/SBDAS-7890/8420 (fig.1-1) is quad-channel AD/DA SIOX (serial I/O expansion) DCM for *TORNADO* DSP systems (*TORNADO-3x/54x/6x/P6x/P33/etc*), *TORNADO-E/EL* stand-alone DSP controllers (*TORNADO-E3x/E54x/E6x/etc*) and *TORNADO-PX/SX* DSP coprocessors (*TORNADO-PX31DP/SX30/etc*) from MicroLAB Systems Ltd.

T/SBDAS-7890/8420 DCM has been designed for high-accuracy multi-channel instrumentation applications, however it can be used for many other applications with similar requirements for the AD/DA front-end.
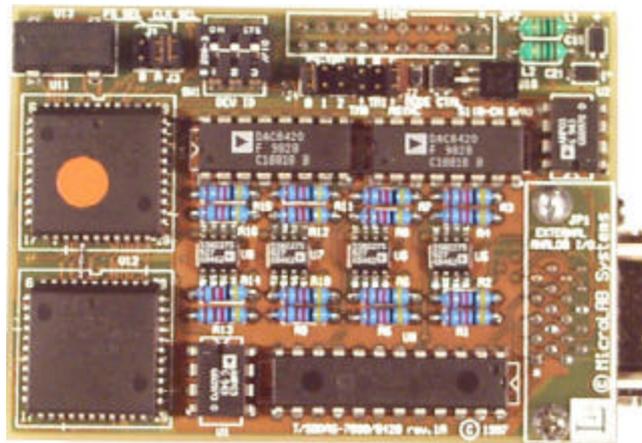
Fig. 1-1.   T/SBDAS-7890/8420 DCM.

Installation

T/SBDAS-7890/8420 DCM installs as SIOX DCM (fig.1-2) into the SIOX site onto *TORNADO* DSP mainboard. If required, the *T/SU-X* SIOX extender can be used for remote connection to SIOX interface of *TORNADO* mainboard.
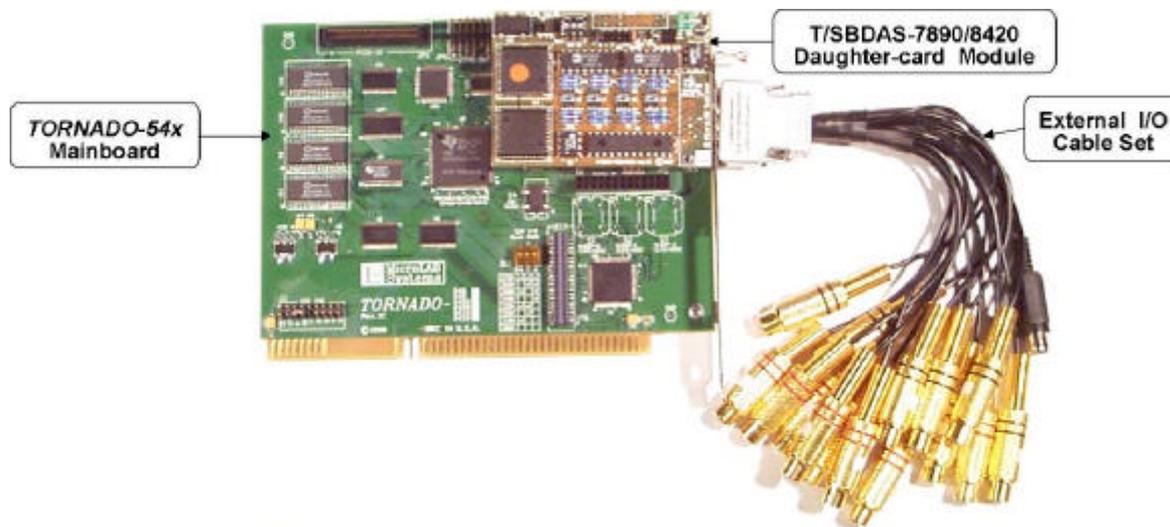
Fig. 1-2.   T/SBDAS-7890/8420 DCM installed onto TORNADO-54x mainboard.

Overview

T/SBDAS-7890/8420 DCM comprises of eight A/D and D/A channels of instrumentation quality and features:

- 12-bit 100ksps ADC with 8-channel input multiplexer
- eight 12-bit 100ksps DACs
- control unit.

On-board AD/DA channels feature 12-bit resolution, excellent linearity and low THD. DCM can operate in "ASYNCHRONOUS" and "SYNCHRONOUS" data acquisition modes, which allow to meet different application requirements. Also, external sampling frequency input or output of any host SIOX interface timers can be selected as the sampling frequency event.

External signal I/O

Connection of *T/SBDAS-7890/8420* DCM to external analog I/O world is performed via the on-board I/O JP1 connector, which is available via rear panel of host PC (if *T/SBDAS-7890/8420* DCM is installed onto *TORNADO* DSP system for PC).

Expansion facilities

T/SBDAS-7890/8420 DCM meets MicroLAB Systems SIOX and SIOX-Bus specifications and allows expansion via SIOX-Bus to totally eight DCMs per one serial port.

Applications

T/SBDAS-7890/8420 AD/DA DCM has been designed for high-accuracy multi-channel instrumentation scalable applications as well as for other general signal processing applications (biomedical, speech/audio, etc), which feature similar AD/DA requirements.

1.2   Technical Specifications

The following are technical specifications for *T/SBDAS-7890/8420* AD/DA DCM for temperature of external environment +25°C.

parameter description	*parameter value*
A/D channel:	
ADC type	AD7890-10 from Analog Devices Inc
number of multiplexed input channels (AIN)	8
input signal voltage	± 10 V
maximum input signal voltage	± 17 V
input impedance for analog inputs	> 20 kOhm
resolution	12 bits
zero offset error	4 LSB max
scale error	2.5 LSB max
harmonic distortions (Fin=10kHz, Fs=100kHz)	≤ -75 dB
SNR (Fin=10kHz, Fs=100kHz)	≥ 68dB
internal bias voltage for each of AIN-0..7 analog inputs	1.4285 V @ input impedance
D/A channel	
DAC type	AD8420 from Analog Devices Inc
number DAC channels	4/8
output signal voltage	± 10 V @ 2 kOhm
resolution	12 bits

zero offset error	± 2 mV max
scale error	1% max
differential nonlinearity	±1 LSB max
integral nonlinearity	±2 LSB max
output voltage settling time	13 us max

common parameters:

maximum scan frequency in SYNCHRONOUS mode	100 kHz
maximum sampling frequency per channel in SYNCHRONOUS mode	100 kHz
maximum sampling frequency per channel in ASYNCHRONOUS mode	95 kHz
CLKX0 transmitter clock frequency (in case CLKX0 SIOX signal is used as external synchro-clock frequency)	10 MHz ± 1%
digital I/O logical levels for SIOX I/F signals and external sampling frequency inputs	TTL

physical and power:

dimensions	55mm (2.14") x 77mm (3") (full size SIOX rev.B DCM)
power consumption via SIOX interface	+5v @ 100mA +12v @ 50mA -12v @ 50 mA

Chapter 2. Technical Description

This chapter contains detail technical description for architecture and construction of *T/SBDAS-7890/8420* SIOX DCM.

2.1 Block Diagram

Basic configuration of *T/SBDAS-7890/8420* DCM is presented at fig.2-1.
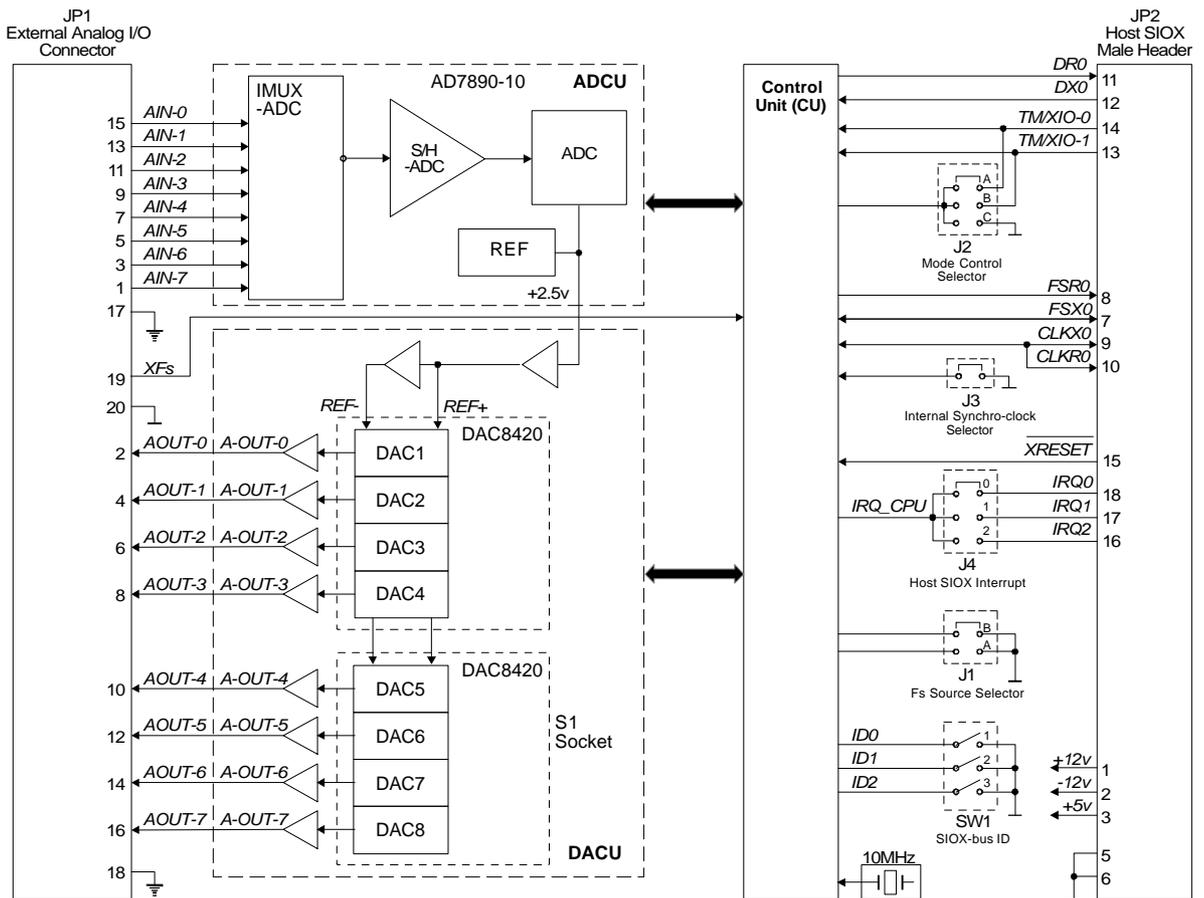
Fig. 2-1. Block diagram of *T/SBDAS-7890/8420* DCM.

T/SBDAS-7890/8420 DCM installs as SIOX (serial I/O expansion interface) DCM onto *TORNADO* mainboard and assumes that communication with *TORNADO* on-board DSP is provided via the DSP on-chip serial port.

T/SBDAS-7890/8420 DCM comprises of:
- analog input section (ADCU), which contains 12-bit 100ksps ADC with 8-channel analog input multiplexer
- analog output section (DACU), which contains eight 12-bit 100ksps DACs with output signal buffers
- control unit (CU)
- external signal I/O connector (JP1)
- host SIOX interface header (JP2) for installation onto *TORNADO* DSP systems.

analog input section

Analog input section (ADCU) of *T/SBDAS-7890/8420* DCM is based on 12-bit 100ksps ADC with 8-channel analog input multiplexer (AD7890-10 chip from Analog Devices Inc), and is designed for analog-to-digital conversion of input analog signals from AIN-0..AIN-7 analog inputs and further transmission of digital code to the receiver of SIO-0 port of host SIOX interface of *TORNADO* DSP system via control unit. AD7890-10 ADC chip features excellent linearity and high-accuracy at 100ksps conversion rates.

CAUTION

The AIN-0..7 analog inputs of AD7890-10 ADC chip are directly connected to the JP1 external analog I/O connector of *T/SBDAS-7890/8420* DCM without analog signal buffering.

Each of AIN-0..7 analog inputs features minimum input impedance 20 kOhm. The AIN inputs are DC coupled and can accept external DC analog signals within allowed analog input voltage range.

CAUTION

Due to internal design of AD7890-10 ADC chip, each of AIN-0..7 analog inputs generates bias current to external analog signal source, which is defined by 1.4285V internal bias voltage source and input impedance of AIN-0..7 analog inputs (typically 34 kOhm). Refer to original datasheet for AD7890-10 chip from Analog Devices Inc.

External analog signal sources, which are connected to AIN-0..7 analog inputs, shall provide small output impedance in order to exclude effect of input bias current/voltage of of AD7890-10 ADC chip. Using external analog signal followers or operational amplifiers is recommended for connection to AIN-0..7 analog inputs of *T/SBDAS-7890/8420* DCM.

Selection of particular AIN-0..7 analog input for analog-to-digital conversion is defined by host DSP via the corresponding bits of *COMMAND DATA WORD*, which is transmitted via transmitter of SIO-0 serial channel of host SIOX interface to the control unit of *T/SBDAS-7890/8420* DCM. The output ADC digital

code (*ADC OUTPUTDATA WORD*) is transmitted from *T/SBDAS-7890/8420* DCM to host DSP via receiver of SIO-0 port of host SIOX interface.

analog output section

Analog output section (DACU) of *T/SBDAS-7890/8420* DCM comprises of eight D/A channels, and is designed for conversion of digital code from transmitter of SIO-0 port of host SIOX interface of *TORNADO* DSP system into output analog signals (AOUT-0..7).

Each D/A channel of analog output section comprises of the following components:
- 12-bit 100ksps DAC, which is the internal DAC of one of two DAC8420 quad DAC chips from Analog Devices
- output analog buffers (A-OUT-0..7) with gain factor +6dB.

Each DAC channel of *T/SBDAS-7890/8420* DCM features excellent linearity and high-accuracy at 100 ksps conversion rates. The output voltage range of each D/A channel is well matched within 1% tolerance with the analog input range of A/D channels. A-OUT analog output buffers are used for interfacing to external low-impedance loads and provide minimum signal distortions.

CAUTION

T/SBDAS-7890/8420 DCM comes either with 4-channel or
8-channel DAC configurations.

In order to update 4-channel DAC configuration of *T/SBDAS-7890/8420* DCM to 8-channel DAC configuration, the second DAC8420 chip from Analog Devices must be installed into the on-board S1 socket (refer to fig.A-1).

Selection of particular D/A analog output channel for digital-to-analog conversion is defined by host DSP via the corresponding bits of *COMMAND DATA WORD*, which is transmitted via transmitter of SIO-0 serial channel of host SIOX interface to the control unit of *T/SBDAS-7890/8420* DCM.

control unit (CU)

On-board Control Unit (CU) of *T/SBDAS-7890/8420* DCM is implemented with the FPGA chips and offers software control of DCM operation via transmitter of SIO-0 serial channel of host SIOX interface and A/D data read via receiver of SIO-0 serial channel of host SIOX interface.

Control unit of *T/SBDAS-7890/8420* DCM can be configured by the on-board jumpers and switches, which allow selection of the following operation parameters:
- data acquisition mode, which can be selected between "SYNCHRONOUS" and "ASYNCHRONOUS" modes
- sampling frequency source
- clock frequency source
- host SIOX interrupt request input
- SIOX-Bus device ID.

data acquisition modes

Control unit of *T/SBDAS-7890/8420* DCM can operate in either of "ASYNCHRONOUS" and "SYNCHRONOUS" data acquisition modes, which differ in software programming procedures and maximum sampling rate (refer to the corresponding sections later in this chapter):

- "ASYNCHRONOUS" data acquisition mode provides AD/DA signal acquisition with simplified timing and no pipelining at reduced maximum sampling rate (typically 95kHz against maximum 100kHz in "SYNCHRONOUS" mode). This mode assumes that the AD/DA conversion cycle is initiated upon reception of software generated *CONTROL DATA WORD* via transmitter of SIO-0 port of host SIOX interface, and therefore, this mode may feature the time jitter (instability) of sampling events, which is completely defined by host DSP software. This mode must be normally used for single-time AD/DA conversions and for applications, which either feature low sampling rates or when probable sampling frequency jitter is insignificant.
- "SYNC-DATA" mode, which provides AD/DA signal acquisition with pipelining at full sampling rate 100ksps. This mode features pipelined timing diagram, possibility to select sampling frequency from different sources (SIOX timers outputs or external sampling frequency input), and no sampling frequency jitter. This mode must be normally used for full-speed AD/DA conversions for instrumentation applications, which require no sampling jitter.

Selection of data acquisition mode might be performed either by host DSP software via TM/XIO-0/1 output pins of host SIOX interface or by on-board jumper set J2-A/B/C (fig 2-1 and A-1) in accordance with table 2-1.

Table 2-1. Selection of data acquisition mode.

J2 jumper setting			TM/XIO-0 output pin of host SIOX I/F	TM/XIO-1 output pin of host SIOX I/F	data acquisition mode
J2-C	**J2-B**	**J2-A**			
OFF	*OFF*	*ON*	0	x	"ASYNHRONOUS", programmed via TM/XIO-0 SIOX output pin.
OFF	*OFF*	*ON*	1	x	"SYNCHRONOUS", programmed via TM/XIO-0 SIOX output pin.
OFF	*ON*	*OFF*	x	0	"ASYNHRONOUS", programmed via TM/XIO-1 SIOX output pin.
OFF	*ON*	*OFF*	x	1	"SYNCHRONOUS" , programmed via TM/XIO-1 SIOX output pin.
ON	*OFF*	*OFF*	x	x	"ASYNHRONOUS"
OFF	*OFF*	*OFF*	x	x	"SYNCHRONOUS"

Notes:
1. Highlighted configuration corresponds to the factory setting.
2. Jumper settings: 'OFF' - jumper not installed; 'ON' - jumper installed.
3. Logical states: '0' - logical '0'; '1' - logical '1'; 'x' - don't care.
4. Not shown configurations of J2-A/B/C jumper set are reserved and are not allowed.

CAUTION

In case data acquisition mode for *T/SBDAS-7890/8420* DCM is configured by the J2-A/B/C jumper set in accordance with table 2-1 to be defined by either TM/XIO-0 or TM/XIO-1 pin of host SIOX interface of *TORNADO* DSP system, then the corresponding TM/XIO-0 or TM/XIO-1 pin must be configured by *TORNADO* on-board DSP as output pin.

---

sampling frequency

Sampling frequency (Fs) defines time interval between sequential acquisition/conversion of the same A/D or D/A channel for multi-channel A/D and D/A devices.

In "ASYNCHRONOUS" data acquisition mode the sampling frequency is entirely defined by host DSP software as time interval between transmission of succeeding *CONTROL DATA WORDs*, which correspond to conversion of the same A/D and D/A channels. There is no possibility to use either external or SIOX timer controlled sampling frequency, so the sampling events may feature time instability (jitter).

In "SYNCHRONOUS" data acquisition mode the sampling frequency for *T/SBDAS-7890/8420* DCM can be sources either from TM/XIO-0/1 host SIOX interface output timer pins or from external sampling frequency

source XFs from external signal I/O connector JP1. Selection of particular sampling frequency source is defined by the on-board J1-A/B jumper set (fig 2-1 and A-1) in accordance with table 2-2.

Table 2-2.   Selection of sampling frequency source for "SYNCHRONOUS" data acquisition mode.

J1 jumper setting		sampling frequency (Fs) source
J1-B	**J1-A**	
OFF	*OFF*	Sampling frequency is defined by TM/XIO-1 SIOX output pin.
ON	*OFF*	Sampling frequency is defined by external XFs sampling frequency input from JP1 external I/O connector.
OFF	*ON*	Sampling frequency is defined by TM/XIO-0 SIOX output pin.

Notes: 1.   Highlighted configuration corresponds to the factory setting.
              2.   Jumper setting: 'OFF' - jumper not installed; 'ON' - jumper installed.
              3.   Not shown configurations are reserved and are not allowed.

CAUTION

In case sampling frequency source for "SYNCHRONOUS" mode of *T/SBDAS-7890/8420* DCM is configured by the J1-A/B jumper set in accordance with table 2-2 to be defined by either TM/XIO-0 or TM/XIO-1 pin of host SIOX interface of *TORNADO* DSP system, then the corresponding TM/XIO-0 or TM/XIO-1 pin must be configured by *TORNADO* on-board DSP as output pin.

---

host SIOX interrupt

In case *T/SBDAS-7890/8420* DCM is operating in "SYNCHRONOUS" mode (see the corresponding section later in this chapter), then it normally generates host DSP interrupt request in order to request for the *COMMAND DATA WORD* for the succeeding A/D and D/A conversion cycle.

Interrupt request input, which is generated by *T/SBDAS-7890/8420* DCM can be routed to either of *IRQ-0..3* SIOX interrupt request inputs via on-board jumper set J4-0/1/2 (refer to fig.2-1 and A-1) in accordance with table 2-3.

Table 2-3. Host SIOX interrupt line selection.

J4 jumper set			Host SIOX interrupt line
J4-2	**J4-1**	**J4-0**	
OFF	*OFF*	*OFF*	Host SIOX interrupt is not used.
OFF	*OFF*	*ON*	*IRQ-0* host SIOX interrupt line is used.
OFF	*ON*	*OFF*	*IRQ-1* host SIOX interrupt line is used.
ON	*OFF*	*OFF*	*IRQ-2* host SIOX interrupt line is used.

Notes:
1. Jumper setting: 'OFF' - jumper not installed; 'ON' - jumper installed.
2. Highlighted configurations correspond to the factory setting.

SIOX-Bus compliance

T/SBDAS-7890/8420 DCM meets MicroLAB Systems SIOX-Bus specifications and allows parallel connection of up to eight SIOX-Bus compliant DCMs to one SIO port of host SIOX interface.

SIOX-Bus is software superset for serial data communication protocol, which is used for data transmission via SIO ports of host SIOX interface, and has been designed in order to extend number of SIOX DCMs, which can connect to one SIO port of host SIOX interface. SIOX-Bus concept assumes that installed DCMs are a command-oriented devices and are controlled by software commands, which are transmitted from host DSP via transmitter of SIO port of host SIOX interface. Three most significant bits of transmitted data frame are interpreted as SIOX-Bus device ID and are used to select the particular SIOX-Bus DCM, which will execute the transmitted command. Once DCM recognizes that the received SIOX-Bus device ID matches its unique device ID, which is set by on-board jumpers, then this DCMs executes this command. In case this command is data read-back, then addressed DCM activates output transmitter and sends requested data to the receiver of SIO port of host SIOX interface. Unique SIOX-Bus device ID for every installed DCM must be defined by the on-board jumpers and it is not allowed to have two SIOX-Bus DCMs installed with equal SIOX-Bus device ID.

SIOX-Bus device ID for *T/SBDAS-7890/8420* DCM is defined by means of on-board 3-button SW1 switch (refer to fig.2-1 and A-1) in accordance with table 2-4.

Table 2-4.   SIOX-Bus Device ID definition.

SW1 switch setting			SIOX-Bus device ID
SW1-3	**SW1-2**	**SW1-1**	
OFF	*OFF*	*OFF*	SIOX-Bus device ID is 7.
OFF	*OFF*	*ON*	SIOX-Bus device ID is 6.
OFF	*ON*	*OFF*	SIOX-Bus device ID is 5.
OFF	*ON*	*ON*	SIOX-Bus device ID is 4.
ON	*OFF*	*OFF*	SIOX-Bus device ID is 3.
ON	*OFF*	*ON*	SIOX-Bus device ID is 2.
ON	*ON*	*OFF*	SIOX-Bus device ID is 1.
ON	*ON*	*ON*	SIOX-Bus device ID is 0.

Notes: 1. Highlighted configurations correspond to the factory setting.

CAUTION

Even in case *T/SBDAS-7890/8420* DCM is the only DCM connected to host SIOX
interface (i.e. actual multi-DCM SIOX-Bus expansion facility is not used), then host DSP
software must still provide appropriate *SIOX-Bus_DEV_ID* code in three most significant
bits of transmitted data frame in order to address *T/SBDAS-7890/8420* DCM.

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internal synchro-clock

Internal synchro-clock (SYN-CLK) for *T/SBDAS-7890/8420* DCM is used to synchronize DCM operation, and requires 10 MHz ± 1% clock source in order to obtain maximum AD/DA performance.

Internal synchro-clock for *T/SBDAS-7890/8420* DCM can be source either from the on-board 10 MHz oscillator or from the *CLKX0* pin (transmitter of SIO-0 port) of host SIOX interface. Selection of particular synchro-clock source is defined by the on-board jumper J3 jumper (refer to fig.2-1 and A-1) in accordance with table 2-5.

Table 2-5. Selection of synchro-clock source.

J3 jumper	sampling frequency (Fs) source
OFF	Internal synchro-clock is sourced from *CLKX0* output pin of host SIOX interface. *CLKX0* transmitter clock of SIO-0 port of host SIOX interface must be configured as output serial clock pin.
ON	Internal synchro-clock is sourced from on-board 10 MHz oscillator. *CLKX0* transmitter clock of SIO-0 port of host SIOX interface must be configured as input serial clock pin.

Notes: 1.   Highlighted configuration corresponds to the factory setting.
              2.   Jumper setting: 'OFF' - jumper not installed; 'ON' - jumper installed.

communication via SIOX SIO-0 serial port

T/SBDAS-7890/8420 DCM communicates with SIO-0 port of host SIOX interface via both transmitter and receiver of SIO-0 port.

The only information, which is transmitted by host DSP via transmitter of SIO-0 port of host SIOX interface is the 24-bit *COMMAND DATA WORD*, which contains addressed SIOX-Bus device ID, number of A/D channel for analog-to-digital conversion, number D/A channel for digital-to-analog conversion and the corresponding data for this D/A channel. Format of *COMMAND DATA WORD* slightly varies for "ASYNCHRONOUS: and "SYNCHRONOUS" data acquisition modes. For more details refer to the corresponding sections later in this chapter.

The only information, which is transmitted from *T/SBDAS-7890/8420* DCM to host DSP via receiver of SIO-0 port of host SIOX interface is the 16-bit ADC data. For more details refer to the corresponding sections later in this chapter.

2.2 "ASYNCHRONOUS" Data Acquisition Mode

"ASYNCHRONOUS" data acquisition mode can be set in accordance with table 2-1 either by host SIOX TM/XIO-0/1 output pins or on-board hardware via J2-A/B/C jumper set.

CAUTION

In case SIOX TM/XIO-0/1 output pins are used for selection of data acquisition mode, then the TM/XIO-0/1 output must be set to logical '0' in order to set "ASYNCHRONOUS" data acquisition mode.

---

operation description

"ASYNCHRONOUS" data acquisition mode provides AD/DA signal acquisition with simplified timing and no pipelining at reduced maximum sampling rate (typically 95kHz against maximum 100kHz in "SYNCHRONOUS" mode).

In "ASYNCHRONOUS" data acquisition mode the AD/DA conversion cycle is initiated immediately on transmission of *CONTROL DATA WORD* via transmitter of SIO-0 port of host SIOX interface. Since data transmission event via DSP on-chip serial port is completely defined by DSP software, then "ASYNCHRONOUS" mode may feature the time jitter (instability) of AD/DA sampling events.

"ASYNCHRONOUS" mode must be normally used for single/occasional AD/DA conversions and for applications, which either feature low sampling rates or when probable sampling frequency jitter is insignificant.

CONTROL DATA WORD for "ASYNCHRONOUS" data acquisition mode

CONTROL DATA WORD is the only data, which must be transmitted from host DSP to *T/SBDAS-7890/8420* DCM via transmitter of SIO-0 port of host SIOX interface.

CONTROL DATA WORD for "ASYNCHRONOUS" data acquisition mode has the following 24-bit format (data bits description is presented in table 2-6):

CONTROL DATA WORD for "ASYNCHRONOUS" data acquisition mode

DEV_ID-2..0	ADC-A2..A0	0	DAC-A2..A0	0	0	DAC-D11..D0
bit-23.. bit-21	bit-20..bit-18	bit-17	bit-16.. bit-14	bit-13	bit-12	bit-11..bit-0

CAUTION

DAC data must be specified in 2s compliment binary format, i.e. 000H data code corresponds to 0V DAC analog output voltage.

Table 2-6. Data bits description for *COMMAND DATA WORD* for "ASYNCHRONOUS" data acquisition mode.

data bit(s) of *COMMAND DATA WORD*	description
DEV_ID-2..0	SIOX-Bus device ID code. In order to address *T/SBDAS-7890/8420* DCM this received SIOX-Bus device ID code must match device ID, which is defined by the on-board switch SW1 in accordance with table 2-4.
ADC-A2..A0	Number of AIN-0..7 analog input channel (#0..#7), which will be multiplexed to the ADC input for A/D conversion.
DAC-A2..A0	Number of D/A analog output channel (#0..#7), which will be loaded with the *DAC-D11..D0* code for D/A conversion.
DAC-D11..D0	Data for D/A analog output channel, which is selected by the *DAC-A2..A0* data bits.

ADC OUTPUT DATA WORD

ADC OUTPUTDATA WORD is the only data, which is transmitted from *T/SBDAS-7890/8420* DCM to host DSP via receiver of SIO-0 port of host SIOX interface during both "ASYNCHRONOUS" and "SYNCHRONOUS" data acquisition modes.

ADC OUTPUT DATA WORD for "ASYNCHRONOUS" data acquisition mode has the following 16-bit format (data bits description is presented in table 2-7):

ADC OUTPUT DATA WORD for "ASYNCHRONOUS" data acquisition mode
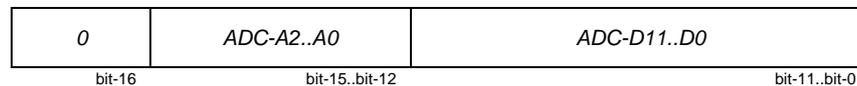
0	ADC-A2..A0	ADC-D11..D0
bit-16	bit-15..bit-12	bit-11..bit-0

CAUTION

ADC output data code is specified in 2s compliment binary format, i.e. 000H data code corresponds to 0V ADC analog input voltage.

Table 2-7.   Data bits description for *ADC OUTPUT DATA WORD* for "ASYNCHRONOUS" data acquisition mode.

data bit(s) of *ADC OUTPUT DATA WORD*	description
ADC-A2..A0	Number of AIN-0..7 analog input channel (#0..#7), which has been converted.
ADC-D11..D0	ADC data output code for selected AIN analog input.

timing diagram for "ASYNCHRONOUS" data acquisition mode

Timing diagram for "ASYNCHRONOUS" data acquisition mode and 10 MHz internal synchro-clock frequency (0.1 uS internal synchro-clock period) is presented at fig.2-2.
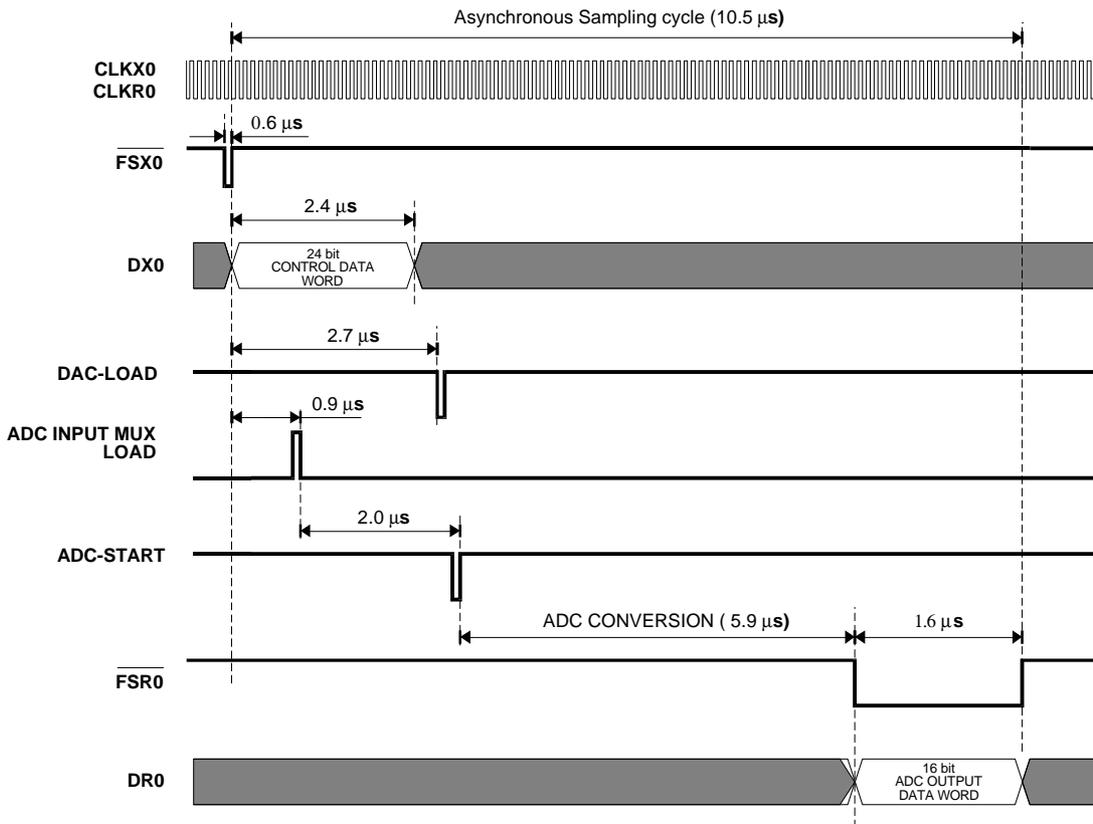

Fig. 2-2.   Timing diagram for "ASYNCHRONOUS" data acquisition mode.

Each sampling cycle during "ASYNCHRONOUS" data acquisition mode is initialized by active low FSX0 transmitter frame synch pulse, which is generated by transmitter of host DSP and which denotes transmission of 24-bit *COMMAND DATA WORD* from host DSP to *T/SBDAS-7890/8420* DCM. Active low FSX0 frame synch pulse is also the sampling event for "ASYNCHRONOUS" data acquisition mode.

Within the 0.9 uS time interval after reception of the sampling event the on-board control unit receives/verifies transmitted SIOX-Bus device ID and sets the particular A/D multiplexer input, which will be sampled and converted to digital code. Within the next 2 uS time interval the analog input signal of selected A/D multiplexer input is latched by ADC on-chip track-and-hold circuit, and active *ADC_START* signal is generated in order to start A/D conversion. After A/D conversion completes within 5.9 uS, active FSR0 receiver frame synch pulse will be generated and the ADC output data will be transmitted to the receiver of SIO-0 port of host SIOX interface during next 1.6 uS time interval. Specified analog output channel is selected and D/A data is loaded within 2.7 uS from the sampling event.

Total duration of sampling cycle for "ASYNCHRONOUS" data acquisition mode is 10.5 uS, which corresponds to 95kHz maximum sampling rate per one A/D and one D/A channels of *T/SBDAS-7890/8420* DCM.

2.3   "SYNCHRONOUS" Data Acquisition Mode

"SYNCHRONOUS" data acquisition mode can be set in accordance with table 2-1 either by host SIOX TM/XIO-0/1 output pins or on-board hardware via J2-A/B/C jumper set.

CAUTION

In case SIOX TM/XIO-0/1 output pins are used for selection of data acquisition mode, then the TM/XIO-0/1 output must be set to logical '1' in order to set "ASYNCHRONOUS" data acquisition mode.

---

operation description

"SYNCHRONOUS" data acquisition mode provides AD/DA signal acquisition with pipelined timing at maximum available 100 kHz sampling rate, and features no sampling jitter for A/D and D/A channels and accurate analog I/O signal spectrum reproduction.

 "SYNCHRONOUS" data acquisition mode provides multichannel A/D and D/A conversion via *multichannel AD/DA sampling packets*. Each sampling packet is initialized by active sampling frequency event and consists of multiple *AD/DA scan cycles*, which are executed at 100 ksps frequency, and which correspond to conversion of particular A/D and D/A channel. Number of AD/DA scan cycles is defined by the number of AD/DA channels, which have to be converted at the desired sampling frequency.

CAUTION

Total number of A/D channels, which are converted within the sampling packet, must be equal to the total number of D/A channels within the same sampling packet.

In case user application requires different number of A/D and D/A channels involved into the same sampling packet, then this application must provide extra either A/D or D/A 'false' conversions depending upon the total number of either D/A or A/D channels whichever is larger.

The particular sequence of scanned A/D and D/A channels is defined by host DSP software via the *CONTROL DATA WORDs*, which are transmitted from host DSP to *T/SBDAS-7890/8420* DCM via transmitter of SIO-0 port of host SIOX interface during every AD/DA scan cycle. Last AD/DA scan cycle sets EOS end-of-scan bit in *CONTROL DATA WORD*, so the scan controller can stall upon reception of new sampling frequency event.

CAUTION

"SYNCHRONOUS" data acquisition mode features pipelined operation for AD/DA scan cycle, i.e. the numbers of A/D and D/A channels, which are converted in the current scan cycle, shall be defined in the *CONTROL DATA WORD*, which has been transmitted in the previous scan cycle.

The A/D conversion of pre-selected AIN analog input and reload of data for pre-selected D/A channel are both performed at the scan frequency event and do not have any time jitter.

"SYNCHRONOUS" mode must be used for full-speed AD/DA conversions for instrumentation and other applications, which require no sampling jitter.

sampling frequency

"SYNCHRONOUS" data acquisition mode allows selection of sampling frequency from either TM/XIO-0/1 timers output pins of host SIOX interface or from external sampling frequency input XFs of external signal I/O connector JP1. Selection of sampling frequency source is performed by means of the on-board J1-A/B jumper in accordance with table 2-2.

CAUTION

In case J1 jumper set is configured for external XFs sampling frequency signal source, then this XFs signal must provide active low duration at least two internal synchro-clock periods for *T/SBDAS-7890/8420* DCM.

CAUTION

In case J1 jumper set is configured for using TM/XIO-0/1 timer outputs of host SIOX interface as sampling frequency signal source, then TM/XIO-0/1 output must provide XFs signal must provide active low duration at least two internal synchro-clock periods for *T/SBDAS-7890/8420* DCM.

CONTROL DATA WORD for "SYNCHRONOUS" data acquisition mode

CONTROL DATA WORD is the only data, which must be transmitted from host DSP to *T/SBDAS-7890/8420* DCM via transmitter of SIO-0 port of host SIOX interface.

CONTROL DATA WORD for "SYNCHRONOUS" data acquisition mode has the following 24-bit format (data bits description is presented in table 2-8):

CONTROL DATA WORD for "SYNCHRONOUS" data acquisition mode

DEV_ID-2..0	ADC-A2..A0	EOS	DAC-A2..A0	0	0	DAC-D11..D0
bit-23.. bit-21	bit-20..bit-18	bit-17	bit-16.. bit-14	bit-13	bit-12	bit-11..bit-0

CAUTION

DAC data must be specified in 2s compliment binary format, i.e. 000H data code corresponds to 0V DAC analog output voltage.

Table 2-8.   Data bits description for *COMMAND DATA WORD* for "ASYNCHRONOUS" data acquisition mode.

data bit(s) of *COMMAND DATA WORD*	description
DEV_ID-2..0	SIOX-Bus device ID code. In order to address *T/SBDAS-7890/8420* DCM this received SIOX-Bus device ID code must match device ID, which is defined by the on-board switch SW1 in accordance with table 2-4.
ADC-A2..A0	Number of AIN-0..7 analog input channel (#0..#7), which will be multiplexed to the ADC input for A/D conversion.
EOS	End-of-scan flag, which must be set to logical '1' by the last scan cycle within the sampling packet in order to stall scan controller upon reception of new sampling event and beginning of new sampling packet. In case continuous scan cycles are required, then EOS flag must be transmitted as logical '0'.
DAC-A2..A0	Number of D/A analog output channel (#0..#7), which will be loaded with the *DAC-D11..D0* code for D/A conversion.
DAC-D11..D0	Data for D/A analog output channel, which is selected by the *DAC-A2..A0* data bits.

ADC OUTPUT DATA WORD

ADC OUTPUTDATA WORD is the only data, which is transmitted from *T/SBDAS-7890/8420* DCM to host DSP via receiver of SIO-0 port of host SIOX interface during both "ASYNCHRONOUS" and "SYNCHRONOUS" data acquisition modes.

ADC OUTPUT DATA WORD for "SYNCHRONOUS" data acquisition mode has the following 16-bit format (data bits description is presented in table 2-9):

ADC OUTPUT DATA WORD for "SYNCHRONOUS" data acquisition mode
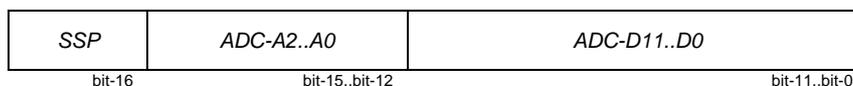
SSP	ADC-A2..A0	ADC-D11..D0
bit-16	bit-15..bit-12	bit-11..bit-0

CAUTION

ADC output data code is specified in 2s compliment binary format, i.e. 000H data code corresponds to 0V ADC analog input voltage.

Table 2-9. Data bits description for *ADC OUTPUT DATA WORD* for "SYNCHRONOUS" data acquisition mode.

data bit(s) of *ADC OUTPUT DATA WORD*	description
ADC-A2..A0	Number of AIN-0..7 analog input channel (#0..#7), which has been converted.
ADC-D11..D0	ADC data output code for selected AIN analog input.
SSP	Start of sampling packet flag. When SSP=1, then this received ADC data corresponds to the first scan cycle within new sampling packet.

timing diagram for "SYNCHRONOUS" data acquisition mode

Timing diagram for "SYNCHRONOUS" data acquisition mode and 10 MHz internal synchro-clock frequency (0.1 uS internal synchro-clock period) is presented at fig.2-3.
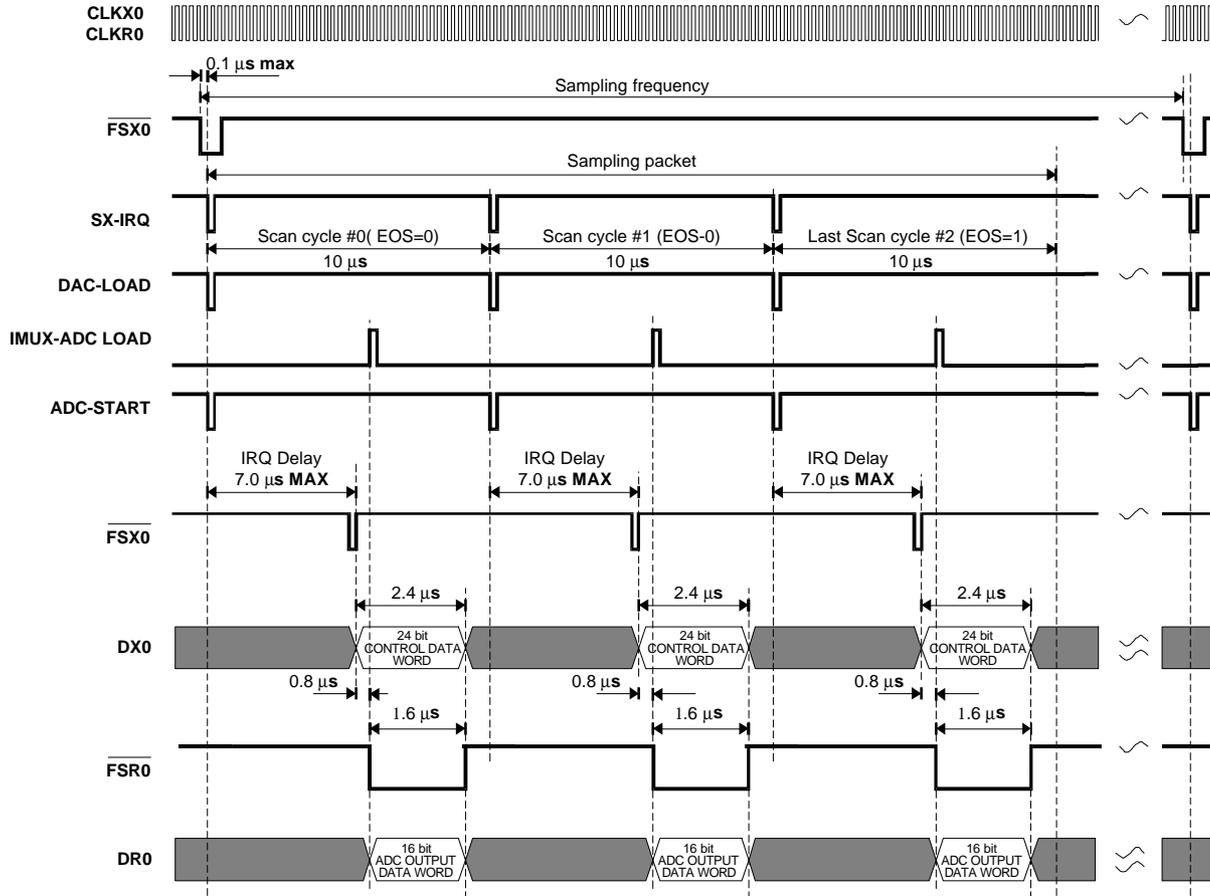
Fig. 2-3.   Timing diagram for "SYNCHRONOUS" data acquisition mode.

Each sampling cycle during "SYNCHRONOUS" data acquisition mode is initialized on the falling edge of input sampling frequency input, which is called the sampling event.

New sampling event enables new sampling packet and restarts scan controller, which generates a series of scan cycles within new sampling packet.

Every scan cycle within the sampling packet latches the analog input signal of pre-selected A/D multiplexer input by means of ADC on-chip track-and-hold circuit and generates *ADC_START* and *LOAD_DAC* signals in order to start A/D conversion and load pre-selected D/A channel correspondingly.

CAUTION

Pre-selection of A/D multiplexer input and of D/A channel, which will be correspondingly converted and loaded in the current scan cycle, shall be specified via *CONTROL DATA WORD*, which must be transmitted from host DSP in the previous scan cycle.

Also, every scan cycle generates active *SX_IRQ* interrupt request for host DSP via SIOX interface. This SIOX interrupt request must be used by host DSP to transmit new *CONTROL DATA WORD*, which can be performed either by means of true DSP interrupt procedure (DSP interrupt procedure must load data to the transmitter of DSP on-chip serial port), or by means of DSP on-chip DMA controller (*SX_IRQ* interrupt request for host DSP must be configured as synchro-event for DMA controller). *CONTROL DATA WORD* for "SYNCHRONOUS" data acquisition mode (refer to table 2-6 for more details) is used to enable/stall scan controller by EOS bit and contains information about A/D and D/A channels, which will be correspondingly converted and loaded in the next scan cycle.

CAUTION

Transmitter of SIO-0 port of host SIOX interface must begin transmission of new *CONTROL DATA WORD* within 7.5 µS from the beginning of current scan cycle in order to leave enough time room for loading the ADC analog input multiplexer, sampling the selected analog input by ADC on-chip track-and-hold circuit, and in order to set EOS bit prior beginning of new scan cycle.

CAUTION

Reception of *CONTROL DATA WORD* with EOS=0 condition within current scan cycle denotes that new scan cycle will be generated immediately after the current scan cycle.

Reception of *CONTROL DATA WORD* with EOS=1 condition within current scan cycle denotes that new scan cycle will stall scan controller after the current scan cycle completes. Scan controller can be restarted only by new sampling event, i.e. by the beginning of the next sampling packet.

Transmission of ADC data to host DSP via receiver of SIO-0 port of host SIOX interface is initiated within 0.8 µS time interval after reception of FSX0 transmitter frame synch pulse of SIO-0 port of host SIOX interface and is performed only in case the received SIOX-Bus device ID in *CONTROL DATA WORD* matches the on-board configured SIOX-Bus device ID via on-board SW1 switch.

Transmitted *ADC OUTPUT DATA WORD* contains 16-bit data (refer to the corresponding subsection above in this section) and is framed by active low FSR0 receiver frame synch pulse for SIO-0 port of host SIOX interface. Transmission of *ADC OUTPUT DATA WORD* takes 1.6 µS for 10 MHz internal synchro-clock.

<div style="border:1px solid">

CAUTION

Scan cycles within the sampling packet are generated by hardware scan controller with 10 uS
period (actually with period, which is equal to 100 periods of internal synchro-clock), which
corresponds to maximum ADC and DAC performance. Hardware generated scan cycles
feature high time stability and exclude time jitter for converted A/D and D/A signals, i.e. do
not induce any distortions into I/O signal spectrum.

</div>

2.4   Host SIOX Serial Port Configurations

Transmitter of SIO-0 port of host SIOX interface is used to transmit *CONTROL DATA WORD* to *T/SBDAS-
7890/8420* DCM, whereas the receiver of SIO-0 port of host SIOX interface is used to receive *ADC OUTPUT
DATA WORD*.

Transmitter and receiver configurations are identical for both "ASYNCHRONOUS" and "SYNCHRONOUS"
data acquisition modes..

SIOX SIO-0 port transmitter configuration

Transmitter of SIO-0 port of host SIOX interface is used for transmission of *CONTROL DATA WORD* from
host DSP to *T/SBDAS-7890/8420* DCM.

Timing diagram for transmission of *CONTROL DATA WORD* from host DSP via transmitter of SIO-0 port
of host *TORNADO* SIOX interface to *T/SBDAS-7890/8420* DCM is presented at fig.2-4.
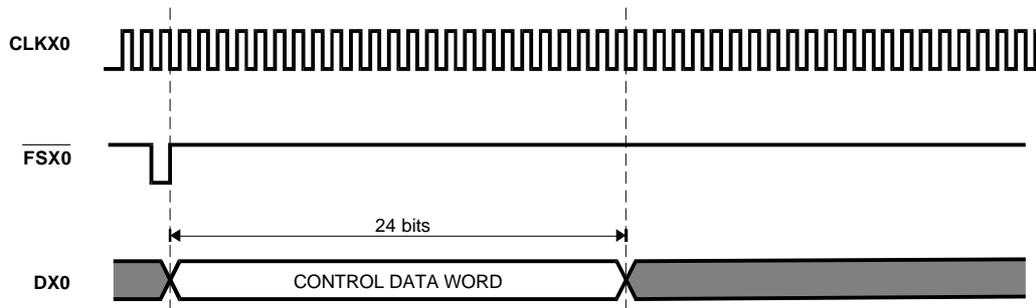
Fig. 2-4. Timing diagram for transmission of *CONTROL DATA WORD* from host DSP to *T/SBDAS-
7890/8420* DCM via transmitter of SIOX SIO-0 port.

The DSP on-chip transmitter, which is wired to the transmitter of SIO-0 port of host SIOX interface, must be
configured as the following:
  • transmitter clock (CLKX) must be configured as external active low clock (active falling edge) in
    case jumper J3 is configured for on-board generated 10 MHz synchro-clock for *T/SBDAS-
    7890/8420* DCM in accordance with table 2-5

- transmitter clock (CLKX) must be configured as internally DSP generated active low clock (active falling edge) in case jumper J3 is configured for using CLKX0 as synchro-clock for *T/SBDAS-7890/8420* DCM in accordance with table 2-5
- transmitter data (DX) must be configured as active high with data frame containing 24-bits for transmission of *CONTROL DATA WORD*
- transmitter frame synch pulse (FSX) must be configured as active low output with 1 cycle advance feature in order to have FSX generated one cycle before transmitter data are being transmitted (for TMS320C3x DSP this is performed by means of setting STANDARD MODE and FIXED DATA RATE for transmitter).

SIOX SIO-0 port receiver configuration

Receiver of SIO-0 port of host SIOX interface is used for transmission *ADC OUTPUT DATA WORD* from *T/SBDAS-7890/8420* DCM to host DSP.

Timing diagram for transmission of *ADC OUTPUT DATA WORD* from *T/SBDAS-7890/8420* DCM to host DSP via receiver of SIO-0 port of host *TORNADO* SIOX interface is presented at fig.2-5.
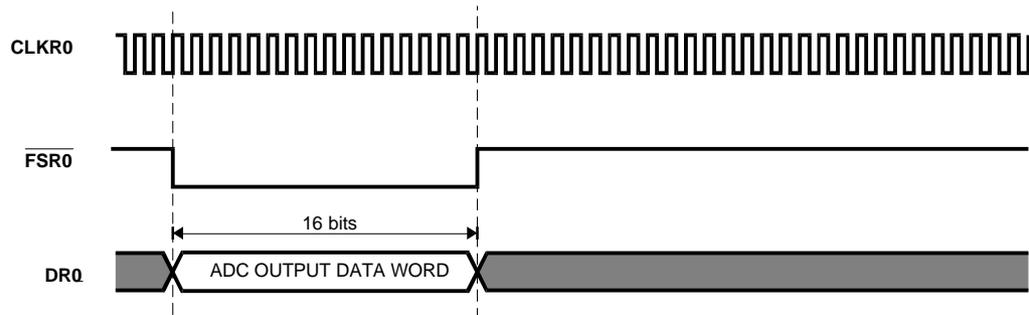
Fig. 2-5. Timing diagram for transmission of *ADC OUTPUT DATA WORD* from *T/SBDIO-16 DCM* to host DSP via receiver of SIOX SIO-0 port.

The DSP on-chip receiver, which is wired to the receiver of SIO-0 port of host SIOX interface, must be configured as the following:
- receiver clock (CLKR) must be configured as external active high clock (active rising edge)
- receiver data (DR) must be configured as active high with data frame containing 16-bits for reception of *ADC OUTPUT DATA WORD*
- receiver frame synch pulse (FSX) must be configured as active low input with the framing feature in order to support FSR, which is generated *T/SBDAS-7890/8420* DCM along with data transmitted to host SIOX interface (for TMS320C3x DSP this is performed by means of setting STANDARD MODE and VARIABLE DATA RATE for receiver).

2.5   Construction

T/SBDAS-7890/8420 DCM (fig.1-1, fig.A-1) meets standard SIOX rev.B daughter-card form-factor. Construction of *T/SBDAS-7890/8420* DCM assumes that host *TORNADO* DSP system with *T/SBDAS-7890/8420* DCM installed fits into one ISA-bus slot of PC chassis.

Connection of *T/SBDAS-7890/8420* DCM to external analog I/O world is performed via the on-board JP1 connector, which is available via rear panel of host PC (if *T/SBDAS-7890/8420* is installed onto *TORNADO* DSP system for PC). Compatible cable with sixteen analog I/O RCA jacks and one external sampling frequency RCA jack is provided as standard with *T/SBDAS-7890/8420* DCM.

Chapter 3. Installation

This chapter contains information for installation and configuration of *T/SBDAS-7890/8420* DCM.

3.1   Installation

T/SBDAS-7890/8420 DCM installs as SIOX daughter-card DCM onto *TORNADO* DSP system mainboard.

For installation of *T/SBDAS-7890/8420* DCM into SIOX site of *TORNADO* DSP system follow the recommendations below (fig.3-1):

1. Switch off the power of host PC.
2. Remove *TORNADO* mainboard from PC slot.
3. Take *T/SBDAS-7890/8420* DCM and slant it for about 30°..40° degrees refer to *TORNADO* mainboard. Insert JP1 external I/O connector of *T/SBDAS-7890/8420* DCM into the corresponding hole of mounting bracket of *TORNADO* DSP system.
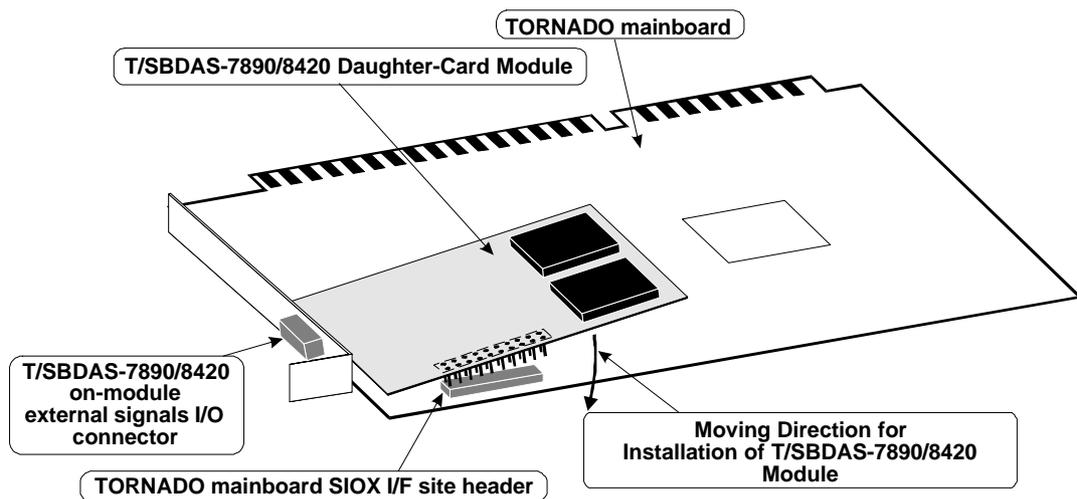

Fig. 3-1.   Installation of *T/SBDAS-7890/8420* DCM into SIOX site of *TORNADO* DSP system.

4. Rotate *T/SBDAS-7890/8420* DCM around mounting bracket and allocate pin #1 of JP2 connector of *T/SBDAS-7890/8420* DCM against pin #1 of SIOX interface header on *TORNADO* mainboard.

CAUTION

Female connector of host SIOX interface has 20 pins for *TORNADO-31/31Z/31M/32L/32LX/E31* DSP systems and controllers and 26 pins for *TORNADO-30/54x/6x/E6x/E54x* DSP systems and controllers. Pin #1 of host SIOX site connectors always fit into the same physical position on *TORNADO* DSP systems and controllers.

Pin #1 of SIOX connector of *T/SBDAS-7890/8420* DCM must always plug into pin #1 of host SIOX site connector not regarding type of host *TORNADO* DSP systems or controller.

Missing doing this will result in damage of *T/SBDAS-7890/8420* DCM and/or host *TORNADO* hardware.

5. Safely plug-in SIOX male header of *T/SBDAS-7890/8420* DCM into SIOX female header of *TORNADO* DSP system.
6. Screw external analog I/O connector shell of *T/SBDAS-7890/8420* DCM to the mounting bracket of *TORNADO* DSP system.
7. Configure on-board switch SW1 in order to set desired SIOX-Bus device ID to match your software provided SIOX-Bus device ID for addressing this *T/SBDAS-7890/8420* DCM (refer to table 2-4).
8. Configure on-board jumper set J1 for selection of sampling frequency source in accordance with table 2-2.
9. Configure on-board jumper set J2 for selection of data acquisition mode control in accordance with table 2-1.
10. Configure on-board jumper J3 for selection of internal synchro-clock source in accordance with table 2-5.
11. Configure on-board jumper set J4 in order to select particular host SIOX interrupt request line to meet requirements of your software (refer to table 2-3).
12. Install *TORNADO* board into PC slot and screw it to rear panel of PC.
13. Connect the plug to external analog I/O connector of *T/SBDAS-7890/8420* DCM.
14. Switch on power of host PC.

3.2   Connection to external signal I/O equipment

Connection of *T/SBDAS-7890/8420* DCM to external analog I/O equipment is performed by means of on-board JP1 connector (fig.A-1) and external I/O cable set.

```
┌─────────────────────────────────────────────────────────────────────────┐
│ ┌───────────────────────────────────────────────────────────────────────┐ │
│ │                                                                       │ │
│ │                             CAUTION                                   │ │
│ │                                                                       │ │
│ │   It is highly recommended to plug-in and unplug external I/O cable   │ │
│ │   set into/from on-board                                              │ │
│ │   JP1 connector of T/SBDAS-7890/8420 DCM when host TORNADO power      │ │
│ │   is switched off.                                                    │ │
│ │                                                                       │ │
│ │   The ground signal of T/SBDAS-7890/8420 DCM has no halvanic          │ │
│ │   isolation from host                                                 │ │
│ │   TORNADO and/or PC ground signal and chassis.                        │ │
│ │                                                                       │ │
│ └───────────────────────────────────────────────────────────────────────┘ │
└─────────────────────────────────────────────────────────────────────────┘
```

CAUTION

It is highly recommended to plug-in and unplug external I/O cable set into/from on-board JP1 connector of *T/SBDAS-7890/8420* DCM when host *TORNADO* power is switched off.

The ground signal of *T/SBDAS-7890/8420* DCM has no halvanic isolation from host *TORNADO* and/or PC ground signal and chassis.

CAUTION

When connecting external analog I/O equipment to *T/SBDAS-7890/8420* DCM you should be aware that AIN-0..7 analog inputs and AOUT-0..7 analog outputs of *T/SBDAS-7890/8420* DCM are DC coupled. If required, external DC isolation capacitors should be used.

External I/O cable set for *T/SBDAS-7890/8420* DCM uses standard miniature RCA jacks for connection to external analog I/O equipment with single-ended I/O signals. This set comprises of 16 jacks:

- AIN-0..7 analog in channels #0..#7
- AOUT-0..7 analog out channels #0..#7
- XFs external sampling frequency input.

Appendix A.   On-board Connectors, Switches and Jumpers

This appendix contains a summary for the on-board connectors, configuration jumpers, configuration switches and sockets for *T/SBDAS-7890/8420* DCM.

The on-board connectors, switches, configuration jumpers and sockets are presented at fig.A-1.
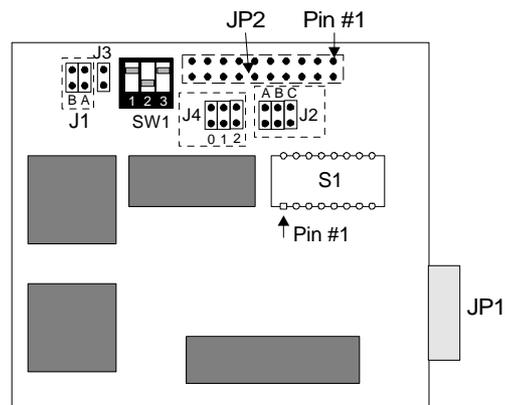

Fig. A-1. On-board connectors, switches and jumpers for *T/SBDAS-7890/8420* DCM.

A.1   Configuration Jumpers

Table A-1 contains the list of on-board configuration jumpers.

<p align="center">*Table A-1.* Configuration jumpers.</p>

Jumper	Description	Reference information
J1	Selects sampling frequency source.	Section 2-1 table 2-2
J2	Selects data acquisition mode control.	Section 2-1 table 2-1
J3	Selects internal synchro-clock source.	Section 2-1 table 2-5
J4	Selects host SIOX interrupt request line.	Section 2-1 table 2-3

A.2   On-board Connectors

Table A-2 contains the list of on-board connectors.

<p align="center">*Table A-2.* On-board connectors of *T/SBDAS-7890/8420* DCM.</p>

Connector	description
JP1	External analog I/O connector.
JP2	SIOX interface site male header.

Pinout of JP2 host SIOX connector is presented in the user's guide of host *TORNADO* DSP system or controller, which is used for installation of *T/SBDAS-7890/8420* DCM. general description of host SIOX interface site is presented in Appendix B.

Pinout for external I/O connector

Pinout of JP1 external I/O connector for *T/SBDAS-7890/8420* DCM is presented at fig.A-2, and description of signals is presented in table A-3.

The connector p/n for JP1 is DHA-RA20 female half-pitch connector from DDK Ltd manufacturer. P/n for compatible plug-in connector is DHA-PC20. In case customer needs to design his own application specific cable for connection to *T/SBDAS-7890/8420* DCM, then compatible plug-in connectors for JP1 are available from MicroLAB Systems upon request.

AOUT-0	2		1	AIN-7
AOUT-1	4		3	AIN-6
AOUT-2	6		5	AIN-5
AOUT-3	8		7	AIN-4
AOUT-4	10		9	AIN-3
AOUT-5	12		11	AIN-2
AOUT-6	14		13	AIN-1
AOUT-7	16		15	AIN-0
A_GND	18		17	A_GND
GND	20		19	XFs
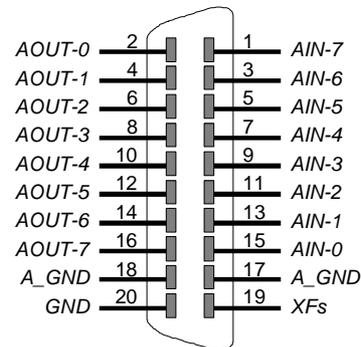
Fig. A-2. Pinout for JP1 external I/O connector of *T/SBDAS-7890/8420* DCM.

Table A-3. Signal description for JP1 external I/O connector of *T/SBDAS-7890/8420* DCM.

Signal name	type	description
AIN-0 *AIN-1* *AIN-2* *AIN-3* *AIN-4* *AIN-5* *AIN-6* *AIN-7*	AI	Analog input channels A/D-0..A/D-7.
AOUT-0 *AOUT-1* *AOUT-2* *AOUT-3* *AOUT-4* *AOUT-5* *AOUT-6* *AOUT-7*	AO	Analog output channels D/A-0..D/A-7.
XFs	TTL/IN	External sampling frequency input.
GND	-	Ground.

Notes: 1. Signal types: *AI* - analog input; *AO* - analog output; *TTL/IN* - TTL compatible digital input.

A.3   Configuration Switches

Table A-4 contains the list of on-board configuration switches.

Table A-4. Configuration switches.

Switch	Description	Reference information
SW1	Defines SIOX-Bus device ID for *T/SBDAS-7890/8420* DCM.	Section 2-1 table 2-4

A.4 On-board Sockets.

Table A-5 contains the list of on-board sockets.

Table A-5. On-board sockets.

Socket	Description	Reference information
S1	Socket for ADI DAC8420 chip in DIP-16 IC package, which must be installed in order to upgrade 4-channel DAC configuration of *T/SBDAS-7890/8420* DCM to 8-channel DAC configuration.	Section 2-1

Appendix B. SIOX Rev.B Interface Site

This appendix contains information about *TORNADO* SIOX rev.B interface site specifications. This description is general to all *TORNADO* DSP systems/controllers/coprocessors, whereas different *TORNADO* boards with different DSP platforms may differ in the number and in the on-board routing of SIOX serial ports, timer/IO pin specifications. Refer to your particular *TORNADO* user's guide for more details.

B.1   General Description

TORNADO architecture provides expansion of the on-board DSP I/O resources via on-board serial I/O expansion interface sites (SIOX-A and SIOX-B) (fig.B-1), which are designed to carry compatible DCMs (DCM).

Fig.B-1.   TORNADO-54x board with two SIOX sites.

Some *TORNADO* boards (typically *TORNADO* DSP systems for PC) provide two SIOX interface sites, whereas other *TORNADO* boards (typically *TORNADO* stand-alone DSP controllers and DSP coprocessors) provide only one SIOX site.

TORNADO SIOX rev.B interface site comprises of signals for one or two SIO-0/SIO-1 logical serial ports, timers/IO pins, DSP interrupts, and host power supplies.

CAUTION

In case *TORNADO* on-board DSP features two or more on-chip serial ports (TMS320C30,
TMS320C54x, TMS320C6x), then *TORNADO* on-board SIOX sites provides two SIO-0 and
SIO-1 serial ports and the SIOX site headers are 26-pin headers.

In case *TORNADO* on-board DSP features only one on-chip serial ports (TMS320C31,
TMS320C32), then *TORNADO* on-board SIOX sites provides only one SIO-0 serial port
and the SIOX site headers are 20-pin headers.

Both *TORNADO* on-board SIOX-A and SIOX-B interface sites feature identical pinout control and may only
differ in the routing of DSP physical serial ports to SIO-0 and SIO-1 logical serial ports. If *TORNADO* on-
board DSP features two or more on-chip serial ports (TMS320C30, TMS320C54x, TMS320C6x), then DSP
serial ports routing is performed on *TORNADO* mainboard, and allows simultaneous operation of two or more
SIOX DCM, which are routed to different DSP serial ports.

B.2   SIOX Site Connector and Signals

TORNADO SIOX rev.B interface site comprises of signals for SIO-0 and SIO-1 logical serial ports, DSP on-
chip TM/XIO-0/1 timers/IO pins, three DSP interrupts, SIOX reset control, and power ±5V/±12V host power
supplies.

TORNADO on-board SIOX site connector with two serial ports

TORNADO on-board SIOX site connector with two serial ports is an industry standard dual-row 26-pin
female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM should be the industry
standard either 26-pin 0.1"x0.1"male header (in case both SIO-0 and SIO-1 serial ports are utilized on SIOX
plugged-in DCM) or 20-pin 0.1"x0.1"male header (in case only SIO-0 serial port is utilized on SIOX plugged-
in DCM).

SIOX site connector pinout with two serial ports is shown at fig.B-2 and signal specifications are listed in table
B-1.
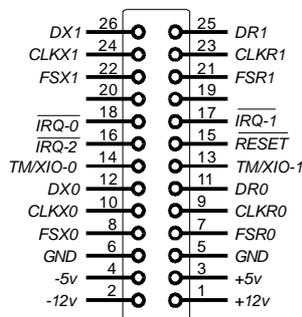
Fig.B-2. TORNADO on-board SIOX connector pinout with two serial ports (top view).

TORNADO on-board SIOX site connector with one serial port

TORNADO on-board SIOX site connector with one serial port is an industry standard dual-row 20-pin female header with 0.1"x0.1" pin pattern. Compatible SIOX plug-in part on SIOX DCM should be the industry standard 20-pin 0.1"x0.1"male header.

SIOX site connector pinout with one serial ports is shown at fig.B-3 and signal specifications are listed in table B-1.
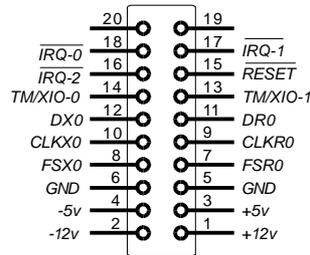

Fig.B-3. TORNADO on-board SIOX connector pinout with one serial port (top view).

SIOX site signal description

Description for SIOX interface site signals is presented in table B-1.

Table B-1. SIOX interface signal description.

SIOX signal name	signal type	description
SIO-0 port control		
DX0 FSX0 CLKX0	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-0 port of SIOX site..
DR0 FSR0 CLKR0	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-0 port of SIOX site..
SIO-1 port control *(available in SIOX site connector with two serial ports only)*		
DX1 FSX1 CLKX1	O/Z I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for transmitter of SIO-1 port of SIOX site..
DR1 FSR1 CLKR1	I I/O/Z I/O/Z	Data, frame synchronization and serial clock signals for receiver of SIO-1 port of SIOX site..

DSP Timers/IO, DSP Interrupt Requests and SIOX Reset		
TM/XIO-0	I/O/Z	This signal is typically connected to the DSP on-chip timer-0 I/O pin and can be software configured by DSP as either timer or I/O pin.
TM/XIO-1	I/O/Z	This signal is typically connected to the DSP on-chip timer-1 I/O pin and can be software configured by DSP as either timer or I/O pin.
$\overline{RESET}$	O	Active low SIOX reset signal. Some *TORNADO* boards (for example *TORNADO-3x* boards) wires this signal directly from the DSP reset signal and SIOX plugged-in DCM reset is performed simultaneously with *TORNADO* on-board DSP reset, however other *TORNADO* boards (for example *TORNADO-54x/6x* etc. boards) features dedicated SIOX site reset signal, which is controlled by TORNADO on-board DSP for better synchronization between the DSP software and SIOX DCM operation.
$\overline{IRQ\text{-}0}$, $\overline{IRQ\text{-}1}$, $\overline{IRQ\text{-}2}$	I	Active low external interrupt request lines for TORNADO on-board DSP. These line are pulled up.
Power Supplies		
GND		Ground.
+5v		+5v
+12v		+12v
-5v		-5v
-12v		-12v

Note: 1.   Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.
            1.   All logical signal levels and load currents correspond to that for CMOS/TTL signals.

SIOX site signal levels

Signal levels for SIOX interface signals correspond to that for the CMOS/TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

> **CAUTION**
>
> Some *TORNADO* boards (*TORNADO-3x/542L/E31*) provide SIOX interface signal levels
> for CMOS/TTL only, whereas other *TORNADO* boards (*TORNADO-54xx/6x/E6x/P6x*)
> provide SIOX interface signal levels universal for both 3V TLL and standard TTL. Refer to
> documentation for your particular *TORNADO* board for information about SIOX interface
> signal levels.

B.3   Physical Dimensions for SIOX DCM

Physical dimensions for SIOX DCM are presented at fig.B-4. This information is intended for those customers,
who need to design customized SIOX DCMs.
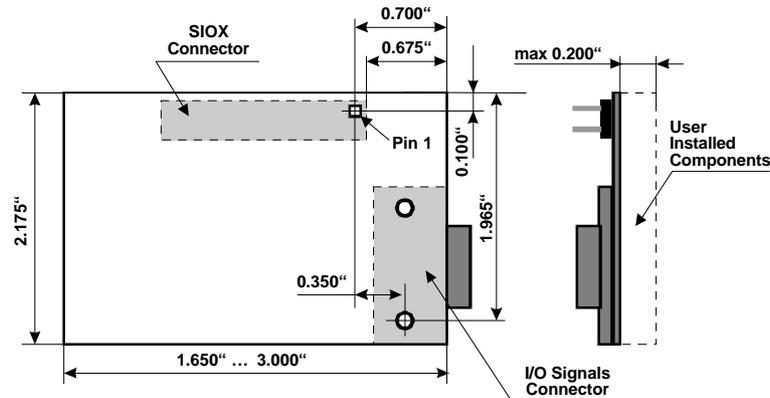
SIOX connector: 20-pin or 26-pin straight dual-row mail header
(0.025" Sq., 0.1"x0.1" pattern)

Recommended connector for Analog I/O: DDK DHA-RC14-R122N
DDK DHA-RC20-R122N
DDK DHA-RC26-R122N

Fig.B-4.   Physical dimensions for SIOX DCM.