T/PDAS-AD8/12D/65M-DA2/12D/65M

65 Msps 12-bit Multi-channel Instrumentation AD/DA PIOX-16 DCM
for *TORNADO* DSP Systems/Controllers

User's Guide

covers:
T/PDAS-AD8/12D/65M-DA2/12D/65M rev.1A/1B

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About this Document

This user's guide contains description for *T/PDAS-AD8/12D/65M-DA2/12D/65M* 65 Msps multi-channel instrumentation AD/DA daughter-card module (DCM) for *TORNADO* DSP systems/controllers.

This document does not include detail description neither for the on-board components nor for the corresponding software and hardware applications. To get the corresponding information refer to the following documentation:
1. *TORNADO-3x. User's Guide.* MicroLAB Systems, 1998.
2. *TORNADO-P33. User's Guide.* MicroLAB Systems, 2000.
3. *TORNADO-54x. User's Guide.* MicroLAB Systems, 1998.
4. *TORNADO-6x. User's Guide.* MicroLAB Systems, 1998.
5. *TORNADO-P6x. User's Guide.* MicroLAB Systems, 1999.
6. *TORNADO-E31. User's Guide.* MicroLAB Systems, 1996.
7. *TORNADO-E33. User's Guide.* MicroLAB Systems, 2000.
8. *TORNADO-E6x. User's Guide.* MicroLAB Systems, 1998.

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Chapter 1.   Introduction

This chapter contains general description for *T/PDAS-AD8/12D/65M-DA2/12D/65M* 65 Msps multi-channel instrumentation AD/DA PIOX-16 daughter-card module (DCM) for *TORNADO* DSP systems/controllers.

1.1   General Information

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM (fig.1-1) provides 65 Msps 8-channel 12-bit A/D and 2-channel 12-bit D/A data acquisition facilities and plugs into the PIOX-16 (parallel I/O expansion) site of *TORNADO* DSP systems (*TORNADO-3x/54x/6x/P3x/P6x/etc*) and *TORNADO-E* stand-alone DSP controllers (*TORNADO-E3x/E6x/etc*) from MicroLAB Systems Ltd.

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM has been designed for multi-channel ultra high-frequency and accurate analog and digital I/O instrumentation applications.

Fig. 1-1.   T/PDAS-AD8/12D/65M-DA2/12D/65M DCM.

Installation onto TORNADO DSP System/Controller

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM installs as PIOX-16 DCM (fig.1-2) into the PIOX-16 site onto *TORNADO* DSP system/controller mainboard.
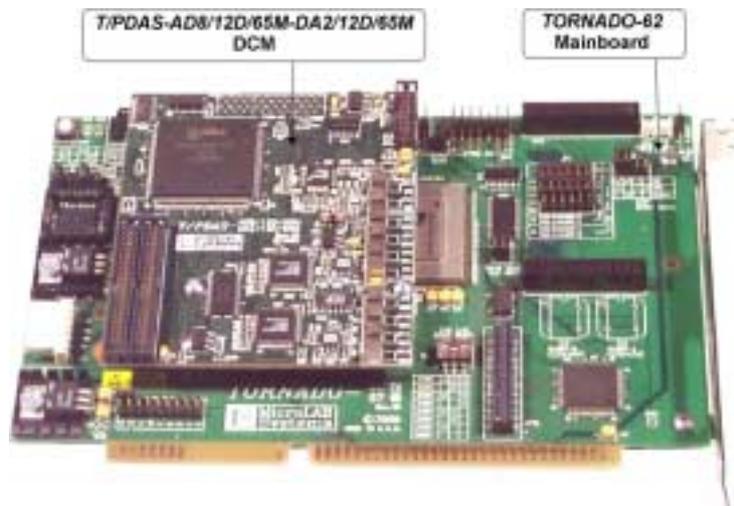
Fig. 1-2.   T/PDAS-AD8/12D/65M-DA2/12D/65M DCM installed onto *TORNADO-31* mainboard.

Overview

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM features the following main on-board components:
- dual-channel synchronous 12-bit 65 Msps analog-to-digital converter (ADC) with 4:1 analog input multiplexer for each ADC channel
- alternative 32-bit synchronous parallel digital stream input
- input data streams multiplexer with high-depth FIFO
- dual-channel synchronous 12-bit 65 Msps digital-to-analog converters (DAC)
- alternative 32-bit synchronous parallel digital stream output
- output data streams multiplexer with high-depth FIFO
- set of programmable peripherals
- host PIOX-16 interface.

On-board dual-channel synchronous A/D and D/A sections feature 12-bit resolution and excellent linearity at up to 65 MHz sampling frequency, which guarantee minimum signal distortion during A/D and D/A conversions at ultra-high sampling frequencies. Also, each A/D channel allows undersampling of input signals and features 4:1 analog input multiplexer, which allows to select particular analog input pair from four available for A/D conversion (totally 8 analog inputs).

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM also allows to perform alternative synchronous digital I/O of external 32-bit I/O data streams instead of ADC and DAC data in order to operate as digital signal synthesizer/registrator and to interface to external devices, which require ultra-high speed parallel digital I/O data streams instead of analog I/O.

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM provides on-board input and output data streams multiplexers in order to select between ADC data and external digital input stream and between DAC data and external digital output data stream correspondingly. Each I/O data stream multiplexer features high-depth 32-bit FIFO.

Multiple *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, which are installed on different *TORNADO* DSP systems/controllers, can be configured to run synchronously in order to extend number of AD/DA or digital I/O while maintaining absolutely synchronous data acquisition timing.

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM also contains a set of on-board peripherals, which are controlled via host PIOX-16 interface. These on-board peripherals comprise of high-resolution sampling frequency generator and 4-bit general purpose digital I/O.

Host PIOX-16 interface provides access to on-board I/O FIFO and contains a set of control registers for data acquisition control, host interrupt selection, and for error processing.

External signal I/O

Connection of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM to external analog and digital I/O world is performed either via on-board I/O connectors or by means of external I/O board (*T/X-XIOB/PDAS-AD8/12D/65M-DA2/12D/65M*) (fig.1-3 and refer to Appendix C).

T/X-XIOB/PDAS65M external I/O board splits *T/PDAS-AD8/12D/65M-DA2/12D/65M* on-board I/O connectors into two groups: the 1st group contains analog I/O signals, whereas the 2nd group comprises of external clock and synchronization I/O pins and general purpose digital I/O pins.
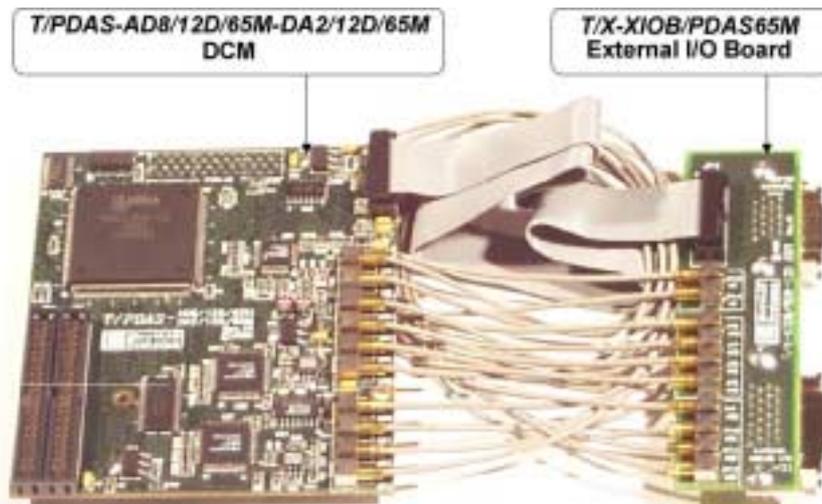
Fig. 1-3. *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and *T/X-XIOB/PDAS65M* external I/O board.

T/X-XIOB/PDAS65M external I/O board installs either to the rear mounting bracket of host *TORNADO* DSP system in case *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is installed onto *TORNADO* DSP system for PC (fig.1-4), or can install directly at the rear panel of host PC.

Fig. 1-4.   T/PDAS-AD8/12D/65M-DA2/12D/65M DCM with *T/X-XIOB/PDAS65M* external I/O board installed onto *TORNADO-62* PC plug-in DSP system.

Two external cable sets (*T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M*, refer to Appendix C for more details) come standard with *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and provide direct connection to any external high-frequency signal sources and I/O synchronization using industry-standard connectors (fig.1-5). *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* external cable sets connect to *T/X-XIOB/PDAS65M* external I/O board for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.
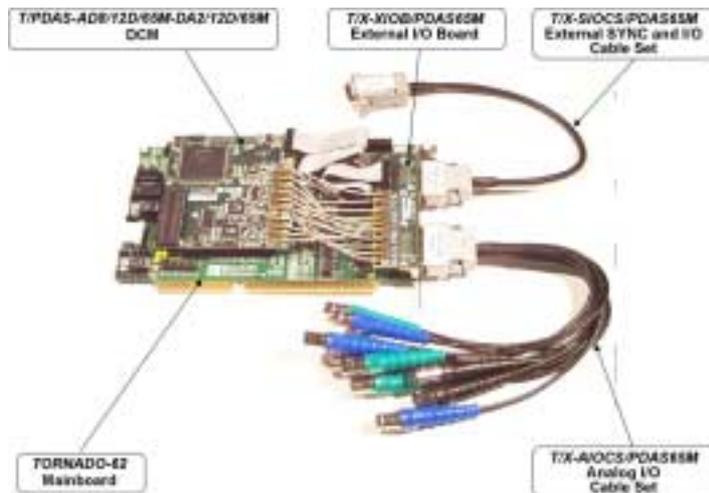
Fig. 1-5.   TORNADO-62 PC plug-in DSP system with *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, *T/X-XIOB/PDAS65M* external I/O board and external cable sets.

Applications

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM has been designed for multi-channel ultra high-frequency and accurate analog and digital I/O instrumentation applications, as well as for other industrial and general signal processing applications, which assumes similar analog and digital signal I/O requirements and meets the specifications of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

1.2   Technical Specification

The following are detail technical specifications for *T/PDAS-AD8/12D/65M-DA2/12D/65M* PIOX-16 DCM for *TORNADO* DSP systems/controllers.

CAUTION

Some of on-board components of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM may appear very hot during operation and can deliver skin sore in case of direct contact.

Although it is generally not required for normal operation of the *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, it is recommended to provide airflow over *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM board surface by means of optional fan/blower in order to exclude excessive heating of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and of the neighbor boards installed into the same chassis compartment.

Parameter description	*parameter value*
analog inputs and ADC	
number of analog inputs	4x2 (4 pairs of 2 channels each)
number of ADC channels	2 (synchronous sampling of both channels)
analog input signal range	± 1 V (typ)
input impedance for analog inputs	50 Ohm
analog input signal bandwidth of analog input amplifiers (at –3 dB)	standard : 0 .. 32.5 MHz (1st order LPF) -X1 option: 0 .. 97 MHz (1st order LPF) -XX option: 0 .. 150 MHz (no LPF)
ADC resolution	12 bits
maximum ADC sampling frequency	65 MHz
minimum ADC sampling frequency	6.5 MHz

SNR (Fs=31MHz)	67 dB (typ)
differential non-linearity	± 1.5 LSB (max)
gain error	± 10% full scale max
zero offset error	± 25 mV typ (± 58 mV max) @ Rx = 50 Ohm (rev.1A only)
ADC input signal bandwidth	300 MHz (max)

analog outputs and DAC

number of DAC channels	2 (synchronous sampling of both channels)
analog output signal range	± 1 V (typ) @ 50 Ohm ± 2 V (typ) @ ∞ Ohm
output impedance	50 Ohm
load impedance	50 Ohm
DAC resolution	12 bits
maximum sampling frequency	65 MHz
differential non-linearity	± 1 LSB max
zero offset error	± 8 mV (max)
gain error	± 10% full scale max
output voltage settling time (to 0.1%)	< 38 ns
output voltage settling time (to 10%)	< 7 ns

external I/O data streams

number of input data streams	1
number of output data streams	1
number of data bits in each I/O data stream	32 (organized as 2 channels of 16-bit each)
I/O signal level	3v/5v TTL
output load current	< 3.2 mA
external input data setup time for XDSIN external digital input stream to the XDSIN_CLK high ($T_{XDSIN-CLKH}$)	4 ns min

external output data delay for XDSIN external digital output stream after the XDSOUT_CLK high ($T_{XDSOUT-CLKH}$)	6 ns max

I/O data streams FIFO

FIFO depth	256 Kwords x16 bits
number of FIFO for each I/O data stream	2

Programmable Sampling Frequency Generator (PFG)

Programmable output frequency range	0.0625 MHz .. 65 MHz
stability of reference clock frequency	$\pm$ 50 PPM
PLL lock time to within 1% of output frequency	< 10 mS
period jitter	$\pm$ 40 pS (MSV) $\pm$ 90 pS (absolute)

External Sampling Frequency (XFS) and Synchronization I/O

maximum XFS input frequency	65 MHz
logical I/O level	3v/5v TTL
input impedance for XFS input	110 Ohm

general purpose digital I/O

number of programmable digital I/O bits	4 I/O bits with programmable direction
I/O signal level	3v/5v TTL
output load current	< 3.2 mA

Host PIOX-16 Interface

I/O ports	control registers I/O FIFO
access time	12 ns max (control register access) 30ns max (FIFO access)
PIOX-16 interrupt request inputs	software selectable from IRQ-0, IRQ-1, IRQ-2, IRQ-3

physical and power:

Dimensions	65 mm (2.55") x 85 mm (3.34")

power consumption via host PIOX I/F	+5v @ 1.1 A
	+12v @ 0.43 A
	-12v @ 0.1 A
external operating temperature	0°C .. +55°C
recommended fan/blower airflow	>0.2 m^3/min

Chapter 2. System Architecture and Construction

This chapter contains detail technical description for architecture and construction of *T/PDAS-AD8/12D/65M-DA2/12D/65M* PIOX-16 AD/DA DCM.

2.1 System Architecture

System architecture and construction for *T/PDAS-AD8/12D/65M-DA2/12D/65M* PIOX-16 AD/DA DCM are presented at fig.2-1 and fig.2-1.
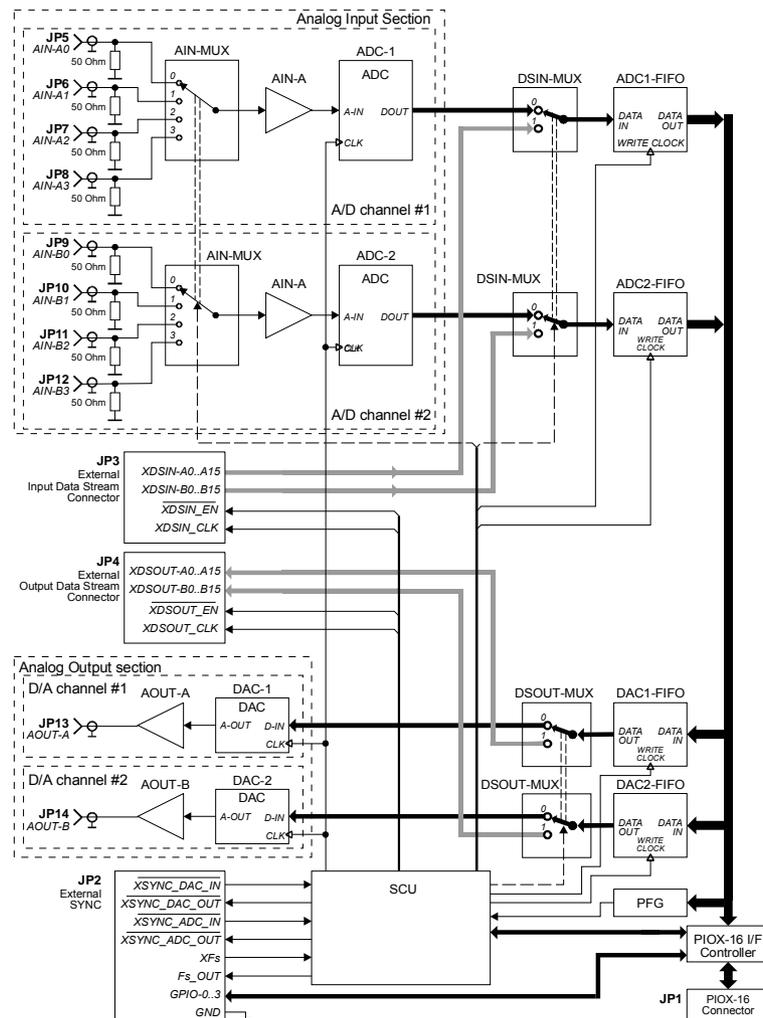
Fig.2-1. Block diagram of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.
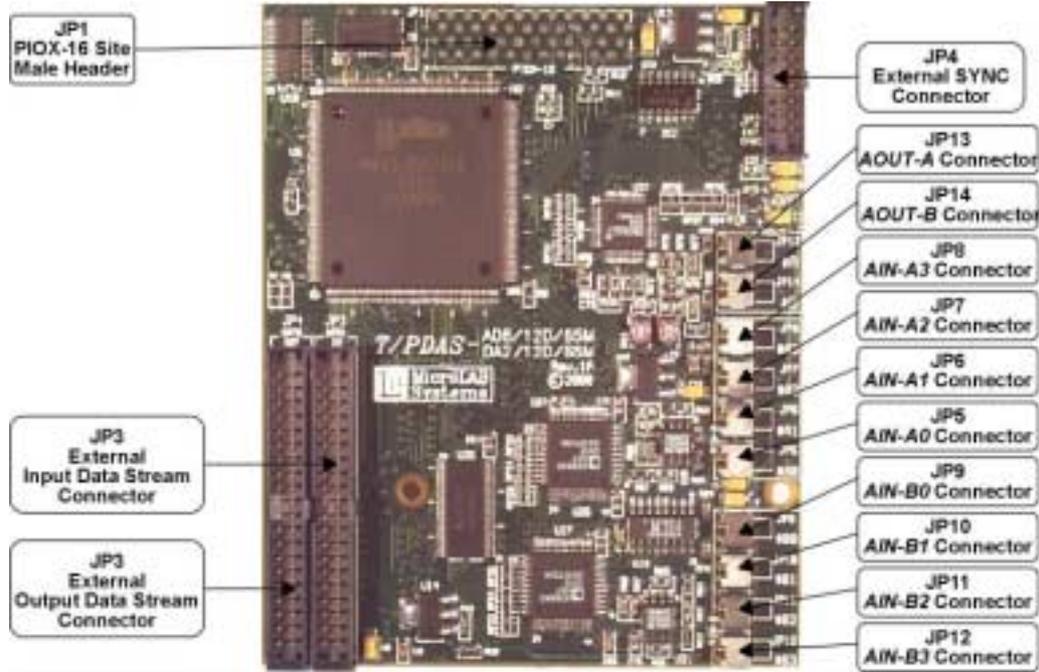
Fig.2-2.   Construction of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM comprises of the following components:

- 2-channel analog input section comprising of two synchronous 12-bit 65 Msps analog-to-digital converters (ADC1 and ADC2), two input amplifiers (AIN-A), two 4:1 analog input multiplexers (AIN-MUX) and analog input connectors (JP5..JP12) for AIN-A0..A3 and AIN-B0..AIN-B3 analog inputs
- alternative 32-bit synchronous parallel input digital stream (XDSIN) coming from JP3 on-board connector
- dual-channel input data streams multiplexer (DSIN-MUX)
- two 256Kx16 synchronous FIFO for input data streams (ADC1-FIFO and ADC2-FIFO)
- 2-channel analog output section comprising of two synchronous 12-bit 65 Msps digital-to-analog converters (DAC1 and DAC2), analog output amplifiers (AOUT-A) and analog output connectors (JP13 and JP14) for AOUT-A and AOUT-B analog outputs
- alternative 32-bit synchronous parallel output digital stream (XDSOUT) routed to JP4 on-board connector
- dual-channels output data streams multiplexer (DSOUT-MUX)
- two 256Kx16 synchronous FIFO for output data streams (DAC1-FIFO and DAC2-FIFO)
- 4-bit general purpose programmable digital I/O (GPIO-0..3)
- high-resolution programmable sampling frequency generator (PFG)
- synchronization and control unit (SCU)
- external synchronization and I/O connector (JP2)
- host PIOX-16 interface controller and host PIOX-16 interface header (JP1) for installation onto *TORNADO* DSP systems/controllers.

analog input section

Analog input section of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM (fig.2-1) comprises of two identical A/D channels (#1 and #2), and is designed for synchronous analog-to-digital conversion of any pre-selected pair of analog input signals from AIN-A0..A3 and AIN-B0..B3 analog inputs. ADC output data streams are further routed to the DSIN-MUX digital input stream multiplexer.

Each A/D channel of analog input section comprises of the following components:
- 4:1 analog input multiplexer (AIN-MUX) with four analog inputs (AIN-A0..A3 for A/D channel #1 and AIN-B0..B3 for A/D channel #2)
- analog input amplifier (AIN-A)
- 12-bit 65 Msps ADC (ADC1 and ADC2 correspondingly).

For more details about analog input section of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to section "Data Acquisition Control" later in this chapter.

input data streams multiplexer (DSIN-MUX) and input FIFO

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM allows to input external 32-bit parallel digital input data stream (XDSIN) as an alternative to dual-channel ADC output data stream from analog input section. This feature provides interfacing of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM to a variety of high-frequency digital telecommunication and instrumentation equipment, which provides parallel digital output data.

32-bit XDSIN external digital input stream comes from on-board JP3 connector and is splitted into two 16-bit data streams (XDSIN-A0..A15 and XDSIN-B0..B15) with common synchronization.

24-bit ADC output data stream (ADC1-0..11 and ADC2-0..11) and 32-bit XDSIN external digital input stream (XDSIN-A0..A15 and XDSIN-B0..B15) are multiplexed by dual-channel 16-bit input data stream multiplexer (DSIN-MUX).

Two 16-bit output data streams from DSIN-MUX multiplexer are routed to the corresponding input of two 256Kx16-bit ADC FIFO (ADC1-FIFO and ADC2-FIFO). ADC FIFO can acquire any programmable number of ADC/XDSIN output data samples and is controlled by SCU and host PIOX-16 interface.

For more details about operation of XDSIN, DSIN-MUX and ADC FIFO of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to section "Data Acquisition Control" later in this chapter.

analog output section

Analog output section of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM comprises of two identical D/A channels (#1 and #2), and is designed for digital-to-analog conversion of output data stream from DSOUT-MUX digital output stream multiplexer to analog output signals.

Each D/A channel of analog input section comprises of the following components:
- 12-bit 65 Msps DAC (DAC1 and DAC2 correspondingly)
- analog output amplifier (AOUT-A).

For more details about analog output section of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to section "Data Acquisition Control" later in this chapter.

output data streams multiplexer (DSOUT-MUX) and output FIFO

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM allows to output external 32-bit parallel digital output data stream (XDSOUT) as an alternative to dual-channel analog outputs via analog output section. This feature provides interfacing of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM to a variety of high-frequency digital telecommunication and instrumentation equipment, which requires input digital data.

32-bit XDSOUT external digital output stream is routed to on-board JP4 connector and is splitted into two 16-bit data streams (XDSOUT-A0..A15 and XDSOUT-B0..B15) with common synchronization.

24-bit DAC input data stream (DAC1-0..11 and DAC2-0..11) and 32-bit XDSOUT external digital output stream (XDSOUT-A0..A15 and XDSOUT-B0..B15) are demultiplexed by dual-channel 16-bit output data stream multiplexer (DSOUT-MUX) from the outputs of the corresponding 256Kx16-bit DAC FIFO (DAC1-FIFO and DAC2-FIFO). DAC FIFO can acquire any programmable number of DAC/XDSOUT data samples and is controlled by SCU and host PIOX-16 interface.

For more details about operation of XDSOUT, DSOUT-MUX and DAC FIFO of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to section "Data Acquisition Control" later in this chapter.

data acquisition start synchronization

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM allows to start data acquisition process for A/D and/or D/A channels either by setting the corresponding software flag in *DAQ_CNTR2_RG* register of host PIOX-16 interface (refer to section "Host PIOX-16 Interface" later in this chapter) or on external synchronization event at the dedicated *DAC_XSYNCH_IN* and *ADC_XSYNC_IN* inputs, which are available via on-board JP2 external synchronization connector. External synchronization events can be selected either level or edge sensitive.

For more details about data acquisition synchronization for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to section "Data Acquisition Control" later in this chapter.

Master/Slave operation

Multiple *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, which are installed on different *TORNADO* DSP systems/controllers, can be configured to run synchronously in order to extend number of A/D and D/A channels while maintaining absolutely synchronous data acquisition timing. This is performed by means of Master and Slave synchronization: one DCM must be configured in Master synchronization mode in order to generate output synchronization, while all other DCM shall be configured in Slave synchronization mode in order to synchronize to the Master DCM.

For more details about Master/Slave operation of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to section "Data Acquisition Control" later in this chapter.

sampling frequency

Sampling frequency is common for ADC/XDSIN and DAC/XDSOUT and can be selected by host DSP software of host *TORNADO* DSP system/controller to come from either on-board high-resolution programmable sampling frequency generator (PFG), or from external sampling frequency input (XFS) from on-board JP2 connector, or from any of two timer inputs of host PIOX-16 interface (TM/XIO-0 and TM/XIO-1).

programmable sampling frequency generator (PFG)

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM provides on-board programmable high-resolution sampling frequency generator (PFG). PFG allows accurate setting of virtually any sampling frequency value for ADC/XDSIN and DAC/XDSOUT within the 62.5 kHz .. 65 MHz frequency range. The sampling frequency, which value is out of this frequency range, must be supplied either from external sampling frequency input (XFS) or from PIOX-16 interface timer pins (TM/XIO-0 and TM/XIO-1).

For more details about PFG programming for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to section "Data Acquisition Control" later in this chapter.

synchronization and control unit (SCU)

T/PDAS-AD8/12D/65M-DA2/12D/65M on-board synchronization and control unit (SCU) provides timing and control and timing for A/D and D/A data acquisition. SCU comprises of ADC and DAC data acquisitions controllers and ADC and DAC interrupt retriggable transmission (IRT) controllers.

For more details about SCU operation of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to sections "Data Acquisition Control" and "ADC IRT and DAC IRT Controllers" later in this chapter.

programmable general purpose I/O

T/PDAS-AD8/12D/65M-DA2/12D/65M provides four programmable general purpose I/O bits (GPIO-0..3), which are available at JP2 external synchronization connector. GPIO-0..3 I/O pins are 3v/5v TTL compatible and can be used as general purpose I/O for control and interfacing to external peripherals. Moreover, active low condition at GPIO-0 and GPIO-1 I/O pins can be used to generate interrupts to host PIOX-16 interface.

Direction and input/output data for GPIO-0..3 pins are programmable via *GPIO_DIR_RG* and *GPIO_DATA_RG* registers of host PIOX-16 interface.

For more details about GPIO of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to section "Host PIOX-16 Interface" later in this chapter.

host PIOX-16 interface and controller

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM installs as PIOX-16 DCM onto host *TORNADO* DSP system/controller using host 16-bit PIOX-16 interface (JP1 connector).

Host PIOX-16 interface controller provides access to on-board FIFO, PFG and GPIO and contains a set of control registers for SCU control.

For more details about host PIOX-16 interface of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to section "Host PIOX-16 Interface" later in this chapter.

host PIOX-16 interrupts

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM allows generation of up to four host PIOX-16 interrupts via any of PIOX-16 interrupt request lines. Host PIOX-16 interrupts can be generated on multiple data acquisition events, error events and active low events at GPIO-0 and GPIO-1 I/O pins.

For more details about host PIOX-16 interrupts of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM refer to sections "Host PIOX-16 Interface" and "Data Acquisition Control" later in this chapter.

2.2   Host PIOX-16 Interface

Host 16-bit PIOX-16 interface of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM provides access from host *TORNADO* DSP system/controller to on-board FIFO, PFG, GPIO and SCU control registers. On-board JP1 connector of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM (fig.A-1) is used to install into PIOX-16 site of host *TORNADO* DSP system/controller.

host PIOX-16 interface address map

Host PIOX-16 interface address map for of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM comprises of control register area and input/output FIFO area. Table 2-1 specifies details about host PIOX-16 interface address map.

Table 2-1. Host PIOX-16 interface address map.

address area and register name	value on PIOX-16 reset condition	access mode	address (note 3)	Reference information
Control Register area: *DAQ_CNTR1_RG* registers (ADC/DAC data acquisition mode and data format)	00H	r/w	*BA*+0000H (bits D0..D7 only)	table 2-2
Control Register area: *DAQ_CNTR2_RG* register (real-time data acquisition control)	00H	r/w	*BA*+0001H (bits D0..D7 only)	table 2-3
Control Register area: *DAQ_CNTR3_RG* register (data acquisition termination/IRT flags selector)	00H	r/w	*BA*+0002H (bits D0..D7 only)	table 2-4
Control Register area: *DAQ_SYNC_RG* register (sampling frequency and data acquisition synchronization selectors)	00H	r/w	*BA*+0003H (bits D0..D7 only)	table 2-5
Control Register area: *DAQ_MUX_RG* register (ADC input MUX and DSIN-MUX/DSOUT-MUX data streams MUX control)	00H	r/w	*BA*+0004H (bits D0..D7 only)	table 2-6
Control Register area: *ADC_FIFO_STAT_RG* register (ADC FIFO status)	00H	r	*BA*+0006H (bits D0..D7 only)	table 2-7
Control Register area: *DAC_FIFO_STAT_RG* register (DAC FIFO status)	00H	r	*BA*+0007H (bits D0..D7 only)	table 2-7
Control Register area: *ERR_STAT_RG* register (read-only) (data acquisition error status) *ERR_CLR_RG* register (write-only) (data acquisition error clear)	00H -	r w	*BA*+0008H (bits D0..D7 only)	table 2-8
Control Register area: *PFG_CNTR1_RG* register (PFG control: V0..V7)	16H	r/w	*BA*+000AH (bits D0..D7 only)	table 2-12
Control Register area: *PFG_CNTR2_RG* register (PFG control: V8, R0..R6)	92H	r/w	*BA*+000BH (bits D0..D7 only)	table 2-12

Control Register area: *PFG_CNTR3_RG* register (PFG control: S0..S2, X)	00H	r/w	*BA*+000CH (bits D0..D7 only)	table 2-12
Control Register area: *GPIO_DATA_RG* register (GPIO I/O data)	-	r/w	*BA*+000EH (bits D0..D7 only)	table 2-13a
Control Register area: *GPIO_DIR_RG* register (GPIO direction control)	00H	r/w	*BA*+000FH (bits D0..D7 only)	table 2-13b
Control Register area: *HIRQ0_SEL_RG* register (host PIOX-16 IRQ-0 interrupt control)	00H	r/w	*BA*+0010H (bits D0..D7 only)	table 2-14
Control Register area: *HIRQ1_SEL_RG* register (host PIOX-16 IRQ-1 interrupt control)	00H	r/w	*BA*+0011H (bits D0..D7 only)	table 2-14
Control Register area: *HIRQ2_SEL_RG* register (host PIOX-16 IRQ-2 interrupt control)	00H	r/w	*BA*+0012H (bits D0..D7 only)	table 2-15
Control Register area: *HIRQ3_SEL_RG* register (host PIOX-16 IRQ-3 interrupt control)	00H	r/w	*BA*+0013H (bits D0..D7 only)	table 2-15
Control Register area: *XIM_ERR_RG* register (expansion error interrupt mask)	00H	r/w	*BA*+0016H (bits D0..D7 only)	table 2-16
FIFO area: *ADC1_FIFO_DATA_RG* register (ADC1 FIFO output data)	-	r	*BA*+8000H	table 2-9
FIFO area: *ADC2_FIFO_DATA_RG* register (ADC2 FIFO output data)	-	r	*BA*+8001H	table 2-9
FIFO area: *DAC1_FIFO_DATA_RG* register (DAC1 FIFO input data)	-	w	*BA*+8004H	table 2-10
FIFO area: *DAC2_FIFO_DATA_RG* register (DAC2 FIFO input data)	-	w	*BA*+8005H	table 2-10
FIFO area: *ADC_FIFO_SIN_RG* register (Configuration data for ADC FIFO)	-	w	*BA*+8002H (bit D0 only)	table 2-11
FIFO area: *DAC_FIFO_SIN_RG* register (Configuration data for DAC FIFO)	-	w	*BA*+8006H (bit D0 only)	table 2-11

Control Register area: *ADC_DAQ_RESET_RG* register (Reset for ADC data acquisition controller)	-	w	*BA*+8008H (written data ignored)	-
Control Register area: *DAC_DAQ_RESET_RG* register (Reset for DAC data acquisition controller)	-	w	*BA*+8009H (written data ignored)	-
Control Register area: *DAQ_RESET_RG* register (Reset for ADC and DAC data acquisition controllers)	-	w	*BA*+800AH (written data ignored)	-

Notes:
1. Access modes: *r* - read only, *w* - write only, *r/w* - read/write.
2. '*BA*' denotes base address for host PIOX-16 interface within the DSP address map of host *TORNADO* DSP system/controller.
3. Address values are specified at the data word boundaries for the DSP of host *TORNADO* DSP system/controller, which are true for TMS320C3x and TMS320C5xxx DSP. For TMS320C6xxx DSP these addresses shall be multiplied by x4 in order to meet the byte addressing for TMS320C6xxx DSP.

CAUTION

DSP software of host *TORNADO* DSP system/controller must perform access to *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM as referenced to the corresponding PIOX-16 interface base address, which is specific for particular *TORNADO* DSP system/controller (refer to documentation for your *TORNADO* DSP system/control for more details about addressing PIOX-16 interface area).

CAUTION

When accessing Control Register area of host PIOX-16 interface of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM from host *TORNADO* DSP system/controller, only data bits D0..D7 are valid.

When accessing FIFO data registers of host PIOX-16 interface of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM from host *TORNADO* DSP system/controller, all bits D0..D15 are valid.

CAUTION

Reset signal for on-board PIOX-16 interface of host *TORNADO* DSP system/controller must be set to inactive state prior communication with *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

data acquisition control registers

On-board SCU synchronization and control unit and ADC/DAC data acquisition are configured and controlled via a set of control registers:

- *DAQ_CNTR1_RG* register, which is used to select ADC/DAC data acquisition modes and data formats
- *DAQ_CNTR2_RG* register, which is used to perform real-time control for ADC/DAC data acquisition
- *DAQ_CNTR3_RG* register, which is used to select ADC/DAC data acquisition termination flags and interrupt retriggable transmission (IRT) flags
- *DAQ_SYNC_RG* register, which is used to select sampling frequency source, ADC/DAC data acquisition synchronization mode, external synchronization mode and Master/Slave mode
- *DAQ_MUX_RG* register, which is used to select analog input channel for analog input section, and to configure input and output data stream multiplexers.

For details about ADC and DAC data acquisition control and timing refer to section "Data Acquisition Control" later in this chapter, whereas this subsection will describe details for data acquisition control registers.

DAQ_CNTR1_RG register must be used to set ADC/DAC data acquisition mode and data format. *DAQ_CNTR1_RG* register is available for read/write and is allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

DAQ_CNTR1_RG register (r/w)

x	DAC_FMT-1 (r/w, 0+)	DAC_FMT-0 (r/w, 0+)	ADC_FMT-1 (r/w, 0+)	ADC_FMT-0 (r/w, 0+)	DAC_MODE-1 (r/w, 0+)	DAC_MODE-0 (r/w, 0+)	ADC_MODE-1 (r/w, 0+)	ADC_MODE-0 (r/w, 0+)
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-2 provides details about *DAQ_CNTR1_RG* register bits.

Table 2-2. Register bits of *DAQ_CNTR1_RG* register.

register bits	access mode	default value on PIOX-16 reset	Description
{*ADC_MODE-1, ADC_MODE-0*}	r/w	{0,0}	Defines operation mode for ADC data acquisition controller. Refer to section "Data Acquisition Control" later in this chapter for more details about operation of ADC data acquisition controller. {*ADC_MODE-1, ADC_MODE-0*} ={0,0} corresponds to *ADC FIFO configuration mode*, which must be used to program ADC FIFO PAE/PAF flags offset values by means of writing to *ADC_FIFO_SIN_RG* register. {*ADC_MODE-1, ADC_MODE-0*} ={0,1} configuration is reserved and should not be used in customer applications. {*ADC_MODE-1, ADC_MODE-0*} ={1,0} corresponds to *ADC pass-through data acquisition mode (PTM)*, which must be used for continuous acquisition of ADC input data and continuous transmission of acquired data to host DSP via ADC FIFO. ADC PTM data acquisition process can be initialized by setting bit *ADC_DAQ_RUN* of *DAQ_CNTR2_RG* register to the '1' state and can be aborted by host DSP software by either setting bit *ADC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to the '1' state or by resetting ADC FIFO (write to either *ADC_FIFO_RESET_RG* or to *FIFO_RESET_RG* registers). Host DSP software must provide continuous download of ADC data samples from ADC FIFO using either DSP on-chip DMA controllers synchronized by ADC IRT controller, or any other download technique. In case of ADC FIFO overflow or underflow condition, the corresponding error bit (*ADC_FIFO_OVF* bit or *ADC_FIFO_UNF* bit) in *ERR_STAT_RG* register will be set, however ADC PTM data acquisition process will be not terminated. {*ADC_MODE-1, ADC_MODE-0*} ={1,1} corresponds to *ADC one-pass data acquisition mode (OPM)*, which must be used to acquire and store any predefined number of ADC input data samples. ADC OPM data acquisition process can be initialized by setting bit *ADC_DAQ_RUN* of *DAQ_CNTR2_RG* register to the '1' state and can be either terminated normally on the ADC termination flag event in accordance with bit *ADC_DAQ_TF_SEL* bit of *DAQ_CNTR3_RG* register, or can be aborted by host DSP software by either setting bit *ADC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to the '1' state or by resetting ADC FIFO (write to either *ADC_FIFO_RESET_RG* or to *FIFO_RESET_RG* registers).

{*DAC_MODE-1, DAC_MODE-0*}	r/w	{0,0}	Defines operation mode for DAC data acquisition controller. Refer to section "Data Acquisition Control" later in this chapter for more details about operation of DAC data acquisition controller. {*DAC_MODE-1, DAC_MODE-0*} ={0,0} corresponds to *DAC FIFO configuration mode*, which must be used to program DAC FIFO PAE/PAF flags offset values by means of writing to *DAC_FIFO_SIN_RG* register. {*DAC_MODE-1, DAC_MODE-0*} ={0,1} configuration is reserved and should not be used in customer applications. {*DAC_MODE-1, DAC_MODE-0*} ={1,0} corresponds to *DAC pass-through data acquisition mode (PTM)*, which must be used for continuous acquisition of DAC input data and continuous transmission of acquired data to host DSP via DAC FIFO. DAC PTM data acquisition process can be initialized by setting bit *DAC_DAQ_RUN* of *DAQ_CNTR2_RG* register to the '1' state and can be aborted by host DSP software by either setting bit *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to the '1' state or by resetting DAC FIFO (write to either *DAC_FIFO_RESET_RG* or to *FIFO_RESET_RG* registers). Host DSP software must provide continuous download of DAC data samples from DAC FIFO using either DSP on-chip DMA controllers synchronized by DAC IRT controller, or any other download technique. In case of DAC FIFO overflow or underflow condition, the corresponding error bit (*DAC_FIFO_OVF* bit or *DAC_FIFO_UNF* bit) in *ERR_STAT_RG* register will be set, however DAC PTM data acquisition process will be not terminated. {*DAC_MODE-1, DAC_MODE-0*} ={1,1} corresponds to *DAC one-pass data acquisition mode (OPM)*, which must be used to acquire and store any predefined number of DAC input data samples. DAC OPM data acquisition process can be initialized by setting bit *DAC_DAQ_RUN* of *DAQ_CNTR2_RG* register to the '1' state and can be either terminated normally on the DAC termination flag event in accordance with bit *DAC_DAQ_TF_SEL* bit of *DAQ_CNTR3_RG* register, or can be aborted by host DSP software by either setting bit *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to the '1' state or by resetting DAC FIFO (write to either *DAC_FIFO_RESET_RG* or to *FIFO_RESET_RG* registers).

{*ADC_FMT-1, ADC_FMT-0*}	r/w	{0,0}	Defines data format for ADC data acquisition controller and ADC IRT controller. Refer to section "Data Acquisition Control" later in this chapter for more details about operation of ADC data acquisition and ADC IRT controllers. {*ADC_FMT-1, ADC_FMT-0*} ={0,0} corresponds to 16-bit ADC data acquisition using ADC1 only. ADC data acquisition termination flag and ADC IRT termination flag, which are selected by bits *ADC_DAQ_TF_SEL* and *ADC_IRT_TF_SEL* of *DAQ_CNTR3_RG* register, are using output flags of ADC1-FIFO. Also, *ADC_FIFO_OVF* an *ADC_FIFO_UNF* error bits of *ERR_STAT_RG* register are set by will be set by output flags of ADC1-FIFO. Finally ADC IRT controller assumes that only one 16-bit ADC1-FIFO data word shall be downloaded by host DSP software in each download cycle. {*ADC_FMT-1, ADC_FMT-0*} ={0,1} corresponds to 16-bit ADC data acquisition using ADC2 only. ADC data acquisition termination flag and ADC IRT termination flag, which are selected by bits *ADC_DAQ_TF_SEL* and *ADC_IRT_TF_SEL* of *DAQ_CNTR3_RG* register, are using output flags of ADC2-FIFO. Also, *ADC_FIFO_OVF* an *ADC_FIFO_UNF* error bits of *ERR_STAT_RG* register are set by will be set by output flags of ADC2-FIFO. Finally ADC IRT controller assumes that only one 16-bit ADC2-FIFO data word shall be downloaded by host DSP software in each download cycle. {*ADC_FMT-1, ADC_FMT-0*} ={1,0} corresponds to 32-bit ADC data acquisition using ADC1 and ADC2. ADC data acquisition termination flag and ADC IRT termination flag, which are selected by bits *ADC_DAQ_TF_SEL* and *ADC_IRT_TF_SEL* of *DAQ_CNTR3_RG* register, are using output flags of ADC1-FIFO. *ADC_FIFO_OVF* an *ADC_FIFO_UNF* error bits of *ERR_STAT_RG* register are set by will be set in case or error condition for output flags of either ADC1-FIFO or ADC2-FIFO. ADC IRT controller assumes that both 16-bit ADC1-FIFO data word and 16-bit ADC2-FIFO data word shall be downloaded by host DSP software in each download cycle. {*ADC_FMT-1, ADC_FMT-0*} ={1,1} configuration is reserved and should not be used in customer applications.

{DAC_FMT-1, DAC_FMT-0}	r/w	{0,0}	Defines data format for DAC data acquisition controller and DAC IRT controller. Refer to section "Data Acquisition Control" later in this chapter for more details about operation of DAC data acquisition and DAC IRT controllers. *{DAC_FMT-1, DAC_FMT-0}* ={0,0} corresponds to 16-bit DAC data acquisition using DAC1 only. DAC data acquisition termination flag and DAC IRT termination flag, which are selected by bits *DAC_DAQ_TF_SEL* and *DAC_IRT_TF_SEL* of *DAQ_CNTR3_RG* register, are using output flags of DAC1-FIFO. Also, *DAC_FIFO_OVF* an *DAC_FIFO_UNF* error bits of *ERR_STAT_RG* register are set by will be set by output flags of DAC1-FIFO. Finally DAC IRT controller assumes that only one 16-bit DAC1-FIFO data word shall be downloaded by host DSP software in each download cycle. {DAC_FMT-1, DAC_FMT-0} ={0,1} corresponds to 16-bit DAC data acquisition using DAC2 only. DAC data acquisition termination flag and DAC IRT termination flag, which are selected by bits *DAC_DAQ_TF_SEL* and *DAC_IRT_TF_SEL* of *DAQ_CNTR3_RG* register, are using output flags of DAC2-FIFO. Also, *DAC_FIFO_OVF* an *DAC_FIFO_UNF* error bits of *ERR_STAT_RG* register are set by will be set by output flags of DAC2-FIFO. Finally DAC IRT controller assumes that only one 16-bit DAC2-FIFO data word shall be downloaded by host DSP software in each download cycle. {DAC_FMT-1, DAC_FMT-0} ={1,0} corresponds to 32-bit DAC data acquisition using DAC1 and DAC2. DAC data acquisition termination flag and DAC IRT termination flag, which are selected by bits *DAC_DAQ_TF_SEL* and *DAC_IRT_TF_SEL* of *DAQ_CNTR3_RG* register, are using output flags of DAC1-FIFO. *DAC_FIFO_OVF* an *DAC_FIFO_UNF* error bits of *ERR_STAT_RG* register are set by will be set in case or error condition for output flags of either DAC1-FIFO or DAC2-FIFO. DAC IRT controller assumes that both 16-bit DAC1-FIFO data word and 16-bit DAC2-FIFO data word shall be downloaded by host DSP software in each download cycle. {DAC_FMT-1, DAC_FMT-0} ={1,1} configuration is reserved and should not be used in customer applications.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

DAQ_CNTR2_RG register must be used for real-time control and status information of ADC/DAC data acquisition controllers. *DAQ_CNTR2_RG* register is available for read/write and is allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

DAQ_CNTR2_RG register (r/w)

x	DAC_ DAQ_END (r,0+) DAC_ DAQ_ABORT (w)	ADC_ DAQ_END (r,0+) ADC_ DAQ_ABORT (w)	DAC_ SYNC_OK (r,0+)	ADC_ SYNC_OK (r,0+)	0	0	DAC_ DAQ_RUN (r/w, 0+)	ADC_ DAQ_RUN (r/w, 0+)
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-3 provides details about *DAQ_CNTR2_RG* register bits.

Table 2-3. Register bits of *DAQ_CNTR2_RG* register.

register bits	access mode	default value on PIOX-16 reset	Description
ADC_DAQ_RUN	r/w	0	Initializes ADC data acquisition process in case either ADC OPM or PTM data acquisition modes are selected. Refer to section "Data Acquisition Control" later in this chapter for more details about ADC data acquisition controller. Reading *ADC_DAQ_RUN* =0 corresponds to no currently active ADC data acquisition process. Reading *ADC_DAQ_RUN* =1 corresponds to currently active ADC data acquisition process. Writing '0' to *ADC_DAQ_RUN* bit does not effect current state of ADC data acquisition process. Writing '1' to *ADC_DAQ_RUN* bit while *ADC_DAQ_RUN*=1 will initialize ADC data acquisition process. Writing '1' to *ADC_DAQ_RUN* bit while *ADC_DAQ_RUN*=1 has no effect. ADC data acquisition process can be either terminated normally on the ADC termination flag event in accordance with bit *ADC_DAQ_TF_SEL* bit of *DAQ_CNTR3_RG* register for ADC OPM mode (in case bits {*ADC_MODE-1, ADC_MODE-0*} of *DAQ_CNTR1_RG* register are set to the {1,1} state), or can be aborted by host DSP software by either setting bit *ADC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to the '1' state, or by resetting ADC FIFO (write to either *ADC_FIFO_RESET_RG* or to *FIFO_RESET_RG* registers), or by setting ADC FIFO configuration mode (in case bits {*ADC_MODE-1, ADC_MODE-0*} of *DAQ_CNTR1_RG* register are set to the {0,0} state).

DAC_DAQ_RUN	r/w	0	Initializes DAC data acquisition process in case either DAC OPM or PTM data acquisition modes are selected. Refer to section "Data Acquisition Control" later in this chapter for more details about ADC data acquisition controller. Reading *DAC_DAQ_RUN* =0 corresponds to no currently active DAC data acquisition process. Reading *DAC_DAQ_RUN* =1 corresponds to currently active DAC data acquisition process. Writing '0' to *DAC_DAQ_RUN* bit does not effect current state of DAC data acquisition process. Writing '1' to *DAC_DAQ_RUN* bit while *DAC_DAQ_RUN*=0 will initialize DAC data acquisition process. Writing '1' to *DAC_DAQ_RUN* bit while *DAC_DAQ_RUN*=1 has no effect. DAC data acquisition process can be either terminated normally on the DAC termination flag event in accordance with bit *DAC_DAQ_TF_SEL* bit of *DAQ_CNTR3_RG* register for DAC OPM mode (in case bits {*DAC_MODE-1, DAC_MODE-0*} of *DAQ_CNTR1_RG* register are set to the {0,0} state), or can be aborted by host DSP software by either setting bit *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to the '1' state, or by resetting DAC FIFO (write to either *DAC_FIFO_RESET_RG* or to *FIFO_RESET_RG* registers), or by setting DAC FIFO configuration mode (in case bits {*DAC_MODE-1, DAC_MODE-0*} of *DAQ_CNTR1_RG* register are set to the {0,0} state).
ADC_DAQ_ SYNC_OK	R	0	Returns status information for ADC data acquisition synchronization detector during ADC data acquisition process in case either ADC OPM or PTM data acquisition modes are selected. *ADC_DAQ_SYNC_OK* bit is set to the '0' state during no currently active ADC data acquisition process (in case *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register is in the '0' state). Refer to section "Data Acquisition Control" later in this chapter for more details about ADC data acquisition controller. *ADC_DAQ_SYNC_OK*=0 corresponds to either no currently active ADC data acquisition process (in case *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register is in the '0' state), or to not yet detected synchronization event during currently active acquisition process (in case *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register is in the '1' state). *ADC_DAQ_SYNC_OK* =1 corresponds to already detected synchronization event during currently active acquisition process (in case *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register is in the '1' state).

| DAC_DAQ_
SYNC_OK | R | 0 | Returns status information for DAC data acquisition synchronization detector during ADC data acquisition process in case either DAC OPM or PTM data acquisition modes are selected. *DAC_DAQ_SYNC_OK* bit is set to the '0' state during no currently active DAC data acquisition process (in case *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register is in the '0' state). Refer to section "Data Acquisition Control" later in this chapter for more details about DAC data acquisition controller.

DAC_DAQ_SYNC_OK =0 corresponds to either no currently active DAC data acquisition process (in case *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register is in the '0' state), or to not yet detected synchronization event during currently active acquisition process (in case *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register is in the '1' state).

DAC_DAQ_SYNC_OK =1 corresponds to already detected synchronization event during currently active acquisition process (in case *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register is in the '1' state). |
| ADC_DAQ_ABORT
ADC_DAQ_END | W
r | -
0 | During writes this bit is used to abort currently active ADC data acquisition process for both ADC OPM and PTM modes, and during reads this bit returns normal termination status of ADC data acquisition process for ADC OPM mode. Refer to section "Data Acquisition Control" later in this chapter for more details about operation of ADC data acquisition controller.

Writing *ADC_DAQ_ABORT* =0 will have no effect on ADC data acquisition process.

Writing *ADC_DAQ_ABORT* =1 will abort currently active ADC data acquisition process during both ADC OPM and PTM modes (in case bits {*ADC_MODE-1, ADC_MODE-0*} of *DAQ_CNTR1_RG* register are set to either {1,0} or {1,1} state), and will clear bits *ADC_DAQ_RUN* and *ADC_DAQ_END* of *DAQ_CNTR2_RG* register, and bit *ADC_IRT_ERR* of *ERR_STAT_RG* register.

Reading *ADC_DAQ_END* =0 corresponds to either ADC data acquisition process is in progress for ADC OPM mode (in case bits {*ADC_MODE-1, ADC_MODE-0*} of *DAQ_CNTR1_RG* register are set to the {1,1} state and bit *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register is in the '1' state), or to no currently active ADC data acquisition process.

Reading *ADC_DAQ_END* =1 corresponds to normally terminated ADC data acquisition process on ADC data acquisition termination event for ADC OPM mode (in case bits {*ADC_MODE-1, ADC_MODE-0*} of *DAQ_CNTR1_RG* register are set to the {1,1} state). Termination flag for ADC data acquisition process during ADC OPM mode must be selected via bit *ADC_DAQ_TF_SEL* of *DAQ_CNTR3_RG* register. *ADC_DAQ_END* bit resets to the '0' state by either writing '1' to the *ADC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register, or by resetting ADC FIFO (by writing to either *ADC_FIFO_RESET_RG* or to *FIFO_RESET_RG* registers), or by setting ADC FIFO configuration mode (in case bits {*ADC_MODE-1, ADC_MODE-0*} of *DAQ_CNTR1_RG* register are set to the {0,0} state). |

DAC_DAQ_ABORT DAC_DAQ_END	W r	- 0	During writes this bit is used to abort currently active DAC data acquisition process for both DAC OPM and PTM modes, and during reads this bit returns normal termination status of DAC data acquisition process for DAC OPM mode. Refer to section "Data Acquisition Control" later in this chapter for more details about operation of DAC data acquisition controller.
			Writing *DAC_DAQ_ABORT* =0 will have no effect on DAC data acquisition process.
			Writing *DAC_DAQ_ABORT* =1 will abort currently active DAC data acquisition process during both DAC OPM and PTM modes (in case bits {*DAC_MODE-1, DAC_MODE-0*} of *DAQ_CNTR1_RG* register are set to either {1,0} or {1,1} state), and will clear bits *DAC_DAQ_RUN* and *DAC_DAQ_END* of *DAQ_CNTR2_RG* register, and bit *DAC_IRT_ERR* of *ERR_STAT_RG* register.
			Reading *DAC_DAQ_END* =0 corresponds to either DAC data acquisition process is in progress for DAC OPM mode (in case bits {*DAC_MODE-1, DAC_MODE-0*} of *DAQ_CNTR1_RG* register are set to the {1,1} state and bit *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register is in the '1' state), or to no currently active DAC data acquisition process.
			Reading *DAC_DAQ_END* =1 corresponds to normally terminated DAC data acquisition process on DAC data acquisition termination event for DAC OPM mode (in case bits {*DAC_MODE-1, DAC_MODE-0*} of *DAQ_CNTR1_RG* register are set to the {1,1} state). Termination flag for DAC data acquisition process during DAC OPM mode must be selected via bit *DAC_DAQ_TF_SEL* of *DAQ_CNTR3_RG* register. *DAC_DAQ_END* bit resets to the '0' state by either writing '1' to the *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register, or by resetting DAC FIFO (by writing to either *DAC_FIFO_RESET_RG* or to *FIFO_RESET_RG* registers), or by setting DAC FIFO configuration mode (in case bits {*DAC_MODE-1, DAC_MODE-0*} of *DAQ_CNTR1_RG* register are set to the {0,0} state).

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
             2. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

DAQ_CNTR3_RG register must be used to select the termination flags for ADC/DAC data acquisition controllers for OPM modes, and to select the start-up and termination flags for ADC/DAC IRT controllers. *DAQ_CNTR3_RG* register is available for read/write and is allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

DAQ_CNTR3_RG register (r/w)

X	0	0	0	0	DAC_ IRT_TF_SEL (r/w, 0+)	ADC_ IRT_TF_SEL (r/w, 0+)	DAC_ DAQ_TF_SEL (r/w, 0+)	ADC_ DAQ_TF_SEL (r/w, 0+)
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-4 provides details about *DAQ_CNTR3_RG* register bits.

Table 2-4. Register bits of *DAQ_CNTR3_RG* register.

register bits	access mode	default value on PIOX-16 reset	Description
ADC_DAQ_TF_SEL	r/w	0	Selects termination flag for ADC data acquisition process for ADC OPM mode. This bit also selects transmission start flag for ADC IRT controller during ADC OPM and ADC PTM data acquisition modes. Refer to sections "Data Acquisition Control" and "ADC IRT and DAC IRT Controllers" later in this chapter for more details about ADC data acquisition controller and ADC IRT controller. *ADC_DAQ_TF_SEL*=0 corresponds to ADC FIFO FF flag is selected to terminate ADC data acquisition process in ADC OPM mode and to start the transmission cycle of ADC IRT controller. Particular ADC FIFO (ADC1-FIFO or ADC2-FIFO), which FF flag is used, is defined by the {*ADC_FMT-1, ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register. *ADC_DAQ_TF_SEL*=1 corresponds to ADC FIFO PAF flag is selected to terminate ADC data acquisition process in ADC OPM mode and to start transmission cycle of ADC IRT controller. Particular ADC FIFO (ADC1-FIFO or ADC2-FIFO), which PAF flag is used, is defined by the {*ADC_FMT-1, ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register.
DAC_DAQ_TF_SEL	r/w	0	Selects termination flag for DAC data acquisition process for DAC OPM mode. This bit also selects transmission start flag for DAC IRT controller during DAC OPM and DAC PTM data acquisition modes. Refer to sections "Data Acquisition Control" and "ADC IRT and DAC IRT Controllers" later in this chapter for more details about DAC data acquisition controller and DAC IRT controller. *DAC_DAQ_TF_SEL*=0 corresponds to DAC FIFO EF flag is selected to terminate DAC data acquisition process in DAC OPM mode and to start transmission cycle of DAC IRT controller. Particular DAC FIFO (DAC1-FIFO or DAC2-FIFO), which EF flag is used, is defined by the {*DAC_FMT-1, DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register. *DAC_DAQ_TF_SEL*=1 corresponds to DAC FIFO PAE flag is selected to terminate DAC data acquisition process in DAC OPM mode and to start transmission cycle of DAC IRT controller. Particular DAC FIFO (DAC1-FIFO or DAC2-FIFO), which PAE flag is used, is defined by the {*DAC_FMT-1, DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register.

| ADC_IRT_TF_SEL | r/w | 0 | Selects transmission termination flag for ADC IRT controller, i.e. the flag, which is used to terminate currently active ADC IRT transmission cycle. Refer to section "ADC IRT and DAC IRT Controllers" later in this chapter for more details about and ADC IRT controller.

ADC_IRT_TF_SEL=0 corresponds to ADC FIFO EF flag is selected to terminate currently active ADC IRT transmission cycle. Particular ADC FIFO (ADC1-FIFO or ADC2-FIFO), which EF flag is used, is defined by the {*ADC_FMT-1, ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register.

ADC_IRT_TF_SEL=1 corresponds to ADC FIFO PAE flag is selected to terminate currently active ADC IRT transmission cycle. Particular ADC FIFO (ADC1-FIFO or ADC2-FIFO), which PAE flag is used, is defined by the {*ADC_FMT-1, ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register. |
| DAC_IRT_TF_SEL | r/w | 0 | Selects termination flag for DAC IRT controller, i.e. the flag, which is used to terminate currently active DAC IRT transmission cycle. Refer to section "ADC IRT and DAC IRT Controllers" later in this chapter for more details about and DAC IRT controller.

DAC_IRT_TF_SEL=0 corresponds to DAC FIFO FF flag is selected to terminate currently active DAC IRT transmission cycle. Particular DAC FIFO (DAC1-FIFO or DAC2-FIFO), which FF flag is used, is defined by the {*DAC_FMT-1, DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register.

DAC_IRT_TF_SEL=1 corresponds to DAC FIFO PAF flag is selected to terminate currently active DAC IRT transmission cycle. Particular DAC FIFO (DAC1-FIFO or DAC2-FIFO), which PAF flag is used, is defined by the {*DAC_FMT-1, DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register. |

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
            2. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

DAQ_SYNC_RG register must be used to select sampling frequency source, synchronization source, external synchronization mode and Master/Slave mode for ADC/DAC data acquisition controllers. *DAQ_SYNC_RG* register is available for read/write and is allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

DAQ_SYNC_RG register (r/w)

X	SYNC_MODE (r/w, 0+)	XSYNC_MODE (r/w, 0+)	DAC_DAQ_ SYNC_SEL (r/w, 0+)	ADC_DAQ_ SYNC_SEL (r/w, 0+)	0	0	FS_SEL-1 (r/w, 0+)	FS_SEL-0 (r/w, 0+)
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-5 provides details about *DAQ_SYNC_RG* register bits.

Table 2-5. Register bits of *DAQ_SYNC_RG* register.

register bits	access mode	default value on PIOX-16 reset	Description
{*FS_SEL-1, FS_SEL-0*}	r/w	{0,0}	Selects sampling frequency source for ADC and DAC data acquisition controllers. Refer to section "Data Acquisition Control" later in this chapter for more details about ADC data acquisition controller. {*FS_SEL-1, FS_SEL-0*}={0,0} corresponds to on-board programmable sampling frequency generator (PFG) used as the sampling frequency source. {*FS_SEL-1, FS_SEL-0*}={0,1} corresponds to external sampling frequency (XFS) input from on-board JP2 connector used as the sampling frequency source (refer to Appendix A). {*FS_SEL-1, FS_SEL-0*}={1,0} corresponds to PIOX-16 interface timer #0 pin (TM/XIO-0) used as the sampling frequency source. {*FS_SEL-1, FS_SEL-0*}={1,1} corresponds to PIOX-16 interface timer #1 pin (TM/XIO-0) used as the sampling frequency source.
ADC_DAQ_ SYNC_SEL	r/w	0	Selects synchronization source for ADC data acquisition controller. Refer to section "Data Acquisition Control" later in this chapter for more details about ADC data acquisition controller. *ADC_DAQ_SYNC_SEL*=0 corresponds to software synchronization for ADC data acquisition controller. ADC data acquisition process will start immediately after host DSP software will set bit *ADC_DAQ_RUN* of *DAQ_CNTR2_RG* register to the '1' state during ADC OPM or PTM mode. *ADC_DAQ_SYNC_SEL*=1 corresponds to external synchronization for ADC data acquisition controller using ADC_XSYNC_IN input pin of on-board JP2 connector (refer to Appendix A). ADC data acquisition process will start on external synchronization event at ADC_XSYNC_IN input pin after host DSP software will set bit *ADC_DAQ_RUN* of *DAQ_CNTR2_RG* register to the '1' state during ADC OPM or PTM mode. External synchronization event at ADC_XSYNC_IN input pin can be selected either as active low level or falling edge depending upon the state of *XSYNC_MODE* bit of *DAQ_CNTR2_RG* register.

DAC_DAQ_ SYNC_SEL	r/w	0	Selects synchronization source for DAC data acquisition controller. Refer to section "Data Acquisition Control" later in this chapter for more details about DAC data acquisition controller. *DAC_DAQ_SYNC_SEL*=0 corresponds to software synchronization for DAC data acquisition controller. DAC data acquisition process will start immediately after host DSP software will set bit *DAC_DAQ_RUN* of *DAQ_CNTR2_RG* register to the '1' state during DAC OPM or PTM mode. *DAC_DAQ_SYNC_SEL*=1 corresponds to external synchronization for DAC data acquisition controller using DAC_XSYNC_IN input pin of on-board JP2 connector (refer to Appendix A). DAC data acquisition process will start on external synchronization event at DAC_XSYNC_IN input pin after host DSP software will set bit *DAC_DAQ_RUN* of *DAQ_CNTR2_RG* register to the '1' state during DAC OPM or PTM mode. External synchronization event at DAC_XSYNC_IN input pin can be selected either as active low level or falling edge depending upon the state of *XSYNC_MODE* bit of *DAQ_CNTR2_RG* register.
XSYNC_MODE	r/w	0	Selects synchronization event at ADC_XSYNC_IN and DAC_XSYNC_IN input pins of on-board JP2 connector (refer to Appendix A) for ADC and DAC data acquisition controllers correspondingly. Refer to section "Data Acquisition Control" later in this chapter for more details about ADC and DAC data acquisition controllers. *XSYNC_MODE*=0 corresponds to active low level as synchronization event at ADC_XSYNC_IN and DAC_XSYNC_IN input pins of on-board JP2 connector for ADC and DAC data acquisition controllers correspondingly in case external synchronization is selected as synchronization source for ADC and/or DAC data acquisition controllers. *XSYNC_MODE*=1 corresponds to the falling edge as synchronization event at ADC_XSYNC_IN and DAC_XSYNC_IN input pins of on-board JP2 connector for ADC and DAC data acquisition controllers correspondingly in case external synchronization is selected as synchronization source for ADC and/or DAC data acquisition controllers.
SYNC_MODE	r/w	0	Selects either Master or Slave synchronization mode for ADC and DAC data acquisition controllers. Refer to section "Data Acquisition Control" later in this chapter for more details about ADC and DAC data acquisition controllers. *SYNC_MODE*=0 corresponds to Master synchronization mode for ADC and DAC data acquisition controllers, i.e. this *T/PDAS-AD8/12D-DA2/12D/65M* DCM will generate synchronization to external Slaves during ADC and DAC data acquisition processes. *XSYNC_MODE*=1 corresponds to Slave synchronization mode for ADC and DAC data acquisition controllers, i.e. this *T/PDAS-AD8/12D-DA2/12D/65M* DCM will synchronize to external Master during ADC and DAC data acquisition processes.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
              2. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

DAQ_MUX_RG register must be used to configure analog input multiplexers AIN-MUX of analog input section, and to select input and output data streams for input (DSIN-MUX) and output (DSOUT-MUX) data

stream multiplexers. *DAQ_SYNC_RG* register is available for read/write and is allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

DAQ_MUX_RG register (r/w)

X	0	0	DSOUT_SEL (r/w, 0+)	DSIN_SEL (r/w, 0+)	0	0	ADC_IMUX-1 (r/w, 0+)	ADC_IMUX-0 (r/w, 0+)
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-6 provides details about *DAQ_MUX_RG* register bits.

Table 2-6. Register bits of *DAQ_MUX_RG* register.

register bits	access mode	default value on PIOX-16 reset	Description
{ADC_IMUX-1, ADC_IMUX-0}	r/w	{0,0}	Configures analog input multiplexer AIN-MUX of analog input section (refer to fig.2-1 and section 2.1), i.e. selects a pair of analog inputs from eight available inputs, which will be connected to the inputs of the corresponding ADC chips for conversion to digital code. {ADC_IMUX-1, ADC_IMUX-0}={0,0} corresponds to AIN-A0 and AIN-B0 analog inputs being connected to the inputs of ADC1 and ADC2 correspondingly for conversion to digital code. {ADC_IMUX-1, ADC_IMUX-0}={0,1} corresponds to AIN-A1 and AIN-B1 analog inputs being connected to the inputs of ADC1 and ADC2 correspondingly for conversion to digital code. {ADC_IMUX-1, ADC_IMUX-0}={1,0} corresponds to AIN-A2 and AIN-B2 analog inputs being connected to the inputs of ADC1 and ADC2 correspondingly for conversion to digital code. {ADC_IMUX-1, ADC_IMUX-0}={1,1} corresponds to AIN-A3 and AIN-B3 analog inputs being connected to the inputs of ADC1 and ADC2 correspondingly for conversion to digital code.
DSIN_SEL	r/w	0	Configures DSIN-MUX input data stream multiplexer (refer to fig.2-1 and section 2.1), i.e. selects an input data stream for ADC FIFO. DSIN_SEL=0 corresponds to the ADC output data stream being selected as an input data stream for ADC FIFO. DSIN_SEL=1 corresponds to the 32-bit XDSIN external input data stream from on-board JP3 connector (refer to Appendix A) being selected as an input data stream for ADC FIFO.
DSOUT_SEL	r/w	0	Configures DSOUT-MUX output data stream multiplexer (refer to fig.2-1 and section 2.1), i.e. selects destination for output data stream from DAC FIFO. DSOUT_SEL=0 corresponds to the output data stream from DAC FIFO being routed to the digital inputs of on-board DAC1 and DAC2 digital-to-analog converters from analog output section in order to generate analog output signals AOUT-A and AOUT-B. DSOUT_SEL=1 corresponds to the output data stream from DAC FIFO being routed to 32-bit XDSOUT external output data stream at on-board JP4 connector (refer to Appendix A).

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

ADC/DAC data acquisition controllers reset registers

ADC/DAC data acquisition controllers can be reset by host DSP software in order to reset the corresponding ADC and DAC FIFO read and write pointers and to reset the corresponding ADC/DAC data acquisition controllers hardware. Refer to section "Data Acquisition Control" later in this chapter for more details about ADC and DAC data acquisition controllers. Resetting ADC/DAC data acquisition controller(s) will also reset the corresponding ADC/DAC IRT controller(s).

ADC FIFO, ADC data acquisition controller and ADC IRT controller can be reset by writing to either *ADC_DAQ_RESET_RG* or *DAQ_RESET_RG* register, whereas DAC FIFO, DAC data acquisition controller and DAC IRT controller can be reset by writing to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register.

CAUTION

When writing to *ADC_DAQ_RESET_RG*, *DAC_DAQ_RESET_RG* and *DAQ_RESET_RG* registers written data is ignored.

ADC_DAQ_RESET_RG register (w)

x	x (w)	X (w)	X (w)	x (w)	x (w)	x (w)	x (w)	x (w)
bits 15..8	bit-7	Bit-6	Bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

DAC_DAQ_RESET_RG register (w)

x	x (w)	x (w)	X (w)	x (w)	x (w)	x (w)	x (w)	x (w)
bits 15..8	bit-7	Bit-6	Bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

DAQ_RESET_RG register (w)

x	x (w)	x (w)	X (w)	x (w)	x (w)	x (w)	x (w)	x (w)
bits 15..8	bit-7	Bit-6	Bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

ADC FIFO and DAC FIFO status registers

ADC_FIFO_STAT_RG and *DAC_FIFO_STAT_RG* registers must be used to get current status of EF/PAE/FF/PAF flags for each of the ADC and DAC FIFO. *ADC_FIFO_STAT_RG* and *DAC_FIFO_STAT_RG* registers are available for read-only and are allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

ADC_FIFO_STAT_RG register (r)

X	ADC2_ FIFO_PAE (r,1+)	ADC2_ FIFO_EF (r,1+)	ADC2_ FIFO_PAF (r,0+)	ADC2_ FIFO_FF (r,0+)	ADC1_ FIFO_PAE (r,1+)	ADC1_ FIFO_EF (r,1+)	ADC1_ FIFO_PAF (r,0+)	ADC1_ FIFO_FF (r,0+)
bits 15..8	Bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	Bit-1	bit-0

DAC_FIFO_STAT_RG register (r)

X	DAC2_ FIFO_PAE (r,1+)	DAC2_ FIFO_EF (r,1+)	DAC2_ FIFO_PAF (r,0+)	DAC2_ FIFO_FF (r,0+)	DAC1_ FIFO_PAE (r,1+)	DAC1_ FIFO_EF (r,1+)	DAC1_ FIFO_PAF (r,0+)	DAC1_ FIFO_FF (r,0+)
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	Bit-1	bit-0

Table 2-7 provides details about *ADC_FIFO_STAT_RG* and *DAC_FIFO_STAT_RG* registers bits.

Table 2-7. Register bits of *ADC_FIFO_STAT_RG* and *DAC_FIFO_STAT_RG* registers.

register bits	access mode	default value on PIOX-16 reset	Description
ADC1_FIFO_FF *ADC2_FIFO_FF* *DAC1_FIFO_FF* *DAC2_FIFO_FF*	r	0	Status of full flag (EF) for the corresponding FIFO. FF flag is non-programmable. FF flag or each FIFO flags can be used to generate IRQ-0 and IRQ-1 host PIOX-16 interrupt requests. *xxxx_FIFO_FF*=0 corresponds to non-full condition of the corresponding FIFO. *xxxx_FIFO_FF*=1 corresponds to the full condition of the corresponding FIFO.
ADC1_FIFO_PAF *ADC2_FIFO_PAF* *DAC1_FIFO_PAF* *DAC2_FIFO_PAF*	r	0	Status of partially full flag (PAF) for the corresponding FIFO. Offset value for PAF flag can be programmed during configuration mode for the corresponding FIFO. PAF flag of each FIFO can be used to generate IRQ-0 and IRQ-1 host PIOX-16 interrupt requests. *xxxx_FIFO_PAF*=0 corresponds to (2^{18}-M-1) or less number of unread samples inside the corresponding FIFO (M is the programmed offset for FIFO PAF flag). *xxxx_FIFO_PAF*=1 corresponds to (2^{18}-M) or more number of unread samples inside the corresponding FIFO (M is the programmed offset for FIFO PAF flag).
ADC1_FIFO_EF *ADC2_FIFO_EF* *DAC1_FIFO_EF* *DAC2_FIFO_EF*	r	1	Status of empty flag (EF) for the corresponding FIFO. EF flag is non-programmable. EF flag of each FIFO can be used to generate IRQ-0 and IRQ-1 host PIOX-16 interrupt requests. *xxxx_FIFO_EF*=0 corresponds to non-empty condition of the corresponding FIFO. *xxxx_FIFO_EF*=0 corresponds to the empty condition of the corresponding FIFO.
ADC1_FIFO_PAE *ADC2_FIFO_PAE* *DAC1_FIFO_PAE* *DAC2_FIFO_PAE*	r	1	Status of partially empty flag (PAE) for the corresponding FIFO. Offset value for PAE flag can be programmed during configuration mode for the corresponding FIFO. PAE flag of each FIFO can be used to generate IRQ-0 and IRQ-1 host PIOX-16 interrupt requests. *xxxx_FIFO_PAE*=0 corresponds to more than N unread samples inside the corresponding FIFO (N is the programmed offset for FIFO PAE flag). *xxxx_FIFO_PAE*=1 corresponds to N or less unread samples inside the corresponding FIFO (N is the programmed offset for FIFO PAE flag).

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

error status (ERR_STAT_RG) and error clear (ERR_CLR_RG) registers

ERR_STAT_RG and *ERR_CLR_RG* registers shall be used correspondingly to read current error status and to clear errors for ADC/DAC data acquisition and IRT controllers. *ERR_STAT_RG* and *ERR_CLR_RG* registers are available for read-only and write-only correspondingly and are allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

ERR_STAT_RG register (r)
ERR_CLR_RG register (w)

X	0	0	DAC_IRT_ERR (r,0+) CLR_DAC_IRT_ERR (w)	ADC_IRT_ERR (r,0+) CLR_ADC_IRT_ERR (w)	DAC_FIFO_UNF (r,0+) CLR_DAC_FIFO_UNF (w)	DAC_FIFO_OVF (r,0+) CLR_DAC_FIFO_OVF (w)	ADC_FIFO_UNF (r,0+) CLR_ADC_FIFO_UNF (w)	ADC_FIFO_OVF (r,0+) CR_ADC_FIFO_OVF (w)
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	Bit-1	bit-0

Table 2-8 provides details about *ERR_STAT_RG* and *ERR_CLR_RG* registers bits.

Table 2-8. Register bits of *ERR_STAT_RG* and *ERR_CLR_RG* registers.

register bits	access mode	default value on PIOX-16 reset	Description
ADC_FIFO_OVF *CLR_ADC_FIFO_OVF*	r w	0 -	During reads this bit returns current status of ADC FIFO overflow error for ADC data acquisition controller. During writes this bit is used to clear ADC FIFO overflow error. Refer to section "Data Acquisition Control" later in this chapter for more details about ADC data acquisition controller. Read-only *ADC_FIFO_OVF* bit can be used to generate host PIOX-16 interrupt requests. Particular ADC FIFO (ADC1-FIFO or ADC2-FIFO), which is being used for tracking the overflow condition, is defined by the {*ADC_FMT-1, ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register. Reading *ADC_FIFO_OVF*=0 corresponds to no detected ADC FIFO overflow error. Reading *ADC_FIFO_OVF*=1 corresponds to active ADC FIFO overflow error, which can be cleared by writing '1' to this bit (*CLR_ADC_FIFO_OVF*). Writing *CLR_ADC_FIFO_OVF*=0 has no effect on current state of ADC FIFO overflow error. Writing *CLR_ADC_FIFO_OVF*=1 clears currently active ADC FIFO overflow error.
ADC_FIFO_UNF *CLR_ADC_FIFO_UNF*	r w	0 -	During reads this bit returns current status of ADC FIFO underflow error for ADC data acquisition controller. During writes this bit is used to clear ADC FIFO underflow error. Refer to section "Data Acquisition Control" later in this chapter for more details about ADC data acquisition controller. Read-only *ADC_FIFO_UNF* bit can be used to generate host PIOX-16 interrupt requests. Particular ADC FIFO (ADC1-FIFO or ADC2-FIFO), which is being used for tracking the underflow condition, is defined by the {*ADC_FMT-1, ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register. Reading *ADC_FIFO_UNF*=0 corresponds to no detected ADC FIFO underflow error. Reading *ADC_FIFO_UNF*=1 corresponds to active ADC FIFO underflow error, which can be cleared by writing '1' to this bit (*CLR_ADC_FIFO_UNF*). Writing *CLR_ADC_FIFO_UNF*=0 has no effect on current state of ADC FIFO underflow error. Writing *CLR_ADC_FIFO_UNF*=1 clears currently active ADC FIFO underflow error.

DAC_FIFO_OVF *CLR_DAC_FIFO_OVF*	r w	0 -	During reads this bit returns current status of DAC FIFO overflow error for DAC data acquisition controller. During writes this bit is used to clear DAC FIFO overflow error. Refer to section "Data Acquisition Control" later in this chapter for more details about DAC data acquisition controller. Read-only *DAC_FIFO_OVF* bit can be used to generate host PIOX-16 interrupt requests. Particular DAC FIFO (DAC1-FIFO or DAC2-FIFO), which is being used for tracking the overflow condition, is defined by the {*DAC_FMT-1, DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register. Reading *DAC_FIFO_OVF*=0 corresponds to no detected DAC FIFO overflow error. Reading *DAC_FIFO_OVF*=1 corresponds to active DAC FIFO overflow error, which can be cleared by writing '1' to this bit (*CLR_DAC_FIFO_OVF*). Writing *CLR_DAC_FIFO_OVF*=0 has no effect on current state of DAC FIFO overflow error. Writing *CLR_DAC_FIFO_OVF*=1 clears currently active DAC FIFO overflow error.
DAC_FIFO_UNF *CLR_DAC_FIFO_UNF*	r w	0 -	During reads this bit returns current status of DAC FIFO underflow error for DAC data acquisition controller. During writes this bit is used to clear DAC FIFO underflow error. Refer to section "Data Acquisition Control" later in this chapter for more details about DAC data acquisition controller. Read-only *DAC_FIFO_UNF* bit can be used to generate host PIOX-16 interrupt requests. Particular DAC FIFO (DAC1-FIFO or DAC2-FIFO), which is being used for tracking the underflow condition, is defined by the {*DAC_FMT-1, DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register. Reading *DAC_FIFO_UNF*=0 corresponds to no detected DAC FIFO underflow error. Reading *DAC_FIFO_UNF*=1 corresponds to active DAC FIFO underflow error, which can be cleared by writing '1' to this bit (*CLR_DAC_FIFO_UNF*). Writing *CLR_DAC_FIFO_UNF*=0 has no effect on current state of DAC FIFO underflow error. Writing *CLR_DAC_FIFO_UNF*=1 clears currently active DAC FIFO underflow error.

ADC_IRT_ERR	r	0	During reads this bit returns current error status of ADC IRT controller. During writes this bit is used to clear ADC IRT error. Refer to section "ADC IRT and DAC IRT Controllers" later in this chapter for more details about ADC IRT controller. Read-only *ADC_IRT_ERR* bit can be used to generate host PIOX-16 interrupt requests.
CLR_ADC_IRT_ERR	w	-	
			Reading *ADC_IRT_ERR*=0 corresponds to no detected ADC IRT error.
			Reading *ADC_IRT_ERR*=1 corresponds to active ADC IRT error, which can be cleared by writing '1' to this bit (*CLR_ADC_IRT_ERR*).
			Writing *CLR_ADC_IRT_ERR*=0 has no effect on current state of ADC IRT error.
			Writing *CLR_ADC_IRT_ERR*=1 clears currently active ADC IRT error.
DAC_IRT_ERR	r	0	During reads this bit returns current error status of DAC IRT controller. During writes this bit is used to clear DAC IRT error. Refer to section "ADC IRT and DAC IRT Controllers" later in this chapter for more details about DAC IRT controller. Read-only *DAC_IRT_ERR* bit can be used to generate host PIOX-16 interrupt requests.
CLR_DAC_IRT_ERR	w	-	
			Reading *DAC_IRT_ERR*=0 corresponds to no detected DAC IRT error.
			Reading *DAC_IRT_ERR*=1 corresponds to active DAC IRT error, which can be cleared by writing '1' to this bit (*CLR_DAC_IRT_ERR*).
			Writing *CLR_DAC_IRT_ERR*=0 has no effect on current state of DAC IRT error.
			Writing *CLR_DAC_IRT_ERR*=1 clears currently active DAC IRT error.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

ADC FIFO data registers

Real-time ADC data as well as the XDSIN external input data stream data can be read by host DSP software via *ADC1_FIFO_DATA_RG* and *ADC2_FIFO_DATA_RG* read-only registers, which are available for read-only and occupy full 16-bit data word of host PIOX-16 interface.

In case DSIN-MUX input data stream multiplexer is configured to route the ADC output data streams to ADC FIFO inputs, i.e. in case *DSIN_SEL* bit of *DAQ_MUX_RG* register is set to the *DSIN_SEL*=0 state, then *ADC1_FIFO_DATA_RG* and *ADC2_FIFO_DATA_RG* read-only registers contain ADC1 and ADC2 output data correspondingly. The 12-bit ADC1 and ADC2 output data are aligned to the least significant bit of 16-bit data words of host PIOX-16 interface. Also, the *ADC1_FIFO_DATA_RG* register returns current configuration of ADCIN-MUX ADC input multiplexer.

ADC1_FIFO_DATA_RG register (r)
for reads of ADC1 data
(*DSIN_SEL* bit of *DAQ_MUX_RG* register is set to the *DSIN_SEL*=0 state)

ADC_ RIMUX-1 (r,0+)	ADC_ RIMUX-0 (r,0+)	x	x	ADC1_DATA-11.. ADC1_DATA-0 (r)
Bit 15	bit-14	bit-13	Bit-12	bits-11..0

ADC2_FIFO_DATA_RG register (r)
for reads of ADC2 data
(*DSIN_SEL* bit of *DAQ_MUX_RG* register is set to the *DSIN_SEL*=0 state)

x	x	x	x	ADC2_DATA-11.. ADC2_DATA-0 (r)
Bit 15	bit-14	bit-13	Bit-12	bits-11..0

Table 2-9a provides details about *ADC1_FIFO_DATA_RG* and *ADC2_FIFO_DATA_RG* registers bits for ADC1/ADC2 data reads.

Table 2-9a. Register bits of *ADC1_FIFO_DATA_RG* and *ADC2_FIFO_DATA_RG* registers for reads of ADC1/ADC2 data.

Register bits	access mode	Default value on PIOX-16 reset	Description
{ADC1_DATA-11.. ADC1_DATA-0} {ADC2_DATA-11.. ADC2_DATA-0}	r	-	12-bit ADC1 and ADC2 signed output data correspondingly.
{ADC_RIMUX-1, ADC_RIMUX-0}	r	{0,0}	Current read-back configuration of ADC analog input multiplexers. {ADC_RIMUX-1, ADC_RIMUX-0} data bits shall be decoded in accordance with {ADC_IMUX-1, ADC_IMUX-0} data bits of *DAQ_MUX_RG* register (refer to table 2-6).

Note: 1.   Access modes: r/w – read/write; r – read-only; w – write only.

In case DSIN-MUX input data stream multiplexer is configured to route 32-bit XDSIN external input data stream from on-board JP3 connector to ADC FIFO inputs, i.e. in case *DSIN_SEL* bit of *DAQ_MUX_RG* register is set to the *DSIN_SEL*=1 state, then *ADC1_FIFO_DATA_RG* and *ADC2_FIFO_DATA_RG* read-only registers contain 16-bit XDSIN-A0..A15 and XDSIN-B0..B15 data correspondingly and occupy full 16-bit data words of host PIOX-16 interface.

ADC1_FIFO_DATA_RG register (r)
for reads of 32-bit XDSIN external input data stream
(*DSIN_SEL* bit of *DAQ_MUX_RG* register is set to the *DSIN_SEL*=1 state)

XDSIN-A15.. XDSIN-A0 (r)

bits-15..0

ADC2_FIFO_DATA_RG register (r)
for reads of 32-bit XDSIN external input data stream
(*DSIN_SEL* bit of *DAQ_MUX_RG* register is set to the *DSIN_SEL*=1 state)

XDSIN-B15.. XDSIN-B0 (r)

bits-15..0
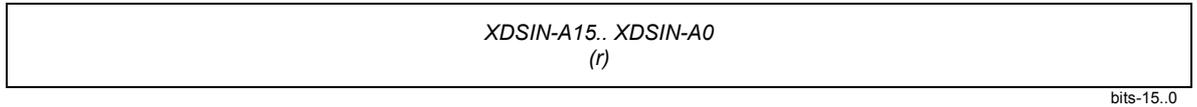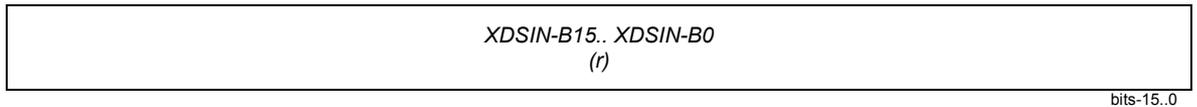
Table 2-9b provides details about *ADC1_FIFO_DATA_RG* and *ADC2_FIFO_DATA_RG* registers bits for 32-bit XDSIN input data stream reads.

Table 2-9b. Register bits of *ADC1_FIFO_DATA_RG* and *ADC2_FIFO_DATA_RG* registers for reads of 32-bit XDSIN external input data stream.

register bits	access mode	default value on PIOX-16 reset	Description
{XDSIN-A15.. XDSIN-A0} {XDSIN-B15.. XDSIN-B0}	r	-	16-bit halfwords of 32-bit XDSIN external input data stream words, which are routed from on-board JP3 connector.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

DAC FIFO data registers

Real-time data for on-board DAC and 32-bit XDSOUT external output data streams can be written by host DSP software via *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* write-only registers, which are available for write-only and occupy full 16-bit data word of host PIOX-16 interface.

In case DSOUT-MUX output data stream multiplexer is configured to route output DAC FIFO data to the inputs of on-board DAC1/DAC2 digital-to-analog converters, i.e. in case *DSOUT_SEL* bit of *DAQ_MUX_RG* register is set to the *DSOUT_SEL*=0 state, then *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* write-only registers shall contain output data for DAC1 and DAC2 correspondingly. The 12-bit DAC1 and DAC2 input data are aligned to the least significant bit of 16-bit data words of host PIOX-16 interface.

DAC1_FIFO_DATA_RG register (w)
for writes to DAC1
(*DSOUT_SEL* bit of *DAQ_MUX_RG* register is set to the *DSOUT_SEL*=0 state)

X	X	x	x	DAC1_DATA-11.. DAC1_DATA-0 *(w)*
Bit 15	Bit-14	bit-13	Bit-12	bits-11..0
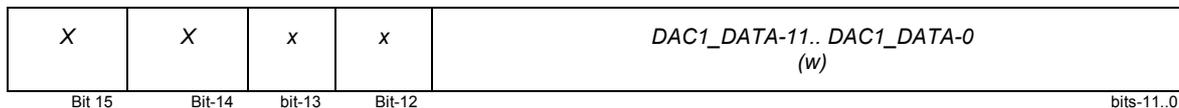
DAC2_FIFO_DATA_RG register (w)
for writes to DAC2
(*DSOUT_SEL* bit of *DAQ_MUX_RG* register is set to the *DSOUT_SEL*=0 state)

X	X	x	x	DAC2_DATA-11.. DAC2_DATA-0 *(w)*
Bit 15	Bit-14	bit-13	Bit-12	bits-11..0
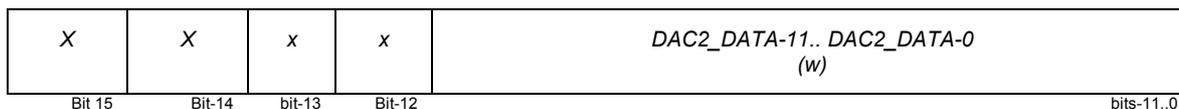
Table 2-10a provides details about *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* registers bits for DAC1/DAC2 data writes.

Table 2-10a. Register bits of *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* registers for writes to DAC1/DAC2.

register bits	access mode	default value on PIOX-16 reset	Description
{DAC1_DATA-11.. DAC1_DATA-0} {DAC2_DATA-11.. DAC2_DATA-0}	W	-	12-bit DAC1 and DAC2 signed input data correspondingly.

Note: 1.   Access modes: r/w – read/write; r – read-only; w – write only.

In case DSOUT-MUX output data stream multiplexer is configured to route output DAC FIFO data to 32-bit XDSOUT output data stream at on0boad JP4 connector, i.e. in case *DSOUT_SEL* bit of *DAQ_MUX_RG* register is set to the *DSOUT_SEL*=1 state, then *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* write-only registers shall contain output data for 16-bit XDSOUT-A0..A15 and XDSOUT-B0..B15 data words of 32-bit XDSOUT output data stream correspondingly and occupy full 16-bit data words of host PIOX-16 interface.

DAC1_FIFO_DATA_RG register (w)
for writes to 32-bit XDSOUT external output data stream
(*DSOUT_SEL* bit of *DAQ_MUX_RG* register is set to the *DSOUT_SEL*=1 state)

XDSOUT-A15.. XDSOUT-A0 *(w)*
bits-15..0

DAC2_FIFO_DATA_RG register (w)
for writes to 32-bit XDSOUT external output data stream
(*DSOUT_SEL* bit of *DAQ_MUX_RG* register is set to the *DSOUT_SEL*=1 state)

XDSOUT-B15.. XDSOUT-B0 (w)

bits-15..0
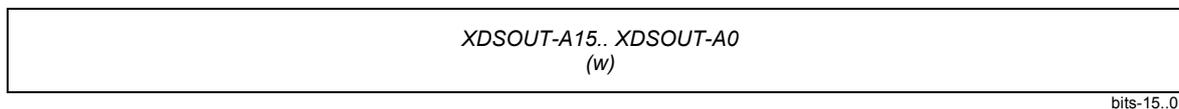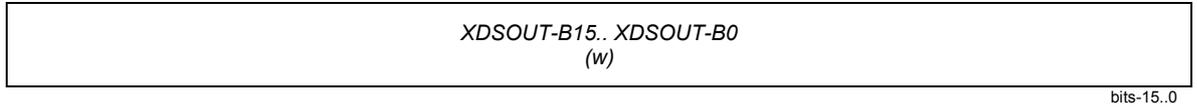
Table 2-10b provides details about *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* registers bits for 32-bit XDSOUT output data stream writes.

Table 2-10b. Register bits of *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* registers for writes to 32-bit XDSOUT external output data stream.

register bits	access mode	default value on PIOX-16 reset	Description
{XDSOUT-A15.. XDSOUT-A0} {XDSOUT-B15.. XDSOUT-B0}	w	-	16-bit halfwords of 32-bit XDSOUT external output data stream words, which are routed to on-board JP4 connector.

Note: 1.   Access modes: r/w – read/write; r – read-only; w – write only.

ADC/DAC FIFO serial configuration registers

ADC_FIFO_SIN_RG and *DAC_FIFO_SIN_RG* write-only registers shall be used to program the offset values for PAE/PAF flags of ADC and DAC FIFO correspondingly while ADC and/or DAC data acquisition controllers are configured in the corresponding configuration modes via *DAQ_CNTR1_RG* register (table 2-2).

ADC and DAC FIFO have been designed to program PAE/PAF flags using serial programming technique via serial-in input (SIN), so *ADC_FIFO_SIN_RG* and *DAC_FIFO_SIN_RG* registers actually appear as 1-bit write-only registers allocated to the least significant bit of 16-bit data word of host PIOX-16 interface.

ADC_FIFO_SIN_RG register (w)

X	x	X	X	x	X	X	x	ADC_FIFO_SIN (w)
Bits 15..8	bit-7	bit-6	Bit-5	bit-4	bit-3	Bit-2	bit-1	bit-0
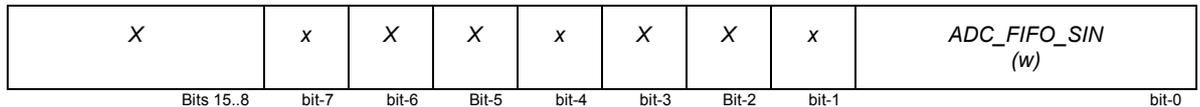
DAC_FIFO_SIN_RG register (w)

X	x	X	X	x	X	X	x	DAC_FIFO_SIN (w)
Bits 15..8	bit-7	bit-6	Bit-5	bit-4	bit-3	Bit-2	bit-1	bit-0

Table 2-11. Register bits of *ADC_FIFO_SIN_RG* and *DAC_FIFO_SIN_RG* registers.

register bits	access mode	default value on PIOX-16 reset	description
ADC_XFIFO_SIN *DAC_XFIFO_SIN*	w	-	FIFO serial-in (SIN) input data for serial programming of ADC and DAC FIFO correspondingly.

Note: 1.   Access modes: r/w – read/write; r – read-only; w – write only.

Refer to section "Data Acquisition Control" later in this chapter for more details about how to program PAE/PAF flags of ADC and DAC FIFO.

PFG control registers

The output frequency of on-board high-resolution programmable sampling frequency generator (PFG) can be set by means of 20-bit code comprising of V, R, S and X fields (refer to section "Data Acquisition Control" later in this chapter for more details about how to program the PFG output frequency).

PFG V, R, S and X fields can be set by host DSP software using *PFG_CNTR1_RG*, *PFG_CNTR2_RG* and *PFG_CNTR3_RG* registers, which are available for read/write and are allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

PFG_CNTR1_RG register (r/w)

x	PFG_V7 (r/w, 0+)	PFG_V6 (r/w, 0+)	PFG_V5 (r/w, 0+)	PFG_V4 (r/w, 0+)	PFG_V3 (r/w, 0+)	PFG_V2 (r/w, 0+)	PFG_V1 (r/w, 0+)	PFG_V0 (r/w, 0+)
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	Bit-2	bit-1	bit-0

PFG_CNTR2_RG register (r/w)

x	PFG_R6 (r/w, 0+)	PFG_R5 (r/w, 0+)	PFG_R4 (r/w, 0+)	PFG_R3 (r/w, 0+)	PFG_R2 (r/w, 0+)	PFG_R1 (r/w, 0+)	PFG_R0 (r/w, 0+)	PFG_V8 (r/w, 0+)
bits 15..8	bit-7	bit-6	bit-5	bit-4	bit-3	Bit-2	bit-1	bit-0

PFG_CNTR3_RG register (r/w)

x	0	0	0	PFG_X (r/w, 0+)	0	PFG_S2 (r/w, 0+)	PFG_S1 (r/w, 0+)	PFG_S0 (r/w, 0+)
bits 15..8	bit-7	Bit-6	bit-5	bit-4	bit-3	Bit-2	bit-1	bit-0

Table 2-12 provides details about *PFG_CNTR1_RG*, *PFG_CNTR2_RG* and *PFG_CNTR3_RG* registers bits.

Table 2-12. Register bits of *PFG_CNTR1_RG*, *PFG_CNTR2_RG* and *PFG_CNTR3_RG* registers.

register bits	access mode	default value on PIOX-16 reset	Description
{V8..V0}	r/w	16H	Defines 9-bit V-field for on-board PFG. Refer to section "Data Acquisition Control" later in this chapter for more details about how to program the PFG output frequency.
{R6..R0}	r/w	49H	Defines 7-bit R-field for on-board PFG. Refer to section "Data Acquisition Control" later in this chapter for more details about how to program the PFG output frequency.
{S2..S0}	r/w	0H	Defines 3-bit S-field for on-board PFG. Refer to section "Data Acquisition Control" later in this chapter for more details about how to program the PFG output frequency.
X	r/w	0	Defines 1-bit X-field for on-board PFG. Refer to section "Data Acquisition Control" later in this chapter for more details about how to program the PFG output frequency.

Note: 1.   Access modes: r/w – read/write; r – read-only; w – write only.

CAUTION

Host PIOX-16 interface reset condition will preset *PFG_CNTR1_RG*, *PFG_CNTR2_RG* and *PFG_CNTR3_RG* registers to default values, which correspond to 2 MHz PFG output frequency.

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general purpose I/O (GPIO) control

GPIO-0..3 are general purpose I/O pins, which are available via on-board JP2 external synchronization connector. *GPIO-0..3* I/O pins are controlled by two control registers (refer to table 2-2):

- *GPIO_DIR_RG* register (*GPIO* direction register)
- *GPIO_DATA_RG* register (*GPIO* data register)

GPIO_DIR_RG register must be used to define direction for *GPIO-0..3* I/O pins, whereas *GPIO_DATA_RG* register must be used to define output value and read current status of *GPIO-0..3* I/O pins. *GPIO_DIR_RG* and

GPIO_DATA_RG registers are available for read/write and are allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

GPIO_DIR_RG register (r/w)

X	0	0	0	0	GPIO-3_DIR (r/w, 0+)	GPIO-2_DIR (r/w, 0+)	GPIO-1_DIR (r/w, 0+)	GPIO-0_DIR (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	Bit-1	bit-0

GPIO_DATA_RG register (r/w)

X	0	0	0	0	GPIO-3_DATA (r/w, 0+)	GPIO-2_DATA (r/w, 0+)	GPIO-1_DATA (r/w, 0+)	GPIO-0_DATA (r/w, 0+)
bits-15..8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	Bit-1	bit-0

Tables 2-13a and 2-13b provides details about *GPIO_DIR_RG* and *GPIO_DATA_RG* registers bits.

Table 2-13a. Register bits of *GPIO_DIR_RG* register.

Register bits	access mode	Default value on PIOX-16 reset	Description
GPIO-0_DIR *GPIO-1_DIR* *GPIO-2_DIR* *GPIO-3_DIR*	*r/w*	0	Define direction for *GPIO-0..3* I/O pin correspondingly. *GPIO-x_DIR* =0 corresponds to the input direction for the corresponding *GPIO-x* I/O pin. In this case the current state of *GPIO-x* input pin can be read by host DSP software via the *GPIO-x_DATA* bit of *GPIO_DATA_RG* register. All writes to the *GPIO-x_DATA* bit of *GPIO_DATA_RG* register are ignored until the *GPIO-x* I/O pin will be configure as output pin. *GPIO-x_DIR* =1 corresponds to the output direction for the corresponding *GPIO-x* I/O pin. In this case the output value of *GPIO-x* input pin can be set by host DSP software by writing to the *GPIO-x_DATA* bit of *GPIO_DATA_RG* register, whereas current state of *GPIO-x* pin can be read by host DSP software via the *GPIO-x_DATA* bit of *GPIO_DATA_RG* register.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.
         2. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

Table 2-13b. Register bits of *GPIO_DATA_RG* register.

register bits	access mode	Default value on PIOX-16 reset	Description
GPIO-0_DATA *GPIO-1_DATA* *GPIO-2_DATA* *GPIO-3_DATA*	r/w	-	Returns current state of *GPIO-0..3* I/O pins correspondingly during read cycle. Defines output value for *GPIO-0..3* pins during write cycle in case *GPIO-0..3* pins are configured as outputs. Reading *GPIO-x_DATA* =0 corresponds to current '0' state for the corresponding *GPIO-x* I/O pin. Reading *GPIO-x_DATA* =1 corresponds to current '1' state for the corresponding *GPIO-x* I/O pin. Writing *GPIO-x_DATA* =0 sets the output '0' value for the corresponding *GPIO-x* I/O pin. However, the written output value will not take effect until the *GPIO-x* I/O pin will be configured as the output via *GPIO_DIR_RG* register. Writing *GPIO-x_DATA* =1 sets the output '1' value for the corresponding *GPIO-x* I/O pin. However, the written output value will not take effect until the *GPIO-x* I/O pin will be configured as the output via *GPIO_DIR_RG* register.

Note: 1. Access modes: r/w – read/write; r – read-only; w – write only.

CAUTION

In case any of *GPIO-0..3* I/O pins is configured as input, then writing to the corresponding bit of *GPIO_DATA_RG* register is ignored, however data written will be held in *GPIO_DATA_RG* register and will appear on the corresponding *GPIO-0..3* outputs as soon as it (they) will be configured as the output(s).

CAUTION

Active low condition at the *GPIO-0* and/or *GPIO-1* I/O pins can be used to generate host PIOX-16 interrupt requests.

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host PIOX-16 interrupt control

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM offers software programmable source selectors and enable control for each of four host PIOX-16 interrupt requests (IRQ-0..3). Host PIOX-16 interrupt requests can be generated on a variety of data acquisition conditions and external events.

Since the total number of possible host DSP interrupt sources for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is well above four sources, then individual interrupt source selector and enable control for each of host PIOX-16 interrupt requests allow outstanding flexibility for run-time host interrupt system configuration for *T/PDAS-AD8/12D/65M-DA2/12D/65M* in order to meet requirements of virtually any application.

Selection of interrupt source for IRQ-0..3 host PIOX-16 interrupt requests is performed by host DSP software by means of programming *HIRQ0_SEL_RG..HIRQ3_SEL_RG* interrupt control registers, which are available for read/write and are allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

HIRQ0_SEL_RG register (r/w)

x	HIRQ0_EN (r/w, 0+)	0	0	HIRQ0_SEL-4 (r/w, 0+)	HIRQ0_SEL-3 (r/w, 0+)	HIRQ0_SEL-2 (r/w, 0+)	HIRQ0_SEL-1 (r/w, 0+)	HIRQ0_SEL-0 (r/w, 0+)
bit-15...8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

HIRQ1_SEL_RG register (r/w)

x	HIRQ1_EN (r/w, 0+)	0	0	HIRQ1_SEL-4 (r/w, 0+)	HIRQ1_SEL-3 (r/w, 0+)	HIRQ1_SEL-2 (r/w, 0+)	HIRQ1_SEL-1 (r/w, 0+)	HIRQ1_SEL-0 (r/w, 0+)
bit-15...8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

HIRQ2_SEL_RG register (r/w)

x	HIRQ2_EN (r/w, 0+)	0	0	0	HIRQ2_SEL-3 (r/w, 0+)	HIRQ2_SEL-2 (r/w, 0+)	HIRQ2_SEL-1 (r/w, 0+)	HIRQ2_SEL-0 (r/w, 0+)
bit-15...8	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0

HIRQ3_SEL_RG register (r/w)

x	HIRQ3_EN (r/w, 0+)	0	0	0	HIRQ3_SEL-3 (r/w, 0+)	HIRQ3_SEL-2 (r/w, 0+)	HIRQ3_SEL-1 (r/w, 0+)	HIRQ3_SEL-0 (r/w, 0+)
bit-15...8	bit-7	bit-6	bit-5	Bit-4	bit-3	bit-2	bit-1	bit-0

Table 2-14 provides details about *HIRQ0_SEL_RG .. HIRQ3_SEL_RG* registers bits.

Table 2-14. Register bits of *HIRQ0_SEL_RG*, *HIRQ1_SEL_RG*, *HIRQ2_SEL_RG* and *HIRQ3_SEL_RG* registers.

Register bits	access mode	default value on PIOX-16 reset	Description
{*HIRQ0_SEL-4.. HIRQ0_SEL-0*} {*HIRQ1_SEL-4.. HIRQ1_SEL-0*} {*HIRQ2_SEL-3.. HIRQ2_SEL-0*} {*HIRQ3_SEL-3.. HIRQ3_SEL-0*}	r/w	0H	Select interrupt source for the corresponding host PIOX-16 interrupt request in accordance with table 2-15a and 2-15b.
HIRQ0_EN HIRQ1_EN HIRQ2_EN HIRQ3_EN	r/w	0	Enables the corresponding host PIOX-16 interrupt. *HIRQx-_EN* =0 corresponds to disabled IRQ-x host PIOX-16 interrupt request, i.e. IRQ-x host PIOX-16 interrupt request is tri-stated. *HIRQx-_EN* =1 corresponds to enabled IRQ-x host PIOX-16 interrupt request with an interrupt source being selected with the corresponding {*HIRQx_SEL-4..HIRQx_SEL-0*} register field.

Note: 1.   Access modes: r/w – read/write; r – read-only; w – write only.
             2.   Highlighted configurations correspond to default settings on PIOX-16 reset condition.

Host PIOX-16 interface IRQ-0 and IRQ-1 interrupt source selectors of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM allow selection of one interrupt source from 27 available interrupt sources in accordance with table 2-15a, whereas host PIOX-16 interface IRQ-2 and IRQ-3 interrupt source selectors allow selection of one interrupt source from 11 available interrupt sources in accordance with table 2-15b.

Table 2-15a. Interrupt sources for IRQ-0 and IRQ-1 host PIOX-16 interrupt requests.

bits #4..#0 of HIRQ0_SEL_RG and HIRQ1_SEL_RG					interrupt source
bit #4	bit #3	bit #2	bit #1	bit #0	
0	0	0	0	0	Interrupt is disabled. This is the default value on PIOX-16 reset condition.
0	0	0	0	1	Interrupt on the end of ADC data acquisition process for ADC OPM mode (bit *ADC_DAQ_EN* of *DAQ_CNTR2_RG* register is set to the '1' state).
0	0	0	1	0	Interrupt on the end of DAC data acquisition process for DAC OPM mode (bit *DAC_DAQ_EN* of *DAQ_CNTR2_RG* register is set to the '1' state).
0	0	0	1	1	Interrupt on detection of synchronization event for ADC data acquisition process (bit *ADC_SYNC_OK* of *DAQ_CNTR2_RG* register is set to the '1' state).
0	0	1	0	0	Interrupt on detection of synchronization event for DAC data acquisition process (bit *DAC_SYNC_OK* of *DAQ_CNTR2_RG* register is set to the '1' state).
0	0	1	0	1	Interrupt from ADC IRT controller (positive polarity output).
0	0	1	1	0	Interrupt from ADC IRT controller (negative polarity output).
0	0	1	1	1	Interrupt from DAC IRT controller (positive polarity output).
0	1	0	0	0	Interrupt from DAC IRT controller (negative polarity output).
0	1	0	0	1	Interrupt on active low condition at *GPIO-0* I/O pin.
0	1	0	1	0	Interrupt on active low condition at *GPIO-1* I/O pin.
0	1	0	1	1	Interrupt on logical OR of data acquisition error conditions in accordance with *XIM_ERR_RG* register.
1	0	0	0	0	Interrupt on ADC1-FIFO full condition (FF flag of ADC1-FIFO is set to the '1' state).
1	0	0	0	1	Interrupt on ADC1-FIFO partially full condition (PAF flag of ADC1-FIFO is set to the '1' state).
1	0	0	1	0	Interrupt on ADC1-FIFO empty condition (EF flag of ADC1-FIFO is set to the '1' state).
1	0	0	1	1	Interrupt on ADC1-FIFO partially empty condition (PAE flag of ADC1-FIFO is set to the '1' state).
1	0	1	0	0	Interrupt on ADC2-FIFO full condition (FF flag of ADC2-FIFO is set to the '1' state).

1	0	1	0	1	Interrupt on ADC2-FIFO partially full condition (PAF flag of ADC2-FIFO is set to the '1' state).
1	0	1	1	0	Interrupt on ADC2-FIFO empty condition (EF flag of ADC2-FIFO is set to the '1' state).
1	0	1	1	1	Interrupt on ADC2-FIFO partially empty condition (PAE flag of ADC2-FIFO is set to the '1' state).
1	1	0	0	0	Interrupt on DAC1-FIFO full condition (FF flag of DAC1-FIFO is set to the '1' state).
1	1	0	0	1	Interrupt on DAC1-FIFO partially full condition (PAF flag of DAC1-FIFO is set to the '1' state).
1	1	0	1	0	Interrupt on DAC1-FIFO empty condition (EF flag of DAC1-FIFO is set to the '1' state).
1	1	0	1	1	Interrupt on DAC1-FIFO partially empty condition (PAE flag of DAC1-FIFO is set to the '1' state).
1	1	1	0	0	Interrupt on DAC2-FIFO full condition (FF flag of DAC2-FIFO is set to the '1' state).
1	1	1	0	1	Interrupt on DAC2-FIFO partially full condition (PAF flag of DAC2-FIFO is set to the '1' state).
1	1	1	1	0	Interrupt on DAC2-FIFO empty condition (EF flag of DAC2-FIFO is set to the '1' state).
1	1	1	1	1	Interrupt on DAC2-FIFO partially empty condition (PAE flag of DAC2-FIFO is set to the '1' state).

Notes: 1. Unlisted combinations are reserved and will result in no interrupt selection.
          2. Highlighted selection corresponds to default setting on host PIOX-16 interface condition.

Table 2-15b. Interrupt sources for IRQ-2 and IRQ-3 host PIOX-16 interrupt requests.

bits #4..#0 of HIRQ0_SEL_RG and HIRQ1_SEL_RG				interrupt source
bit #3	bit #2	bit #1	bit #0	
0	0	0	0	Interrupt is disabled. This is the default value on PIOX-16 reset condition.
0	0	0	1	Interrupt on the end of ADC data acquisition process for ADC OPM mode (bit *ADC_DAQ_EN* of *DAQ_CNTR2_RG* register is set to the '1' state).
0	0	1	0	Interrupt on the end of DAC data acquisition process for DAC OPM mode (bit *DAC_DAQ_EN* of *DAQ_CNTR2_RG* register is set to the '1' state).
0	0	1	1	Interrupt on detection of synchronization event for ADC data acquisition process (bit *ADC_SYNC_OK* of *DAQ_CNTR2_RG* register is set to the '1' state).
0	1	0	0	Interrupt on detection of synchronization event for DAC data acquisition process (bit *DAC_SYNC_OK* of *DAQ_CNTR2_RG* register is set to the '1' state).
0	1	0	1	Interrupt from ADC IRT controller (positive output polarity).
0	1	1	0	Interrupt from ADC IRT controller (negative output polarity).
0	1	1	1	Interrupt from DAC IRT controller (positive output polarity).
1	0	0	0	Interrupt from DAC IRT controller (negative output polarity).
1	0	0	1	Interrupt on active low condition at *GPIO-0* I/O pin.
1	0	1	0	Interrupt on active low condition at *GPIO-1* I/O pin.
1	0	1	1	Interrupt on logical OR of data acquisition error conditions in accordance with *XIM_ERR_RG* register.

Notes: 1. Unlisted combinations are reserved and will result in no interrupt selection.
                2. Highlighted selection corresponds to default setting on host PIOX-16 interface condition.

CAUTION

HIRQ0_SEL_RG..HIRQ3_SEL_RG interrupt request selector registers default to the 00H state on host PIOX-16 interface reset condition, which corresponds to no selected interrupt source and disabled interrupt request outputs.

In case any of *HIRQ0_SEL_RG..HIRQ3_SEL_RG* registers is configured to select logical OR of error conditions, then the logical OR of error conditions, which appear in *ERR_STAT_RG* register, is generated

using the *XIM_ERR_RG* expansion error interrupt mask register, which is available for read/write and is allocated to the least significant byte of 16-bit data word of host PIOX-16 interface.

XIM_ERR_RG register (r/w)

X	0	0	XIM_DAC_ IRT_ERR (r/w,0+)	XIM_ADC_ IRT_ERR (r/w,0+)	XIM_DAC_ FIFO_UNF (r/w,0+)	XIM_DAC_ FIFO_OVF (r/w,0+)	XIM_ADC_ FIFO_UNF (r/w,0+)	XIM_ADC_ FIFO_OVF (r/w,0+)
Bits 15..8	bit-7	bit-6	Bit-5	bit-4	Bit-3	bit-2	Bit-1	bit-0

CAUTION

Host PIOX-16 interrupt request on logical OR of error conditions is generated as logical OR of the corresponding enabled (unmasked) error conditions as they appear in *ERR_STAT_RG* register.

Table 2-16 provides details about *XIM_ERR_RG* register bits.

Table 2-16. Register bits of *XIM_ERR_RG* register.

register bits	access mode	default value on PIOX-16 reset	Description
XIM_ADC_FIFO_OVF	r/w	0	Expansion interrupt mask for ADC FIFO overflow error (bit *ADC_FIFO_OVF* of *ERR_STAT_RG* register). *XIM_ADC_FIFO_OVF*=0 corresponds to disabled host PIOX-16 interrupt request on ADC FIFO overflow error condition. *XIM_ADC_FIFO_OVF*=1 corresponds to enabled host PIOX-16 interrupt request on ADC FIFO overflow error condition.
XIM_ADC_FIFO_UNF	r/w	0	Expansion interrupt mask for ADC FIFO underflow error (bit *ADC_FIFO_UNF* of *ERR_STAT_RG* register). *XIM_ADC_FIFO_UNF*=0 corresponds to disabled host PIOX-16 interrupt request on ADC FIFO underflow error condition. *XIM_ADC_FIFO_UNF*=1 corresponds to enabled host PIOX-16 interrupt request on ADC FIFO underflow error condition.
XIM_DAC_FIFO_OVF	r/w	0	Expansion interrupt mask for DAC FIFO overflow error (bit *DAC_FIFO_OVF* of *ERR_STAT_RG* register). *XIM_DAC_FIFO_OVF*=0 corresponds to disabled host PIOX-16 interrupt request on DAC FIFO overflow error condition. *XIM_DAC_FIFO_OVF*=1 corresponds to enabled host PIOX-16 interrupt request on DAC FIFO overflow error condition.
XIM_DAC_FIFO_UNF	r/w	0	Expansion interrupt mask for DAC FIFO underflow error (bit *DAC_FIFO_UNF* of *ERR_STAT_RG* register). *XIM_DAC_FIFO_UNF*=0 corresponds to disabled host PIOX-16 interrupt request on DAC FIFO underflow error condition. *XIM_DAC_FIFO_UNF*=1 corresponds to enabled host PIOX-16 interrupt request on DAC FIFO underflow error condition.
XIM_ADC_IRT_ERR	r/w	0	Expansion interrupt mask for ADC IRT error (bit *ADC_IRT_ERR* of *ERR_STAT_RG* register). *XIM_ADC_IRT_ERR*=0 corresponds to disabled host PIOX-16 interrupt request on ADC IRT error condition. *XIM_ADC_IRT_OVF*=1 corresponds to enabled host PIOX-16 interrupt request on ADC IRT error condition.

XIM_DAC_IRT_ERR	r/w	0	Expansion interrupt mask for DAC IRT error (bit *DAC_IRT_ERR* of *ERR_STAT_RG* register). *XIM_DAC_IRT_ERR*=0 corresponds to disabled host PIOX-16 interrupt request on DAC IRT error condition. *XIM_DAC_IRT_OVF*=1 corresponds to enabled host PIOX-16 interrupt request on DAC IRT error condition.

Note:
1. Access modes: r/w – read/write; r – read-only; w – write only.
2. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

2.2   Data Acquisition Control

A/D and D/A data acquisition processes for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM are configured and controlled via a set of control registers (refer to section "Host PIOX-16 Interface" earlier in this chapter and to table 2-1):

- *DAQ_CNTR1_RG* register, which is used to select ADC/DAC data acquisition modes and data formats
- *DAQ_CNTR2_RG* register, which is used to perform real-time control for ADC/DAC data acquisition
- *DAQ_CNTR3_RG* register, which is used to select ADC/DAC data acquisition termination flags and ADC/DAC interrupt retriggable transmission (IRT) transmission start/termination flags
- *DAQ_SYNC_RG* register, which is used to select sampling frequency source, ADC/DAC data acquisition synchronization mode, external synchronization mode and Master/Slave mode
- *DAQ_MUX_RG* register, which is used to select analog input channel for analog input section, and to configure input and output data stream multiplexers
- *ADC_FIFO_STAT_RG* and *DAC_FIFO_STAT_RG* registers, which indicate current flags status of ADC and DAC FIFO
- *ADC1_FIFO_DATA_RG*, *ADC1_FIFO_DATA_RG*, *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* registers, which are used to read ADC1/ADC2 data streams and to write DAC1/DAC2 data streams
- *ADC_FIFO_SIN_RG* and *DAC_FIFO_SIN_RG* registers, which are used to program offset values for FIFO flags
- *ADC_DAQ_RESET_RG*, *DAC_DAQ_RESET_RG* and *DAQ_RESET_RG* registers, which are used to reset ADC and DAC data acquisition controllers and read/write pointers and flags for the corresponding FIFO
- *ERR_STAT_RG* and *ERR_CLR_RG* registers, which are used to indicate current data acquisition errors and to clear these errors
- *PFG_CNTR1_RG* ,*PFG_CNTR2_RG* and *PFG_CNTR3_RG* registers, which are used to program the sampling frequency value for on-board high-resolution PFG.

This section provides details about operation and how to configure and control A/D and D/A data acquisition processes for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

analog input section

Analog input section of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM (fig.2-1) comprises of two identical A/D channels (#1 and #2), and is designed for synchronous analog-to-digital conversion of any pre-selected pair

of analog input signals from AIN-A0..A3 and AIN-B0..B3 analog inputs. ADC output data streams are further routed to the DSIN-MUX digital input stream multiplexer.

Each A/D channel of analog input section comprises of the following components:
- 4:1 analog input multiplexer (AIN-MUX) with four analog inputs (AIN-A0..A3 for A/D channel #1 and AIN-B0..B3 for A/D channel #2)
- analog input amplifier (AIN-A)
- 12-bit 65 Msps ADC (ADC1 and ADC2 correspondingly).

AIN-MUX 4:1 analog input multiplexers shall be used to select a particular pair of two analog inputs from four available, which will be connected to the inputs of the corresponding ADC chips for conversion to digital code. AIN-MUX analog input multiplexers for both A/D channels are controlled by bits {*ADC_IMUX-1, ADC_IMUX-0*} of *DAQ_MUX_RG* register of host PIOX-16 interface (table 2-6), which allows selection of AIN-A0/B0, AIN-A1/B1, AIN-A2/B2 and AIN-A3/B3 analog input pairs for synchronous A/D conversion by two on-board ADC chips.

CAUTION

AIN-MUX analog input multiplexers of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM are statically controlled and do not allow to multiplex analog inputs in every sampling period.

The analog inputs of A/D channel #1 are labeled as AIN-A0..A3, whereas the analog inputs for A/D channel #2 are labeled as AIN-B0..B3. Each analog input can be connected to external analog world via dedicated mini-coax on-board connector (JP5..JP8 connectors for A/D channel #1 and JP9..JP12 connectors for A/D channel #2). Input impedance for each analog input is 50 Ohm.

The AIN-A analog input amplifiers feature gain factor 0dB and are used for interfacing of the outputs of AIN-MUX analog input multiplexers to the inputs of the corresponding ADC chips. Each AIN-A analog input amplifier is DC coupled with the input of the corresponding ADC chip and allows conversion of DC analog input signals.

CAUTION

Analog input section provides minimum DC zero offset error and analog signal distortion in case output DC impedance of external analog signal source is 50 Ohm (rev.1A only).

Depending upon the particular product part number option, analog input amplifiers of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM can either provide 1st order low-pass filtering of input analog signal with predefined low-pass cutoff frequencies in order to limit signal bandwidth, or can appear as wide-band amplifiers without low-pass filters in order to allow undersampling of ultra-high analog input signals.

Standard configuration of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM comes with the input low-pass filters with the cutoff frequency 32.5 MHz, which appears as 1st order anti-aliasing filter for 65 MHz sampling frequency. Other available product options provide different LPF cutoff frequencies for AIN-A analog input amplifiers, which well exceed the 32.5 MHz bandwidth for 65 MHz maximum ADC sampling frequency value, and therefore allow 1st and 2nd order undersampling. For more details of available product options refer to technical specifications in section 1.2.

On-board ADC chips feature 12-bit resolution and excellent linearity at up to 65 MHz sampling frequency, which guarantee minimum signal distortion during A/D conversion at ultra-high sampling frequencies. Both on-board ADC chips provide synchronous sampling of analog input signals.

CAUTION

On-board ADC chips allow minimum sampling frequency as 6.5 MHz. Setting the lower sampling frequency may result in incorrect operation of on-board ADC.

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input data streams multiplexer (DSIN-MUX)

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM allows to input external 32-bit parallel digital input data stream (XDSIN) as an alternative to dual-channel ADC output data stream from analog input section. This feature provides interfacing of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM to a variety of high-frequency digital telecommunication and instrumentation equipment, which provides parallel digital output data.

32-bit XDSIN external digital input stream comes from on-board JP3 connector and is splitted into two 16-bit data streams (XDSIN-A0..A15 and XDSIN-B0..B15) with common synchronization. External data stream synchronization signals comprises of clock and enable outputs, which are controlled by on-board ADC data acquisition controller (refer to Appendix A and the corresponding subsection later in this section for more details) and allow to synchronize external digital equipment to on-board A/D data acquisition process.

24-bit ADC output data stream (ADC1-0..11 and ADC2-0..11) and 32-bit XDSIN external digital input stream (XDSIN-A0..A15 and XDSIN-B0..B15) are multiplexed by dual-channel 16-bit input data stream multiplexer (DSIN-MUX). Two 16-bit output data streams from DSIN-MUX multiplexer are further routed to the input of the corresponding ADC FIFO (ADC1-FIFO and ADC2-FIFO).

Dual-channel DSIN-MUX input data stream multiplexer is controlled by DSP software of host *TORNADO* DSP system/controller via *DSIN_SEL* bit of *DAQ_MUX_RG* register (table 2-6) of host PIOX-16 interface.

CAUTION

DSIN-MUX input data stream multiplexer of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is statically controlled and do not allow to multiplex input data streams in every sampling period.

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analog output section

Analog output section of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM comprises of two identical D/A channels (#1 and #2), and is designed for digital-to-analog conversion of output data stream from DSOUT-MUX digital output stream multiplexer to analog output signals.

Each D/A channel of analog input section comprises of the following components:
- 12-bit 65 Msps DAC (DAC1 and DAC2 correspondingly)
- analog output amplifier (AOUT-A).

On-board DAC chips feature 12-bit resolution and excellent linearity at up to 65 MHz sampling frequency, which guarantee minimum signal distortion during D/A conversion at ultra-high sampling frequencies. Both on-board DAC chips provide synchronous sampling of input code.

CAUTION

On-board DAC chips do not feature minimum sampling frequency specification and allow to perform D/A conversion at any sampling frequency below 65 MHz.

The AOUT-A analog output amplifiers feature gain factor 0dB and are used to interface of DAC outputs to external low impedance loads. Each analog output can be connected to external analog world via dedicated mini-coax on-board connector (JP13 connector for D/A channel #1 and JP14 connector for D/A channel #2). Output impedance for each analog output is 50 Ohm.

CAUTION

Analog input section provides minimum analog signal distortion in case input impedance of external analog load is 50 Ohm.

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output data streams multiplexer (DSOUT-MUX)

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM supports external 32-bit parallel digital output data stream (XDSOUT) as an alternative to dual-channel analog outputs via analog output section. This feature allows to interface *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM to a variety of high-frequency digital telecommunication and instrumentation equipment, which requires input digital data.

32-bit XDSOUT external digital output stream is routed to on-board JP4 connector and is splitted into two 16-bit data streams (XDSOUT-A0..A15 and XDSOUT-B0..B15) with common synchronization. External data stream synchronization signals comprises of clock and enable outputs, which are controlled by on-board DAC data acquisition controller (refer to Appendix A and the corresponding subsection later in this section for more details) and allow to synchronize external digital equipment to on-board D/A data acquisition process.

24-bit DAC input data stream (DAC1-0..11 and DAC2-0..11) and 32-bit XDSOUT external digital output stream (XDSOUT-A0..A15 and XDSOUT-B0..B15) are demultiplexed by dual-channel 16-bit output data stream multiplexer (DSOUT-MUX) from the outputs of the corresponding DAC FIFO (DAC1-FIFO and DAC2-FIFO). Dual-channel DSOUT-MUX out data stream multiplexer is controlled by DSP software of host *TORNADO* DSP system/controller via *DSOUT_SEL* bit *DAQ_MUX_RG* register of host PIOX-16 interface (table 2-6).

> **CAUTION**
>
> DSOUT-MUX output data stream multiplexer of *T/PDAS-AD8/12D/65M-DA2/12D/65M*
> DCM is statically controlled and do not allow to multiplex output data streams in every
> sampling period.

sampling frequency selector

Sampling frequency is common for ADC and DAC data acquisition controllers and can be selected by DSP software of host *TORNADO* DSP system/controller via {*FS_SEL-1, FS_SEL-0*} bits *DAQ_MUX_RG* register (table 2-5) of host PIOX-16 interface to come from the following sources:

- on-board high-resolution programmable sampling frequency generator (PFG)
- external sampling frequency input (XFS) from on-board JP2 connector
- any of two timer inputs of host PIOX-16 interface (TM/XIO-0 and TM/XIO-1).

The on-board PFG high-resolution programmable sampling frequency generator is the recommended selection for sampling frequency source and can be programmed by host DSP software to any frequency value within the 0.0625 MHz .. 65 MHz frequency range. For more details about PFG refer to the corresponding subsection later in this section.

External sampling frequency input XFS is available at the JP2 external synchronization connector (refer to Appendix A) and feature low impedance 100 Ohm logical input in order to minimize signal distortions when connecting to external signal sources.

Host PIOX-16 interface timer pins (TM/XIO-0 and TM/XIO-1) can be also used as the sampling frequency source for ADC and DAC acquisition controllers of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM. However, since these timer pins outputs are outputs of on-board DSP chip of host *TORNADO* DSP system/controller, these DSP on-chip timers are typically used for software purposes as real-time clock.

Current sampling frequency signal is always available at the FS_OUT output of on-board JP2 connector, and it can be used either to synchronize external circuits or to connect to the XFS input of other *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, which operate in 'Slave' mode.

PFG programmable sampling frequency generator

On-board PFG programmable frequency generator must be used for accurate setting of sampling frequency for ADC and DAC data acquisition controllers within the 62.5 kHz .. 65 MHz frequency range.

On-board PFG is controlled by 9-bit V-field (V0..V8), 7-bit R-field (R0..R6), 2-bit S-field (S0..S2) and 1-bit X-field (X) via *PFG_CNTR1_RG*, *PFG_CNTR2_RG* and *PFG_CNTR3_RG* registers (table 2-12) of host PIOX-16 interface as the following:

$$Fout = \frac{50MHz*(V+8)}{(R+2)*Sv*Xv}$$

where:

Fout   output frequency value (MHz) of the corresponding PFG

V   numeric value of 9-bit V-field

R   numeric value of 7-bit R-field

Sv   value of S-divider, which is defined by 3-bit S-field in accordance with table 2-17a

Xv   value of X-divider, which is defined by 1-bit X-field in accordance with table 2-17b.

Table 2-17a.   S-divider settings for PFG.

value of the S-field			value of S-divider (*Sv*)
S2	*S1*	*S0*	
0	0	0	:10
0	0	1	:2
0	1	0	:8
0	1	1	:4
1	0	0	:5
1	0	1	:7
1	1	0	:9
1	1	1	:6

Table 2-17b.   X-divider settings for PFG.

value of the X-field	value of X-divider (*Xv*)
0	1
1	:16

The following restrictions are applicable for the V- and R- fields when programming PFG sampling frequency generator:

$$4 \leq V \leq 511$$

$$1 \leq R \leq 127$$

$$10MHz \leq \frac{50MHz*(V+8)}{(R+2)} \leq 320MHz$$

$$200kHz \leq \frac{25MHz}{(R+2)}$$

CAUTION

The time interval between succeeding settings of V- and R-fields for on-board PFG sampling frequency generator must be 10 mS or greater in order to meet lock time specification for PFG on-chip PLL.

ADC/DAC FIFO and ADC/DAC data acquisition controllers

A/D and D/A data acquisition processes are performed under the control of the corresponding ADC and DAC data acquisition controllers, which are the part of on-board SCU. On-board high-density ADC and DAC FIFO are used to transfer real-time input/output data streams between on-board ADC/DAC and host PIOX-16 interface.

ADC FIFO and ADC data acquisition controller can be configured and controller absolutely independently from DAC FIFO and DAC data acquisition controller.

Figures 2-3a and 2-3b present block-diagrams correspondingly for on-board ADC FIFO and ADC data acquisition controller, and for DAC FIFO and DAC data acquisition controller. Also included is the logic for ADC/DAC IRT controllers, which function together with the corresponding ADC/DAC FIFO and ADC/DAC data acquisition controllers, and are used to transfer real-time data streams between ADC/DAC FIFO and host PIOX-16 interface. For details about ADC IRT and DAC IRT controllers refer to section "ADC IRT and DAC IRT Controllers" later in this chapter.
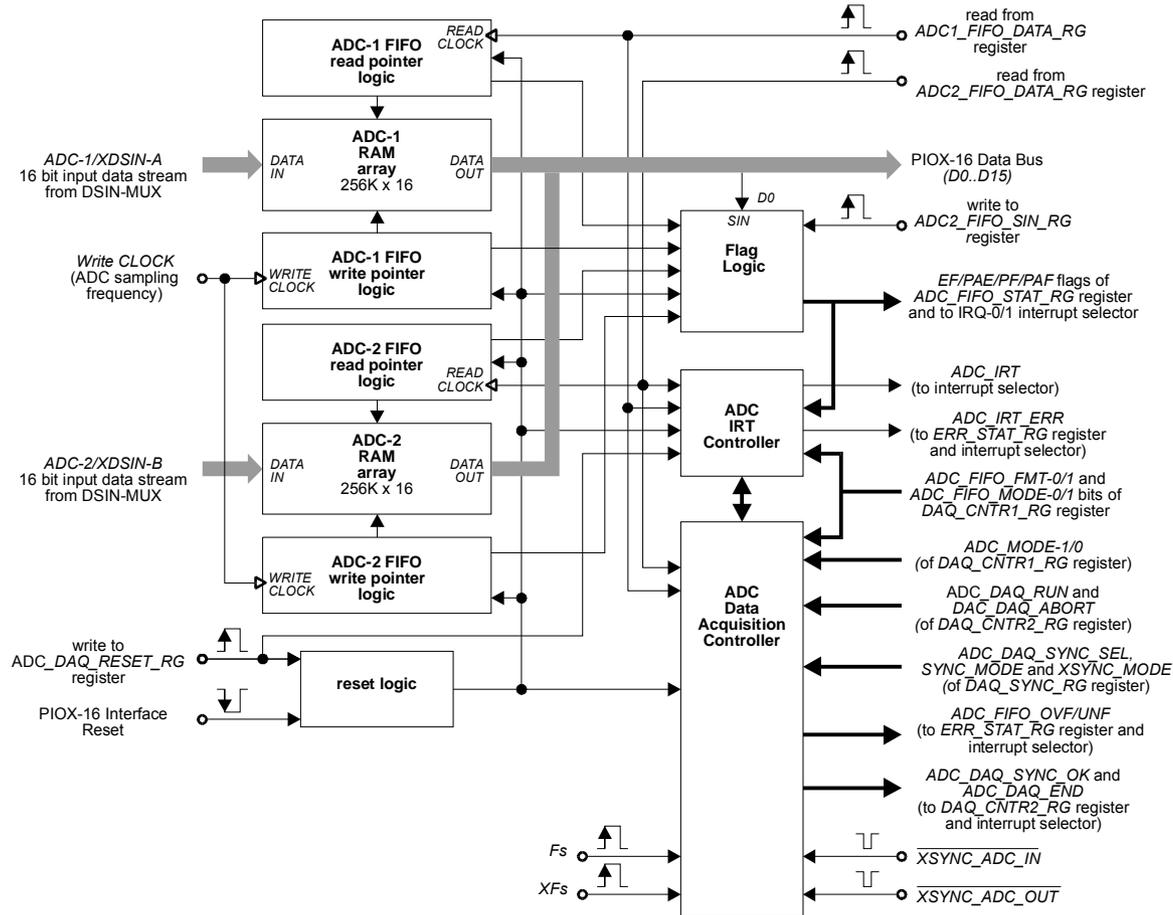
Fig.2-3a. ADC FIFO, ADC data acquisition controller and ADC IRT controller.
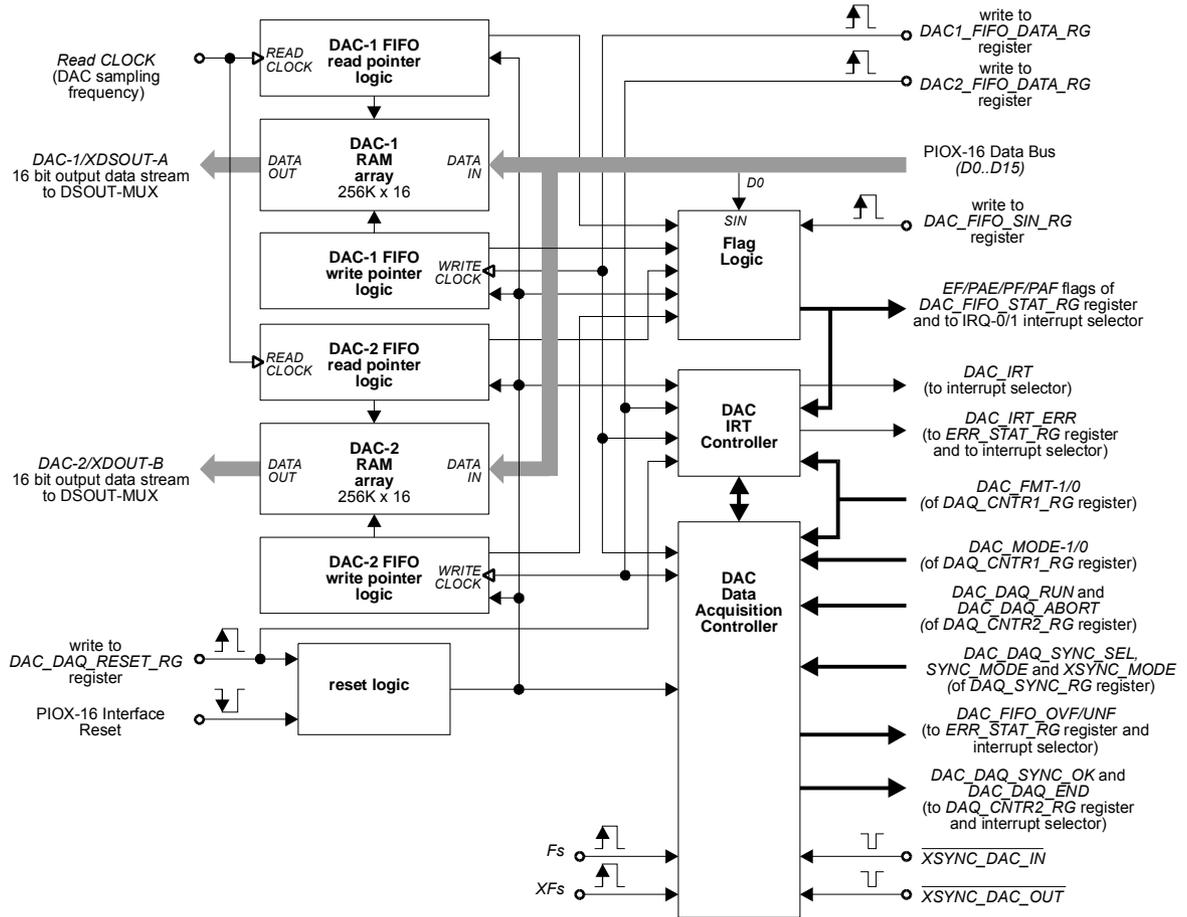
Fig.2-3b. DAC FIFO, DAC data acquisition controller and DAC IRT controller.

ADC/XDSIN input data streams are transferred from either on-board ADC1/ADC2 analog-to-digital converters or 32-bit XDSIN external digital input stream to host PIOX-16 interface via on-board 265Kx32 synchronous ADC FIFO. 32-bit ADC FIFO comprises of 256Kx16 ADC1-FIFO and 256Kx16 ADC2-FIFO, which are used to store 16-bit output sub-streams from the corresponding output of DSIN-MUX input data stream multiplexer. Both ADC1-FIFO and ADC2-FIFO are available for reads from host PIOX-16 interface.

DAC/XDSOUT output data streams are transferred from host PIOX-16 interface to either on-board DAC1/DAC2 digital-to-analog converters or 32-bit XDSOUT external digital output stream via on-board 265Kx32 synchronous DAC FIFO. 32-bit DAC FIFO comprises of 256Kx16 DAC1-FIFO and 256Kx16 DAC2-FIFO, which are used to store 16-bit output sub-streams for the corresponding DSOUT-MUX output data stream multiplexer. Both DAC1-FIFO and DAC2-FIFO are available for writes from host PIOX-16 interface.

Each of the on-board ADC1/ADC2/DAC1/DAC2 FIFO comprises of (256K=262,144)x16 static RAM array with the corresponding read/write pointer logic and programmable FIFO flag logic. ADC/DAC FIFO flag logic generates four output flags, which are used to indicate current FIFO status and to control operation of the

corresponding ADC/DAC data acquisition controller and ADC/DAC IRT controller. For more details about FIFO flag logic refer to the corresponding subsection below.

ADC data acquisition controller can operate in one of the following modes, which are selected via bits {*ADC_MODE-1*, *ADC_MODE-0*} of *DAQ_CNTR1_RG* register (table 2-2):

- *ADC FIFO CONFIGURATION MODE*, which is used to program offsets for ADC FIFO partially empty (PAE) and partially full (PAF) flags, which are used during any of the *ADC OPM* and *ADC PTM* data acquisition modes.
- *ADC OPM* one-pass data acquisition mode, which can be used to acquire and store any specified number of input ADC/XDSIN data stream samples in ADC FIFO RAM array, and further read stored ADC FIFO data by host DSP of host *TORNADO* DSP system/controller. Either host DSP software or ADC IRT controller and host DSP on-chip DMA controllers can be used to transfer stored ADC FIFO data to host DSP environment after *ADC OPM* mode will terminate normally.
- *ADC PTM* pass-through data acquisition mode, which is used to continuously acquire and transfer real-time ADC/XDSIN data stream to host DSP environment of *TORNADO* DSP system/controller via host PIOX-16 interface and ADC FIFO. Either host DSP software or ADC IRT controller and host DSP on-chip DMA controllers shall provide enough performance in order to download ADC FIFO real-time output data stream without ADC FIFO overflow. *ADC PTM* data acquisition mode never terminates until it is aborted via host DSP software.

Correspondingly, DAC data acquisition controller can operate in one of the following modes, which are selected via bits {*DAC_MODE-1*, *DAC_MODE-0*} of *DAQ_CNTR1_RG* register (table 2-2):

- *DAC FIFO CONFIGURATION MODE*, which is used to program offsets for DAC FIFO partially empty (PAE) and partially full (PAF) flags, which are used during any of the *DAC OPM* and *DAC PTM* data acquisition modes.
- *DAC OPM* one-pass data acquisition mode, which can be used to write and store any specified number of input DAC/XDSOUT data stream samples in DAC FIFO RAM array from host DSP of host *TORNADO* DSP system/controller, and further output of stored DAC FIFO data to either DAC or XDSOUT digital output data stream via on-board DSOUT-MUX output data stream multiplexer. Either host DSP software or DAC IRT controller and host DSP on-chip DMA controllers can be used to transfer and store data from host DSP environment to DAC FIFO prior initializing *DAC OPM* mode.
- *DAC PTM* pass-through data acquisition mode, which is used to continuously transfer real-time data stream from host DSP environment of *TORNADO* DSP system/controller to DAC/XDSOUT via host PIOX-16 interface and DAC FIFO. Either host DSP software or DAC IRT controller and host DSP on-chip DMA controllers shall provide enough performance in order to upload real-time output data stream to DAC FIFO without DAC FIFO underflow. *DAC PTM* data acquisition mode never terminates until it is aborted via host DSP software.

ADC FIFO read/write pointer logic, ADC data acquisition controller and ADC IRT controller are activated during any of *ADC OPM* and *ADC PTM* data acquisition modes, and are used to control write to ADC FIFO, read from ADC FIFO via host PIOX-16 interface, and to initialize and terminate ADC data acquisition process.

Correspondingly, DAC FIFO read/write pointer logic, DAC data acquisition controller and DAC IRT controller are activated during any of *DAC OPM* and *DAC PTM* data acquisition modes, and are used to control read from DAC FIFO, write to DAC FIFO via host PIOX-16 interface, and to initialize and terminate DAC data acquisition process.

For more details and timing diagrams for different ADC and DAC data acquisition modes refer to the corresponding subsections below.

The following configuration options are available for ADC and DAC data acquisition controllers, which can be set by host DSP software:

- programmable ADC data format (either ADC1 data only, or ADC2 data only, or ADC1/ADC2 data), which is selected via bits {*ADC_FMT-1*, *ADC_FMT-0*} of *DAQ_CNTR1_RG* register (table 2-2). ADC data format also effects operation of ADC IRT controller. For more details about data formats for ADC data acquisition controller refer to the corresponding subsection later in this section.

- programmable DAC data format (either DAC1 data only, or DAC2 data only, or DAC1/DAC2 data), which is selected via bits {*DAC_FMT-1*, *DAC_FMT-0*} of *DAQ_CNTR1_RG* register (table 2-2). DAC data format also effects operation of DAC IRT controller. For more details about data formats for DAC data acquisition controller refer to the corresponding subsection later in this section.

- programmable AD/DA data acquisition synchronization mode (either MASTER or SLAVE), which is selected common for both ADC and DAC data acquisition controllers via bit *SYNC_MODE* of *DAQ_SYNC_RG* register (table 2-5). MASTER and SLAVE synchronization modes allow to run several *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM synchronously. For more details about MASTER and SLAVE synchronization modes for ADC/DAC data acquisition controllers refer to the corresponding subsection later in this section.

- programmable start-up synchronization (either software or external hardware synchronization) for A/D data acquisition process, which is selected via bit *ADC_DAQ_SYNC_SEL* of *DAQ_SYNC_RG* register (table 2-5) and is used to trigger ADC data acquisition process. Software start-up synchronization allows immediate start of A/D data acquisition process after it has been initialized via setting bit *ADC_DAQ_RUN* of *DAQ_CNTR2_RG* register (table 2-3). Instead, external hardware start-up synchronization allows to trigger the start of A/D data acquisition process from external hardware using XSYNC_ADC_IN input at on-board JP2 connector. Note, that external hardware start-up synchronization can be either edge or level sensitive, which is controlled via bit *XSYNC_MODE* of *DAQ_SYNC_RG* register (table 2-5). For more details about ADC data acquisition start-up synchronization refer to the corresponding subsection later in this section.

- programmable start-up synchronization (either software or external hardware synchronization) for D/A data acquisition process, which is selected via bit *DAC_DAQ_SYNC_SEL* of *DAQ_SYNC_RG* register (table 2-5) and is used to trigger DAC data acquisition process. Software start-up synchronization allows immediate start of D/A data acquisition process after it has been initialized via setting bit *DAC_DAQ_RUN* of *DAQ_CNTR2_RG* register (table 2-3). Instead, external hardware start-up synchronization allows to trigger the start of D/A data acquisition process from external hardware using XSYNC_DAC_IN input at on-board JP2 connector. Note, that external hardware start-up synchronization can be either edge or level sensitive, which is controlled via bit *XSYNC_MODE* of *DAQ_SYNC_RG* register (table 2-5). For more details about DAC data acquisition start-up synchronization refer to the corresponding subsection later in this section.

- programmable external hardware synchronization (either edge or level sensitive) for A/D and D/A data acquisition process, which is selected common for both ADC and DAC external hardware start-up synchronization via bit *XSYNC_MODE* of *DAQ_SYNC_RG* register (table 2-5). Edge sensitive external hardware synchronization will trigger ADC and DAC data acquisition process at the falling edge of XSYNC_ADC_IN input at on-board JP2 connector, whereas level sensitive external hardware synchronization will trigger ADC and DAC data acquisition process at the active low level at XSYNC_ADC_IN input. For more details about external hardware synchronization for ADC and DAC data acquisition controllers refer to the corresponding subsection later in this section.

FIFO flag logic

ADC/DAC FIFO flag logic is used during any of ADC/DAC data acquisition modes in order to terminate the corresponding ADC/DAC FIFO data acquisition process and to monitor FIFO fill-in conditions. FIFO flag logic for each of the ADC/DAC FIFO comprises of the following flags:

- FIFO empty flag (EF)
- FIFO partially empty flag (PAE)
- FIFO full flag (FF)
- FIFO partially full flag (PAF).

FIFO empty flag (EF) for each of the ADC1/ADC2/DAC1/DAC2 FIFO appears for software polling as the corresponding *xxxx_FIFO_EF* bit in read-only *ADC_FIFO_STAT_RG* and *DAC_FIFO_STAT_RG* registers (table 2-7). FIFO EF flag is non-programmable and indicates FIFO empty condition. ADC FIFO EF flags can be used to terminate transmission cycle for ADC IRT controller, whereas DAC FIFO EF flags can be used for normal termination of *DAC OPM* data acquisition process and to initialize transmission cycle for DAC IRT controller. All FIFO EF flags can be also used to generate host PIOX-16 interrupt requests IRQ-0 and IRQ-1 (tables 2-15a).

FIFO partially empty flag (PAE) for each of the ADC1/ADC2/DAC1/DAC2 FIFO appears for software polling as *xxxx_FIFO_PAE* bit in read-only *ADC_FIFO_STAT_RG* and *DAC_FIFO_STAT_RG* registers (table 2-7). FIFO PAE flag can be programmed the corresponding *ADC/DAC FIFO CONFIGURATION MODE* via *ADC_FIFO_SIN_RG* and *DAC_FIFO_SIN_RG* registers (table 2-1). ADC FIFO PAE flags can be used to terminate transmission cycle for ADC IRT controller, whereas DAC FIFO PAE flags can be used for normal termination of *DAC OPM* data acquisition process and to initialize transmission cycle for DAC IRT controller. All FIFO PAE flags can be also used to generate host PIOX-16 interrupt requests IRQ-0 and IRQ-1 (tables 2-15a). In case FIFO PAE flag is not set, then there is more than N unread samples inside bypass FIFO (N is the programmed offset for FIFO PAE flag). In case FIFO PAE flag is set, then there is N or less number of unread samples inside bypass FIFO.

> **CAUTION**
>
> Offset value for FIFO PAE flag is set to default N=1,023 value on the host PIOX-16 reset condition, and can be reprogrammed to any value below 256K=262,144 in the corresponding *ADC/DAC FIFO CONFIGURATION MODE*.

FIFO full flag (FF) for each of the ADC1/ADC2/DAC1/DAC2 FIFO appears for software polling as the corresponding *xxxx_FIFO_FF* bit in read-only *ADC_FIFO_STAT_RG* and *DAC_FIFO_STAT_RG* registers (table 2-7). FIFO FF flag is non-programmable and indicates FIFO full condition. ADC FIFO FF flags can be used for normal termination of *ADC OPM* data acquisition process and to initialize transmission cycle for ADC IRT controller, whereas DAC FIFO FF flags can be used to terminate transmission cycle for DAC IRT controller. All FIFO FF flags can be also used to generate host PIOX-16 interrupt requests IRQ-0 and IRQ-1 (tables 2-15a).

FIFO partially full flag (PAE) for each of the ADC1/ADC2/DAC1/DAC2 FIFO appears for software polling as *xxxx_FIFO_PAF* bit in read-only *ADC_FIFO_STAT_RG* and *DAC_FIFO_STAT_RG* registers (table 2-7). FIFO PAF flag can be programmed the corresponding *ADC/DAC FIFO CONFIGURATION MODE* via *ADC_FIFO_SIN_RG* and *DAC_FIFO_SIN_RG* registers (table 2-1). ADC FIFO PAF flags can be used for normal termination of *ADC OPM* data acquisition process and to initialize transmission cycle for ADC IRT controller, whereas DAC FIFO PAF flags can be used to terminate transmission cycle for DAC IRT controller.

All FIFO PAF flags can be also used to generate host PIOX-16 interrupt requests IRQ-0 and IRQ-1 (tables 2-15a). In case FIFO PAF flag is not set, then there is $(2^{18}-M-1)$ or less number of unread samples inside the corresponding FIFO (M is the programmed offset for FIFO PAF flag). In case FIFO PAF flag is set, then there is $(2^{18}-M)$ or more number of unread samples inside the corresponding FIFO (M is the programmed offset for FIFO PAF flag).

CAUTION

Offset value for FIFO PAF flag is set to default M=1,023 value on the host PIOX-16 reset condition, and can be reprogrammed to any value below 256K=262,144 in the corresponding *ADC/DAC FIFO CONFIGURATION MODE*.

CAUTION

Offset values for FIFO PAE and PAF flags will not change when performing reset of the corresponding data acquisition controllers and FIFO read/write pointer by means of writing to *ADC_DAQ_RESET_RG* and *DAC_DAQ_RESET_RG* register.

Table 2-18 contains description for operation of flag logic for on-board ADC/DAC FIFO during data acquisition modes.

Table 2-18. FIFO flag logic procurement.

Number of words in FIFO	FIFO FF	FIFO PAF	FIFO PAE	FIFO EF
0	0	0	1	1
1 to N	0	0	1	0
(N+1) to (262,144-(M+1))	0	0	0	0
(262,144-M) to 262,143	0	1	0	0
262,144	1	1	0	0

Notes: 1. '*N* ' denotes offset value for FIFO PAE flag.
2. '*M* ' denotes offset value for FIFO PAF flag.

ADC/DAC FIFO Configuration Mode

ADC FIFO CONFIGURATION MODE and *DAC FIFO CONFIGURATION MODE* shall be used to program offset values for the corresponding ADC/DAC FIFO partially empty (PAE) and FIFO partially full (PAF) flags

in case default offset values of FIFO PAE/PAF flags, which are set on the PIOX-16 reset condition, are not desired for user application.

CAUTION

ADC FIFO CONFIGURATION MODE is selected in case {*ADC_MODE-1*, *ADC_MODE-0*} bits of *DAQ_CNTR1_RG* register (table 2-2) are set to the {0,0} state. *ADC FIFO CONFIGURATION MODE* is set as default on PIOX-16 interface reset condition.

DAC FIFO CONFIGURATION MODE is selected in case {*DAC_MODE-1*, *DAC_MODE-0*} bits of *DAQ_CNTR1_RG* register (table 2-2) are set to the {0,0} state. *DAC FIFO CONFIGURATION MODE* is set as default on PIOX-16 interface reset condition.

PAE and PAF flags for ADC and DAC FIFO can be programmed by host DSP software of host *TORNADO* DSP system/controller by means of serial writes to *ADC_FIFO_SIN_RG* and *DAC_FIFO_SIN_RG* registers correspondingly (table 2-11).

CAUTION

Writing to *ADC_FIFO_SIN_RG* register will take effect only in case ADC data acquisition controller has been configured in the *ADC FIFO CONFIGURATION MODE*. PAE/PAF flags for both ADC1-FIFO and ADC2-FIFO will be programmed simultaneously when writing to the *ADC_FIFO_SIN_RG* register.

Writing to *DAC_FIFO_SIN_RG* register will take effect only in case DAC data acquisition controller has been configured in the *DAC FIFO CONFIGURATION MODE*. PAE/PAF flags for both DAC1-FIFO and DAC2-FIFO will be programmed simultaneously when writing to the *DAC_FIFO_SIN_RG* register.

Figures 2-4a and 2-4b provides timing diagrams for programming PAE/PAF flags for ADC and DAC FIFO during *ADC FIFO CONFIGURATION MODE* and *DAC FIFO CONFIGURATION MODE*.
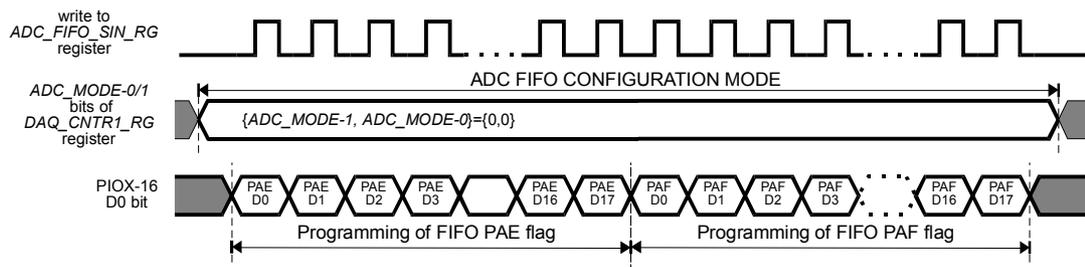

*Fig.2-4a.* Programming of PAE/PAF flags for ADC FIFO.
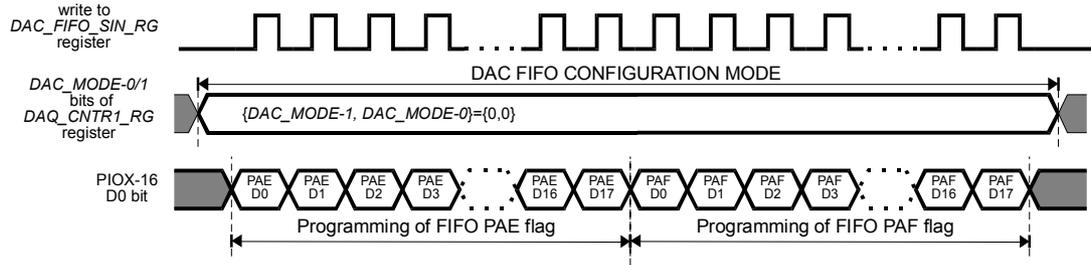
Fig.2-4b. Programming of PAE/PAF flags for DAC FIFO.

After either *ADC FIFO CONFIGURATION MODE* and/or *DAC FIFO CONFIGURATION MODE* has been set by host DSP software, then host DSP software must perform a series of 36 writes to the corresponding either *ADC_FIFO_SIN_RG* and/or *DAC_FIFO_SIN_RG* register in order to program new 18-bit offset values for PAE and PAF flags starting from the least significant bit of offset value for PAE flag and ending with most significant bit of offset value for PAF flag.

CAUTION

When writing to either *ADC_FIFO_SIN_RG* or *DAC_FIFO_SIN_RG* registers in either *ADC FIFO CONFIGURATION MODE* or *DAC FIFO CONFIGURATION MODE*, only D0 data bit of PIOX-16 data bus is valid and is used for serial programming of offset values for PAE and PAF flags of the corresponding FIFO.

CAUTION

New offset values for PAE and PAF flags of ADC1-FIFO and ADC2-FIFO will be set only after the 36-th write to *ADC_FIFO_SIN_RG* register in *ADC FIFO CONFIGURATION MODE.*

New offset values for PAE and PAF flags of DAC1-FIFO and DAC2-FIFO will be set only after the 36-th write to *DAC_FIFO_SIN_RG* register in *DAC FIFO CONFIGURATION MODE.*

It is not possible for DSP software to read back programmed offset values for PAE and PAF flags of ADC FIFO and DAC FIFO.

It is recommended to reset of FIFO logic of ADC FIFO and DAC FIFO prior programming PAE and PAF flags for the corresponding FIFO. This will ensure that internal logic of ADC FIFO and DAC FIFO will correctly interpret external serial programming procedure for PAE/PAF flags as starting from the least significant bit for

PAE flag in order to match serial input data, which will be loaded by host DSP software via *ADC_FIFO_SIN_RG* and *DAC_FIFO_SIN_RG* registers.

CAUTION

Writing to the *ADC_DAQ_RESET_RG* register will reset internal logic of ADC1-FIFO and ADC2-FIFO. Written data is ignored.

Writing to the *DAC_DAQ_RESET_RG* register will reset internal logic of DAC1-FIFO and DAC2-FIFO. Written data is ignored.

Writing to the *DAQ_RESET_RG* register will reset logic for all ADC1/ADC2/DAC1/DAC2-FIFO. Written data is ignored.

ADC OPM one-pass data acquisition mode

ADC OPM one-pass data acquisition mode must be used to acquire and store in the ADC1/ADC2-FIFO any predefined number of samples of either ADC output data stream or XDSIN external digital input stream (via on-board JP3 connector). ADC1-FIFO and ADC2-FIFO data can be further either read by host DSP software or transferred to host DSP environment using ADC IRT controller and host DSP on-chip DMA channel(s).

CAUTION

ADC OPM data acquisition mode is selected in case {*ADC_MODE-1*, *ADC_MODE-0*} bits of *DAQ_CNTR1_RG* register (table 2-2) are set to the {1,1} state.

It is important to note that when configured in *ADC OPM* data acquisition mode, ADC data acquisition controller can run at the sampling frequency as high as 65 MHz. No real-time data transfer is required between *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and host DSP environment via host PIOX-16 interface during *ADC OPM* data acquisition mode.

During *ADC OPM* data acquisition mode ADC1-FIFO and ADC2-FIFO are filled-in with the real-time output data stream from on-board DSIN-MUX input data stream multiplexer (fig.2-1).

ADC OPM data acquisition process is activated by setting *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the *ADC_DAQ_RUN*=1 state. *ADC OPM* data acquisition process either terminates normally on termination flag event, or can be aborted by host DSP software by either setting *ADC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to the *ADC_DAQ_ABORT*=1 state or by resetting ADC data acquisition controller by writing to either *ADC_DAQ_RESET_RG* or *DAQ_RESET_RG* register (written data will be ignored during write to either *ADC_DAQ_RESET_RG* or *DAQ_RESET_RG* register). Normal termination of *ADC OPM* data acquisition process occurs on either FF flag event or PAF flag event of ADC FIFO depending upon the state of the *ADC_DAQ_TF_SEL* bit of *DAQ_CNTR3_RG* register (table 2-4). Particular ADC FIFO (ADC1-FIFO or ADC2-FIFO), which FF/PAF flag is used, is defined by the {*ADC_FMT-1, ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register (table 2-3).

> ### CAUTION
>
> ADC FIFO FF flag must be used as normal termination event for *ADC OPM* data acquisition process in case user application needs to use full FIFO depth (2^{18}=262,144 samples) in order to store input data stream.
>
> Programmable ADC FIFO PAF flag must be used as normal termination event for *ADC OPM* data acquisition process in case user application needs to store short input data streams in ADC FIFO and does not need to use full ADC FIFO depth (2^{18}=262,144 samples).

Timing diagram for *ADC OPM* data acquisition process using normal termination on ADC FIFO PAF flag event is presented at fig. 2-5.
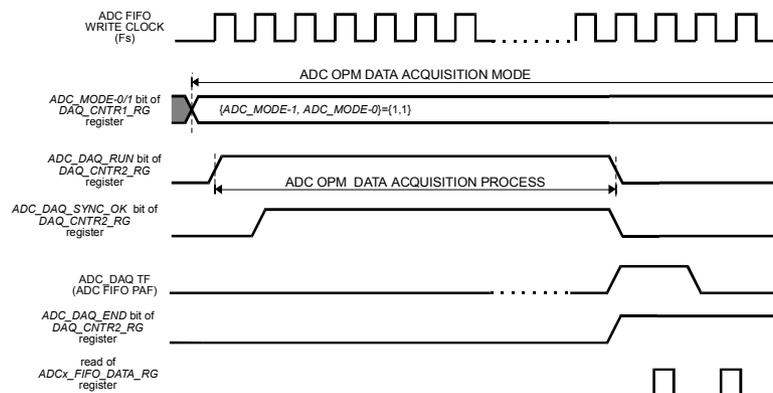
Fig.2-5. Timing diagram for *ADC OPM* data acquisition process.

> ### CAUTION
>
> Timing diagram for *ADC OPM* data acquisition process at fig.2-5 does not provide details about start-up synchronization. For more details refer to the corresponding subsection later in this section.

After *ADC OPM* data acquisition process has been activated by setting *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the *ADC_DAQ_RUN*=1 state and ADC data acquisition start-up synchronization has been confirmed via bit *ADC_DAQ_SYNC_OK* of *DAQ_CNTR2_RG* register (refer to the corresponding subsection later in this section), each A/D sampling period (ADC FIFO write clock) increments ADC1/ADC2-FIFO write pointers, whereas each read cycle of ADC1-FIFO and ADC2-FIFO, which is performed by reading *ADC1_FIFO_DATA_RG* or *ADC2_FIFO_DATA_RG* register correspondingly via host PIOX-16 interface, increments read pointer of the corresponding ADC1/ADC2-FIFO. Note, that all write cycles to ADC1/ADC2-FIFO for *ADC OPM* data acquisition mode are performed during active *ADC OPM* data acquisition process only, whereas reads from ADC1-FIFO and/or ADC2-FIFO can be performed by host DSP software anytime while either *ADC OPM* or *ADC PTM* data acquisition mode is selected.

CAUTION

ADC FIFO PAF flag is synchronous to ADC FIFO write clock during *ADC OPM* data acquisition process, and due to specifics of ADC FIFO synchronization, PAF flag will be set to active state at the 2nd ADC FIFO write clock after actual FIFO PAF condition.

In case it is desired to terminate *ADC OPM* data acquisition process normally at the PAF event after acquiring and storing M samples into ADC FIFO, then the offset value for ADC FIFO PAF flag must be set to the (262,144-M+2) value.

After *ADC OPM* data acquisition process has been terminated normally, then **ADC_DAQ_END** bit of **DAQ_CNTR2_RG** register is set to the '1' state. **ADC_DAQ_END** bit will remain in the '1' state until it will be either reset automatically by initializing new A/D data acquisition process, or can be reset by either setting **ADC_DAQ_ABORT** bit of **DAQ_CNTR2_RG** register to active '1' state, or by resetting ADC data acquisition controller and ADC FIFO logic by writing to either **ADC_DAQ_RESET_RG** or **DAQ_RESET_RG** register (written data will be ignored during write to either **ADC_DAQ_RESET_RG** or **DAQ_RESET_RG** register). Active '1' state of **ADC_DAQ_END** bit of **DAQ_CNTR1_RG** register can be also used to generate host PIOX-16 interrupt (tables 2-15a and 2-15b).

In case it is required to abort currently active *ADC OPM* data acquisition process, then host DSP software must either set the **ADC_DAQ_ABORT** bit of **DAQ_CNTR2_RG** register to active '1' state, or reset ADC data acquisition controller and ADC FIFO logic by writing to either **ADC_DAQ_RESET_RG** or **DAQ_RESET_RG** register (written data will be ignored during write to either **ADC_DAQ_RESET_RG** or **DAQ_RESET_RG** register).

CAUTION

Writing to either **ADC_DAQ_RESET_RG** or **DAQ_RESET_RG** register performs reset of ADC FIFO read and write pointers, thus making stored ADC FIFO data unavailable for read via host PIOX-16 interface.

Instead, abort procedure for *ADC OPM* data acquisition process via setting **ADC_DAQ_ABORT** bit of **DAQ_CNTR2_RG** register will just stop ADC FIFO data acquisition process and freeze last value of ADC FIFO write pointer. Stored ADC FIFO data will remain available for normal read via host PIOX-16 interface. After aborting, the A/D data acquisition process can be restarted by setting **ADC_DAQ_RUN** bit of **DAQ_CNTR2_RG** register to the '1' state.

DAC OPM one-pass data acquisition mode

DAC OPM one-pass data acquisition mode must be used to output any predefined number of samples from DAC1/DAC2-FIFO to either on-board DAC1/DAC2 digital-to-analog converters or XDSOUT external digital output stream (via on-board JP4 connector). DAC1-FIFO and DAC2-FIFO shall be previously uploaded with valid data by either writing from host DSP software or by transferring data from host DSP environment using DAC IRT controller and host DSP on-chip DMA channel(s).

<div style="border: 2px solid black; padding: 10px;">

CAUTION

DAC OPM data acquisition mode is selected in case {*DAC_MODE-1*, *DAC_MODE-0*} bits of *DAQ_CNTR1_RG* register (table 2-2) are set to the {1,1} state.

</div>

It is important to note that when configured in *DAC OPM* data acquisition mode, DAC data acquisition controller can run at the sampling frequency as high as 65 MHz. No real-time data transfer is required between *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and host DSP environment via host PIOX-16 interface during *DAC OPM* data acquisition modes.

DAC OPM data acquisition process is activated by setting *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the *DAC_DAQ_RUN*=1 state. *DAC OPM* data acquisition process either terminates normally on termination flag event, or can be aborted by host DSP software by either setting *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to the *DAC_DAQ_ABORT*=1 state or by resetting DAC data acquisition controller by writing to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register (written data will be ignored during write to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register). Normal termination of *DAC OPM* data acquisition process occurs on either EF flag event or PAE flag event of DAC FIFO depending upon the state of the *DAC_DAQ_TF_SEL* bit of *DAQ_CNTR3_RG* register (table 2-4). Particular DAC FIFO (DAC1-FIFO or DAC2-FIFO), which EF/PAE flag is used, is defined by the {*DAC_FMT-1, DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register (table 2-3).

<div style="border: 2px solid black; padding: 10px;">

CAUTION

DAC FIFO EF flag can be used as normal termination event for *DAC OPM* data acquisition process in case user application needs to output any desired number of samples up to full FIFO depth (2^{18}=262,144 samples) to the corresponding digital-to-analog converter. Host DSP software must write desired number of samples to DAC1-FIFO and DAC2-FIFO prior activating *DAC OPM* data acquisition process.

Programmable DAC FIFO PAE flag must be used as normal termination event for *DAC OPM* data acquisition process in case user application needs to output a fraction of full FIFO depth (2^{18}=262,144 samples) to the corresponding digital-to-analog converter after DAC FIFO has been filled-in with valid data. Host DSP software must fill-in DAC1-FIFO and DAC2-FIFO until they get full prior activating *DAC OPM* data acquisition process.

</div>

Timing diagram for *DAC OPM* data acquisition process using normal termination on DAC FIFO PAE flag event is presented at fig. 2-6.
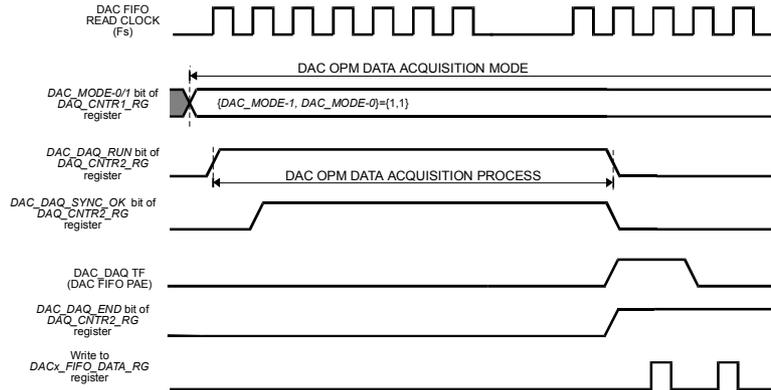
Fig.2-6.   Timing diagram for *DAC OPM* data acquisition process.

CAUTION

Timing diagram for *DAC OPM* data acquisition process at fig.2-6 does not provide details about start-up synchronization. For more details refer to the corresponding subsection later in this section.

After DAC1-FIFO and DAC2-FIFO has been uploaded with valid data and *DAC OPM* data acquisition process has been activated by setting *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the *DAC_DAQ_RUN*=1 state and DAC data acquisition start-up synchronization has been confirmed via bit *DAC_DAQ_SYNC_OK* of *DAQ_CNTR2_RG* register (refer to the corresponding subsection later in this section), each D/A sampling period (DAC FIFO read clock) increments DAC1/DAC2-FIFO read pointers, whereas each write cycle to DAC1-FIFO and ADC2-FIFO, which is performed by writing to the *DAC1_FIFO_DATA_RG* or *DAC2_FIFO_DATA_RG* register correspondingly via host PIOX-16 interface, increments write pointer of the corresponding DAC1/DAC2-FIFO. Note, that all read cycles from DAC1/DAC2-FIFO for *DAC OPM* data acquisition mode are performed during active *DAC OPM* data acquisition process only, whereas writes to DAC1-FIFO and/or DAC2-FIFO can be performed by host DSP software anytime while either *DAC OPM* or *DAC PTM* data acquisition mode is selected.

CAUTION

DAC FIFO PAE flag is synchronous to DAC FIFO read clock during *DAC OPM* data acquisition process, and due to specifics of DAC FIFO synchronization, PAE flag will be set to active state at the 2nd DAC FIFO read clock after actual FIFO PAE condition.

In case it is desired to terminate *DAC OPM* data acquisition process normally at the PAE event after output of N samples from DAC FIFO, then the offset value for DAC FIFO PAE flag must be set to the (N-2) value.

After *DAC OPM* data acquisition process has been terminated normally, then *DAC_DAQ_END* bit of *DAQ_CNTR2_RG* register is set to the '1' state. *DAC_DAQ_END* bit will remain in the '1' state until it will be either reset automatically by initializing new D/A data acquisition process, or can be reset by either setting *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to active '1' state, or by resetting DAC data acquisition controller and DAC FIFO logic by writing to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register (written data will be ignored during write to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register). Active '1' state of *DAC_DAQ_END* bit of *DAQ_CNTR1_RG* register can be also used to generate host PIOX-16 interrupt (tables 2-15a and 2-15b).

In case it is required to abort currently active *DAC OPM* data acquisition process, then host DSP software must either set the *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to active '1' state, or reset DAC data acquisition controller and DAC FIFO logic by writing to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register (written data will be ignored during write to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register).

CAUTION

Writing to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register performs reset of DAC FIFO read and write pointers, thus making stored DAC FIFO data unavailable for further output to DAC/XDSOUT.

Instead, abort procedure for *DAC OPM* data acquisition process via setting *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register will just stop DAC FIFO data acquisition process and freeze last value of DAC FIFO read pointer. Unread DAC FIFO data will still remain available for output to DAC/XDSOUT. After aborting, the D/A data acquisition process can be restarted by setting *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register to the '1' state.

ADC PTM pass-through data acquisition mode

ADC PTM pass-through data acquisition mode must be used to continuously acquire and transfer real-time either ADC output data stream or XDSIN external digital input stream (via on-board JP3 connector) to host DSP environment via ADC1-FIFO and ADC2-FIFO.

> ### CAUTION
>
> *ADC PTM* data acquisition mode is selected in case {*ADC_MODE-1*, *ADC_MODE-0*} bits of *DAQ_CNTR1_RG* register (table 2-2) are set to the {1,0} state.

Real-time data transfer is required between *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and host DSP environment via host PIOX-16 interface during *ADC PTM* data acquisition mode in order to download real-time ADC1-FIFO and ADC2-FIFO data and to exclude ADC FIFO overflow. Real-time ADC1-FIFO and ADC2-FIFO output data can be either read by host DSP software or transferred to host DSP environment using ADC IRT controller and host DSP on-chip DMA channel(s).

It is important to note that when configured in *ADC PTM* data acquisition mode, ADC data acquisition controller can theoretically run at the sampling frequency as high as 65 MHz, however high sampling frequency may result in ADC FIFO overflow since host PIOX-16 interface and host DSP software might be not able to provide enough performance in order to download real-time ADC1-FIFO and ADC2-FIFO data without ADC FIFO overflow.

During *ADC PTM* data acquisition mode ADC1-FIFO and ADC2-FIFO are filled-in with the real-time output data stream from on-board DSIN-MUX input data stream multiplexer (fig.2-1).

ADC PTM data acquisition process is activated by setting *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the *ADC_DAQ_RUN*=1 state. *ADC PTM* data acquisition process never terminates itself until is aborted by host DSP software by either setting *ADC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to the *ADC_DAQ_ABORT*=1 state or by resetting ADC data acquisition controller by writing to either *ADC_DAQ_RESET_RG* or *DAQ_RESET_RG* register (written data will be ignored during write to either *ADC_DAQ_RESET_RG* or *DAQ_RESET_RG* register).

Timing diagram for *ADC PTM* data acquisition process is presented at fig. 2-7.
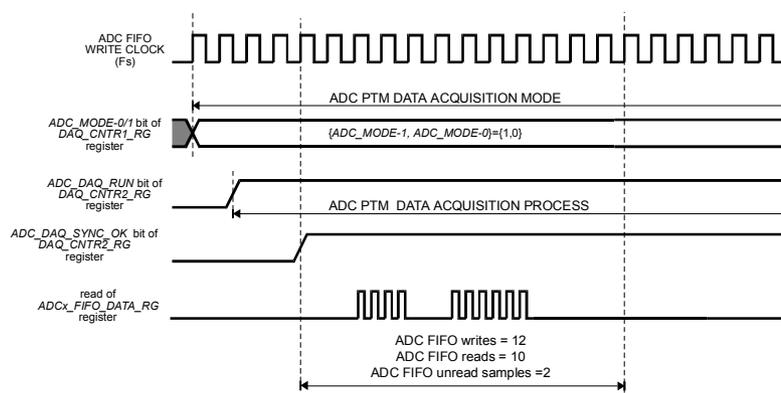
Fig. 2-7. Timing diagram for *ADC PTM* data acquisition process.

CAUTION

Timing diagram for *ADC PTM* data acquisition process at fig.2-7 does not provide details about start-up synchronization. For more details refer to the corresponding subsection later in this section.

After *ADC PTM* data acquisition process has been activated by setting *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the *ADC_DAQ_RUN*=1 state and ADC data acquisition start-up synchronization has been confirmed via bit *ADC_DAQ_SYNC_OK* of *DAQ_CNTR2_RG* register (refer to the corresponding subsection later in this section), each A/D sampling period (ADC FIFO write clock) increments ADC1/ADC2-FIFO write pointers, whereas each read cycle of ADC1-FIFO and ADC2-FIFO, which is performed by reading *ADC1_FIFO_DATA_RG* or *ADC2_FIFO_DATA_RG* register correspondingly via host PIOX-16 interface, increments read pointer of the corresponding ADC1/ADC2-FIFO.

Since all write and read cycles to/from ADC1-FIFO and ADC2-FIFO for *ADC PTM* data acquisition mode are performed in real-time during active *ADC PTM* data acquisition process, then this can result in ADC FIFO error conditions in case the performance of input data stream for ADC FIFO is not balanced with the performance of ADC FIFO output stream. In order host DSP software can take care of ADC FIFO error conditions and perform the corresponding fix-up actions, *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM on-board hardware provides real-time tracking of the following ADC data acquisition error conditions:

- ADC FIFO overflow, which appears as *ADC_FIFO_OVF* bit in *ERR_STAT_RG* register (table 2-8) and is set in case write operation is performed to full ADC FIFO
- ADC FIFO underflow, which appears as *ADC_FIFO_UVF* bit in *ERR_STAT_RG* register (table 2-8) and is set in case read operation is performed from empty ADC FIFO.

CAUTION

Neither of active ADC data acquisition error conditions do not terminate *ADC PTM* data acquisition process.

ADC data acquisition error bits are available for software polling via *ERR_STAT_RG* register and can generate host PIOX-16 interrupts to host DSP (refer to tables 2-15a and 2-15b). For more details about ADC data acquisition errors refer to the corresponding subsection below.

In case it is required to abort currently active *ADC PTM* data acquisition process, then host DSP software must either set the *ADC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to active '1' state, or reset ADC data acquisition controller and ADC FIFO logic by writing to either *ADC_DAQ_RESET_RG* or *DAQ_RESET_RG* register (written data will be ignored during write to either *ADC_DAQ_RESET_RG* or *DAQ_RESET_RG* register).

> **CAUTION**
>
> Writing to either *ADC_DAQ_RESET_RG* or *DAQ_RESET_RG* register performs reset of ADC FIFO read and write pointers, thus making stored ADC FIFO data unavailable for read via host PIOX-16 interface.
>
> Instead, abort procedure for *ADC PTM* data acquisition process via setting *ADC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register will just stop ADC FIFO data acquisition process and freeze last value of ADC FIFO write pointer. Stored ADC FIFO data will remain available for normal read via host PIOX-16 interface. After aborting, the A/D data acquisition process can be restarted by setting *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register to the '1' state.

DAC PTM pass-through data acquisition mode

DAC PTM pass-through data acquisition mode must be used to continuously transfer real-time data from host DSP environment to on-board DAC1/DAC2 digital-to-analog converters or XDSOUT external digital output stream (via on-board JP4 connector) via DAC1-FIFO and DAC2-FIFO.

> **CAUTION**
>
> *DAC PTM* data acquisition mode is selected in case {*DAC_MODE-1*, *DAC_MODE-0*} bits of *DAQ_CNTR1_RG* register (table 2-2) are set to the {1,0} state.

Real-time data transfer is required between *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and host DSP environment via host PIOX-16 interface during *DAC PTM* data acquisition mode in order to upload real-time data to DAC1-FIFO and DAC2-FIFO and to exclude DAC FIFO underflow. Real-time DAC1-FIFO and DAC2-FIFO input data can be either written by host DSP software or transferred from host DSP environment using DAC IRT controller and host DSP on-chip DMA channel(s).

It is important to note that when configured in *DAC PTM* data acquisition mode, DAC data acquisition controller can theoretically run at the sampling frequency as high as 65 MHz, however high sampling frequency may result in DAC FIFO underflow since host PIOX-16 interface and host DSP software might be not able to provide enough performance in order to upload real-time data to DAC1-FIFO and DAC2-FIFO without DAC FIFO underflow.

DAC PTM data acquisition process is activated by setting *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the *DAC_DAQ_RUN*=1 state. *DAC PTM* data acquisition process never terminates itself until it is aborted by host DSP software by either setting *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to the *DAC_DAQ_ABORT*=1 state or by resetting DAC data acquisition controller by writing to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register (written data will be ignored during write to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register).

Timing diagram for *DAC PTM* data acquisition process is presented at fig. 2-8.
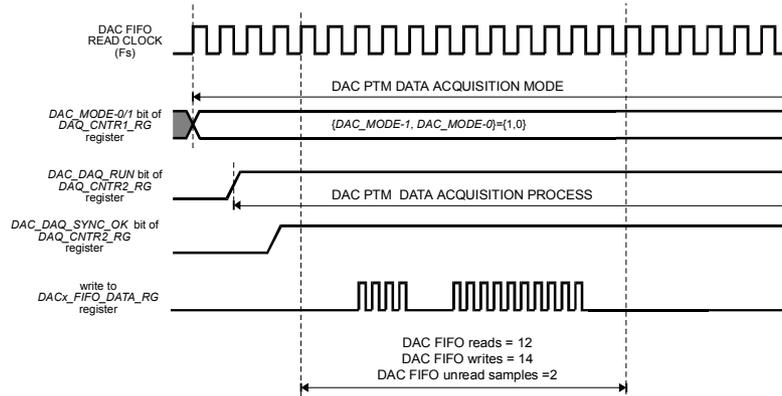
Fig.2-8. Timing diagram for *DAC PTM* data acquisition process.

CAUTION

Timing diagram for *DAC PTM* data acquisition process at fig.2-8 does not provide details about start-up synchronization. For more details refer to the corresponding subsection later in this section.

After *DAC PTM* data acquisition process has been activated by setting *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the '1' state and DAC data acquisition start-up synchronization has been confirmed via bit *DAC_DAQ_SYNC_OK* of *DAQ_CNTR2_RG* register (refer to the corresponding subsection later in this section), each A/D sampling period (DAC FIFO read clock) increments DAC1/DAC2-FIFO read pointers, whereas each write cycle to DAC1-FIFO and DAC2-FIFO, which is performed by writing to *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* register correspondingly via host PIOX-16 interface, increments write pointer of the corresponding DAC1/DAC2-FIFO.

Since all write and read cycles to/from DAC1-FIFO and DAC2-FIFO for *DAC PTM* data acquisition mode are performed in real-time during active *DAC PTM* data acquisition process, then this can result in DAC FIFO error conditions in case the performance of input data stream for DAC FIFO is not balanced with the performance of DAC FIFO output stream. In order host DSP software can take care of DAC FIFO error conditions and perform the corresponding fix-up actions, *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM on-board hardware provides real-time tracking of the following DAC data acquisition error conditions:

- DAC FIFO overflow, which appears as *DAC_FIFO_OVF* bit in *ERR_STAT_RG* register (table 2-8) and is set in case write operation is performed to full DAC FIFO
- DAC FIFO underflow, which appears as *DAC_FIFO_UVF* bit in *ERR_STAT_RG* register (table 2-8) and is set in case read operation is performed from empty DAC FIFO.

CAUTION

Neither of active DAC data acquisition error conditions do not terminate
DAC PTM data acquisition process.

DAC data acquisition error bits are available for software polling via *ERR_STAT_RG* register and can generate host PIOX-16 interrupts to host DSP (refer to tables 2-15a and 2-15b). For more details about DAC data acquisition errors refer to the corresponding subsection below.

In case it is required to abort currently active *DAC PTM* data acquisition process, then host DSP software must either set the *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register to active '1' state, or reset ADC data acquisition controller and DAC FIFO logic by writing to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register (written data will be ignored during write to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register).

CAUTION

Writing to either *DAC_DAQ_RESET_RG* or *DAQ_RESET_RG* register performs reset of DAC FIFO read and write pointers, thus making stored DAC FIFO data unavailable for further output to DAC/XDSOUT.

Instead, abort procedure for *DAC PTM* data acquisition process via setting *DAC_DAQ_ABORT* bit of *DAQ_CNTR2_RG* register will just stop DAC FIFO data acquisition process and freeze last value of DAC FIFO read pointer. Unread DAC FIFO data will still remain available for output to DAC/XDSOUT. After aborting, the D/A data acquisition process can be restarted by setting *DAC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register to the '1' state.

Master/Slave synchronization modes

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM can operate in *MASTER* and *SLAVE* synchronization modes, which allow to synchronize A/D and D/A data acquisition processes on multiple *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, which are installed on different *TORNADO* DSP systems/controllers, in order to increase number of synchronously working A/D and D/A channels.

CAUTION

MASTER and SLAVE synchronization modes are set common to both ADC data acquisition controller and DAC data acquisition controller.

Selection of MASTER/SLAVE synchronization mode for ADC and DAC data acquisition controllers is performed via bit *SYNC_MODE* bit of *DAQ_SYNC_RG* register (table 2-5) as the following:

- MASTER synchronization mode is selected in case *SYNC_MODE* bit of *DAQ_SYNC_RG* register is set to the '0' state, which is also the default setting on the PIOX-16 interface reset condition
- SLAVE synchronization mode is selected in case *SYNC_MODE* bit of *DAQ_SYNC_RG* register is set to the '1' state.

In case *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is configured in *MASTER* synchronization mode, then the following configuration options can be programmed via host DSP software for this DCM:

- sampling frequency for both ADC and DAC data acquisition controllers can be selected from a variety of sources via bits {*FS_SEL-1*, *FS_SEL-0*} of *DAQ_SYNC_RG* register (table 2-5) as it is described earlier in this section
- either software or external hardware start-up synchronization mode can be selected separately for ADC and DAC data acquisition controllers via bits *ADC_DAQ_SYNC_SEL* and *DAC_DAQ_SYNC_SEL* of *DAQ_SYNC_RG* register (table 2-5) as it is described below in this subsection
- either active low or falling edge synchronization event for external hardware start-up synchronization modes can be selected common for both ADC and DAC data acquisition controllers via bit *XSYNC_MODE* of *DAQ_SYNC_RG* register (table 2-5) as it is described below in this subsection.

In case *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is configured in *SLAVE* synchronization mode, then this DCM is assumed to be synchronized by external MASTER and the following restrictions apply to this DCM:

- sampling frequency for ADC and DAC data acquisition controllers of SLAVE is sourced from the input pin XFS of on-board JP2 connector with the bits {*FS_SEL-1*, *FS_SEL-0*} of *DAQ_SYNC_RG* register (table 2-5) being ignored. XFS input pin of SLAVE on-board JP2 connector must be connected to FS_OUT output pin of MASTER on-board JP2 connector.
- external hardware start-up synchronization via input pins XSYNC_ADC_IN and XSYNC_DAC_IN of on-board JP2 connector is being used for ADC and DAC data acquisition controllers correspondingly with the bits *ADC_DAQ_SYNC_SEL* and *DAC_DAQ_SYNC_SEL* of *DAQ_SYNC_RG* register (table 2-5) being ignored. XSYNC_ADC_IN and XSYNC_DAC_IN input pins of SLAVE on-board JP2 connector must be connected to XSYNC_ADC_OUT and XSYNC_DAC_OUT output pins of MASTER on-board JP2 connector.
- active low synchronization event for external hardware start-up synchronization is selected for both ADC and DAC data acquisition controllers with the bit *XSYNC_MODE* of *DAQ_SYNC_RG* register (table 2-5) being ignored.

Figure 2-9 presents MASTER-SLAVE connection diagram for several *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, which are installed onto different *TORNADO* DSP systems/controllers.
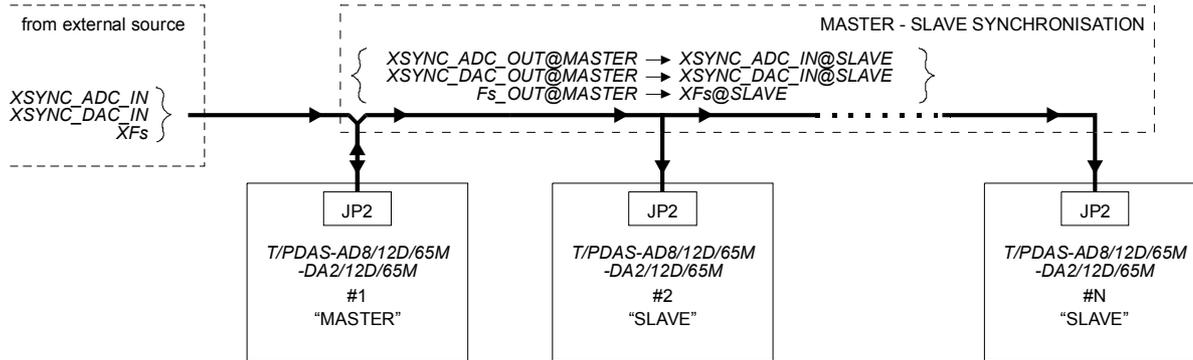
Fig.2-9.   MASTER-SLAVE connection diagram.

The timing diagrams for MASTER and SLAVE synchronization modes of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM are described below in subsection "Data acquisition start-up synchronization" below in this section.

CAUTION

MASTER-SLAVE connection of several *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM provides synchronous start-up of A/D data acquisition processes and D/A data acquisition processes for all DCM in case all DCM has been configured in the corresponding ADC and DAC data acquisition modes the corresponding ADC and DAC data acquisition processes for all SLAVE DCM have been initialized by setting the corresponding *xxx_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the '1' state.

Particular settings for ADC data acquisition modes and DAC data acquisition modes, as well as the number of acquired ADC/XDSIN data stream samples and number of output DAC/XDSOUT data stream samples correspondingly may be set different for different *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

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data acquisition start-up synchronization

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM provides a variety of start-up synchronization modes, which can be selected individually for ADC data acquisition controller and DAC data acquisition controller via host DSP software. Start-up synchronization is required to trigger the start instants of A/D and D/A data acquisition processes and to allow to synchronize to external hardware.

> **CAUTION**
>
> Selection of start-up synchronization mode for *T/PDAS-AD8/12D/65M-DA2/12D/65M*
> DCM is available in MASTER synchronization mode only.

Selection of start-up synchronization mode by host DSP software for ADC data acquisition controller in MASTER synchronization mode is performed via bit *ADC_DAQ_SYNC_SEL* of *DAQ_SYNC_RG* register (table 2-5) as the following:

- in case *ADC_DAQ_SYNC_SEL* bit is set to the '0' state, then *software start-up synchronization* is used to trigger the start instant of A/D data acquisition process
- in case *ADC_DAQ_SYNC_SEL* bit is set to the '1' state, then *external hardware synchronization* from the input pin XSYNC_ADC_IN of on-board JP2 connector is used to trigger the start instant of A/D data acquisition process.

Correspondingly, selection of start-up synchronization mode by host DSP software for DAC data acquisition controller in MASTER synchronization mode is performed via bit *DAC_DAQ_SYNC_SEL* of *DAQ_SYNC_RG* register (table 2-5) as the following:

- in case *DAC_DAQ_SYNC_SEL* bit is set to the '0' state, then *software start-up synchronization* is used to trigger the start instant of D/A data acquisition process
- in case *DAC_DAQ_SYNC_SEL* bit is set to the '1' state, then *external hardware synchronization* from the input pin XSYNC_DAC_IN of on-board JP2 connector is used to trigger the start instant of D/A data acquisition process.

Software start-up synchronization in MASTER synchronization mode must be used in case the corresponding data acquisition process in either *OPM* or *PTM* data acquisition mode can be started immediately after host DSP software sets the corresponding *xxx_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the '1' state without need to synchronize to external hardware.

Figures 2-10a and 2-10b presents timing diagrams for software start-up synchronization timing for A/D and D/A data acquisition processes in *ADC OPM* and *DAC OPM* data acquisition modes correspondingly for the *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM configured in MASTER synchronization mode.
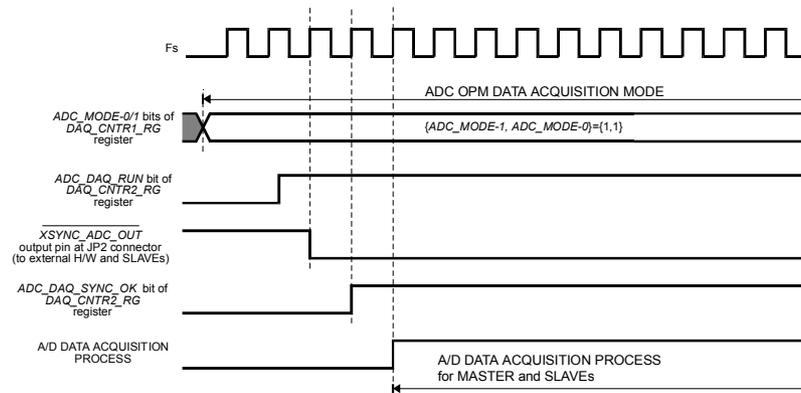

Fig.2-10a.   Timing diagram for software start-up synchronization for *ADC OPM* data acquisition process in MASTER synchronization mode.
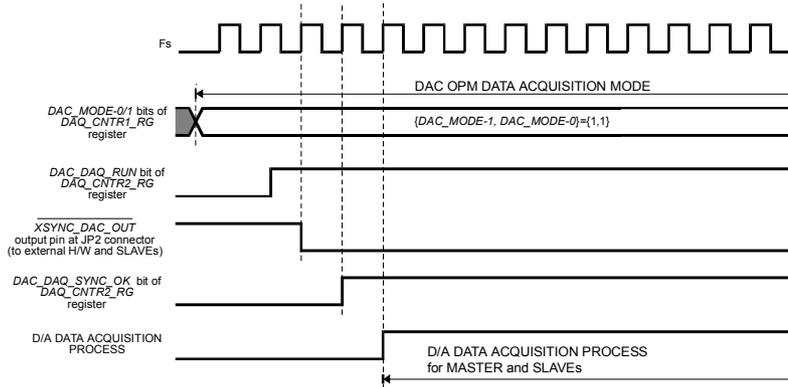
Fig.2-10b. Timing diagram for software start-up synchronization for *DAC OPM* data acquisition process in MASTER synchronization mode.

Below is a brief description of how *software start-up synchronization* works for A/D data acquisition process in MASTER synchronization mode. *Software hardware start-up synchronization* for D/A data acquisition process in MASTER synchronization mode is similar to that for A/D data acquisition process.

After A/D data acquisition process has been initialized via host DSP software by setting bit *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the '1' state, then this is accepted as active start-up synchronization event by ADC data acquisition controller. After the start-up synchronization event for A/D data acquisition process has been detected, the XSYNC_ADC_OUT pin of on-board JP2 connector will immediately go to the active low state in order to synchronize external h/w and all *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, which are configured in the SLAVE synchronization mode. At the next sampling frequency pulse the read-only *ADC_DAQ_SYNC_OK* bit of *DAQ_CNTR2_RG* register (table 2-3) will be set to the '1' state in order to indicate detected start-up synchronization to host DSP software. Actual A/D data acquisition process will start at the next sampling frequency pulse after the *ADC_DAQ_SYNC_OK* bit of *DAQ_CNTR2_RG* register (table 2-3) will go to the '1' state.

External hardware start-up synchronization in MASTER synchronization mode must be used in case the start instant of the corresponding data acquisition process in either *OPM* or *PTM* data acquisition mode must be synchronized to any external hardware event. External triggering of the start instant of ADC and DAC data acquisition processes is performed via XSYNC_ADC_IN and XSYNC_DAC_IN input pins correspondingly, which are available at on-board JP2 connector.

In case external hardware start-up synchronization has been selected in MASTER synchronization mode, then the synchronization event at the XSYNC_ADC_IN and XSYNC_DAC_IN input pins of on-board JP2 connector can be software selected via bit *XSYNC_MODE* of *DAQ_SYNC_RG* register (table 2-5) as the following:
- in case *XSYNC_MODE* bit is set to the '0' state, then *active low external hardware start-up synchronization event* is selected to detect the start instants for both ADC and DAC data acquisition controllers. This setting is default for PIOX-16 interface reset condition.
- in case *XSYNC_MODE* bit is set to the '1' state, then *falling edge external hardware start-up synchronization event* is selected to detect the start instants for both ADC and DAC data acquisition controllers.

Figures 2-11 presents timing diagrams for external hardware start-up synchronization timing for A/D and D/A data acquisition processes in *ADC OPM* and *DAC OPM* data acquisition modes correspondingly for the

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM configured in MASTER synchronization mode. Presented are timing diagrams for active low and falling edge external hardware synchronization events.
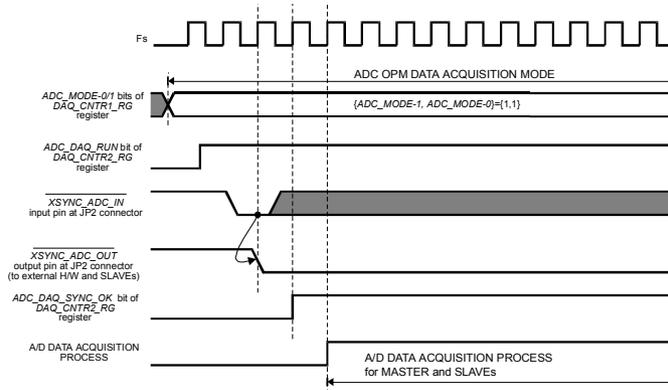
Fig.2-11a. Timing diagram for active low external hardware start-up synchronization for *ADC OPM* data acquisition process in MASTER synchronization mode.
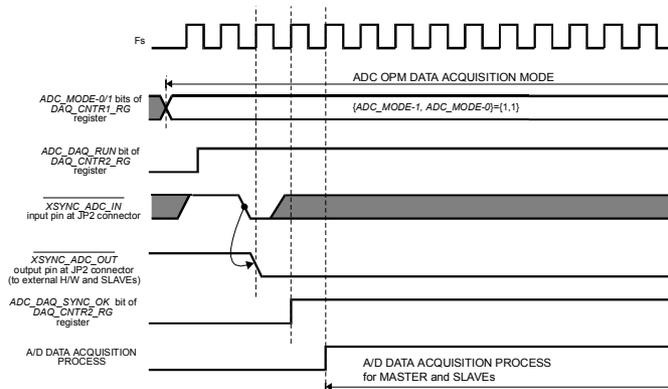
Fig.2-11b. Timing diagram for falling edge sensitive external hardware start-up synchronization for *ADC OPM* data acquisition process in MASTER synchronization mode.
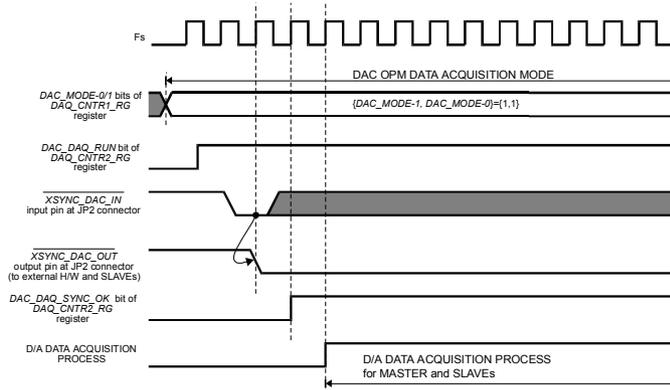
Fig.2-11c.   Timing diagram for active low external hardware start-up synchronization for *DAC OPM* data acquisition process in MASTER synchronization mode.
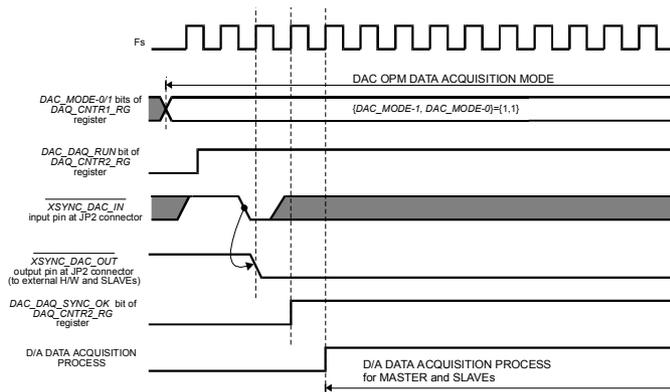

Fig.2-11d.   Timing diagram for falling edge sensitive external hardware start-up synchronization for *DAC OPM* data acquisition process in MASTER synchronization mode.

Below is a brief description of how *external hardware start-up synchronization* works for A/D data acquisition process in MASTER synchronization mode. *External hardware start-up synchronization* for D/A data acquisition process in MASTER synchronization mode is similar to that for A/D data acquisition process.

After A/D data acquisition process has been initialized via host DSP software by setting bit *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the '1' state, then ADC data acquisition controller starts monitoring the state of XSYNC_ADC_IN pin of on-board JP2 connector. In case *active low external hardware start-up synchronization event* is selected by setting bit *XSYNC_MODE* of *DAQ_SYNC_RG* register to the '0' state, then external hardware synchronization event for A/D data acquisition process will be detected at the first rising edge of sampling frequency pulse with the XSYNC_ADC_IN pin of on-board JP2 connector being set to the '0' state by external hardware (fig.2-11a). Correspondingly, in case *falling edge external hardware start-up synchronization event* is selected by setting bit *XSYNC_MODE* of *DAQ_SYNC_RG* register to the '1' state, then external hardware synchronization event for A/D data acquisition process will be detected at the first rising edge of sampling frequency pulse after the falling edge at the XSYNC_ADC_IN pin of on-board JP2

connector (fig.2-11b). Note, that after the external hardware synchronization event for A/D data acquisition process has been detected, the XSYNC_ADC_IN pin of on-board JP2 connector can change its state without any effect to the progress of A/D data acquisition process. After the external hardware synchronization event for A/D data acquisition process has been detected, the XSYNC_ADC_OUT pin of on-board JP2 connector will immediately go to the active low state in order to synchronize external h/w and all *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, which are configured in the SLAVE synchronization mode. At the next sampling frequency pulse the read-only *ADC_DAQ_SYNC_OK* bit of *DAQ_CNTR2_RG* register (table 2-3) will be set to the '1' state in order to indicate detected start-up synchronization to host DSP software. Actual A/D data acquisition process will start at the next sampling frequency pulse after the *ADC_DAQ_SYNC_OK* bit of *DAQ_CNTR2_RG* register (table 2-3) will go to the '1' state.

In case *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is configured in *SLAVE* synchronization mode, then this DCM is assumed to be synchronized by external MASTER (fig.2-9), and the on-board SLAVE hardware will automatically configure ADC and DAC data acquisition controllers as the following:

- sampling frequency for ADC and DAC data acquisition controllers of SLAVE is sourced from the input pin XFS of on-board JP2 connector. XFS input pin of SLAVE on-board JP2 connector must be connected to FS_OUT output pin of MASTER on-board JP2 connector.
- external active low hardware start-up synchronization via input pins XSYNC_ADC_IN and XSYNC_DAC_IN of on-board JP2 connector is being used for ADC and DAC data acquisition controllers correspondingly. XSYNC_ADC_IN and XSYNC_DAC_IN input pins of SLAVE on-board JP2 connector must be connected to XSYNC_ADC_OUT and XSYNC_DAC_OUT output pins of MASTER on-board JP2 connector.

The timing diagrams of start-up synchronization for A/D and D/A data acquisition processes in SLAVE synchronization mode (fig.2-12a and 2-12b) are very similar to that for active low external hardware start-up synchronization in MASTER synchronization mode.
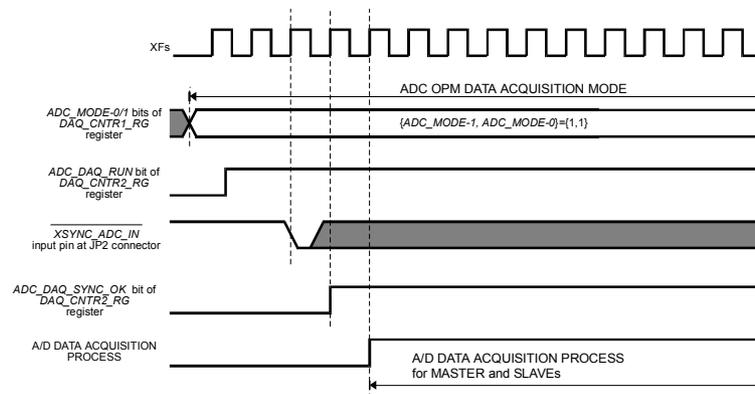

Fig.2-12a. Timing diagram for start-up synchronization for *ADC OPM* data acquisition process in SLAVE synchronization mode.
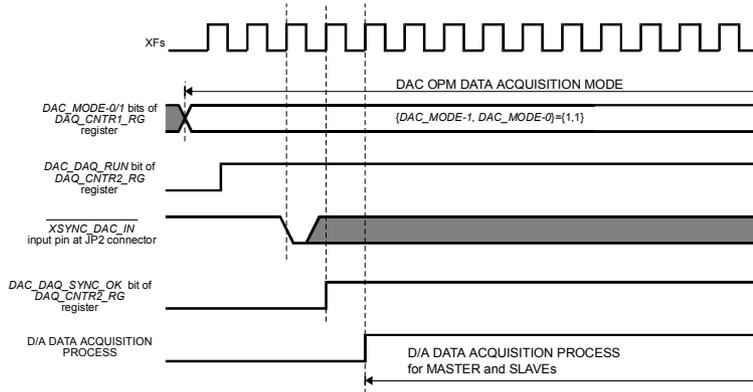
Fig.2-12b.   Timing diagram for start-up synchronization for *DAC OPM* data acquisition process in
SLAVE synchronization mode.

Below is a brief description of how start-up synchronization works for A/D data acquisition process in SLAVE synchronization mode. Start-up synchronization for D/A data acquisition process in SLAVE synchronization mode is similar to that for A/D data acquisition process.

After A/D data acquisition process in SLAVE has been initialized via host DSP software by setting bit *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the '1' state, then ADC data acquisition controller starts monitoring the state of XSYNC_ADC_IN pin of on-board JP2 connector for the active low start-up synchronization event.

Note, that since XSYNC_ADC_IN input pin of on-board JP2 connector of SLAVE is connected to the XSYNC_ADC_OUT output pin of on-board JP2 connector of MASTER, and the sampling frequency of SLAVE is sourced from external sampling frequency input at the XFS input pin of on-board JP2 connector of SLAVE, which is connected to the FS_OUT input pin of on-board JP2 connector of MASTER, then the XSYNC_ADC_IN input pin of on-board JP2 connector of SLAVE is already synchronized to the rising edge of external sampling frequency pulse at XFS input pin of on-board JP2 connector of SLAVE.

Once active low external hardware synchronization event for A/D data acquisition process has been be detected at the first rising edge of XFS external sampling frequency pulse, then the read-only *ADC_DAQ_SYNC_OK* bit of *DAQ_CNTR2_RG* register (table 2-3) of SLAVE will be set to the '1' state at the next XFS sampling frequency pulse in order to indicate detected SLAVE start-up synchronization to host DSP software. Actual A/D data acquisition process for SLAVE will start synchronously with that for the MASTER at the next XFS sampling frequency pulse after the *ADC_DAQ_SYNC_OK* bit of *DAQ_CNTR2_RG* register (table 2-3) will go to the '1' state.

XDSIN and XDSOUT external digital I/O data streams

In case the *DSIN_SEL* bit of *DAQ_MUX_RG* register (table 2-6) is set to the '1' state by host DSP software, then this configures on-board DSIN-MUX input data streams multiplexer of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM to route 32-bit XDSIN external digital input stream from on-board JP3 connector (fig. A-3) instead of the ADC1/ADC2 output data to the input of ADC FIFO.

Correspondingly, in case the *DSOUT_SEL* bit of *DAQ_MUX_RG* register (table 2-6) is set to the '1' state by host DSP software, then this configures on-board DSOUT-MUX output data streams multiplexer of *T/PDAS-*

AD8/12D/65M-DA2/12D/65M DCM to route to the output data of DAC FIFO to the 32-bit XDSOUT external digital output stream at on-board JP4 connector (fig.A-4) instead of the DAC1/DAC2 input data.

Both XDSIN and XDSOUT external digital I/O streams are actually the 32-bit synchronous parallel digital I/O ports, which are synchronized to on-board A/D and D/A data acquisition processes in case the latter are activated. Once selected for external digital I/O, XDSIN and XDSOUT external digital I/O streams appear as just the replacements for ADC output data stream and DAC digital input data correspondingly.

CAUTION

External digital I/O data of XDSIN external digital input stream are sampled at the rising edge of each sampling frequency clock, and the acquired data are routed to the input of ADC FIFO.

Output buffers of XDSOUT external digital output stream are updated at the rising edge of each sampling frequency clock with the output data of DAC FIFO.

In order external hardware can synchronize XDSIN external digital input stream to ADC data acquisition controller, *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM provides XDSIN_EN and XDSIN_CLK output signals via on-board JP3 connector. Correspondingly, in order external hardware can synchronize XDSOUT external digital input stream to DAC data acquisition controller, *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM provides XDSOUT_EN and XDSOUT_CLK output signals via on-board JP4 connector.

Figures 2-13a and 2-13b present timing diagrams for XDSIN/XDSOUT external digital I/O streams timing for A/D and D/A data acquisition process in *ADC OPM* and *DAC OPM* data acquisition modes correspondingly with software start-up synchronization for the *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM configured in MASTER synchronization mode.
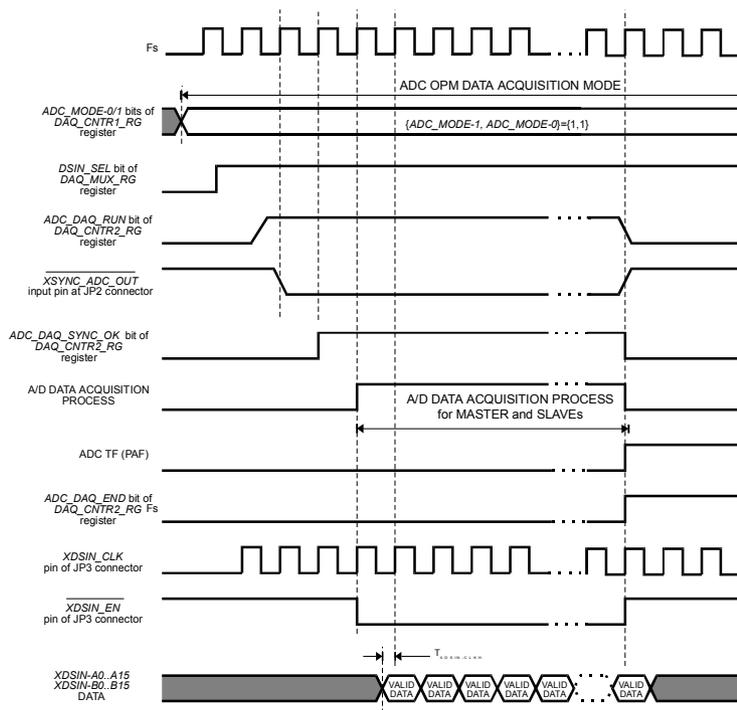
Fig.2-13a. Timing diagram for XDSIN external digital input stream for *ADC OPM* data acquisition process with software start-up synchronization in MASTER synchronization mode.
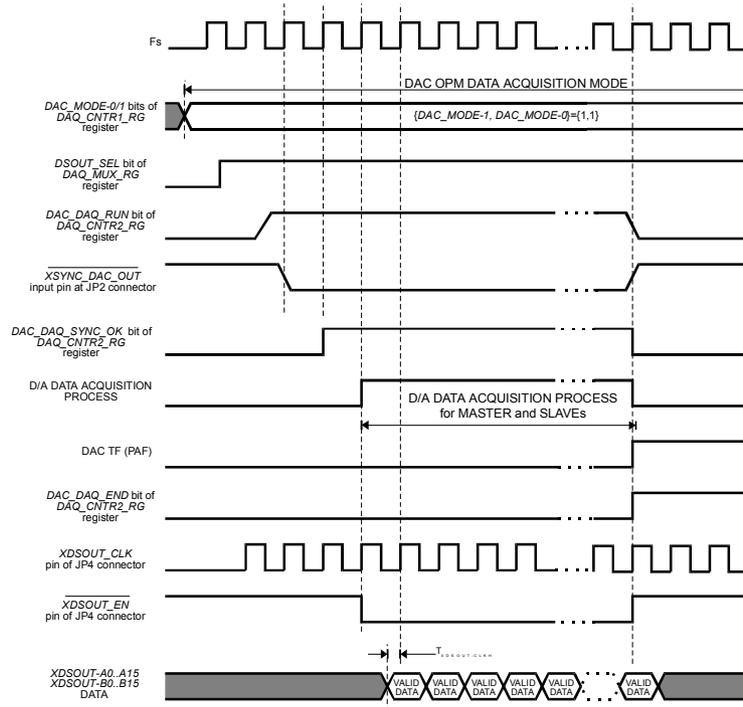
Fig.2-13b. Timing diagram for XDSOUT external digital output stream for *DAC OPM* data acquisition process with software start-up synchronization in MASTER synchronization mode.

Below is a brief description of how XDSIN external digital input stream timing works for A/D data acquisition process in *ADC OPM* data acquisition mode with software start-up synchronization and MASTER synchronization mode. Timing for XDSOUT external digital output stream for D/A data acquisition process in *ADC OPM* data acquisition mode with software start-up synchronization and MASTER synchronization mode is similar to that for A/D data acquisition process.

After the in *ADC OPM* data acquisition mode has been selected via bits {*ADC_MODE-1*, *ADC_MODE-0*} of *DAQ_CNTR1_RG* register, and on-board DSIN-MUX has been configured to XDSIN external digital input stream by setting bit *DSIN_SEL* bit of *DAQ_MUX_RG* register to the '1' state by host DSP software, then XDSIN synchronization clock will immediately appear at the XDSIN_CLK output pin of on-board JP3 connector. After A/D data acquisition process has been initialized via host DSP software by setting bit *ADC_DAQ_RUN* bit of *DAQ_CNTR2_RG* register (table 2-3) to the '1' state, then this is accepted as active start-up synchronization event by ADC data acquisition controller. After the start-up synchronization event for A/D data acquisition process has been detected, the XSYNC_ADC_OUT pin of on-board JP2 connector will immediately go to the active low state in order to synchronize external h/w and all *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, which are configured in the SLAVE synchronization mode. At the next sampling frequency clock the read-only *ADC_DAQ_SYNC_OK* bit of *DAQ_CNTR2_RG* register (table 2-3) will be set to the '1' state in order to indicate detected start-up synchronization to host DSP software. Actual A/D data acquisition process will start at the next sampling frequency pulse after the *ADC_DAQ_SYNC_OK* bit of *DAQ_CNTR2_RG* register (table 2-3) will go to the '1' state. External hardware will be indicated about active A/D data acquisition process by setting XDSIN_EN output signal at on-board JP3 connector to the active low

state. XDSIN_EN output signal at on-board JP3 connector will be held in active low state until the A/D data acquisition process will be either terminated normally (as it is presented at figure 2-13a and described in the corresponding subsection earlier in this section), or will be aborted by host DSP software (as it is described in the corresponding subsection earlier in this section). External digital I/O data of XDSIN external digital input stream are sampled at the rising edge of each sampling frequency clock, and the acquired data are routed to the input of ADC FIFO. External digital I/O data of XDSIN external digital input stream shall be set stable at least $T_{XDSIN-CLKH}$ setup time before the rising edge of sampling frequency clock (refer to chapter 1 for timing specifications).

data acquisition errors

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM provides real-time data acquisition errors control in order host DSP software can monitor correct progress of A/D and D/A data acquisition processes. Data acquisition errors are available for polling via *ERR_STAT_RG* register (table 2-8) and/or can generate host PIOX-16 interrupt requests (tables 2-15a and 2-15b).

The following data acquisition error conditions are being tracked by ADC and DAC data acquisition controllers during any of the corresponding ADC and DAC data acquisition modes:
- ADC FIFO overflow, which appears as *ADC_FIFO_OVF* bit in *ERR_STAT_RG* register
- ADC FIFO underflow, which appears as *ADC_FIFO_UVF* bit in *ERR_STAT_RG* register
- DAC FIFO overflow, which appears as *DAC_FIFO_OVF* bit in *ERR_STAT_RG* register
- DAC FIFO underflow, which appears as *DAC_FIFO_UVF* bit in *ERR_STAT_RG* register
- ADC IRT error, which appears as *ADC_IRT_ERR* bit in *ERR_STAT_RG* register
- DAC IRT error, which appears as *DAC_IRT_ERR* bit in *ERR_STAT_RG* register.

ADC FIFO overflow error (*ADC_FIFO_OVF* bit in *ERR_STAT_RG* register) is set in case ADC data acquisition controller writes to the full ADC FIFO, whereas ADC FIFO underflow error (*ADC_FIFO_OVF* bit in *ERR_STAT_RG* register) is set in case host PIOX-16 interface reads from the empty ADC FIFO. Particular ADC FIFO, which is (are) being tracked for overflow and underflow conditions during ADC data acquisition modes, is (are) defined by the {*ADC_FMT-1*, *ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register (table 2-2) in accordance with table 2-19.

Table 2-19. ADC FIFO source for ADC FIFO overflow/underflow conditions.

{*ADC_FMT-1*, *ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register		ADC FIFO, which is being tracked for the overflow/underflow conditions
ADC_FMT-1	*ADC_FMT-0*	
0	0	ADC1-FIFO
0	1	ADC2-FIFO
1	0	ADC1-FIFO and ADC2-FIFO using logical OR
1	1	-

Note: 1. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

DAC FIFO overflow error (*DAC_FIFO_OVF* bit in *ERR_STAT_RG* register) is set in case host PIOX-16 interface writes from the full DAC FIFO, whereas DAC FIFO underflow error (*DAC_FIFO_OVF* bit in *ERR_STAT_RG* register) is set in case DAC data acquisition controller reads from the empty DAC FIFO. Particular DAC FIFO, which is (are) being tracked for overflow and underflow conditions during DAC data acquisition modes, is (are) defined by the {*DAC_FMT-1*, *DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register (table 2-2) in accordance with table 2-20.

Table 2-20. DAC FIFO source for DAC FIFO overflow/underflow conditions.

{*DAC_FMT-1*, *DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register		DAC FIFO, which is being tracked for the overflow/underflow conditions
DAC_FMT-1	*DAC_FMT-0*	
0	0	DAC1-FIFO
0	1	DAC2-FIFO
1	0	DAC1-FIFO and DAC2-FIFO using logical OR
1	1	-

Note: 1. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

ADC IRT error (*ADC_IRT_ERR* bit in *ERR_STAT_RG* register) and DAC IRT error (*DAC_IRT_ERR* bit in *ERR_STAT_RG* register) appear in case of violation of access sequence from host PIOX-16 interface to *ADC1_FIFO_DATA_RG* and *ADC2_FIFO_DATA_RG* registers and to *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* registers correspondingly during *2-channel operation mode* only for ADC IRT and DAC IRT controllers. For more details about ADC IRT error and DAC IRT error refer to section "ADC IRT and DAC IRT Controllers" later in this chapter.

CAUTION

Neither of data acquisition errors terminates the corresponding data acquisition process in case this error flag is set to the '1' state.

In order to clear data acquisition error(s), host DSP software must perform any of the following actions:
- write to the corresponding bit of *ERR_CLR_RG* register (table 2-8), which allows individual reset as well as to reset any combination of data acquisition errors
- either set *ADC FIFO CONFIGURATION MODE* (by means of setting {*ADC_MODE-1*, *ADC_MODE-0*} bits of *DAQ_CNTR1_RG* register (table 2-2) are set to the {0,0} state), or write to *ADC_DAQ_RESET_RG* (written data will be ignored during write to either), which will reset ADC data acquisition controller along with the ADC overflow/underflow and ADC IRT errors
- either set *DAC FIFO CONFIGURATION MODE* (by means of setting {*DAC_MODE-1*, *DAC_MODE-0*} bits of *DAQ_CNTR1_RG* register (table 2-2) are set to the {0,0} state), or write to

DAC_DAQ_RESET_RG (written data will be ignored during write to either), which will reset DAC data acquisition controller along with the DAC overflow/underflow and DAC IRT errors

- write to *DAQ_RESET_RG* (written data will be ignored during write to either), which will reset ADC/DAC data acquisition controllers along with all data acquisition errors.

Any combination of ADC/DAC data acquisition errors can be used to generate host PIOX-16 interrupt request (refer to table 2-15a and 2-15b). In this case the corresponding host PIOX-16 interrupt request selector (any of the *HIRQ0_SEL_RG..HIRQ3_SEL_RG* register) must be configured to generate interrupt request on logical OR of data acquisition error conditions in accordance with *XIM_ERR_RG* register (table 2-16), whereas *XIM_ERR_RG* register must contain enable mask(s) for the corresponding data acquisition error(s), which is (are) allowed to generate active host PIOX-16 interrupt request. Selected host PIOX-16 interrupt request is generated as logical OR of enabled data acquisition errors.

2.4   ADC IRT and DAC IRT Controllers

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM provides on-board ADC IRT (interrupt retriggable transmission) (fig.2-3a) and DAC IRT controllers (fig.2-3b), which can be used in conjunction with host DSP on-chip DMA controllers in order to download data from ADC FIFO to host DSP environment and upload data to DAC FIFO from host DSP environment during ADC and DAC data acquisition modes correspondingly.

CAUTION

The number of DSP on-chip DMA controllers significantly varies upon the DSP type, and your have to ensure that on-board DSP of host *TORNADO* DSP system/controller provides enough DMA channels in order to perform ADC IRT and DAC IRT data transmissions.

CAUTION

ADC IRT and DAC IRT controllers provide generation of retriggable synchronization events for host DSP on-chip DMA channels via any of host PIOX-16 interrupt request lines (refer to tables 2-15a and 2-15b), whereas actual data transfer is maintained by DSP on-chip DMA controller.

---

operation description for ADC IRT controller

ADC IRT controller can operate in either *1-channel operation mode* or *2-channel operation mode* and is controlled by the following register bits and signals:
- {*ADC_MODE-1*, *ADC_MODE-0*} bits of *DAQ_CNTR1_RG* register (table 2-2), which are used to detect active ADC data acquisition modes
- {*ADC_FMT-1*, *ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register, which are used to set either 1-channel or 2-channel operation mode of ADC IRT controller and to detect a particular ADC FIFO

(either ADC1-FIFO or ADC2-FIFO), which must be downloaded in 1-channel operation mode of ADC IRT controller

- *ADC_DAQ_TF_SEL* and *ADC_IRT_TF_SEL* bits of *DAQ_CNTR3_RG* register (table 2-4), which are used in conjunction with {*ADC_FMT-1*, *ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register in order to select particular ADC FIFO output flags, which will be used as ADC IRT transmission start and transmission termination events
- EF/PAE/FF/PAF output flags of both ADC1-FIFO and ADC2-FIFO
- host PIOX-16 interface logic in order to decode access to *ADC1_FIFO_DATA_RG* and *ADC2_FIFO_DATA_RG* registers (table 2-1).

ADC IRT controller is enabled during any of the *ADC OPM* or *ADC PTM* data acquisition modes. Once any of the *ADC OPM* or *ADC PTM* data acquisition modes has been set by host DSP software, then ADC IRT controller starts 'hunting' for transmission start event. Active transmission start event for ADC IRT controller is detected in case either PAF or FF flag of ADC FIFO comes active depending upon the state of the *ADC_DAQ_TF_SEL* bits of *DAQ_CNTR3_RG* register (table 2-4) and {*ADC_FMT-1*, *ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register, which select a particular ADC FIFO (either ADC1-FIFO or ADC2-FIFO), which output flags are used to trigger transmission start event for ADC IRT controller in accordance with table 2-21.

Table 2-21. ADC IRT transmission start event selector.

{*ADC_FMT-1*, *ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register		*ADC_DAQ_TF_SEL* bit of *DAQ_CNTR3_RG* register	transmission start event for ADC IRT controller	ADC IRT controller operation mode	ADC FIFO, which is involved into A/D data acquisition process
ADC_FMT-1	*ADC_FMT-0*				
0	0	0	FF flag of ADC1-FIFO	*1-channel operation mode*	ADC1-FIFO
0	0	1	PAF flag of ADC1-FIFO	*1-channel operation mode*	ADC1-FIFO
0	1	0	FF flag of ADC2-FIFO	*1-channel operation mode*	ADC2-FIFO
0	1	1	PAF flag of ADC2-FIFO	*1-channel operation mode*	ADC2-FIFO
0	0	0	FF flag of ADC1-FIFO	*2-channel operation mode*	ADC1-FIFO ADC2-FIFO
0	0	1	PAF flag of ADC1-FIFO	*2-channel operation mode*	ADC1-FIFO ADC2-FIFO
1	1	-	-	-	-

Note: 1. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

After transmission start event has been detected, then ADC IRT controller enters the transmission cycle, which terminates on either transmission termination event, or in case ADC IRT error (*ADC_IRT_ERR* bit in

ERR_STAT_RG register) will occur during *2-channel operation mode* of ADC IRT controller (for more details refer to the corresponding subsection below). Active transmission termination event start event for ADC IRT controller is detected in case either PAE or EF flag of ADC FIFO comes active depending upon the state of the *ADC_IRT_TF_SEL* bits of *DAQ_CNTR3_RG* register (table 2-4) and {*ADC_FMT-1*, *ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register, which select a particular ADC FIFO (either ADC1-FIFO or ADC2-FIFO), which output flags are used to trigger transmission start event for ADC IRT controller in accordance with table 2-22.

Table 2-22. ADC IRT transmission termination event selector.

{*ADC_FMT-1*, *ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register		*ADC_IRT_TF_SEL* bit of *DAQ_CNTR3_RG* register	transmission termination event for ADC IRT controller	ADC IRT controller operation mode	ADC FIFO, which is involved into A/D data acquisition process
ADC_FMT-1	*ADC_FMT-0*				
0	0	0	EF flag of ADC1-FIFO	*1-channel operation mode*	ADC1-FIFO
0	0	1	PAE flag of ADC1-FIFO	*1-channel operation mode*	ADC1-FIFO
0	1	0	EF flag of ADC2-FIFO	*1-channel operation mode*	ADC2-FIFO
0	1	1	PAE flag of ADC2-FIFO	*1-channel operation mode*	ADC2-FIFO
0	0	0	EF flag of ADC1-FIFO	*2-channel operation mode*	ADC1-FIFO ADC2-FIFO
0	0	1	PAE flag of ADC1-FIFO	*2-channel operation mode*	ADC1-FIFO ADC2-FIFO
1	1	-	-	-	-

Note: 1. Highlighted configurations correspond to default settings on PIOX-16 reset condition.

While ADC IRT controller is in the transmission cycle, then it continuously generates retriggable synchronization events over selected PIOX-16 interrupt request line for host DSP on-chip DMA controller(s). Active ADC IRT synchronization event is generated in case ADC IRT controller is expecting host DSP to read the corresponding ADC FIFO.

> **CAUTION**
>
> In case *1-channel operation mode* is selected for ADC IRT controller, then particular ADC FIFO, which must be read by host DSP via host PIOX-16 interface, is defined by bits {*ADC_FMT-1*, *ADC_FMT-0*} bits of *DAQ_CNTR1_RG* register in accordance with table 2-21 or 2-22.
>
> In case *2-channel operation mode* is selected for ADC IRT controller, then both ADC1-FIFO and ADC2-FIFO shall be read by host DSP via host PIOX-16 interface during one ADC IRT synchronization cycle. It is no matter what particular ADC FIFO (either ADC1-FIFO or ADC2-FIFO) will be read first.

After ADC FIFO data has (have) been read by host DSP via host PIOX-16 interface, then ADC IRT controller will retrigger ADC IRT synchronization signal, which is passed over selected host PIOX-16 interrupt request line, in order to start new ADC IRT synchronization event for host DSP on-chip DMA controller. This repetitive procedure will proceed until ADC IRT transmission termination event will be detected, i.e. ADC FIFO will either get empty or partially empty (depending upon what particular ADC IRT transmission termination event has been selected).

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM can generate ADC IRT synchronization events for host DSP on-chip DMA controller(s) over any of four host PIOX-16 interrupt request lines. In order to select a particular host PIOX-16 interrupt request line, which will be used to pass ADC IRT synchronization events, then the corresponding interrupt selector register (*HIRQ0_SEL_RG..HIRQ3_SEL_RG* registers, refer to table 2-1) must be configured to either ADC IRT positive polarity or ADC IRT negative polarity interrupt requests (tables 2-15a and 2-15b).

Generated ADC IRT synchronization events with different polarity allows provide compatibility of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM with virtually any host DSP chip, which is installed at host *TORNADO* DSP system/controller.

> **CAUTION**
>
> ADC IRT positive polarity synchronization event, which is passed over active low host PIOX-16 interrupt request lines, results in active low host PIOX-16 interrupt request, whereas ADC IRT negative polarity synchronization event results in active high host PIOX-16 interrupt request.

CAUTION

Positive polarity for ADC IRT synchronization event must be used with all *TORNADO-P6x* DSP systems for PCI, *TORNADO-3x/P3x/E3x* DSP systems/controllers and *TORNADO-54x/E54x* DSP systems/controllers, whereas negative polarity for ADC IRT synchronization event must be used with all *TORNADO-6x/E6x* DSP systems/controllers.

Figures 2-14a and 2-14b present timing diagrams for *1-channel* and *2-channel operation modes* of ADC IRT controller with positive polarity of ADC IRT synchronization event and PAF/PAE ADC FIFO flags, which are used to trigger transmission start and transmission termination events for ADC IRT.
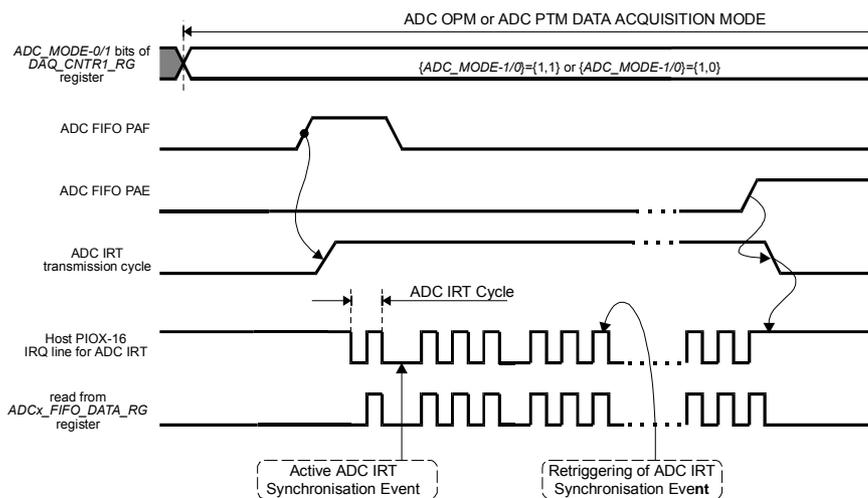

Fig.2-14a. Timing diagram for 1-channel operation mode of ADC IRT controller with positive polarity of synchronization event.
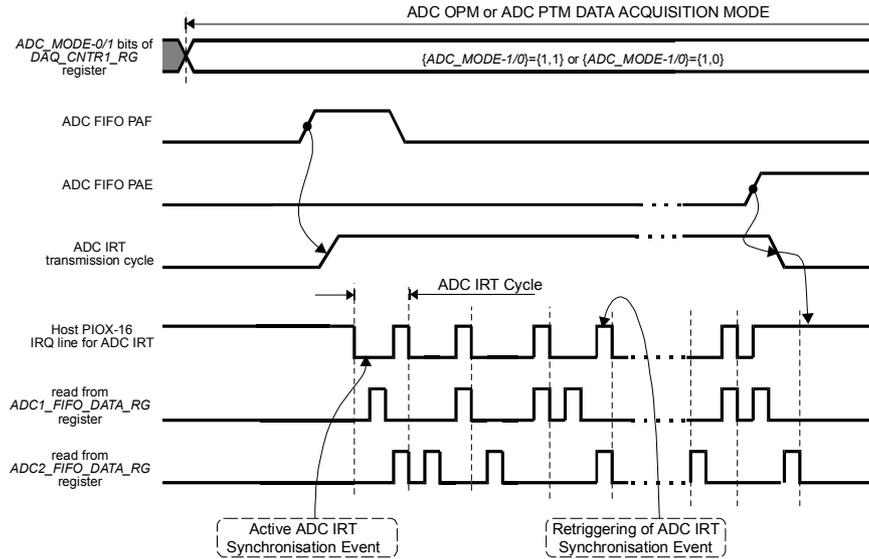
Fig.2-14b. Timing diagram for 2-channel operation mode of ADC IRT controller with positive polarity of synchronization event.

Host DSP software must correctly configure DSP on-chip DMA controller(s) in order to download ADC FIFO data to host DSP environment. Refer to the corresponding TMS320 DSP user's guide for details how to configure DSP on-chip DMA controllers.

CAUTION

In case *1-channel operation mode* is selected for ADC IRT controller, then only one host DSP on-chip controller must be involved into ADC IRT data transfer.

Involved host DSP on-chip DMA controller must be configured to read data from either *ADC1_FIFO_DATA_RG* or *ADC2_FIFO_DATA_RG* register (in accordance with table 2-21 or 2-22) without address indexing/increment, and on external synchronization event over the corresponding DSP external hardware interrupt request input, which is connected to host PIOX-16 interrupt request line and which is used to pass ADC IRT synchronization event (refer to the user's guide for your *TORNADO* DSP system/controller for more details).

<hr>

CAUTION

In case *2-channel operation mode* is selected for ADC IRT controller, then two host DSP on-chip controllers shall be involved into ADC IRT data transfer.

Involved host DSP on-chip DMA controllers shall be configured to read data from *ADC1_FIFO_DATA_RG* and *ADC2_FIFO_DATA_RG* registers correspondingly without address indexing/increment, and on common external synchronization event over the corresponding DSP external hardware interrupt request input, which is connected to host PIOX-16 interrupt request line and which is used to pass ADC IRT synchronization event (refer to the user's guide for your *TORNADO* DSP system/controller for more details).

<hr>

operation description for DAC IRT controller

DAC IRT controller can operate in either *1-channel operation mode* or *2-channel operation mode* and is controlled by the following register bits and signals:
- {*DAC_MODE-1*, *DAC_MODE-0*} bits of *DAQ_CNTR1_RG* register (table 2-2), which are used to detect active ADC data acquisition modes
- {*DAC_FMT-1*, *DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register, which are used to set either 1-channel or 2-channel operation mode of DAC IRT controller and to detect a particular DAC FIFO (either DAC1-FIFO or DAC2-FIFO), which must be downloaded in 1-channel operation mode of DAC IRT controller
- *DAC_DAQ_TF_SEL* and *DAC_IRT_TF_SEL* bits of *DAQ_CNTR3_RG* register (table 2-4), which are used in conjunction with {*DAC_FMT-1*, *DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register in order to select particular DAC FIFO output flags, which will be used as DAC IRT transmission start and transmission termination events
- EF/PAE/FF/PAF output flags of both DAC1-FIFO and DAC2-FIFO
- host PIOX-16 interface logic in order to decode access to *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* registers (table 2-1).

DAC IRT controller is enabled during any of the *DAC OPM* or *DAC PTM* data acquisition modes. Once any of the *DAC OPM* or *DAC PTM* data acquisition modes has been set by host DSP software, then DAC IRT controller starts 'hunting' for transmission start event. Active transmission start event for DAC IRT controller is detected in case either PAE or EF flag of DAC FIFO comes active depending upon the state of the *DAC_DAQ_TF_SEL* bits of *DAQ_CNTR3_RG* register (table 2-4) and {*DAC_FMT-1*, *DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register, which select a particular DAC FIFO (either DAC1-FIFO or DAC2-FIFO), which output flags are used to trigger transmission start event for DAC IRT controller in accordance with table 2-23.

Table 2-23. DAC IRT transmission start event selector.

{*DAC_FMT-1*, *DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register		*DAC_DAQ_TF_SEL* bit of *DAQ_CNTR3_RG* register	transmission start event for DAC IRT controller	DAC IRT controller operation mode	DAC FIFO, which is involved into D/A data acquisition process
DAC_FMT-1	*DAC_FMT-0*				
0	0	0	EF flag of DAC1-FIFO	*1-channel operation mode*	DAC1-FIFO
0	0	1	PAE flag of DAC1-FIFO	*1-channel operation mode*	DAC1-FIFO
0	1	0	EF flag of DAC2-FIFO	*1-channel operation mode*	DAC2-FIFO
0	1	1	PAE flag of DAC2-FIFO	*1-channel operation mode*	DAC2-FIFO
0	0	0	EF flag of DAC1-FIFO	*2-channel operation mode*	DAC1-FIFO DAC2-FIFO
0	0	1	PAE flag of DAC1-FIFO	*2-channel operation mode*	DAC1-FIFO DAC2-FIFO
1	1	-	-	-	-

Note: 1.   Highlighted configurations correspond to default settings on PIOX-16 reset condition.

After transmission start event has been detected, then DAC IRT controller enters the transmission cycle, which terminates on either transmission termination event, or in case DAC IRT error (*DAC_IRT_ERR* bit in *ERR_STAT_RG* register) will occur during *2-channel operation mode* of DAC IRT controller (for more details refer to the corresponding subsection below). Active transmission termination event start event for DAC IRT controller is detected in case either PAF or FF flag of DAC FIFO comes active depending upon the state of the *DAC_IRT_TF_SEL* bits of *DAQ_CNTR3_RG* register (table 2-4) and {*DAC_FMT-1*, *DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register, which select a particular DAC FIFO (either DAC1-FIFO or DAC2-FIFO), which output flags are used to trigger transmission start event for DAC IRT controller in accordance with table 2-24.

Table 2-24.   DAC IRT transmission termination event selector.

{*DAC_FMT-1*, *DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register		*DAC_IRT_TF_SEL* bit of *DAQ_CNTR3_RG* register	transmission termination event for DAC IRT controller	DAC IRT controller operation mode	DAC FIFO, which is involved into D/A data acquisition process
DAC_FMT-1	*DAC_FMT-0*				
0	0	0	FF flag of DAC1-FIFO	*1-channel operation mode*	DAC1-FIFO
0	0	1	PAF flag of DAC1-FIFO	*1-channel operation mode*	DAC1-FIFO
0	1	0	FF flag of DAC2-FIFO	*1-channel operation mode*	DAC2-FIFO
0	1	1	PAF flag of DAC2-FIFO	*1-channel operation mode*	DAC2-FIFO
0	0	0	FF flag of DAC1-FIFO	*2-channel operation mode*	DAC1-FIFO DAC2-FIFO
0	0	1	PAF flag of DAC1-FIFO	*2-channel operation mode*	DAC1-FIFO DAC2-FIFO
1	1	-	-	-	-

Note: 1.   Highlighted configurations correspond to default settings on PIOX-16 reset condition.

While DAC IRT controller is in the transmission cycle, then it continuously generates retriggable synchronization events over selected PIOX-16 interrupt request line for host DSP on-chip DMA controller(s). Active DAC IRT synchronization event is generated in case DAC IRT controller is expecting host DSP to write to the corresponding DAC FIFO.

CAUTION

In case *1-channel operation mode* is selected for DAC IRT controller, then particular DAC FIFO, which must be written by host DSP via host PIOX-16 interface, is defined by bits {*DAC_FMT-1*, *DAC_FMT-0*} bits of *DAQ_CNTR1_RG* register in accordance with table 2-23 or 2-24.

In case *2-channel operation mode* is selected for DAC IRT controller, then both DAC1-FIFO and DAC2-FIFO shall be written by host DSP via host PIOX-16 interface during one DAC IRT synchronization cycle. It is no matter what particular DAC FIFO (either DAC1-FIFO or DAC2-FIFO) will be written first.

After DAC FIFO data has (have) been written by host DSP via host PIOX-16 interface, then DAC IRT controller will retrigger DAC IRT synchronization signal, which is passed over selected host PIOX-16 interrupt

request line, in order to start new DAC IRT synchronization event for host DSP on-chip DMA controller. This repetitive procedure will proceed until DAC IRT transmission termination event will be detected, i.e. DAC FIFO will either get full or partially full (depending upon what particular DAC IRT transmission termination event has been selected).

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM can generate DAC IRT synchronization events for host DSP on-chip DMA controller(s) over any of four host PIOX-16 interrupt request lines. In order to select a particular host PIOX-16 interrupt request line, which will be used to pass DAC IRT synchronization events, then the corresponding interrupt selector register (*HIRQ0_SEL_RG..HIRQ3_SEL_RG* registers, refer to table 2-1) must be configured to either DAC IRT positive polarity or DAC IRT negative polarity interrupt requests (tables 2-15a and 2-15b).

Generated DAC IRT synchronization events with different polarity allows provide compatibility of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM with virtually any host DSP chip, which is installed at host *TORNADO* DSP system/controller.

CAUTION

DAC IRT positive polarity synchronization event, which is passed over active low host PIOX-16 interrupt request lines, results in active low host PIOX-16 interrupt request, whereas DAC IRT negative polarity synchronization event results in active high host PIOX-16 interrupt request.

CAUTION

Positive polarity for DAC IRT synchronization event must be used with all *TORNADO-P6x* DSP systems for PCI, *TORNADO-3x/P3x/E3x* DSP systems/controllers and *TORNADO-54x/E54x* DSP systems/controllers, whereas negative polarity for DAC IRT synchronization event must be used with all *TORNADO-6x/E6x* DSP systems/controllers.

Figures 2-15a and 2-15b present timing diagrams for *1-channel* and *2-channel operation modes* of DAC IRT controller with positive polarity of DAC IRT synchronization event and PAE/PAF DAC FIFO flags, which are used to trigger transmission start and transmission termination events for DAC IRT.
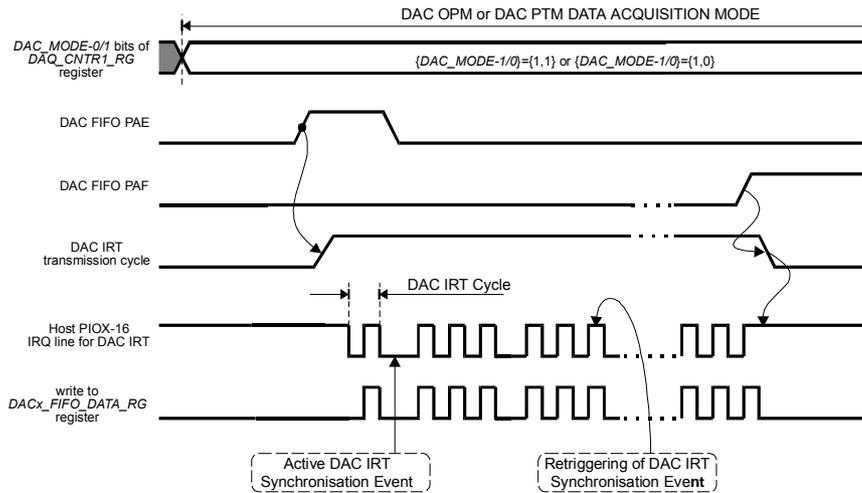
Fig.2-15a.   Timing diagram for 1-channel operation mode of DAC IRT controller with positive polarity of synchronization event.
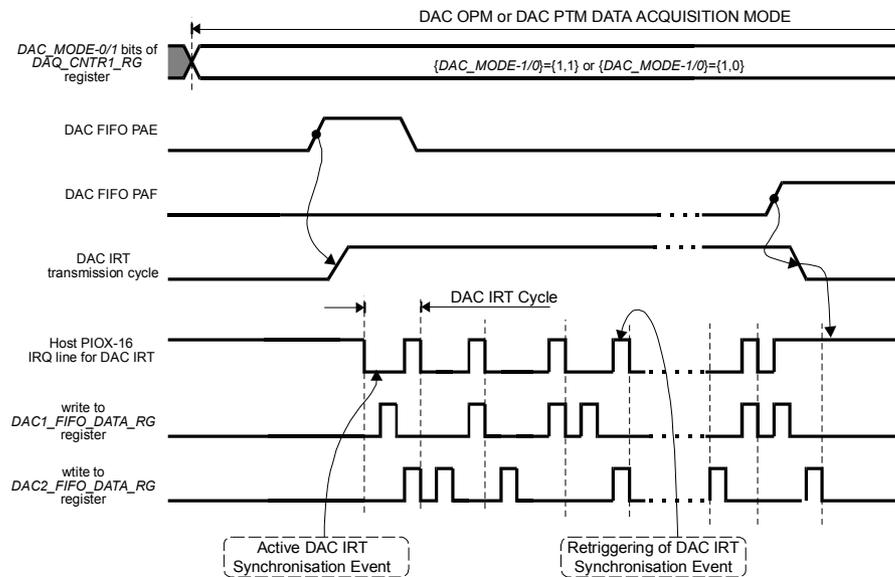

Fig.2-15b.   Timing diagram for 2-channel operation mode of DAC IRT controller with positive polarity of synchronization event.

Host DSP software must correctly configure DSP on-chip DMA controller(s) in order to upload DAC FIFO data from host DSP environment. Refer to the corresponding TMS320 DSP user's guide for details how to configure DSP on-chip DMA controllers.

> **CAUTION**
>
> In case *1-channel operation mode* is selected for DAC IRT controller, then only one host DSP on-chip controller must be involved into DAC IRT data transfer.
>
> Involved host DSP on-chip DMA controller must be configured to write data from either *DAC1_FIFO_DATA_RG* or *DAC2_FIFO_DATA_RG* register (in accordance with table 2-23 or 2-24) without address indexing/increment, and on external synchronization event over the corresponding DSP external hardware interrupt request input, which is connected to host PIOX-16 interrupt request line and which is used to pass DAC IRT synchronization event (refer to the user's guide for your *TORNADO* DSP system/controller for more details).

> **CAUTION**
>
> In case *2-channel operation mode* is selected for DAC IRT controller, then two host DSP on-chip controllers shall be involved into DAC IRT data transfer.
>
> Involved host DSP on-chip DMA controllers shall be configured to write data from *DAC1_FIFO_DATA_RG* and *DAC2_FIFO_DATA_RG* registers correspondingly without address indexing/increment, and on common external synchronization event over the corresponding DSP external hardware interrupt request input, which is connected to host PIOX-16 interrupt request line and which is used to pass DAC IRT synchronization event (refer to the user's guide for your *TORNADO* DSP system/controller for more details).

error conditions for ADC IRT controller

In case ADC IRT controller is configured in *2-channel operation mode*, then each ADC IRT cycle must comprise of two reads over host PIOX-16 interface: one read from *ADC1_FIFO_DATA_RG* register and one read from *ADC2_FIFO_DATA_RG* registers. The order of reads has no matter. This will guarantee integrity of ADC IRT cycle progress during ADC IRT transmission in progress, and will assume that both ADC FIFO are read in each ADC IRT cycle.

However, in case host PIOX-16 interface will violates integrity of ADC IRT cycle for some reason (mis-operation, etc), i.e. some ADC IRT cycle will comprise of two reads from the same *ADCx_FIFO_DATA_RG* register instead of one read from *ADC1_FIFO_DATA_RG* register and one read from *ADC2_FIFO_DATA_RG* registers, then this will result in setting the ADC IRT error flag (*ADC_IRT_ERR* bit in *ERR_STAT_RG* register) and canceling of ADC IRT controller operation. Re-activation of ADC IRT controller can be performed only after host DSP software will recognize and reset ADC IRT error.

Active ADC IRT error (*ADC_IRT_ERR* bit in *ERR_STAT_RG* register) can be used to generate host PIOX-16 interrupt request.

For more details about processing of data acquisition errors refer to section "Data Acquisition Control" earlier in this chapter.

error conditions for DAC IRT controller

In case DAC IRT controller is configured in *2-channel operation mode*, then each DAC IRT cycle must comprise of two writes over host PIOX-16 interface: one write to *DAC1_FIFO_DATA_RG* register and one write to *DAC2_FIFO_DATA_RG* registers. The order of write has no matter. This will guarantee integrity of DAC IRT cycle progress during DAC IRT transmission in progress, and will assume that both DAC FIFO are written in each DAC IRT cycle.

However, in case host PIOX-16 interface will violates integrity of DAC IRT cycle for some reason (mis-operation, etc), i.e. some DAC IRT cycle will comprise of two reads from the same *DACx_FIFO_DATA_RG* register instead of one read from *DAC1_FIFO_DATA_RG* register and one read from *DAC2_FIFO_DATA_RG* registers, then this will result in setting the DAC IRT error flag (*DAC_IRT_ERR* bit in *ERR_STAT_RG* register) and canceling of DAC IRT controller operation. Re-activation of DAC IRT controller can be performed only after host DSP software will recognize and reset DAC IRT error.

Active DAC IRT error (*DAC_IRT_ERR* bit in *ERR_STAT_RG* register) can be used to generate host PIOX-16 interrupt request.

For more details about processing of data acquisition errors refer to section "Data Acquisition Control" earlier in this chapter.

Chapter 3. Installation and Configuration

This chapter includes instructions for installation of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

3.1   Installation onto *TORNADO* DSP System/Controller Mainboard

In case *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is considered to be used in host operation mode, then *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM must be installed as standard PIOX-16 DCM onto host *TORNADO* DSP system/controller mainboard.

For installation of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM into PIOX-16 site of *TORNADO* DSP system/controller follow the recommendations below:

1. Switch off the power of host PC.
2. Remove *TORNADO* mainboard from PC slot.
3. Ensure that two *TORNADO* on-board spacers for mounting PIOX-16 DCM are installed into the corresponding holes on *TORNADO* mainboard (fig.3-1). If spacers are not installed, then install spacers, which are enclosed with *T/PDAS-AD8/12D/65M-DA2/12D/65M* shipment package.
4. Pick-up *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM from the shipment packaging and orient it parallel to *TORNADO* mainboard over PIOX-16 DCM area. Safely plug-in on-board JP1 host PIOX-16 connector of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM into the corresponding 16-bit PIOX-16 site header of host *TORNADO* mainboard (fig.3-1a). In case host *TORNADO* mainboard provides on-board 32-bit PIOX interface site, then you have to plug *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM into the 16-bit PIOX-16 sub-connector of host PIOX interface site at host *TORNADO* mainboard (fig.3-1b).
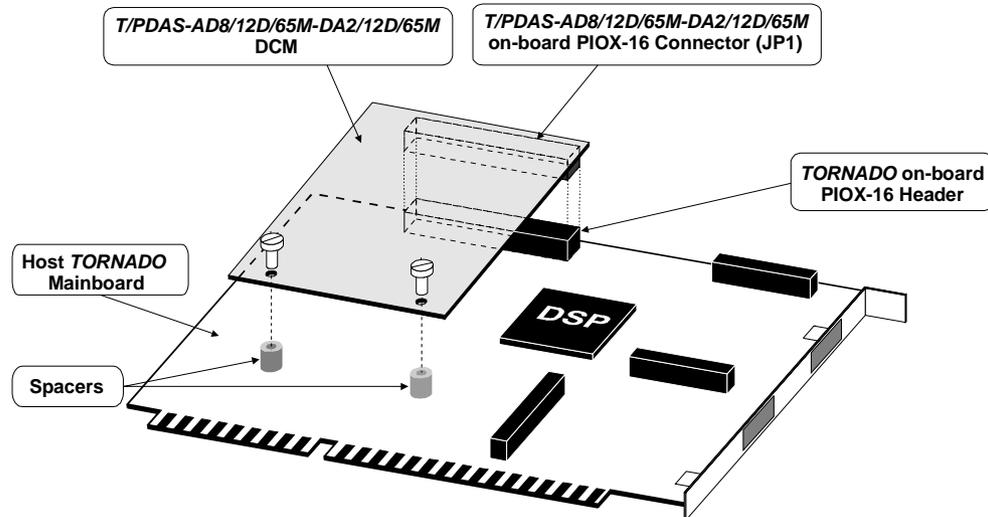

Fig. 3-1a.   Installation of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM into 16-bit PIOX-16 site of host *TORNADO* DSP system.
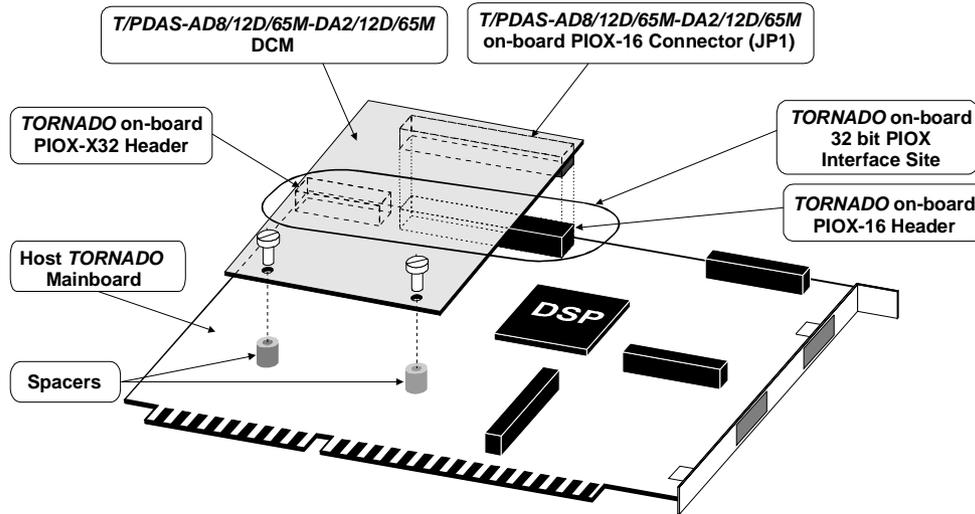
Fig. 3-1b.   Installation of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM into 32-bit PIOX site of host *TORNADO* DSP system.

4. Screw in *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM to the spacers at *TORNADO* mainboard.
5. Connect *T/X-XIOB/PDAS65M* external I/O board to *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM via ten mini-coax cables and one flat cable (refer to Appendix C).
6. If required, plug-in flat cables to *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM on-board JP3 and/or JP4 on-board connectors for connection to 32-bit XDSIN and XDSOUT external digital I/O streams
7. In case *TORNADO* PC plug-in DSP system is used for installation of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, then install *TORNADO* mainboard into PC chassis slot and screw it to the rear panel of PC.
8. In case *TORNADO* PC plug-in DSP system is used for installation of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and in case *T/X-XIOB/PDAS65M* external I/O board for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is not installed onto the rear mounting bracket of host *TORNADO* mainboard, then install and screw *T/X-XIOB/PDAS65M* external I/O board to the rear panel of PC.
9. Plug-in *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* external I/O cable (refer to Appendix C) sets to JP20 and JP21 external I/O connectors of *T/X-XIOB/PDAS65M* external I/O board.
10. Connect external I/O equipment and external analog I/O sources to *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* external I/O cable sets.
11. Switch on power of host PC.

3.2   Connection to external signal I/O equipment

Connection of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM to external analog I/O equipment is performed by means of on-board JP2, JP3/JP4 and JP5..JP14 connectors (fig.A-1) and by means of optional *T/X-XIOB/PDAS65M* external I/O board and *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* external I/O cable sets (Appendix C).

CAUTION

It is highly recommended to plug-in and unplug external I/O cables into/from on-board connectors of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM when power is switched off.

The ground signal of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM has no galvanic isolation neither from host *TORNADO* DSP system/controller, nor from the PC ground and chassis, nor from external I/O peripherals and devices.

CAUTION

When connecting external analog I/O equipment to *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM via on-board JP5..JP16 connectors, be aware that all analog inputs/outputs of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM are DC coupled. If required, external DC isolation capacitors shall be used.

Appendix A.   On-board Connectors.

This Appendix includes a summary description for *T/PDAS-AD8/12D/65M-DA2/12D/65M* on-board connectors.

Board layout for *T/PDAS-AD8/12D/65M-DA2/12D/65M* on-board connectors is presented at fig.A-1.
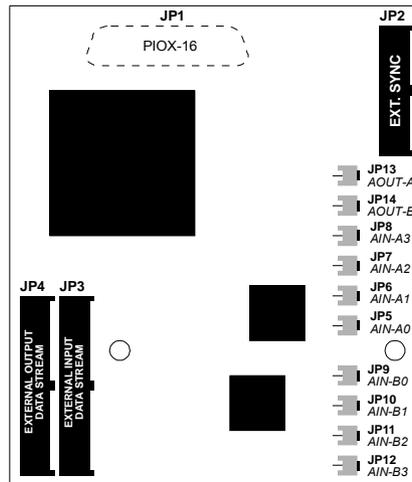

Fig.A-1. On-board connectors for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

Table A-1 contains the list of on-board connectors.

Table A-1. On-board connectors of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

connector ID	Description
JP1	Host PIOX-16 interface site male header. Pinout of JP1 host PIOX-16 connector is presented in Appendix B of this manual and in the user's guide of host *TORNADO* DSP system/controller, which is used for installation of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.
JP2	External synchronization and I/O connector for connection to external equipment. This connector can be either used for connection to external equipment or can connect to optional *T/X-XIOB/PDAS65M* external I/O board via flat cable. Refer to the corresponding subsection below and to Appendix C for more details.
JP3	XDSIN external 32-bit digital input stream connector. Refer to the corresponding subsection below for more details.
JP4	XDSOUT external 32-bit digital output stream connector. Refer to the corresponding subsection below for more details.
JP5 JP6 JP7 JP8	Mini-coax connectors for AIN-A0..A3 analog inputs. These connectors can be either used for direct analog input or can connect to optional *T/X-XIOB/PDAS65M* external I/O board mini-coax cables. Refer to Appendix C for more details.
JP9 JP10 JP11 JP12	Mini-coax connectors for AIN-B0..B3 analog inputs. These connectors can be either used for direct analog input or can connect to optional *T/X-XIOB/PDAS65M* external I/O board mini-coax cables. Refer to Appendix C for more details.
JP13 JP14	Mini-coax connectors for AOUT-A and AOUT-B analog outputs correspondingly. These connectors can be either used for direct analog output or can connect to optional *T/X-XIOB/PDAS65M* external I/O board mini-coax cables. Refer to Appendix C for more details.

pinout for JP2 external synchronization and I/O connector

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM on-board JP2 external synchronization and I/O connector has been designed for connection of multiple *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM using MASTER-SLAVE synchronization, for connection to external synchronization and clock equipment, and for general purpose digital I/O via GPIO-0..3 pins. All pins of JP2 connector comply with 3v/5v TTL logic.

Pinout of JP2 external synchronization and I/O connector for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is presented at fig.A-2, whereas the signal description is presented in table A-2.

On-board JP2 connector is 16-pin guarded 2mm straight mail header, which assumes for mating with the corresponding plug for 2mm flat ribbon cable. *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM has been designed to connect external synchronization devices via *T/X-XIOB/PDAS65M* external I/O board, which connects to *T/PDAS-AD8/12D/65M-DA2/12D/65M* on-board JP2 connector via 16-pin 2 mm flat cable (refer to Appendix C for more details). However, should customer application requires application specific cable for connection directly to JP2 external synchronization and I/O connector at *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, then compatible plugs are available from MicroLAB Systems upon request.
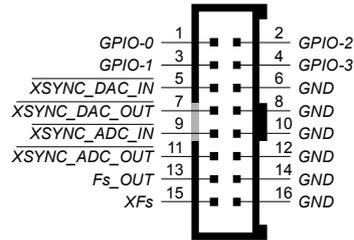
Fig. A-2.   Pinout for JP2 external synchronization and I/O connector of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

Table A-2.   Signal description for JP2 external synchronization and I/O connector of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

signal name	signal type	Description	reference information
XSYNC_ADC_IN XSYNC_DAC_IN	3v/5v TTL/IN	External start-up synchronization inputs for ADC and DAC data acquisition controllers correspondingly.	section 2-3
XSYNC_ADC_OUT XSYNC_DAC_OUT	3v/5v TTL/OUT	External start-up synchronization outputs from ADC and DAC data acquisition controllers correspondingly.	section 2-3
XFS	3v/5v TTL/IN	External sampling frequency input for ADC and DAC data acquisition controllers.	section 2-3
FS_OUT	3v/5v TTL/OUT	Output of sampling frequency clock for ADC and DAC data acquisition controllers.	section 2-3
GPDIO-0 GPDIO-1 GPDIO-2 GPDIO-3	3v/5v TTL/IO	General purpose programmable digital I/O.	section 2-2 table 2-13
GND	-	Ground.	

Notes: 1. Signal types: *TTL/IN* - TTL compatible digital input; *TTL/OUT* - TTL compatible digital output; *TTL/IO* - TTL compatible digital input/output.

pinout for JP3 and JP4 external digital I/O streams connectors

T/PDAS-AD8/12D/65M-DA2/12D/65M on-board JP3 and JP4 connectors has been designed for connection to external high-speed digital I/O equipment, which provides 32-bit external digital input stream and 32-bit external digital output stream correspondingly. All pins of JP3 and JP4 connectors comply with 3v/5v TTL logic.

Pinout of JP3 external digital input stream connector for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is presented at fig.A-3, whereas the signal description is presented in table A-3. Pinout of JP4 external digital

output stream connector for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM is presented at fig.A-4, whereas the signal description is presented in table A-4.

On-board JP3 and JP4 connectors are 40-pin guarded 2mm straight mail headers, which assumes for mating with the corresponding plug for 2mm flat ribbon cable. The mating 40-pin 2mm plugs are available from MicroLAB Systems upon request.
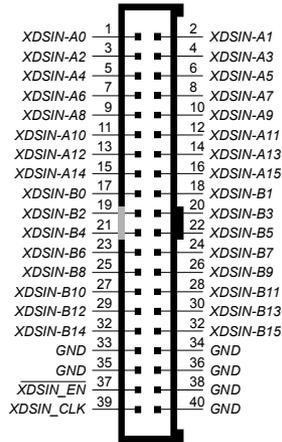

Fig. A-3. Pinout for JP3 external digital input stream connector of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

Table A-3. Signal description for JP3 external digital input stream connector of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

signal name	signal type	description	reference information
XDSIN-A0..15 *XDSIN-B0.15*	3v/5v TTL/IN	Data bits for 32-bit external digital input stream, which is organized as two 16-bit digital input streams.	section 2-3
XDSIN_EN	3v/5v TTL/OUT	Active low output enable signal (framing signal) for data acquisition of XDSIN external digital input stream.	section 2-3
XDSIN_CLK	3v/5v TTL/OUT	Active high synchronization clock signal for XDSIN external digital input stream.	section 2-3
GND	-	Ground.	

Notes: 1. Signal types: *TTL/IN* - TTL compatible digital input; *TTL/OUT* - TTL compatible digital output.
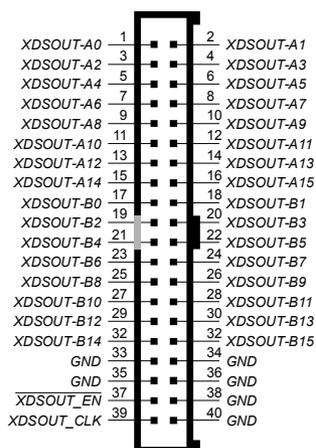
Fig. A-4. Pinout for JP4 external digital output stream connector of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

Table A-4. Signal description for JP4 external digital output stream connector of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

signal name	signal type	description	reference information
XDSOUT-A0..15 *XDSOUT-B0.15*	3v/5v TTL/OUT	Data bits for 32-bit external digital output stream, which is organized as two 16-bit digital input streams.	section 2-3
XDSOUT_EN	3v/5v TTL/OUT	Active low output enable signal (framing signal) for data acquisition of XDSOUT external digital output stream.	section 2-3
XDSOUT_CLK	3v/5v TTL/OUT	Active high synchronization clock signal for XDSOUT external digital input stream.	section 2-3
GND	-	Ground.	

Notes: 1. Signal types: *TTL/IN* - TTL compatible digital input; *TTL/OUT* - TTL compatible digital output.

Appendix B. PIOX-16 Interface Site

This appendix contains information about *TORNADO* PIOX-16 interface site specifications. This description is general to all *TORNADO* DSP systems/controllers, whereas different *TORNADO* boards with different DSP platforms may differ in the number of interrupts requests via PIOX-16 interface and in timer/IO pin specifications. Refer to your particular *TORNADO* user's guide for more details.

B.1   General Description

TORNADO architecture allows expansion of the on-board DSP I/O resources via on-board 16-bit parallel I/O expansion interface site (PIOX-16) (fig.B-1), which is designed to carry compatible DCM (DCM).
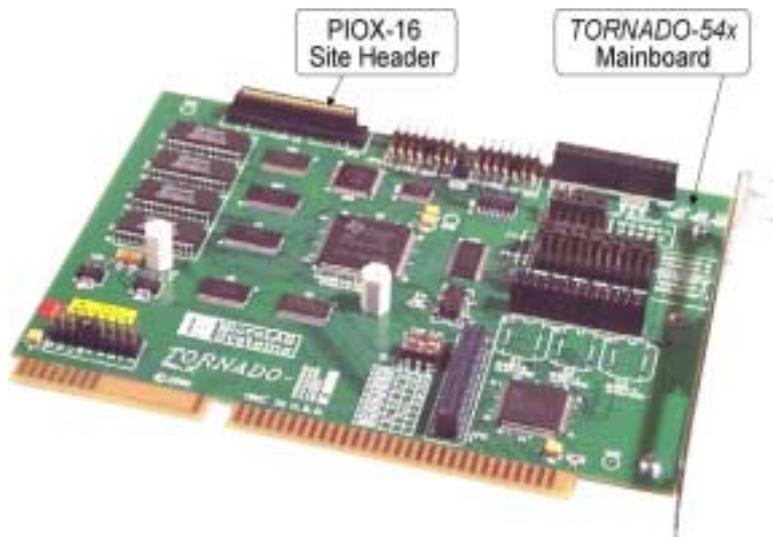

Fig.B-1. PIOX-16 site at *TORNADO-54x* board.

Some *TORNADO* boards (typically 32-bit *TORNADO* DSP systems for PC) provide 16-bit PIOX-16 site as a subset of on-board 32-bit PIOX interface site, whereas other *TORNADO* boards (typically *TORNADO* stand-alone DSP controllers and 16-bit *TORNADO* DSP systems for PC) provide PIOX-16 site only. Refer to your host *TORNADO* board user's guide for information about particular PIOX or PIOX-16 interface site installed.

Figure B-2 demonstrates installation of PIOX-16 DCM into PIOX-16 site of host *TORNADO* DSP system/controller.
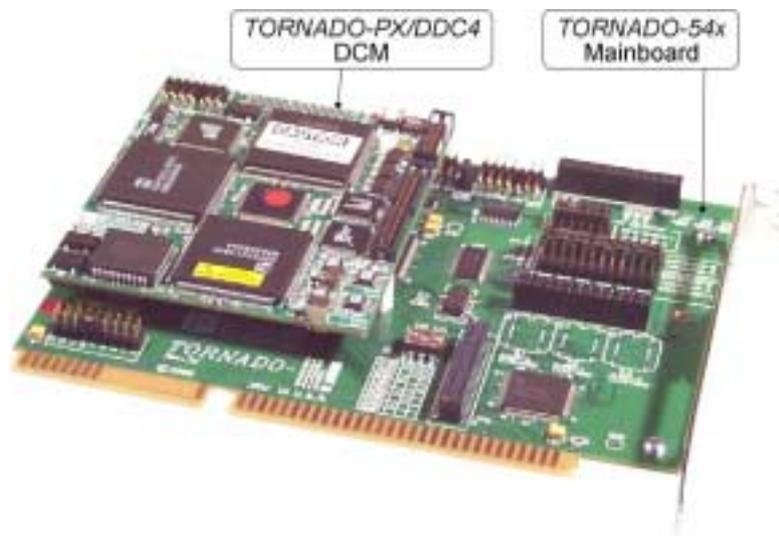
Fig.B-2.   TORNADO-54x board with PIOX-16 DCM installed.

B.2   PIOX-16 Interface Site Connector and Signals

TORNADO PIOX-16 interface site comprises of signals for SIO-0 and SIO-1 logical serial ports, DSP on-chip TM/XIO-0/1 timers/IO pins, three DSP interrupts, PIOX-16 reset control, and power ±5V/±12V power supplies.

PIOX-16 interface appears as the 64Kx16 sub-area of DSP external memory or I/O resources. PIOX-16 features 16-bit data transfer cycles.

PIOX-16 connector and signal description

PIOX-16 connector is a high-density DDK 50-pin DHB-series dual-row female connector with 0.05" pin pitch. Compatible PIOX-16 plugs for customer designed DCM are available upon request from MicroLAB Systems.

PIOX-16 connector pinout is presented at fig B-3, whereas signal description for PIOX-16 connector is presented in table B-1.
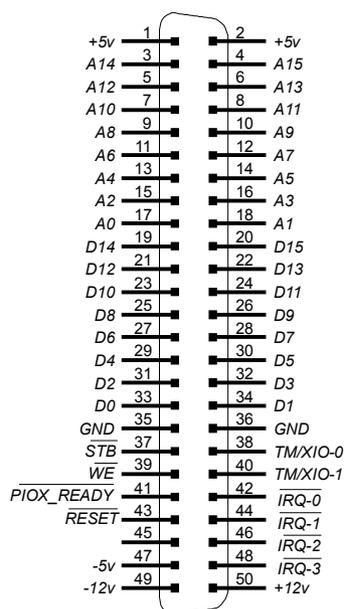
Fig.B-3. PIOX-16 connector pinout (top view).

Table B-1. PIOX-16 signal description.

Signal name	signal type	description
Address and Data Bus		
A0..A15	O	DSP address bus.
D0..D15	I/O	DSP data bus.
Data Transfer Control		
$\overline{STB}$	O	Active low PIOX-16 data transfer strobe.
$\overline{WE}$	O	Active low PIOX-16 write enable signal.
$\overline{PIOX\_READY}$	I	Active low PIOX-16 data ready acknowledge signal. This signal is generated by PIOX-16 DCM in order to complete transmission cycle over PIOX-16 interface. This input has pull-up resistor.

DSP Timers, Reset and Interrupt Requests		
TM/XIO-0 *TM/XIO-1*	I/O/Z	These signals are typically connected to the DSP on-chip TIMER-0 and TIMER-1 I/O pins and can be software configured by DSP as either timer or I/O pin. However, in some *TORNADO* boards (for example *TORNADO-54x* board) these signals can be controlled by on-board I/O controller.
$\overline{RESET}$	O	Active low PIOX-16 reset signal. Some *TORNADO* boards (for example *TORNADO-3x* boards) wires this signal directly from the DSP reset signal, and PIOX-16 plugged-in DCM reset is asserted simultaneously with *TORNADO* on-board DSP reset. However some *TORNADO* boards (for example *TORNADO-54x/6x* etc. boards) feature dedicated PIOX-16 site reset signal, which is controlled by *TORNADO* on-board DSP for better synchronization between the DSP software and PIOX-16 DCM operation.
$\overline{IRQ\text{-}0}$ $\overline{IRQ\text{-}1}$ $\overline{IRQ\text{-}2}$ $\overline{IRQ\text{-}3}$	I	Active low external interrupt request lines for *TORNADO* on-board DSP. These lines are pulled up. Note, that IRQ-2 and IRQ-3 interrupt request input are not available for all *TORNADO* DSP systems/controllers (refer to your *TORNADO* DSP system/controller user's guide for details about on-board PIOX-16 interface).
Power Supplies		
GND		Ground.
+5v		+5v power (from ISA-bus).
+12v		+12v power (from ISA-bus).
-5v		-5v power (from ISA-bus).
-12v		-12v power (from ISA-bus).

Note: 1.   Signal type is denoted as the following: *I* - input, *O* - output, *Z* - high impedance.

PIOX-16 site signal levels

Signal levels for PIOX-16 interface signals correspond to that for the CMOS/TTL signals with I_{OL}=2ma and I_{OH}=-0.3ma load currents.

> **CAUTION**
>
> Some *TORNADO* boards (*TORNADO-30/31/32L/542L*) provide PIOX-16 interface signal
> levels compatible with that for CMOS/TTL only, whereas other *TORNADO* boards
> (*TORNADO-33/54xx/6x/E6x/P6x/E3x/E6x*) provide PIOX-16 interface signal levels
> universal for both 3V TLL and standard TTL. Refer to documentation for your particular
> *TORNADO* board for information about PIOX-16 interface signal levels.

timing diagram for PIOX-16 data transmission cycle

Figure B-4 presents timing diagram for typical PIOX-16 data transmission cycle for *TORNADO-54x* DSP system. This data transfer timing is known as the industry standard MOTOROLA mode and assumes usage of data strobe signal and write enable signal.
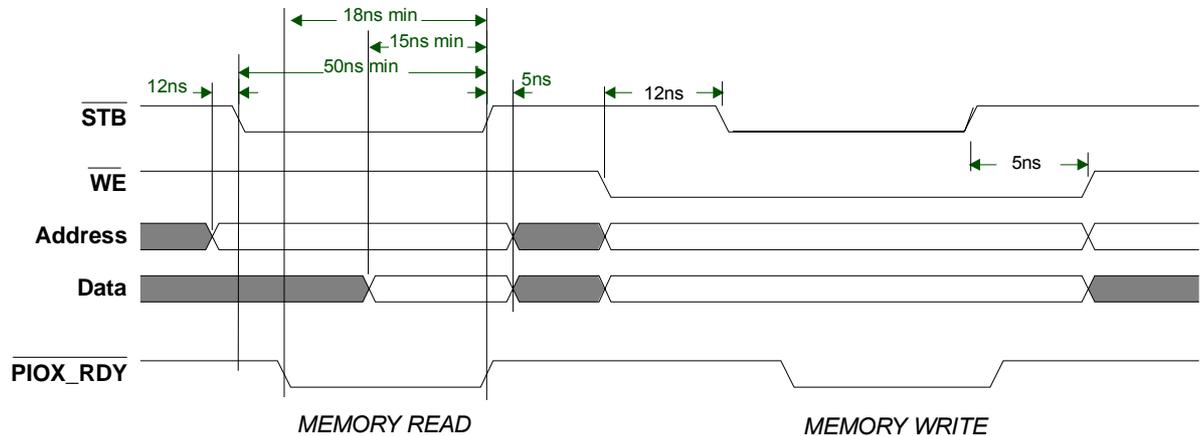

Fig.B-4. Timing diagram of PIOX-16 data transfer for *TORNADO-54x*.

Other *TORNADO* DSP systems/controllers (*TORNADO-3x/6x/P3x/P6x/E3x/E6x*, etc) provide similar timing for PIOX-16 data transmission cycles with the only differences applied to specific timing parameters. Refer to documentation for your particular *TORNADO* board for information about PIOX-16 timing specifications.

B.3   Physical Dimensions for PIOX-16 DCM

Physical dimensions for PIOX-16 DCM are presented at fig.B-5. This information is intended for those customers, who need to design custom PIOX-16 DCM.
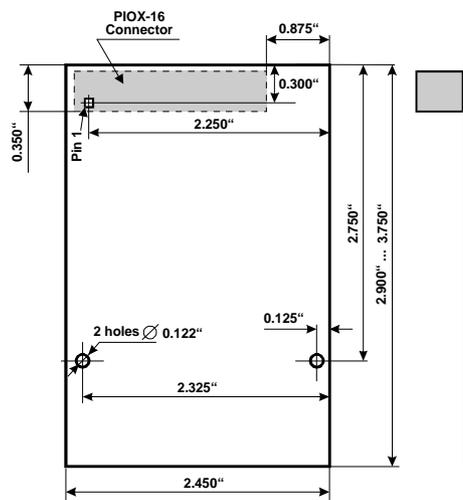
Fig.B-5.   Physical dimensions for PIOX-16 DCM.

Appendix C.   External Cable Sets

This appendix contains information about *T/X-XIOB/PDAS65M* external I/O board and *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* external cable sets for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.

C.1   Connection of external I/O devices to *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM

T/PDAS-AD8/12D/65M-DA2/12D/65M DCM provides on-board JP2 external synchronization and I/O connector and JP5..JP14 mini-coax connectors (refer Appendix A) for MASTER-SLAVE connection of multiple *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and connection to external synchronization and analog I/O devices.

External synchronization and analog I/O devices can either directly connect to *T/PDAS-AD8/12D/65M-DA2/12D/65M* on-board JP2 and JP5..JP14 connectors, or, for more convenience, can connect by means of optional *T/X-XIOB/PDAS65M* external I/O board and two external I/O cable sets (fig.C-1), which include *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* external cable sets and which come standard with *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM shipment package. *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* external cable sets comprise can be used for connection to external synchronization and analog I/O devices via industry standard end connectors.
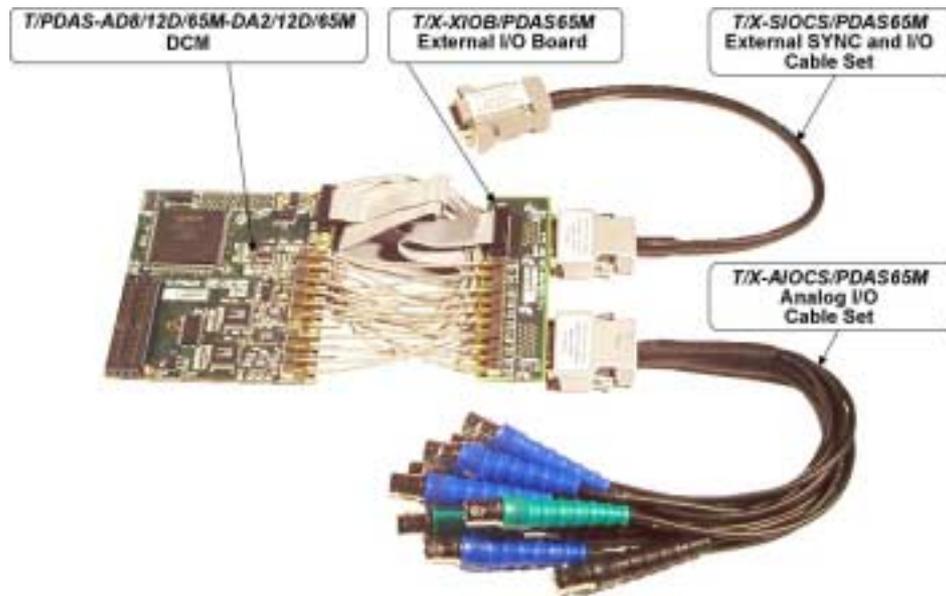

Fig. C-1.   T/PDAS-AD8/12D/65M-DA2/12D/65M DCM with *T/X-XIOB/PDAS65M* external I/O board and *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* external cable sets.

Optional *T/X-XIOB/PDAS65M* external I/O board can be installed at the rear panel of PC chassis and converts JP2 and JP5..JP14 *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM on-board connectors into two remote

external synchronization and I/O and analog /O connectors, which are used for connection to *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* external cable sets.

T/X-SIOCS/PDAS65M and *T/X-AIOCS/PDAS65M* external cable sets provide industry standard connectors for connection to external synchronization and I/O devices and to high-frequency analog I/O peripherals devices.

C.2   *T/X-XIOB/PDAS65M* External I/O Board

T/X-XIOB/PDAS65M external I/O board (fig.C-2) comes standard with *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and must be used for connection to external devices using industry standard connectors via *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* external cable sets and via rear panel of PC chassis.
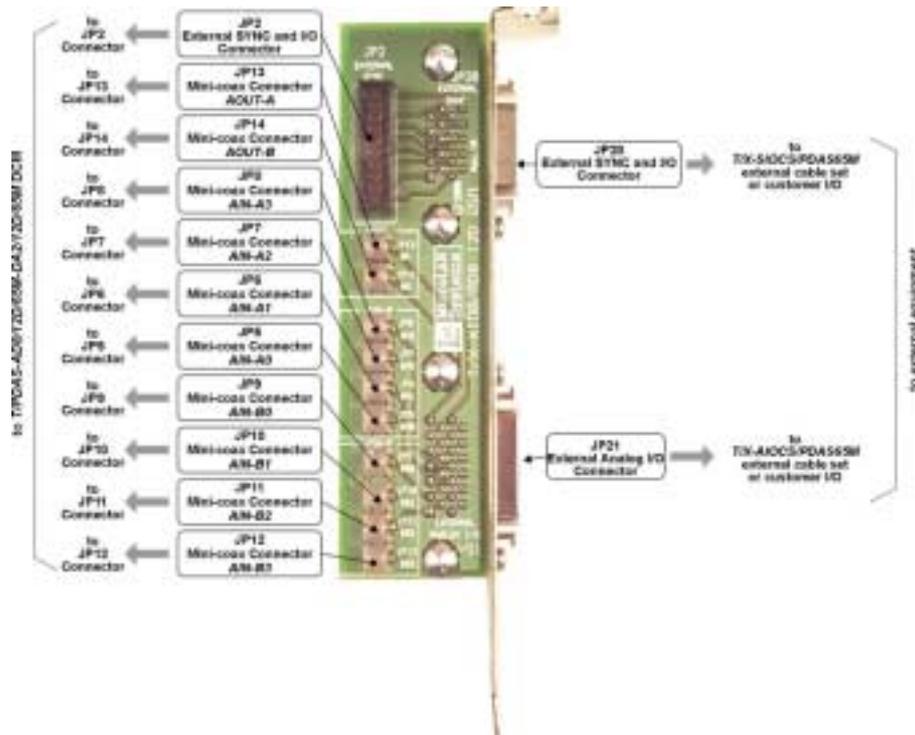

Fig. C-2.   *T/X-XIOB/PDAS65M* external I/O board.

installation

T/X-XIOB/PDAS65M external I/O board either installs in a separate slot at the rear panel of PC chassis, or can be installed directly onto the rear mounting bracket of *TORNADO* PC plug-in DSP systems in order to save space inside PC chassis compartment.

schematic diagram for T/X-XIOB/PDAS65M external I/O connector board

T/X-XIOB/PDAS65M external I/O board comprises of the following on-board connectors:

- Input JP5..JP8 mini-coax connectors, which shall connect to *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM on-board AIN-A0..3 analog input JP5..JP8 mini-coax connectors correspondingly via 12" miniature coax cables.
- Input JP9..JP12 mini-coax connectors, which shall connect to *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM on-board AIN-B0..3 analog input JP9..JP12 mini-coax connectors correspondingly via 12" miniature coax cables.
- Input JP13 and JP14 mini-coax connectors, which shall connect to *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM on-board AOUT-A/B analog output JP13 and JP14 mini-coax connectors correspondingly via 12" miniature coax cables.
- Input JP2 guarded 2mm 16-pin straight male header, which must connect to *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM on-board JP2 external synchronization and I/O connector via 12" 2mm flat ribbon cable.
- Output JP20 external I/O connector, which comprises of the signals from on-board JP2 connector and which allow MASTER-SLAVE connection of multiple *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM as well as connection of to external synchronization and I/O devices via *T/X-SIOCS/PDAS65M* external cable set. *T/X-XIOB/PDAS65M* on-board JP20 connector is 20-pin half pitch DHA-RA20 series receptacles from Fujikura-DDK Ltd. In case customer needs to design his own application specific cable for connection to JP20 connector instead of using provided *T/X-SIOCS/PDAS65M* external cable set, then compatible plug for JP20 connector is available from MicroLAB Systems upon request.
- Output JP21 external I/O connector, which comprises of analog I/O signals from on-board JP5..JP14 on-board mini-coax connectors and which allow connection to external analog I/O devices via *T/X-AIOCS/PDAS65M* external cable set. *T/X-XIOB/PDAS65M* on-board JP21 connector is 26-pin half pitch DHA-RA26 series receptacles from Fujikura-DDK Ltd. In case customer needs to design his own application specific cable for connection to JP21 connector instead of using provided *T/X-AIOCS/PDAS65M* external cable set, then compatible plug for JP21 connector is available from MicroLAB Systems upon request.

Fig.C-3 shows generic schematic diagram of *T/X-XIOB/PDAS65M* external I/O board for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM. Signals description for on-board JP2 external synchronization I/O connector is provided in table A-2 for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.
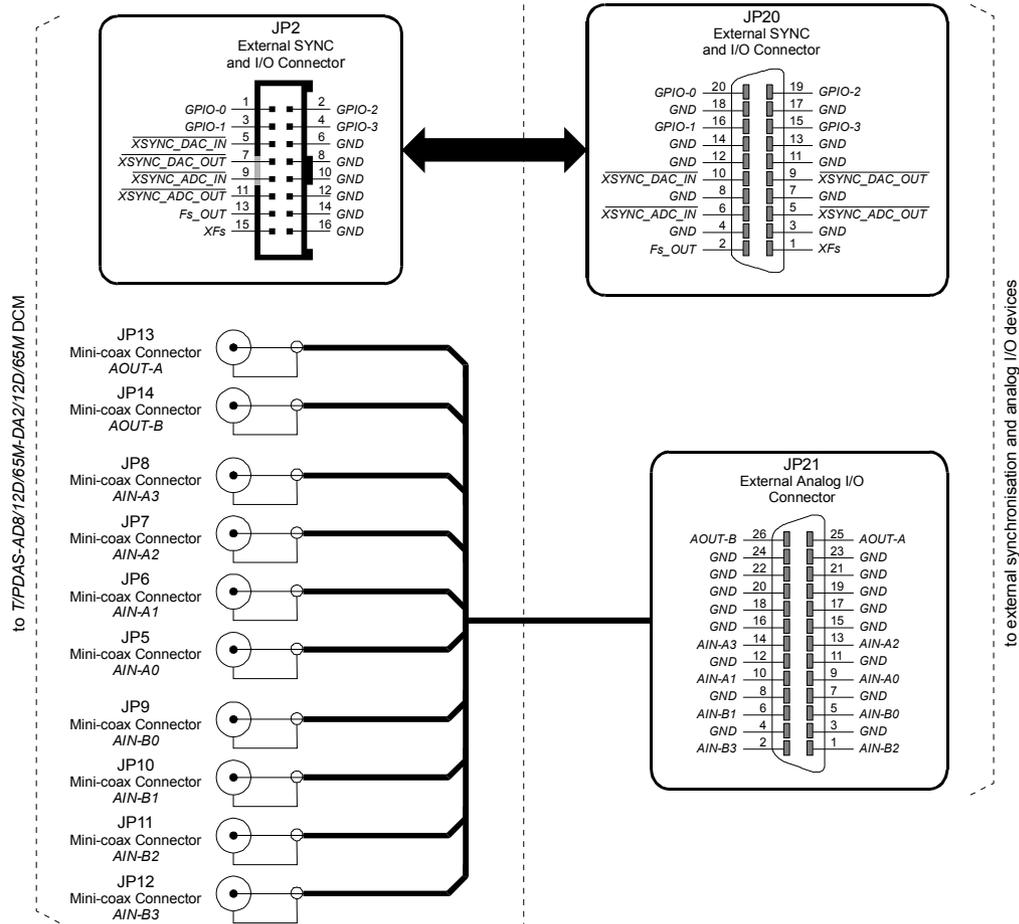
Fig.C-3. Schematic diagram of *T/X-XIOB/PDAS65M* external I/O board.

C.3   *T/X-SIOCS/PDAS65M* and *T/X-AIOCS/PDAS65M* External I/O Cable Sets

T/X-SIOCS/PDAS65M and *T/X-AIOCS/PDAS65M* external cable sets (fig.C-4) come standard with *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM and shall be used for connection to external synchronization and analog I/O devices using industry standard connectors via *T/X-XIOB/PDAS65M* external I/O board.

Fig. C-4a. T/X-SIOCS/PDAS65M external I/O cable set.

Fig. C-4b. T/X-AIOCS/PDAS65M external I/O cable set.

T/X-SIOCS/PDAS65M and *T/X-AIOCS/PDAS65M* external cable sets for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM plugs either into the JP20 and JP21 connectors correspondingly at *T/X-XIOB/PDAS65M* external I/O board for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM (refer to fig.C-1 and section "*T/X-XIOB/PDAS65M* external I/O board" earlier in this appendix) and shall be used for connection to external devices via industry standard end connectors.

schematic diagram for T/X-SIOCS/PDAS65M external cable set

T/X-SIOCS/PDAS65M external cable set converts external synchronization and general purpose I/O signal from 20-pin JP20 connector of *T/X-XIOB/PDAS65M* external I/O board for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM into industry standard DBH-15 female connector.

T/X-SIOCS/PDAS65M external cable set must be used for MASTER-SLAVE connection of multiple *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM as well as connection of to external synchronization and I/O devices.

Schematic diagram of *T/X-SIOCS/PDAS65M* external cable set is presented at figure C-5. Signal description is provided in table A-2 for JP2 external synchronization and I/O connector of *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM.
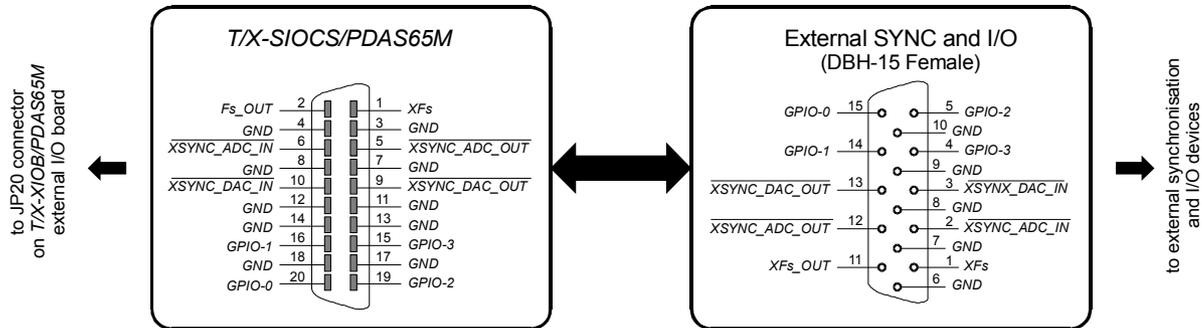

Fig.C-5.   Schematic diagram of *T/X-SIOCS/PDAS65M* external cable set.

schematic diagram for T/X-AIOCS/PDAS65M external cable set

T/X-AIOCS/PDAS65M external cable set converts analog I/O signals from 26-pin JP21 connector of *T/X-XIOB/PDAS65M* external I/O board for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM into ten industry standard female BNC connectors (fig.C-6).

T/X-AIOCS/PDAS65M external cable set must be used for connection to external analog I/O devices and actually routes external analog I/O signals from BNC connectors to JP5..JP14 on-board mini-coax connectors *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM via *T/X-XIOB/PDAS65M* external I/O board.
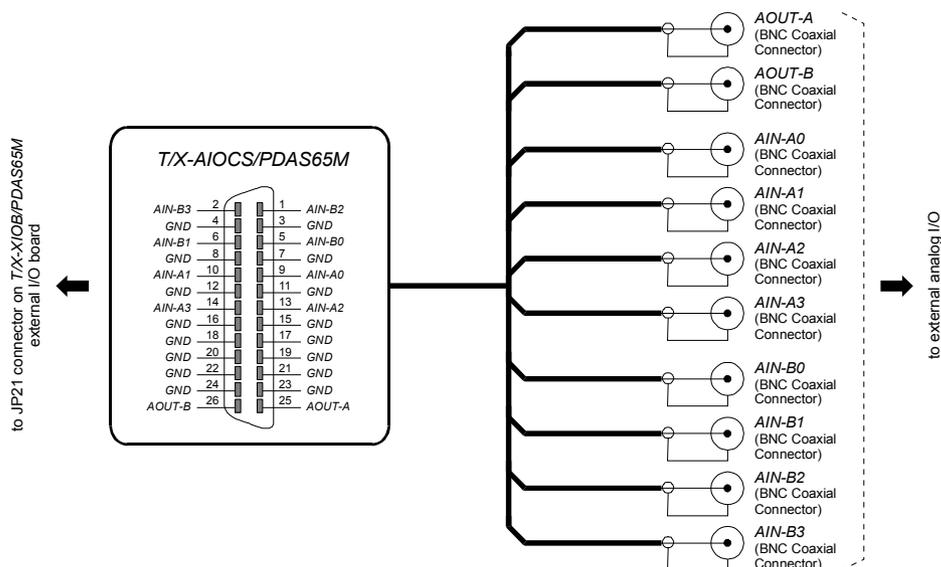

Fig.C-6.   Schematic diagram of *T/X-AIOCS/PDAS65M* external cable set.

Appendix D.   Glossary of Terms.

This Glossary contains definition for terms and other synchronism used along in this databook.

A

ADC_DAQ_RESET_RG

Write-only register, which must be used for reset ADC FIFO, ADC data acquisition controller, ADC IRT controller and ADC data acquisition errors. Refer to sections 2.2 and 2.3 for more details.

ADC_FIFO_SIN_RG

Write-only register, which must be used for serial programming offset values for ADC1-FIFO and ADC2-FIFO. Refer to sections 2.2 and 2.3 for more details.

ADC1, ADC2

On-board analog-to-digital converters. Refer to sections 2.1 and 2.3 for more details.

ADC1_FIFO_DATA_RG, ADC2_FIFO_DATA_RG

Read-only ADC1-FIFO and ADC2-FIFO data registers correspondingly. Refer to sections 2.2 and 2.3 for more details.

ADC_FIFO_STAT_RG

Read-only register, which must be used to read status of ADC FIFO flags. Refer to sections 2.2 and 2.3 for more details.

ADC1-FIFO, ADC2-FIFO

On-board ADC FIFO, which store output data from on-board of ADC1/XDSIN-A0..15 and ADC2/XDSIN-B0..15 correspondingly. Refer to sections 2.1 and 2.3 for more details.

ADC-IMUX

Dual 4:1 ADC analog input multiplexer, which is used to multiplex AIN-A0..3 and AIN-B0..3 analog inputs to the inputs of on-board ADC1 and ADC2 correspondingly. Refer to sections 2.1, 2.2 and 2.3 for more details.

ADC Data Acquisition Controller

A part of on-board SCU unit, which is used to control ADC data acquisition process. Refer to sections 2.1 and 2.3 for more details.

ADC IRT Controller

ADC interrupt retriggable transmission (IRT) controller for generation of retriggable synchronization events to host DSP on-chip DMA controllers via host PIOX-16 interrupt request lines in order to transfer data from ADC FIFO to host DSP environment using host DSP on-chip DMA controllers. Refer to sections 2.2, 2.3 and 2.4 for more details.

B

C

D

DAC_DAQ_RESET_RG
Write-only register, which must be used for reset DAC FIFO, DAC data acquisition controller, DAC IRT controller and DAC data acquisition errors. Refer to sections 2.2 and 2.3 for more details.

DAC1_FIFO_DATA_RG, DAC2_FIFO_DATA_RG
Write-only DAC1-FIFO and DAC2-FIFO data registers correspondingly. Refer to section 2.2 for more details.

DAC_FIFO_SIN_RG
Write-only register, which must be used for serial programming offset values for DAC1-FIFO and DAC2-FIFO. Refer to sections 2.2 and 2.3 for more details.

DAC_FIFO_STAT_RG
Read-only register, which must be used to read status of DAC FIFO flags. Refer to sections 2.2 and 2.3 for more details.

DAC1, DAC2
Digital-to-analog converter. Refer to sections 2.2 and 2.3 for more details.

DAC1-FIFO, DAC2-FIFO
On-board DAC FIFO, which store input data for on-board DAC1/XDSOUT-A0..15 and DAC2/XDSOUT-B0..15 correspondingly. Refer to sections 2.1 and 2.3 for more details.

DAC Data Acquisition Controller
A part of on-board SCU unit, which is used to control DAC data acquisition process. Refer to sections 2.1 and 2.3 for more details.

DAC IRT Controller
DAC interrupt retriggable transmission (IRT) controller for generation of retriggable synchronization events to host DSP on-chip DMA controllers via host PIOX-16 interrupt request lines in order to transfer data to DAC FIFO from host DSP environment using host DSP on-chip DMA controllers. Refer to sections 2.2, 2.3. and 2.4 for more details.

DAC OPM
One-pass DAC data acquisition mode. Refer to section 2.3 for more details.

DAC PTM

Pass-through DAC data acquisition mode. Refer to section 2.3 for more details.

DAQ

Data acquisition.

DAQ_CNTR1_RG

Data acquisition control register, which must be used to configure ADC/DAC data acquisition modes and data formats. Refer to sections 2.2 and 2.3 for more details.

DAQ_CNTR2_RG

Data acquisition control register, which must be used to control and get status of ADC/DAC data acquisition processes. Refer to sections 2.2 and 2.3 for more details.

DAQ_CNTR3_RG

Data acquisition control register, which must be used to select termination flags for ADC OPM and DAC OPM data acquisition modes, and to select start/termination flags for ADC IRT and DAC IRT controllers. Refer to sections 2.2 and 2.3 for more details.

DAQ_MUX_RG

Data acquisition control register, which must be used to configure ADC-IMUX analog input multiplexer and on-board DSIN-MUX and DSOUT-MUX digital I/O streams multiplexers. Refer to sections 2.2 and 2.3 for more details.

DAQ_RESET_RG

Write-only register, which must be used for reset ADC/DAC FIFO, ADC/DAC data acquisition controllers, ADC/DAC IRT controllers and data acquisition errors. Refer to sections 2.2 and 2.3 for more details.

DAQ_SYNC_RG

Data acquisition control register, which must be used to select synchronization modes for ADC/DAC data acquisition processes. Refer to sections 2.2 and 2.3 for more details.

DCM

Daughter-card module. *T/PDAS-AD8/12D/65M-DA2/12D/65M* is DCM, which plugs into PIOX-16 interface site of host *TORNADO* DSP system/controller.

DSIN-MUX

Input digital stream multiplexer, which is used to multiplex output data streams from ADC1/ADC2 and XDSIN external digital input stream to the input of ADC FIFO. Refer to sections 2.1 and 2.3 for more details.

DSOUT-MUX

Output digital stream multiplexer, which is used to multiplex output data stream from DAC FIFO to the inputs of DAC1/DAC2 and XDSOUT external digital output stream. Refer to sections 2.1 and 2.3 for more details.

DSP
> Digital Signal Processor.

E

ERR_CLR_RG
> Write-only register, which must be used to clear data acquisition errors. Refer to sections 2.2 and 2.3 for more details.

ERR_STAT_RG
> Read-only register, which must be used to read status of data acquisition errors. Refer to sections 2.2 and 2.3 for more details.

F

FIFO
> On-board high density First-In-First-Output device, which is used to store ADC/DAC data. Refer to sections 2.1, 2.2 and 2.3 for more details.

G

GPIO-0/1/2/3
> General purpose digital I/O bits, which can be used for control of external peripherals. *GPIO-0/1/2/3* are controlled via *GPIO_DIR_RG* and *GPIO_DATA_RG* registers. Refer to section 2.2 for more details.

GPIO_DIR_RG, GPIO_DATA_RG
> Registers, which are used to set direction and read/write data to the *GPIO-0..3* digital I/O pins. Refer to section 2.2 for more details.

H

Host PIOX-16 interface
> *T/PDAS-AD8/12D/65M-DA2/12D/65M* on-board host PIOX-16 interface, which is used to install onto host *TORNADO* DSP system/controller and for communication with host DSP. Refer to section 2.5 and Appendix B for more details.

HIRQ0_SEL_RG, HIRQ1_SEL_RG, HIRQ2_SEL_RG, HIRQ3_SEL_RG,
> Registers, which shall be used to enable and to select a particular interrupt request source for each of host PIOX-16 interrupt request lines IRQ-0..3. Refer to section 2.2 for more details.

I

IRQ-0, IRQ-1, IRQ-2, IRQ-3

Host PIOX-16 interface interrupt request inputs, which are used to send interrupt request to host DSP of host *TORNADO* DSP system/controller from *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM. Refer to section 2.5 and Appendix B for more details.

IRT

Interrupt retriggable transmission (IRT). Refer to ADC IRT controller or DAC IRT controller and to sections 2.2, 2.3. and 2.4 for more details.

J

K

L

M

MASTER Synchronization Mode

Synchronization mode for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, which allows to select sampling frequency source and start-up synchronization mode for ADC/DAC data acquisition controllers. MASTER device generates output synchronization to SLAVEs in order to start A/D and D/A data acquisition processes synchronously for multiple *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM. Refer to section 2.3 for more details.

MSPS

Sampling frequency parameter specification, which denotes Mega Samples per Second, i.e. how many 10^6 samples per second for A/D and D/A conversions are allowed.

N

O

P

PFG

On-board programmable sampling frequency generator, which can be used to set sampling frequency for on-board ADC and DAC data acquisition controllers. Refer to sections 2.2 and 2.3 for more details.

PFG_CNTR1_RG, PFG_CNTR2_RG, PFG_CNTR3_RG

Configuration registers for on0board PFG, which shall be used to set PFG output frequency. Refer to sections 2.2 and 2.3 for more details.

PIOX

32-bit Parallel I/O eXpansion interface site for compatible daughter-card modules (DCM) at *TORNADO* PC plug-in DSP systems. PIOX comprises of 16-bit PIOX-16 interface site and PIOX-X32 32-bit extension interface site. Refer to sections 2.6 and 3.1, and Appendix B for more details.

PIOX-16

16-bit Parallel I/O eXpansion interface site for compatible daughter-card modules (DCM) at *TORNADO* PC plug-in DSP systems and controllers. *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM plugs into PIOX-16 interface site on host *TORNADO* DSP system/controller. Refer to sections 2.6 and 3.1, and Appendix B for more details.

Q

R

S

SCU

Synchronization and control unit, which performs control of ADC/DAC data acquisition process. Refer to sections 2.1, 2.2 and 2.3 for more details.

SLAVE Synchronization Mode

Synchronization mode for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM, which assumes that external synchronization for ADC and DAC data acquisition controllers of this DCM is provided from external MASTER. MASTER-SLAVE synchronization allows to start A/D and D/A data acquisition processes synchronously for multiple *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM. Refer to section 2.3 for more details.

T

T/X-XIOB/PDAS65M

External I/O board for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM. Refer to Appendix C for more details.

T/X-AIOCS/PDAS65M

External analog I/O cable set for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM. Refer to Appendix C for more details.

T/X-SIOCS/PDAS65M

External synchronization and I/O cable set for *T/PDAS-AD8/12D/65M-DA2/12D/65M* DCM. Refer to Appendix C for more details.

U

V

W

X

XDSIN

32-bit external digital input stream from on-board JP3 connector, which can be used instead of ADC output data in order to store in on-board ADC FIFO. Refer to sections 2.1 and 2.3 for more details.

XDSOUT

32-bit external digital output stream via on-board JP4 connector, which can be used instead of DAC output data in order to output data from on-board DAC FIFO. Refer to sections 2.1 and 2.3 for more details.

XIM_ERR_RG

Expansion error interrupt register, which must be used to set interrupt enable masks for data acquisition errors. Refer to section 2.2 for more details.

Y

Z